

Features

■ HB LED Controller

- Configurable Dimmers Support up to 16 Independent LED Channels
- 8-32 Bits of Resolution per Channel
- Dynamic Reconfiguration Enables LED Controller plus other Features; Battery Charging, Motor Control...

■ Visual Embedded Design, PSoC Express

- LED Based Express Drivers
 - Binning Compensation
 - Temperature Feedback
 - DMX512

■ PrISM Modulation Technology

- Reduces Radiated EMI
- Reduces Low Frequency Blinking

■ Powerful Harvard Architecture Processor

- M8C Processor Speeds to 24 MHz
- 3.0 to 5.25V Operating Voltage
- Operating Voltages down to 1.0V using On-Chip Switch Mode Pump (SMP)
- Industrial Temperature Range: -40°C to +85°C

■ Programmable Pin Configurations

- 25 mA Sink on all GPIO
- Pull up, Pull down, High Z, Strong, or Open Drain Drive Modes on all GPIO
- Up to eight Analog Inputs on GPIO
- Configurable Interrupt on all GPIO

■ Advanced Peripherals (PSoC Blocks)

- 16 Digital PSoC Blocks Provide:
 - 8 to 32-Bit Timers, Counters, and PWMs
 - Up to 2 Full-Duplex UART
 - Multiple SPI™ Masters or Slaves
 - Connectable to all GPIO Pins
- 12 Rail-to-Rail Analog PSoC Blocks Provide:
 - Up to 14-Bit ADCs
 - Up to 9-Bit DACs
 - Programmable Gain Amplifiers
 - Programmable Filters and Comparators
- Complex Peripherals by Combining Blocks

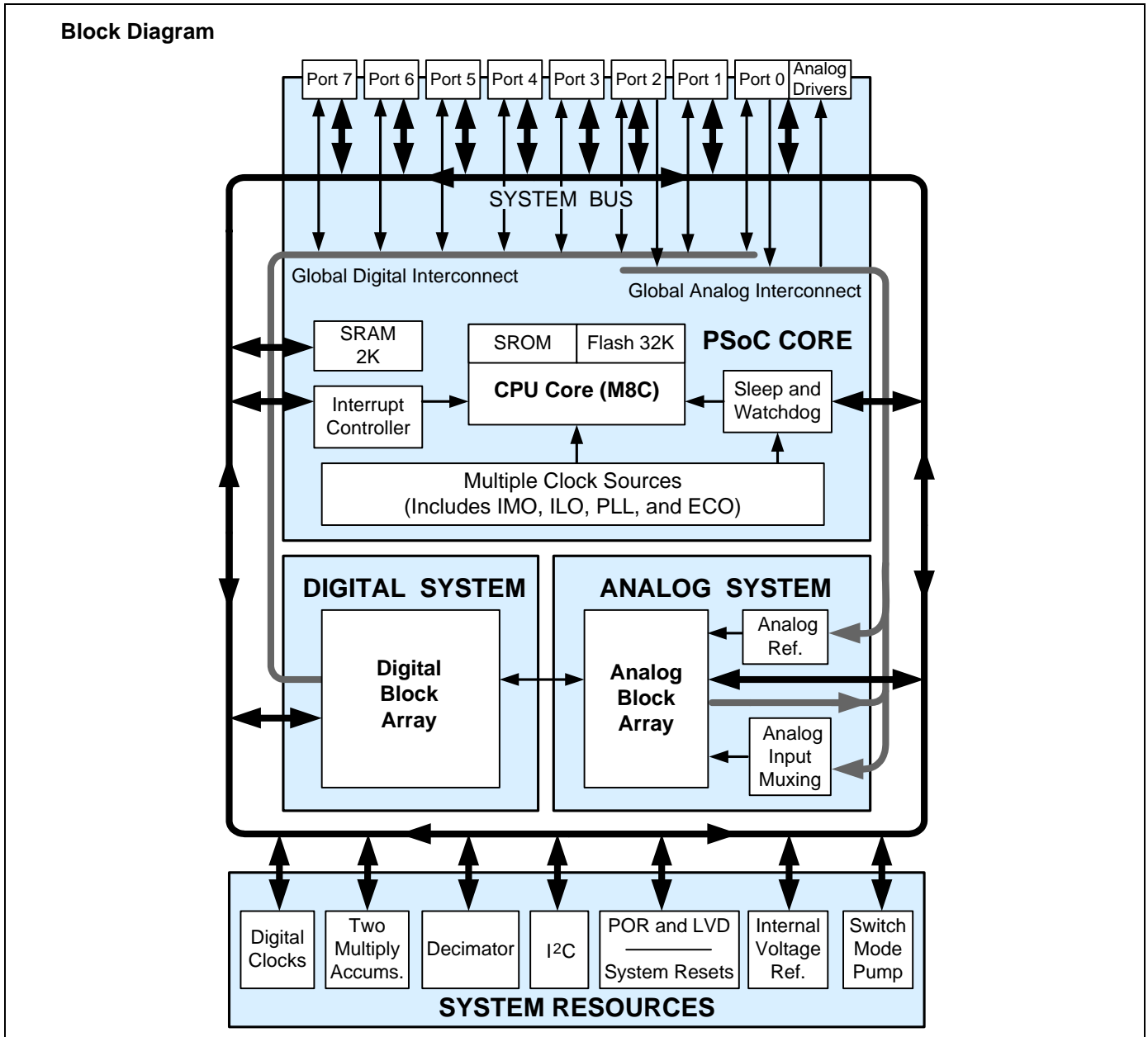
■ Flexible On-Chip Memory

- 32K Flash Program Storage 50,000 Erase/Write Cycles
- 2K SRAM Data Storage
- In-System Serial Programming (ISSP)
- Partial Flash Updates
- Flexible Protection Modes
- EEPROM Emulation in Flash

■ Complete Development Tools

- Free Development Software
 - PSoC Designer™
 - PSoC Express™
- Full-Featured, In-Circuit Emulator and Programmer
- Full Speed Emulation
- Complex Breakpoint Structure
- 128 KBytes Trace Memory

Overview



EZ-Color Functional Overview

Cypress' EZ-Color family of devices offers the ideal control solution for High Brightness LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of PSoC (Programmable System-on-Chip™); with Cypress' PrISM (precise illumination signal modulation) modulation technology providing lighting designers a fully customizable and integrated lighting solution platform.

The EZ-Color family supports up to 16 independent LED channels with up to 32 bits of resolution per channel, enabling lighting designers the flexibility to choose the LED array size and color quality. PSoC Express software, with lighting specific drivers, can significantly cut development time and simplify implementation of fixed color points through temperature and LED binning compensation. EZ-Color's virtually limitless analog and digital customization allow for simple integration of features in addition to intelligent lighting, such as Battery Charging, Image Stabilization, and Motor Control during the development process. These features, along with Cypress' best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

Target Applications

- LCD Backlight
- Large Signs
- General Lighting
- Architectural Lighting
- Camera/Cell Phone Flash
- Flashlights

The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 48 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU utilizes an interrupt controller with 25 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 32 KB of Flash for program storage, 2 KB of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The EZ-Color family incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate

to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the EZ-Color device.

EZ-Color GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

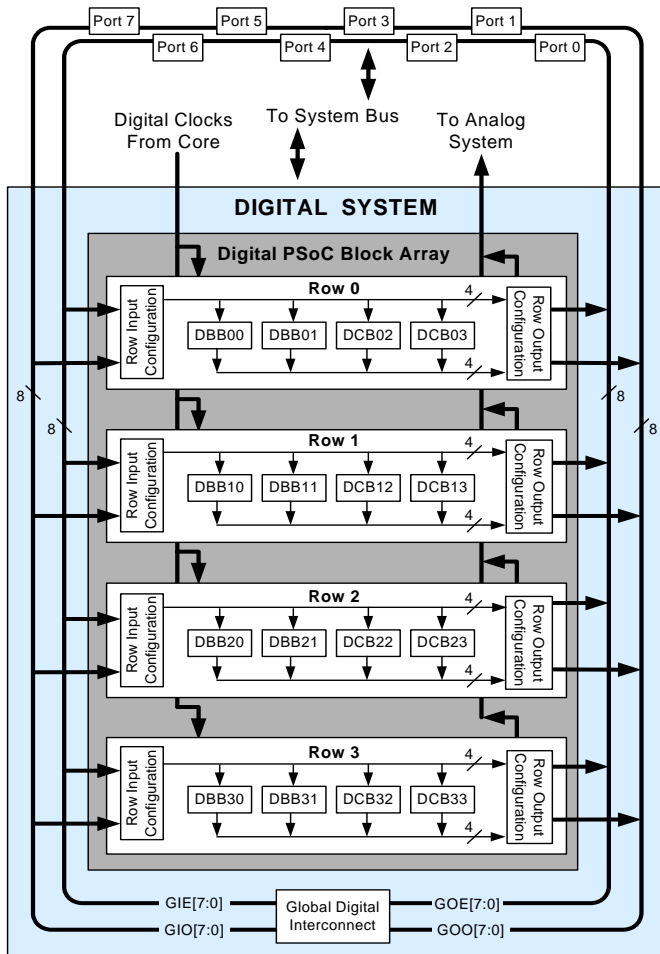
The Digital System is composed of 16 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references. Digital peripheral configurations include those listed below.

- PrISM (8 to 32 bit)
- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to 4)
- SPI master and slave (up to 4 each)
- I2C slave and multi-master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 4)
- Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by EZ-Color device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled EZ-Color Device Characteristics on page 4.

Figure 1. Digital System Block Diagram



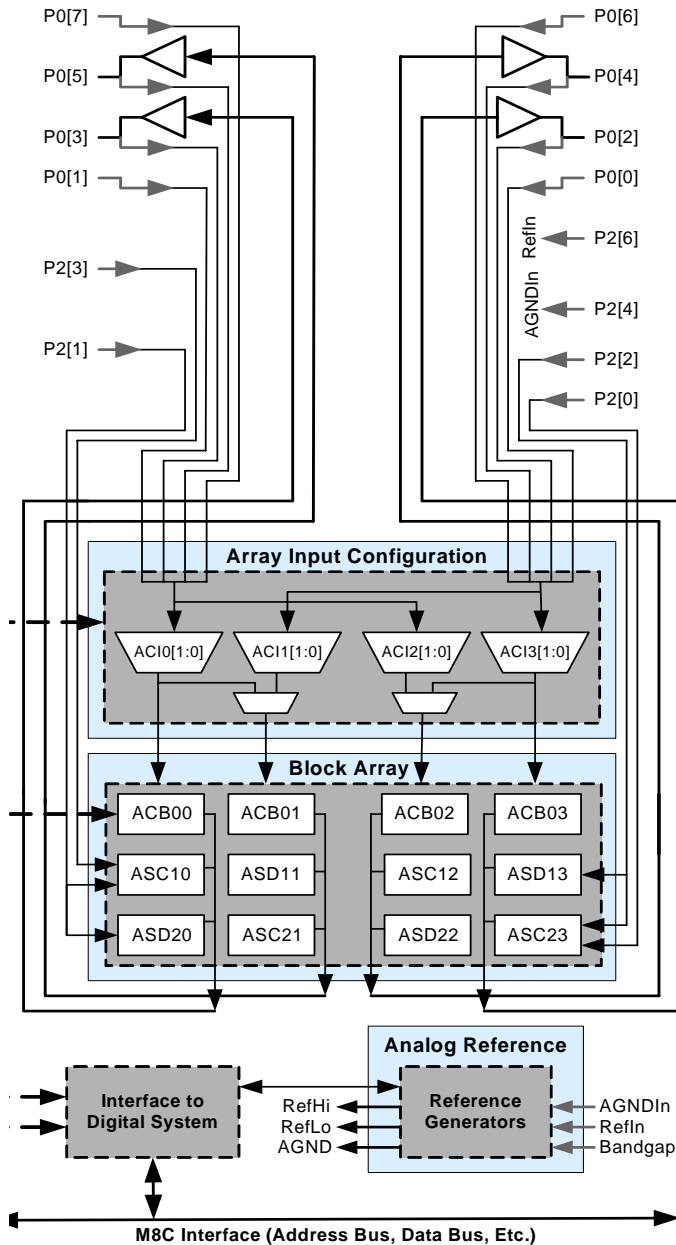
The Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, or 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 40 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF Dialer
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in the figure below.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Multiply accumulate (MAC) provides fast 8-bit multiplier with 32-bit accumulate, to assist in general math and digital filters.
- The decimator provides a custom hardware filter for digital signal, processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

EZ-Color Device Characteristics

Depending on your EZ-Color device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific EZ-Color device groups. The device covered by this data sheet is shown in the highlighted row of the table.

Table 1. EZ-Color Device Characteristics

| PSoC Part Number | LED Channels | Digital IO | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks | SRAM Size | Flash Size | CapSense |
|------------------|--------------|------------|--------------|----------------|---------------|----------------|----------------|---------------|-----------|------------|-----------|
| CY8CLED04 | 4 | 56 | 1 | 4 | 48 | 2 | 2 | 6 | 1K | 16K | Yes |
| CY8CLED08 | 8 | 44 | 2 | 8 | 12 | 4 | 4 | 12 | 256 Bytes | 16K | No |
| CY8CLED16 | 16 | 64 | 4 | 16 | 12 | 4 | 4 | 12 | 2K | 32K | No |

Getting Started

The quickest path to understanding the EZ-Color silicon is by reading this data sheet and using PSoC Express to create HB LED applications. This data sheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest device data sheets on the web at <http://www.cypress.com/ez-color>.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store at <http://www.onfulfillment.com/cypressstore/> contains development kits, C compilers, and all accessories for PSoC development. Click on **EZ-Color** to view a current list of available items.

Technical Training Modules

Free PSoC technical training modules are available for users new to PSoC. Training modules cover designing, debugging, advanced analog, CapSense, and HB LED. Go to <http://www.cypress.com/techtrain>.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to the following Cypress support web site: <http://www.cypress.com/support/cypros.cfm>.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at <http://www.cypress.com/support/login.cfm>.

Application Notes

A long list of application notes will assist you in every aspect of your design effort. To view the PSoC application notes, go to the <http://www.cypress.com> web site and select Application Notes under the Design Resources list located in the center of the web page. Application notes are listed by date by default.

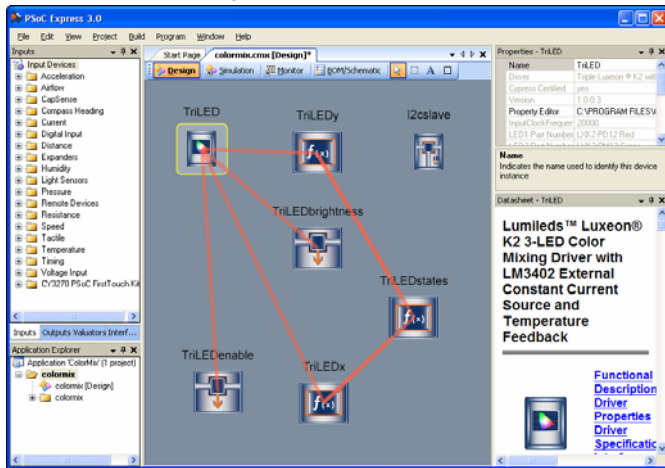
Development Tools

PSoC Express is a high-level design tool for creating embedded systems with devices using Cypress's PSoC Mixed-Signal technology. With PSoC Express you create a complete embedded solution including all necessary on-chip peripherals, block configuration, interrupt handling and application software without writing a single line of assembly or C code.

PSoC Express solves design problems the way you think about the system:

- Select input and output devices based upon system requirements.
- Add a communications interface and define its interface to system (using registers).
- Define when and how an output device changes state based upon any and all other system devices.
- Based upon the design, automatically select one or more PSoC Mixed-Signal Controllers that match system requirements.

Figure 3. PSoC Express



PSoC Express Subsystems

Express Editor

The Express Editor allows you to create designs visually by dragging and dropping inputs, outputs, communication interfaces, and other design elements, and then describing the logic that controls them.

Project Manager

The Project Manager allows you to work with your applications and projects in PSoC Express. A PSoC Express application is a top level container for projects and their associated files. Each project contains a design that uses a single PSoC device. An application can contain multiple projects so if you are creating an application that uses multiple PSoC devices you can keep all of the projects together in a single application.

Most of the files associated with a project are automatically generated by PSoC Express during the build process, but you can make changes directly to the custom.c and custom.h files and also add your own custom code to the project in the Project Manager.

Application Editor

The Application Editor allows you to edit custom.c and custom.h as well as any C or assembly language source code that you add to your project. With PSoC Express you can create application software without writing a single line of assembly or C code, but you have a full featured application editor at your finger tips if you want it.

Build Manager

The Build Manager gives you the ability to build the application software, assign pins, and generate the data sheet, schematic, and BOM for your project.

Board Monitor

The Board Monitor is a debugging tool designed to be used while attached to a prototype board through a communication interface that allows you to monitor changes in the various design elements in real time.

The default communication for the board monitor is I²C. It uses the CY3240-I2USB I²C to USB Bridge Debugging/Communication Kit.

Tuners

A Tuner is a visual interface for the Board Monitor that allows you to view the performance of the HB LED drivers on your test board while your program is running, and manually override values and see the results.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

I²C to USB Bridge

The I²C to USB Bridge is a quick and easy link from any design or application's I²C bus to a PC via USB for design testing, debugging and communication.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

| Acronym | Description |
|---------|---|
| AC | alternating current |
| ADC | analog-to-digital converter |
| API | application programming interface |
| CPU | central processing unit |
| CT | continuous time |
| DAC | digital-to-analog converter |
| DC | direct current |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| FSR | full scale range |
| GPIO | general purpose IO |
| GUI | graphical user interface |
| HBM | human body model |
| ICE | in-circuit emulator |
| ILO | internal low speed oscillator |
| IMO | internal main oscillator |
| IO | input/output |
| IPOR | imprecise power on reset |
| LSb | least-significant bit |
| LVD | low voltage detect |
| MSb | most-significant bit |
| PC | program counter |
| PLL | phase-locked loop |
| POR | power on reset |
| PPOR | precision power on reset |
| PSoC™ | Programmable System-on-Chip™ |
| PWM | pulse width modulator |
| SC | switched capacitor |
| SLIMO | slow IMO |
| SMP | switch mode pump |
| SRAM | static random access memory |

Units of Measure

A units of measure table is located in the Electrical Specifications section. [Table 7 on page 15](#) lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (e.g., '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or '0x' are decimal.

Pin Information

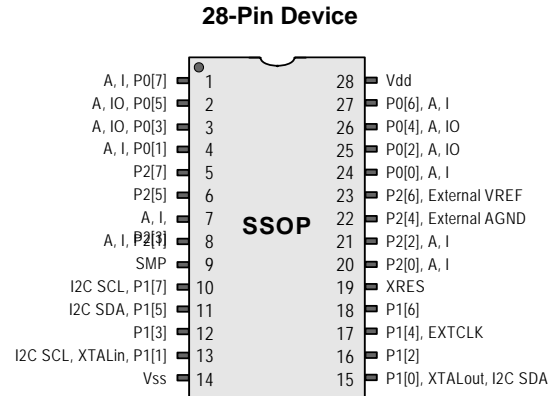
Pinouts

The CY8CLED16 device is available in three packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

28-Pin Part Pinout

Table 2. 28-Pin Part Pinout (SSOP)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|----------|--|
| | Digital | Analog | | |
| 1 | IO | I | P0[7] | Analog column mux input. |
| 2 | IO | IO | P0[5] | Analog column mux input and column output. |
| 3 | IO | IO | P0[3] | Analog column mux input and column output. |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | IO | | P2[7] | |
| 6 | IO | | P2[5] | |
| 7 | IO | I | P2[3] | Direct switched capacitor block input. |
| 8 | IO | I | P2[1] | Direct switched capacitor block input. |
| 9 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 10 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 11 | IO | | P1[5] | I2C Serial Data (SDA). |
| 12 | IO | | P1[3] | |
| 13 | IO | | P1[1] | Crystal (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 14 | Power | | Vss | Ground connection. |
| 15 | IO | | P1[0] | Crystal (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 16 | IO | | P1[2] | |
| 17 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 18 | IO | | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull down. |
| 20 | IO | I | P2[0] | Direct switched capacitor block input. |
| 21 | IO | I | P2[2] | Direct switched capacitor block input. |
| 22 | IO | | P2[4] | External Analog Ground (AGND). |
| 23 | IO | | P2[6] | External Voltage Reference (VREF). |
| 24 | IO | I | P0[0] | Analog column mux input. |
| 25 | IO | IO | P0[2] | Analog column mux input and column output. |
| 26 | IO | IO | P0[4] | Analog column mux input and column output. |
| 27 | IO | I | P0[6] | Analog column mux input. |
| 28 | Power | | Vdd | Supply voltage. |



LEGEND: A = Analog, I = Input, and O = Output.

* These are the ISSP pins, which are not High Z at POR (Power On Reset).

48-Pin Part Pinouts

Table 3. 48-Pin Part Pinout (SSOP)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|----------|--|
| | Digital | Analog | | |
| 1 | IO | I | P0[7] | Analog column mux input. |
| 2 | IO | IO | P0[5] | Analog column mux input and column output. |
| 3 | IO | IO | P0[3] | Analog column mux input and column output. |
| 4 | IO | I | P0[1] | Analog column mux input. |
| 5 | IO | | P2[7] | |
| 6 | IO | | P2[5] | |
| 7 | IO | I | P2[3] | Direct switched capacitor block input. |
| 8 | IO | I | P2[1] | Direct switched capacitor block input. |
| 9 | IO | | P4[7] | |
| 10 | IO | | P4[5] | |
| 11 | IO | | P4[3] | |
| 12 | IO | | P4[1] | |
| 13 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 14 | IO | | P3[7] | |
| 15 | IO | | P3[5] | |
| 16 | IO | | P3[3] | |
| 17 | IO | | P3[1] | |
| 18 | IO | | P5[3] | |
| 19 | IO | | P5[1] | |
| 20 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 21 | IO | | P1[5] | I2C Serial Data (SDA). |
| 22 | IO | | P1[3] | |
| 23 | IO | | P1[1] | Crystal (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 24 | Power | | Vss | Ground connection. |
| 25 | IO | | P1[0] | Crystal (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 26 | IO | | P1[2] | |
| 27 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 28 | IO | | P1[6] | |
| 29 | IO | | P5[0] | |
| 30 | IO | | P5[2] | |
| 31 | IO | | P3[0] | |
| 32 | IO | | P3[2] | |
| 33 | IO | | P3[4] | |
| 34 | IO | | P3[6] | |
| 35 | Input | | XRES | Active high external reset with internal pull down. |
| 36 | IO | | P4[0] | |
| 37 | IO | | P4[2] | |
| 38 | IO | | P4[4] | |
| 39 | IO | | P4[6] | |
| 40 | IO | I | P2[0] | Direct switched capacitor block input. |
| 41 | IO | I | P2[2] | Direct switched capacitor block input. |
| 42 | IO | | P2[4] | External Analog Ground (AGND). |
| 43 | IO | | P2[6] | External Voltage Reference (VREF). |
| 44 | IO | I | P0[0] | Analog column mux input. |
| 45 | IO | IO | P0[2] | Analog column mux input and column output. |
| 46 | IO | IO | P0[4] | Analog column mux input and column output. |
| 47 | IO | I | P0[6] | Analog column mux input. |
| 48 | Power | | Vdd | Supply voltage. |

LEGEND: A = Analog, I = Input, and O = Output.
 * These are the ISSP pins, which are not High Z at POR (Power On Reset).

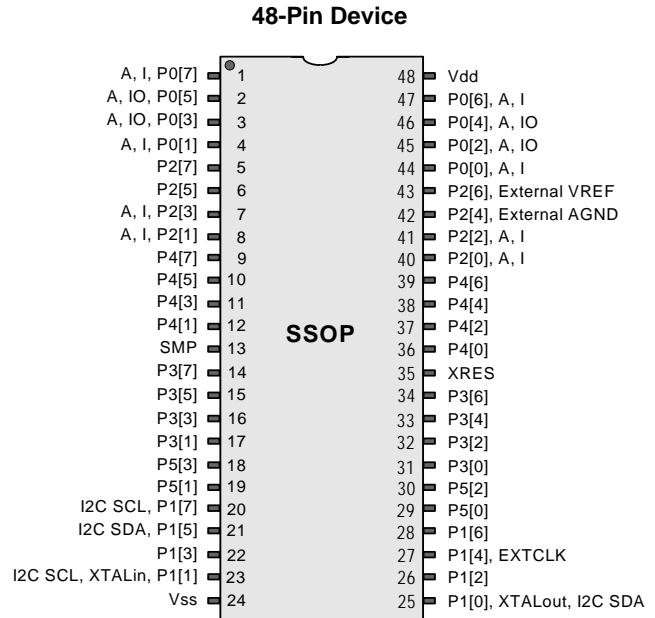


Table 4. 48-Pin Part Pinout (QFN**)

| Pin No. | Type | | Pin Name | Description |
|---------|---------|--------|----------|--|
| | Digital | Analog | | |
| 1 | IO | I | P2[3] | Direct switched capacitor block input. |
| 2 | IO | I | P2[1] | Direct switched capacitor block input. |
| 3 | IO | | P4[7] | |
| 4 | IO | | P4[5] | |
| 5 | IO | | P4[3] | |
| 6 | IO | | P4[1] | |
| 7 | Power | | SMP | Switch Mode Pump (SMP) connection to external components required. |
| 8 | IO | | P3[7] | |
| 9 | IO | | P3[5] | |
| 10 | IO | | P3[3] | |
| 11 | IO | | P3[1] | |
| 12 | IO | | P5[3] | |
| 13 | IO | | P5[1] | |
| 14 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 15 | IO | | P1[5] | I2C Serial Data (SDA). |
| 16 | IO | | P1[3] | |
| 17 | IO | | P1[1] | Crystal (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 18 | Power | | Vss | Ground connection. |
| 19 | IO | | P1[0] | Crystal (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 20 | IO | | P1[2] | |
| 21 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 22 | IO | | P1[6] | |
| 23 | IO | | P5[0] | |
| 24 | IO | | P5[2] | |
| 25 | IO | | P3[0] | |
| 26 | IO | | P3[2] | |
| 27 | IO | | P3[4] | |
| 28 | IO | | P3[6] | |
| 29 | Input | | XRES | Active high external reset with internal pull down. |
| 30 | IO | | P4[0] | |
| 31 | IO | | P4[2] | |
| 32 | IO | | P4[4] | |
| 33 | IO | | P4[6] | |
| 34 | IO | I | P2[0] | Direct switched capacitor block input. |
| 35 | IO | I | P2[2] | Direct switched capacitor block input. |
| 36 | IO | | P2[4] | External Analog Ground (AGND). |
| 37 | IO | | P2[6] | External Voltage Reference (VREF). |
| 38 | IO | I | P0[0] | Analog column mux input. |
| 39 | IO | IO | P0[2] | Analog column mux input and column output. |
| 40 | IO | IO | P0[4] | Analog column mux input and column output. |
| 41 | IO | I | P0[6] | Analog column mux input. |
| 42 | Power | | Vdd | Supply voltage. |
| 43 | IO | I | P0[7] | Analog column mux input. |
| 44 | IO | IO | P0[5] | Analog column mux input and column output. |
| 45 | IO | IO | P0[3] | Analog column mux input and column output. |

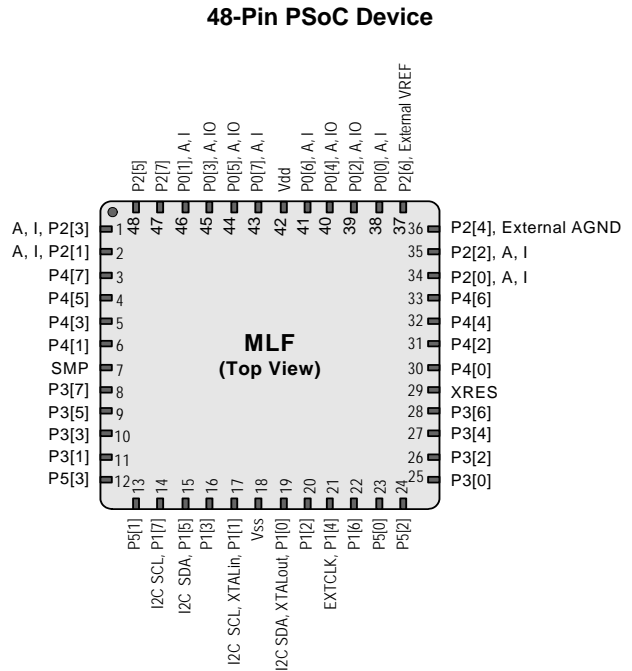


Table 4. 48-Pin Part Pinout (QFN**)

| | | | | |
|----|----|---|-------|--------------------------|
| 46 | IO | I | P0[1] | Analog column mux input. |
| 47 | IO | | P2[7] | |
| 48 | IO | | P2[5] | |

LEGEND: A = Analog, I = Input, and O = Output.

* These are the ISSP pins, which are not High Z at POR (Power On Reset).

** The QFN package has a center pad that must be connected to ground (Vss).

Register Reference

Register Conventions

Abbreviations Used

The register conventions specific to this section are listed in the following table.

| Convention | Description |
|------------|------------------------------|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

Register Mapping Tables

This chapter lists the registers of the CY8CLED16 EZ-Color device.

The device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XO1 bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XO1 bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Table 5. Register Map Bank 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---------|--------------|--------|----------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT0DR | 00 | RW | DBB20DR0 | 40 | # | ASC10CR0 | 80 | RW | RD12RI | C0 | RW |
| PRT0IE | 01 | RW | DBB20DR1 | 41 | W | ASC10CR1 | 81 | RW | RD12SYN | C1 | RW |
| PRT0GS | 02 | RW | DBB20DR2 | 42 | RW | ASC10CR2 | 82 | RW | RD12IS | C2 | RW |
| PRT0DM2 | 03 | RW | DBB20CR0 | 43 | # | ASC10CR3 | 83 | RW | RD12LT0 | C3 | RW |
| PRT1DR | 04 | RW | DBB21DR0 | 44 | # | ASD11CR0 | 84 | RW | RD12LT1 | C4 | RW |
| PRT1IE | 05 | RW | DBB21DR1 | 45 | W | ASD11CR1 | 85 | RW | RD12RO0 | C5 | RW |
| PRT1GS | 06 | RW | DBB21DR2 | 46 | RW | ASD11CR2 | 86 | RW | RD12RO1 | C6 | RW |
| PRT1DM2 | 07 | RW | DBB21CR0 | 47 | # | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DR | 08 | RW | DCB22DR0 | 48 | # | ASC12CR0 | 88 | RW | RD13RI | C8 | RW |
| PRT2IE | 09 | RW | DCB22DR1 | 49 | W | ASC12CR1 | 89 | RW | RD13SYN | C9 | RW |
| PRT2GS | 0A | RW | DCB22DR2 | 4A | RW | ASC12CR2 | 8A | RW | RD13IS | CA | RW |
| PRT2DM2 | 0B | RW | DCB22CR0 | 4B | # | ASC12CR3 | 8B | RW | RD13LT0 | CB | RW |
| PRT3DR | 0C | RW | DCB23DR0 | 4C | # | ASD13CR0 | 8C | RW | RD13LT1 | CC | RW |
| PRT3IE | 0D | RW | DCB23DR1 | 4D | W | ASD13CR1 | 8D | RW | RD13RO0 | CD | RW |
| PRT3GS | 0E | RW | DCB23DR2 | 4E | RW | ASD13CR2 | 8E | RW | RD13RO1 | CE | RW |
| PRT3DM2 | 0F | RW | DCB23CR0 | 4F | # | ASD13CR3 | 8F | RW | | CF | |
| PRT4DR | 10 | RW | DBB30DR0 | 50 | # | ASD20CR0 | 90 | RW | CUR_PP | D0 | RW |
| PRT4IE | 11 | RW | DBB30DR1 | 51 | W | ASD20CR1 | 91 | RW | STK_PP | D1 | RW |
| PRT4GS | 12 | RW | DBB30DR2 | 52 | RW | ASD20CR2 | 92 | RW | | D2 | |
| PRT4DM2 | 13 | RW | DBB30CR0 | 53 | # | ASD20CR3 | 93 | RW | IDX_PP | D3 | RW |
| PRT5DR | 14 | RW | DBB31DR0 | 54 | # | ASC21CR0 | 94 | RW | MVR_PP | D4 | RW |
| PRT5IE | 15 | RW | DBB31DR1 | 55 | W | ASC21CR1 | 95 | RW | MVW_PP | D5 | RW |
| PRT5GS | 16 | RW | DBB31DR2 | 56 | RW | ASC21CR2 | 96 | RW | I2C_CFG | D6 | RW |
| PRT5DM2 | 17 | RW | DBB31CR0 | 57 | # | ASC21CR3 | 97 | RW | I2C_SCR | D7 | # |
| PRT6DR | 18 | RW | DCB32DR0 | 58 | # | ASD22CR0 | 98 | RW | I2C_DR | D8 | RW |
| PRT6IE | 19 | RW | DCB32DR1 | 59 | W | ASD22CR1 | 99 | RW | I2C_MSCR | D9 | # |
| PRT6GS | 1A | RW | DCB32DR2 | 5A | RW | ASD22CR2 | 9A | RW | INT_CLR0 | DA | RW |
| PRT6DM2 | 1B | RW | DCB32CR0 | 5B | # | ASD22CR3 | 9B | RW | INT_CLR1 | DB | RW |
| PRT7DR | 1C | RW | DCB33DR0 | 5C | # | ASC23CR0 | 9C | RW | INT_CLR2 | DC | RW |
| PRT7IE | 1D | RW | DCB33DR1 | 5D | W | ASC23CR1 | 9D | RW | INT_CLR3 | DD | RW |

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Table 5. Register Map Bank 0 Table: User Space (continued)

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|----------|--------------|--------|----------|--------------|--------|----------|--------------|--------|----------|--------------|--------|
| PRT7GS | 1E | RW | DCB33DR2 | 5E | RW | ASC23CR2 | 9E | RW | INT_MSK3 | DE | RW |
| PRT7DM2 | 1F | RW | DCB33CR0 | 5F | # | ASC23CR3 | 9F | RW | INT_MSK2 | DF | RW |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | | 61 | | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | | 62 | | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | ARF_CR | 63 | RW | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | DEC_DH | E4 | RC |
| DBB01DR1 | 25 | W | ASY_CR | 65 | # | | A5 | | DEC_DL | E5 | RC |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | | 68 | | MUL1_X | A8 | W | MUL0_X | E8 | W |
| DCB02DR1 | 29 | W | | 69 | | MUL1_Y | A9 | W | MUL0_Y | E9 | W |
| DCB02DR2 | 2A | RW | | 6A | | MUL1_DH | AA | R | MUL0_DH | EA | R |
| DCB02CR0 | 2B | # | | 6B | | MUL1_DL | AB | R | MUL0_DL | EB | R |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | ACC1_DR1 | AC | RW | ACC0_DR1 | EC | RW |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | ACC1_DR0 | AD | RW | ACC0_DR0 | ED | RW |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | ACC1_DR3 | AE | RW | ACC0_DR3 | EE | RW |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | ACC1_DR2 | AF | RW | ACC0_DR2 | EF | RW |
| DBB10DR0 | 30 | # | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| DBB10DR1 | 31 | W | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| DBB10DR2 | 32 | RW | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| DBB10CR0 | 33 | # | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBB11DR0 | 34 | # | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| DBB11DR1 | 35 | W | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| DBB11DR2 | 36 | RW | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| DBB11CR0 | 37 | # | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12DR0 | 38 | # | ACB02CR3 | 78 | RW | RDI1RI | B8 | RW | | F8 | |
| DCB12DR1 | 39 | W | ACB02CR0 | 79 | RW | RDI1SYN | B9 | RW | | F9 | |
| DCB12DR2 | 3A | RW | ACB02CR1 | 7A | RW | RDI1IS | BA | RW | | FA | |
| DCB12CR0 | 3B | # | ACB02CR2 | 7B | RW | RDI1LT0 | BB | RW | | FB | |
| DCB13DR0 | 3C | # | ACB03CR3 | 7C | RW | RDI1LT1 | BC | RW | | FC | |
| DCB13DR1 | 3D | W | ACB03CR0 | 7D | RW | RDI1RO0 | BD | RW | | FD | |
| DCB13DR2 | 3E | RW | ACB03CR1 | 7E | RW | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| DCB13CR0 | 3F | # | ACB03CR2 | 7F | RW | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space

| Name | Addr(1,Hex) | Access | Name | Addr(1,Hex) | Access | Name | Addr(1,Hex) | Access | Name | Addr(1,Hex) | Access |
|---------|-------------|--------|---------|-------------|--------|----------|-------------|--------|----------|-------------|--------|
| PRT0DM0 | 00 | RW | DBB20FN | 40 | RW | ASC10CR0 | 80 | RW | RDI2RI | C0 | RW |
| PRT0DM1 | 01 | RW | DBB20IN | 41 | RW | ASC10CR1 | 81 | RW | RDI2SYN | C1 | RW |
| PRT0IC0 | 02 | RW | DBB20OU | 42 | RW | ASC10CR2 | 82 | RW | RDI2IS | C2 | RW |
| PRT0IC1 | 03 | RW | | 43 | | ASC10CR3 | 83 | RW | RDI2LT0 | C3 | RW |
| PRT1DM0 | 04 | RW | DBB21FN | 44 | RW | ASD11CR0 | 84 | RW | RDI2LT1 | C4 | RW |
| PRT1DM1 | 05 | RW | DBB21IN | 45 | RW | ASD11CR1 | 85 | RW | RDI2RO0 | C5 | RW |
| PRT1IC0 | 06 | RW | DBB21OU | 46 | RW | ASD11CR2 | 86 | RW | RDI2RO1 | C6 | RW |
| PRT1IC1 | 07 | RW | | 47 | | ASD11CR3 | 87 | RW | | C7 | |
| PRT2DM0 | 08 | RW | DCB22FN | 48 | RW | ASC12CR0 | 88 | RW | RDI3RI | C8 | RW |
| PRT2DM1 | 09 | RW | DCB22IN | 49 | RW | ASC12CR1 | 89 | RW | RDI3SYN | C9 | RW |
| PRT2IC0 | 0A | RW | DCB22OU | 4A | RW | ASC12CR2 | 8A | RW | RDI3IS | CA | RW |
| PRT2IC1 | 0B | RW | | 4B | | ASC12CR3 | 8B | RW | RDI3LT0 | CB | RW |
| PRT3DM0 | 0C | RW | DCB23FN | 4C | RW | ASD13CR0 | 8C | RW | RDI3LT1 | CC | RW |
| PRT3DM1 | 0D | RW | DCB23IN | 4D | RW | ASD13CR1 | 8D | RW | RDI3RO0 | CD | RW |
| PRT3IC0 | 0E | RW | DCB23OU | 4E | RW | ASD13CR2 | 8E | RW | RDI3RO1 | CE | RW |
| PRT3IC1 | 0F | RW | | 4F | | ASD13CR3 | 8F | RW | | CF | |
| PRT4DM0 | 10 | RW | DBB30FN | 50 | RW | ASD20CR0 | 90 | RW | GDI_O_IN | D0 | RW |
| PRT4DM1 | 11 | RW | DBB30IN | 51 | RW | ASD20CR1 | 91 | RW | GDI_E_IN | D1 | RW |
| PRT4IC0 | 12 | RW | DBB30OU | 52 | RW | ASD20CR2 | 92 | RW | GDI_O_OU | D2 | RW |
| PRT4IC1 | 13 | RW | | 53 | | ASD20CR3 | 93 | RW | GDI_E_OU | D3 | RW |
| PRT5DM0 | 14 | RW | DBB31FN | 54 | RW | ASC21CR0 | 94 | RW | | D4 | |
| PRT5DM1 | 15 | RW | DBB31IN | 55 | RW | ASC21CR1 | 95 | RW | | D5 | |
| PRT5IC0 | 16 | RW | DBB31OU | 56 | RW | ASC21CR2 | 96 | RW | | D6 | |
| PRT5IC1 | 17 | RW | | 57 | | ASC21CR3 | 97 | RW | | D7 | |

Blank fields are Reserved and should not be accessed.

Access is bit specific.

Table 6. Register Map Bank 1 Table: Configuration Space (continued)

| Name | Addr(1,Hex) | Access | Name | Addr(1,Hex) | Access | Name | Addr(1,Hex) | Access | Name | Addr(1,Hex) | Access |
|---------|-------------|--------|----------|-------------|--------|----------|-------------|--------|-----------|-------------|--------|
| PRT6DM0 | 18 | RW | DCB32FN | 58 | RW | ASD22CR0 | 98 | RW | | D8 | |
| PRT6DM1 | 19 | RW | DCB32IN | 59 | RW | ASD22CR1 | 99 | RW | | D9 | |
| PRT6IC0 | 1A | RW | DCB32OU | 5A | RW | ASD22CR2 | 9A | RW | | DA | |
| PRT6IC1 | 1B | RW | | 5B | | ASD22CR3 | 9B | RW | | DB | |
| PRT7DM0 | 1C | RW | DCB33FN | 5C | RW | ASC23CR0 | 9C | RW | | DC | |
| PRT7DM1 | 1D | RW | DCB33IN | 5D | RW | ASC23CR1 | 9D | RW | OSC_GO_EN | DD | RW |
| PRT7IC0 | 1E | RW | DCB33OU | 5E | RW | ASC23CR2 | 9E | RW | OSC_CR4 | DE | RW |
| PRT7IC1 | 1F | RW | | 5F | | ASC23CR3 | 9F | RW | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | | 64 | | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | | E5 | |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | | E6 | |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | DEC_CR2 | E7 | RW |
| DCB02FN | 28 | RW | ALT_CR1 | 68 | RW | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | CLK_CR2 | 69 | RW | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | | 6B | | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| DBB10FN | 30 | RW | ACB00CR3 | 70 | RW | RDI0RI | B0 | RW | | F0 | |
| DBB10IN | 31 | RW | ACB00CR0 | 71 | RW | RDI0SYN | B1 | RW | | F1 | |
| DBB10OU | 32 | RW | ACB00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACB00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| DBB11FN | 34 | RW | ACB01CR3 | 74 | RW | RDI0LT1 | B4 | RW | | F4 | |
| DBB11IN | 35 | RW | ACB01CR0 | 75 | RW | RDI0RO0 | B5 | RW | | F5 | |
| DBB11OU | 36 | RW | ACB01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACB01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| DCB12FN | 38 | RW | ACB02CR3 | 78 | RW | RDI1RI | B8 | RW | | F8 | |
| DCB12IN | 39 | RW | ACB02CR0 | 79 | RW | RDI1SYN | B9 | RW | | F9 | |
| DCB12OU | 3A | RW | ACB02CR1 | 7A | RW | RDI1IS | BA | RW | FLS_PR1 | FA | RW |
| | 3B | | ACB02CR2 | 7B | RW | RDI1LT0 | BB | RW | | FB | |
| DCB13FN | 3C | RW | ACB03CR3 | 7C | RW | RDI1LT1 | BC | RW | | FC | |
| DCB13IN | 3D | RW | ACB03CR0 | 7D | RW | RDI1RO0 | BD | RW | | FD | |
| DCB13OU | 3E | RW | ACB03CR1 | 7E | RW | RDI1RO1 | BE | RW | CPU_SCR1 | FE | # |
| | 3F | | ACB03CR2 | 7F | RW | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and should not be accessed.

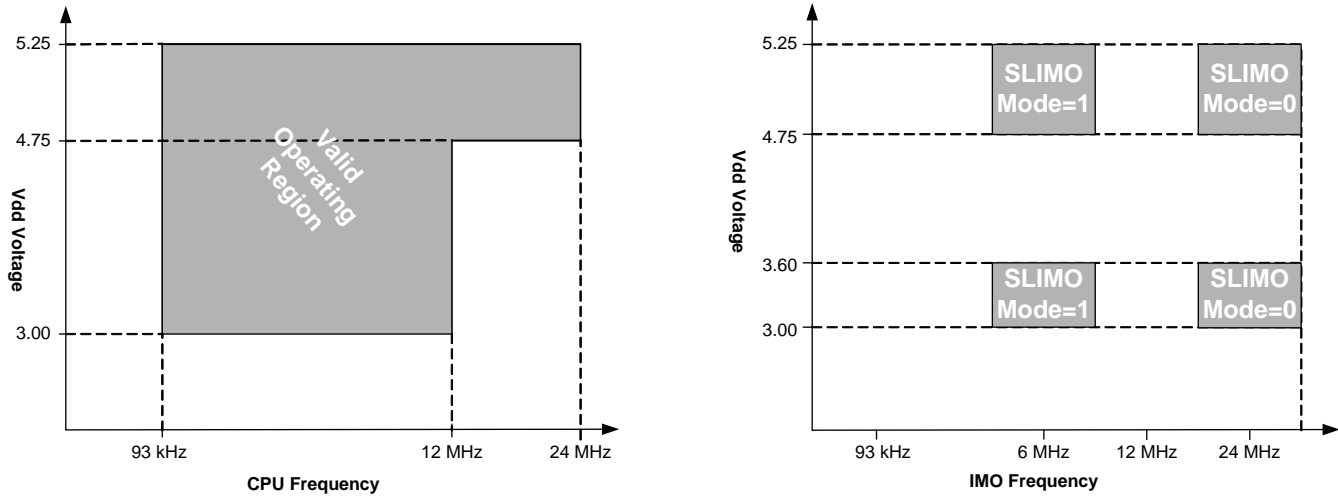
Access is bit specific.

Electrical Specifications

This chapter presents the DC and AC electrical specifications of the CY8CLED16 EZ-Color device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at <http://www.cypress.com/ez-color>.

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Refer to Table 23 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 4. Voltage versus CPU Frequency, and IMO Frequency Trim Options



The following table lists the units of measure that are used in this chapter.

Table 7. Units of Measure

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------------------|-----------------------------|---------------|-------------------------------|
| $^{\circ}\text{C}$ | degree Celsius | μW | microwatts |
| dB | decibels | mA | milli-ampere |
| fF | femto farad | ms | milli-second |
| Hz | hertz | mV | milli-volts |
| KB | 1024 bytes | nA | nanoampere |
| Kbit | 1024 bits | ns | nanosecond |
| kHz | kilohertz | nV | nanovolts |
| k Ω | kilohm | Ω | ohm |
| MHz | megahertz | pA | picoampere |
| M Ω | megaohm | pF | picofarad |
| μA | microampere | pp | peak-to-peak |
| μF | microfarad | ppm | parts per million |
| μH | microhenry | ps | picosecond |
| μs | microsecond | sps | samples per second |
| μV | microvolts | σ | sigma: one standard deviation |
| μVrms | microvolts root-mean-square | V | volts |

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|---|-----------------------|-----|-----------------------|-------|---|
| T _{STG} | Storage Temperature | -55 | 25 | +100 | °C | Higher storage temperatures will reduce data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C will degrade reliability. |
| T _A | Ambient Temperature with Power Applied | -40 | – | +85 | °C | |
| V _{DD} | Supply Voltage on V _{DD} Relative to V _{SS} | -0.5 | – | +6.0 | V | |
| V _{IO} | DC Input Voltage | V _{SS} - 0.5 | – | V _{DD} + 0.5 | V | |
| V _{IOZ} | DC Voltage Applied to Tri-state | V _{SS} - 0.5 | – | V _{DD} + 0.5 | V | |
| I _{MIO} | Maximum Current into any Port Pin | -25 | – | +50 | mA | |
| I _{MAIO} | Maximum Current into any Port Pin Configured as Analog Driver | -50 | – | +50 | mA | |
| ESD | Electro Static Discharge Voltage | 2000 | – | – | V | Human Body Model ESD. |
| LU | Latch-up Current | – | – | 200 | mA | |

Operating Temperature

Table 9. Operating Temperature

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------|----------------------|-----|-----|------|-------|--|
| T _A | Ambient Temperature | -40 | – | +85 | °C | |
| T _J | Junction Temperature | -40 | – | +100 | °C | The temperature rise from ambient to junction is package specific. See "Thermal Impedances per Package" on page 36. The user must limit the power consumption to comply with this requirement. |

DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 10. DC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|---|------|-----|------|-------|---|
| V _{DD} | Supply Voltage | 3.00 | – | 5.25 | V | See DC POR and LVD specifications, Table 3-15 on page 27. |
| I _{DD} | Supply Current | – | 8 | 14 | mA | Conditions are 5.0V, T _A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz. |
| I _{DD3} | Supply Current | – | 5 | 9 | mA | Conditions are V _{DD} = 3.3V, T _A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz. |
| I _{DDP} | Supply current when IMO = 6 MHz using SLIMO mode. | – | 2 | 3 | mA | Conditions are V _{DD} = 3.3V, T _A = 25 °C, CPU = 0.75 MHz, SYSCLK doubler disabled, VC1 = 0.375 MHz, VC2 = 23.44 kHz, VC3 = 0.09 kHz. |
| I _{SB} | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. | – | 3 | 10 | μA | Conditions are with internal slow speed oscillator, V _{DD} = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$. |
| I _{SBH} | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. | – | 4 | 25 | μA | Conditions are with internal slow speed oscillator, V _{DD} = 3.3V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$. |
| I _{SBXTL} | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, internal slow oscillator, and 32 kHz crystal oscillator active. | – | 4 | 12 | μA | Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3V, $-40^{\circ}\text{C} \leq T_A \leq 55^{\circ}\text{C}$. |
| I _{SBXTLH} | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and 32 kHz crystal oscillator active. | – | 5 | 27 | μA | Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. V _{DD} = 3.3V, $55^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$. |
| V _{REF} | Reference Voltage (Bandgap) | 1.28 | 1.3 | 1.32 | V | Trimmed for appropriate V _{DD} . |

DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 11. DC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------------|-----------------------------------|-----------------------|-----|------|-------|--|
| R _{PU} | Pull up Resistor | 4 | 5.6 | 8 | kΩ | |
| R _{PD} | Pull down Resistor | 4 | 5.6 | 8 | kΩ | |
| V _{OH} | High Output Level | V _{DD} - 1.0 | – | – | V | I _{OH} = 10 mA, V _{DD} = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget. |
| V _{OL} | Low Output Level | – | – | 0.75 | V | I _{OL} = 25 mA, V _{DD} = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined IOL budget. |
| V _{IL} | Input Low Level | – | – | 0.8 | V | V _{DD} = 3.0 to 5.25. |
| V _{IH} | Input High Level | 2.1 | – | – | V | V _{DD} = 3.0 to 5.25. |
| V _H | Input Hysteresis | – | 60 | – | mV | |
| I _{IL} | Input Leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 μA. |
| C _{IN} | Capacitive Load on Pins as Input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |
| C _{OUT} | Capacitive Load on Pins as Output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |

DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 12. 5V DC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------------|---|-----------------------|------|-----------------------|--------------------------------|---|
| V _{OSOA} | Input Offset Voltage (absolute value) | | | | | |
| | Power = Low, Opamp Bias = High | – | 1.6 | 10 | mV | |
| | Power = Medium, Opamp Bias = High | – | 1.3 | 8 | mV | |
| | Power = High, Opamp Bias = High | – | 1.2 | 7.5 | mV | |
| TCV _{OSOA} | Average Input Offset Voltage Drift | – | 7.0 | 35.0 | $\mu\text{V}/^{\circ}\text{C}$ | |
| I _{EBOA} | Input Leakage Current (Port 0 Analog Pins) | – | 200 | – | pA | Gross tested to 1 μA . |
| C _{INOA} | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C . |
| V _{CMOA} | Common Mode Voltage Range. All Cases, except high-est. Power = High, Opamp Bias = High | 0.0 | – | V _{dd} | V | |
| | | 0.5 | – | V _{dd} - 0.5 | V | |
| CMRR _{OA} | Common Mode Rejection Ratio | 60 | – | – | dB | |
| G _{OLOA} | Open Loop Gain | 80 | – | – | dB | |
| V _{OHIGHOA} | High Output Voltage Swing (internal signals) | V _{dd} - .01 | – | – | V | |
| V _{OLOWOA} | Low Output Voltage Swing (internal signals) | – | – | 0.1 | V | |
| I _{SOA} | Supply Current (including associated AGND buffer) | | | | | |
| | Power = Low, Opamp Bias = Low | – | 150 | 200 | μA | |
| | Power = Low, Opamp Bias = High | – | 300 | 400 | μA | |
| | Power = Medium, Opamp Bias = Low | – | 600 | 800 | μA | |
| | Power = Medium, Opamp Bias = High | – | 1200 | 1600 | μA | |
| | Power = High, Opamp Bias = Low | – | 2400 | 3200 | μA | |
| | Power = High, Opamp Bias = High | – | 4600 | 6400 | μA | |
| PSRR _{OA} | Supply Voltage Rejection Ratio | 67 | 80 | – | dB | V _{ss} \leq VIN \leq (V _{dd} - 2.25) or (V _{dd} - 1.25V) \leq VIN \leq V _{dd} . |

Table 13. 3.3V DC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------------|--|-----------------------|------|-----------------|--------------------------------|--|
| V _{OSOA} | Input Offset Voltage (absolute value) | | | | | |
| | Power = Low, Opamp Bias = High | – | 1.65 | 10 | mV | |
| | Power = Medium, Opamp Bias = High | – | 1.32 | 8 | mV | |
| | High Power is 5 Volts Only | | | | | |
| TCV _{OSOA} | Average Input Offset Voltage Drift | – | 7.0 | 35.0 | $\mu\text{V}/^{\circ}\text{C}$ | |
| I _{EBOA} | Input Leakage Current (Port 0 Analog Pins) | – | 200 | – | pA | Gross tested to 1 μA . |
| C _{INOA} | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C . |
| V _{CMOA} | Common Mode Voltage Range | 0 | – | V _{dd} | V | |
| CMRR _{OA} | Common Mode Rejection Ratio | 60 | – | – | dB | |
| G _{OLOA} | Open Loop Gain | 80 | – | – | dB | |
| V _{OHIGHOA} | High Output Voltage Swing (internal signals) | V _{dd} - .01 | – | – | V | |
| V _{OLOWOA} | Low Output Voltage Swing (internal signals) | – | – | .01 | V | |

Table 13. 3.3V DC Operational Amplifier Specifications (continued)

| | | | | | | |
|-------------|---|----|------|------|---------|---|
| I_{SOA} | Supply Current (including associated AGND buffer) | | | | | |
| | Power = Low, Opamp Bias = Low | – | 150 | 200 | μA | |
| | Power = Low, Opamp Bias = High | – | 300 | 400 | μA | |
| | Power = Medium, Opamp Bias = Low | – | 600 | 800 | μA | |
| | Power = Medium, Opamp Bias = High | – | 1200 | 1600 | μA | |
| | Power = High, Opamp Bias = Low | – | 2400 | 3200 | μA | |
| | Power = High, Opamp Bias = High | – | – | – | | Not Allowed |
| $PSRR_{OA}$ | Supply Voltage Rejection Ratio | 54 | 80 | – | dB | $V_{SS} \leq V_{IN} \leq (V_{DD} - 2.25)$ or $(V_{DD} - 1.25V) \leq V_{IN} \leq V_{DD}$ |

DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, 3.0V to 3.6V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, or 2.4V to 3.0V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 14. DC Low Power Comparator Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|--|-----|-----|--------------|---------|-------|
| V_{REFLPC} | Low power comparator (LPC) reference voltage range | 0.2 | – | $V_{DD} - 1$ | V | |
| I_{SLPC} | LPC supply current | – | 10 | 40 | μA | |
| V_{OSLPC} | LPC voltage offset | – | 2.5 | 30 | mV | |

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, or 3.0V to 3.6V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 15. 5V DC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------|---|---------------------------|-----|---------------------------|-------------------|-------|
| V_{OSOB} | Input Offset Voltage (Absolute Value) | – | 3 | 12 | mV | |
| TCV_{OSOB} | Average Input Offset Voltage Drift | – | +6 | – | $\mu V/^{\circ}C$ | |
| V_{CMOB} | Common-Mode Input Voltage Range | 0.5 | – | $V_{DD} - 1.0$ | V | |
| R_{OUTOB} | Output Resistance | | | | | |
| | Power = Low | – | – | 1 | Ω | |
| | Power = High | – | – | 1 | Ω | |
| $V_{OHIGHOB}$ | High Output Voltage Swing (Load = 32 ohms to $V_{DD}/2$) | | | | | |
| | Power = Low | $0.5 \times V_{DD} + 1.3$ | – | – | V | |
| | Power = High | $0.5 \times V_{DD} + 1.3$ | – | – | V | |
| V_{LOWOB} | Low Output Voltage Swing (Load = 32 ohms to $V_{DD}/2$) | | | | | |
| | Power = Low | – | – | $0.5 \times V_{DD} - 1.3$ | V | |
| | Power = High | – | – | $0.5 \times V_{DD} - 1.3$ | V | |
| I_{SOB} | Supply Current Including Bias Cell (No Load) | | | | | |
| | Power = Low | – | 1.1 | 2 | mA | |
| | Power = High | – | 2.6 | 5 | mA | |
| $PSRR_{OB}$ | Supply Voltage Rejection Ratio | 40 | 64 | – | dB | |

Table 16. 3.3V DC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|----------------------|---|--|------------|--|----------|-------|
| V _{OSOB} | Input Offset Voltage (Absolute Value) | – | 3 | 12 | mV | |
| TCV _{OSOB} | Average Input Offset Voltage Drift | – | +6 | – | μV/°C | |
| V _{CMOB} | Common-Mode Input Voltage Range | 0.5 | - | V _{dd} - 1.0 | V | |
| R _{OUTOB} | Output Resistance Power = Low Power = High | – – | – – | 10 10 | Ω Ω | |
| V _{OHIGHOB} | High Output Voltage Swing (Load = 1k ohms to V _{dd} /2) Power = Low Power = High | 0.5 x V _{dd} + 1.0 0.5 x V _{dd} + 1.0 | – – | – – | V V | |
| V _{OLOWOB} | Low Output Voltage Swing (Load = 1k ohms to V _{dd} /2) Power = Low Power = High | – – | – – | 0.5 x V _{dd} - 1.0 0.5 x V _{dd} - 1.0 | V V | |
| I _{SOB} | Supply Current Including Bias Cell (No Load) Power = Low Power = High | – – | 0.8 2.0 | 1 5 | mA mA | |
| PSRR _{OB} | Supply Voltage Rejection Ratio | 60 | 64 | – | dB | |

DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 17. DC Switch Mode Pump (SMP) Specifications

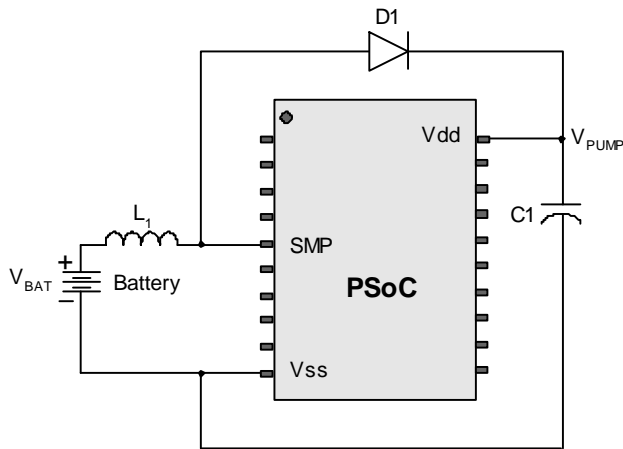
| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------------|---|--------|--------|--------|-----------------|--|
| V _{PUMP 5V} | 5V Output Voltage at V _{dd} from Pump | 4.75 | 5.0 | 5.25 | V | Configuration of footnote. ^a Average, neglecting ripple. SMP trip voltage is set to 5.0V. |
| V _{PUMP 3V} | 3V Output Voltage at V _{dd} from Pump | 3.00 | 3.25 | 3.60 | V | Configuration of footnote. ^a Average, neglecting ripple. SMP trip voltage is set to 3.25V. |
| I _{PUMP} | Available Output Current V _{BAT} = 1.5V, V _{PUMP} = 3.25V V _{BAT} = 1.8V, V _{PUMP} = 5.0V | 8 5 | – – | – – | mA mA | Configuration of footnote. ^a SMP trip voltage is set to 3.25V. SMP trip voltage is set to 5.0V. |
| V _{BAT5V} | Input Voltage Range from Battery | 1.8 | – | 5.0 | V | Configuration of footnote. ^a SMP trip voltage is set to 5.0V. |
| V _{BAT3V} | Input Voltage Range from Battery | 1.0 | – | 3.3 | V | Configuration of footnote. ^a SMP trip voltage is set to 3.25V. |
| V _{BATSTART} | Minimum Input Voltage from Battery to Start Pump | 1.2 | – | – | V | Configuration of footnote. ^a 0°C ≤ T _A ≤ 100. 1.25V at T _A = -40°C. |
| ΔV _{PUMP_Line} | Line Regulation (over V _{BAT} range) | – | 5 | – | %V _O | Configuration of footnote. ^a V _O is the “V _{dd} Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-15 on page 27. |
| ΔV _{PUMP_Load} | Load Regulation | – | 5 | – | %V _O | Configuration of footnote. ^a V _O is the “V _{dd} Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-15 on page 27. |
| ΔV _{PUMP_Ripple} | Output Voltage Ripple (depends on capacitor/load) | – | 100 | – | mVpp | Configuration of footnote. ^a Load is 5 mA. |
| E ₃ | Efficiency | 35 | 50 | – | % | Configuration of footnote. ^a Load is 5 mA. SMP trip voltage is set to 3.25V. |

Table 17. DC Switch Mode Pump (SMP) Specifications (continued)

| | | | | | | |
|--------------------|----------------------|---|-----|---|-----|--|
| F _{PUMP} | Switching Frequency | – | 1.4 | – | MHz | |
| DC _{PUMP} | Switching Duty Cycle | – | 50 | – | % | |

a. L₁ = 2 μH inductor, C₁ = 10 μF capacitor, D₁ = Schottky diode. See Figure 5.

Figure 5. Basic Switch Mode Pump Circuit



DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 18. 5V DC Analog Reference Specifications

| Symbol | Description | Min | Typ | Max | Units |
|------------------|--|----------------------------|---------------------------|----------------------------|-------|
| V _{BG5} | Bandgap Voltage Reference 5V | 1.28 | 1.30 | 1.32 | V |
| – | AGND = V _{dd} /2 ^a | V _{dd} /2 - 0.02 | V _{dd} /2 | V _{dd} /2 + 0.02 | V |
| – | AGND = 2 x BandGap ^a | 2.52 | 2.60 | 2.72 | V |
| – | AGND = P2[4] (P2[4] = V _{dd} /2) ^a | P2[4] - 0.013 | P2[4] | P2[4] + 0.013 | V |
| – | AGND = BandGap ^a | 1.27 | 1.3 | 1.34 | V |
| – | AGND = 1.6 x BandGap ^a | 2.03 | 2.08 | 2.13 | V |
| – | AGND Block to Block Variation (AGND = V _{dd} /2) ^a | -0.034 | 0.000 | 0.034 | V |
| – | RefHi = V _{dd} /2 + BandGap | V _{dd} /2 + 1.21 | V _{dd} /2 + 1.3 | V _{dd} /2 + 1.382 | V |
| – | RefHi = 3 x BandGap | 3.75 | 3.9 | 4.05 | V |
| – | RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V) | P2[6] + 2.478 | P2[6] + 2.6 | P2[6] + 2.722 | V |
| – | RefHi = P2[4] + BandGap (P2[4] = V _{dd} /2) | P2[4] + 1.218 | P2[4] + 1.3 | P2[4] + 1.382 | V |
| – | RefHi = P2[4] + P2[6] (P2[4] = V _{dd} /2, P2[6] = 1.3V) | P2[4] + P2[6] - 0.058 | P2[4] + P2[6] | P2[4] + P2[6] + 0.058 | V |
| – | RefHi = 2 x BandGap | 2.50 | 2.60 | 2.70 | V |
| – | RefHi = 3.2 x BandGap | 4.02 | 4.16 | 4.29 | V |
| – | RefLo = V _{dd} /2 - BandGap | V _{dd} /2 - 1.369 | V _{dd} /2 - 1.30 | V _{dd} /2 - 1.231 | V |
| – | RefLo = BandGap | 1.20 | 1.30 | 1.40 | V |
| – | RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V) | 2.489 - P2[6] | 2.6 - P2[6] | 2.711 - P2[6] | V |
| – | RefLo = P2[4] - BandGap (P2[4] = V _{dd} /2) | P2[4] - 1.368 | P2[4] - 1.30 | P2[4] - 1.232 | V |
| – | RefLo = P2[4] - P2[6] (P2[4] = V _{dd} /2, P2[6] = 1.3V) | P2[4] - P2[6] - 0.042 | P2[4] - P2[6] | P2[4] - P2[6] + 0.042 | V |

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.

Table 19. 3.3V DC Analog Reference Specifications

| Symbol | Description | Min | Typ | Max | Units |
|-------------------|--|---------------------------|--------------------|---------------------------|-------|
| V _{BG33} | Bandgap Voltage Reference 3.3V | 1.28 | 1.30 | 1.32 | V |
| – | AGND = V _{dd} /2 ^a | V _{dd} /2 - 0.02 | V _{dd} /2 | V _{dd} /2 + 0.02 | V |
| – | AGND = 2 x BandGap ^a | Not Allowed | | | |
| – | AGND = P2[4] (P2[4] = V _{dd} /2) | P2[4] - 0.009 | P2[4] | P2[4] + 0.009 | V |
| – | AGND = BandGap ^a | 1.27 | 1.30 | 1.34 | V |
| – | AGND = 1.6 x BandGap ^a | 2.03 | 2.08 | 2.13 | V |
| – | AGND Block to Block Variation (AGND = V _{dd} /2) ^a | -0.034 | 0.000 | 0.034 | mV |
| – | RefHi = V _{dd} /2 + BandGap | Not Allowed | | | |
| – | RefHi = 3 x BandGap | Not Allowed | | | |
| – | RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V) | Not Allowed | | | |
| – | RefHi = P2[4] + BandGap (P2[4] = V _{dd} /2) | Not Allowed | | | |
| – | RefHi = P2[4] + P2[6] (P2[4] = V _{dd} /2, P2[6] = 0.5V) | P2[4] + P2[6] - 0.042 | P2[4] + P2[6] | P2[4] + P2[6] + 0.042 | V |
| – | RefHi = 2 x BandGap | 2.50 | 2.60 | 2.70 | V |
| – | RefHi = 3.2 x BandGap | Not Allowed | | | |
| – | RefLo = V _{dd} /2 - BandGap | Not Allowed | | | |
| – | RefLo = BandGap | Not Allowed | | | |
| – | RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V) | Not Allowed | | | |
| – | RefLo = P2[4] - BandGap (P2[4] = V _{dd} /2) | Not Allowed | | | |
| – | RefLo = P2[4]-P2[6] (P2[4] = V _{dd} /2, P2[6] = 0.5V) | P2[4] - P2[6] - 0.036 | P2[4] - P2[6] | P2[4] - P2[6] + 0.036 | V |

a. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 20. DC Analog PSoC Block Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------|---------------------------------------|-----|------|-----|-------|-------|
| R _{CT} | Resistor Unit Value (Continuous Time) | – | 12.2 | – | kΩ | |
| C _{SC} | Capacitor Unit Value (Switch Cap) | – | 80 | – | fF | |

DC POR, SMP, and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 21. DC POR, SMP, and LVD Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|--|------|------|-------------------|-------|-------|
| V_{PPOR0R} | Vdd Value for PPOR Trip (positive ramp) PORLEV[1:0] = 00b | | 2.91 | | V | |
| V_{PPOR1R} | PORLEV[1:0] = 01b | – | 4.39 | – | V | |
| V_{PPOR2R} | PORLEV[1:0] = 10b | | 4.55 | | V | |
| V_{PPOR0} | Vdd Value for PPOR Trip (negative ramp) PORLEV[1:0] = 00b | | 2.82 | | V | |
| V_{PPOR1} | PORLEV[1:0] = 01b | – | 4.39 | – | V | |
| V_{PPOR2} | PORLEV[1:0] = 10b | | 4.55 | | V | |
| V_{PH0} | PPOR Hysteresis PORLEV[1:0] = 00b | – | 92 | – | mV | |
| V_{PH1} | PORLEV[1:0] = 01b | – | 0 | – | mV | |
| V_{PH2} | PORLEV[1:0] = 10b | – | 0 | – | mV | |
| V_{LVD0} | Vdd Value for LVD Trip VM[2:0] = 000b | 2.86 | 2.92 | 2.98 ^a | V | |
| V_{LVD1} | VM[2:0] = 001b | 2.96 | 3.02 | 3.08 | V | |
| V_{LVD2} | VM[2:0] = 010b | 3.07 | 3.13 | 3.20 | V | |
| V_{LVD3} | VM[2:0] = 011b | 3.92 | 4.00 | 4.08 | V | |
| V_{LVD4} | VM[2:0] = 100b | 4.39 | 4.48 | 4.57 | V | |
| V_{LVD5} | VM[2:0] = 101b | 4.55 | 4.64 | 4.74 ^b | V | |
| V_{LVD6} | VM[2:0] = 110b | 4.63 | 4.73 | 4.82 | V | |
| V_{LVD7} | VM[2:0] = 111b | 4.72 | 4.81 | 4.91 | V | |
| V_{PUMP0} | Vdd Value for SMP Trip VM[2:0] = 000b | 2.96 | 3.02 | 3.08 | V | |
| V_{PUMP1} | VM[2:0] = 001b | 3.03 | 3.10 | 3.16 | V | |
| V_{PUMP2} | VM[2:0] = 010b | 3.18 | 3.25 | 3.32 | V | |
| V_{PUMP3} | VM[2:0] = 011b | 4.11 | 4.19 | 4.28 | V | |
| V_{PUMP4} | VM[2:0] = 100b | 4.55 | 4.64 | 4.74 | V | |
| V_{PUMP5} | VM[2:0] = 101b | 4.63 | 4.73 | 4.82 | V | |
| V_{PUMP6} | VM[2:0] = 110b | 4.72 | 4.82 | 4.91 | V | |
| V_{PUMP7} | VM[2:0] = 111b | 4.90 | 5.00 | 5.10 | V | |

- a. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
- b. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 22. DC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-----------------------|--|----------------|-----|-----------------|-------|--------------------------------------|
| I_{DDP} | Supply Current During Programming or Verify | – | 10 | 30 | mA | |
| V_{ILP} | Input Low Voltage During Programming or Verify | – | – | 0.8 | V | |
| V_{IHP} | Input High Voltage During Programming or Verify | 2.2 | – | – | V | |
| I_{ILP} | Input Current when Applying V_{ilp} to P1[0] or P1[1] During Programming or Verify | – | – | 0.2 | mA | Driving internal pull-down resistor. |
| I_{IHP} | Input Current when Applying V_{ihp} to P1[0] or P1[1] During Programming or Verify | – | – | 1.5 | mA | Driving internal pull-down resistor. |
| V_{OLV} | Output Low Voltage During Programming or Verify | – | – | $V_{SS} + 0.75$ | V | |
| V_{OHV} | Output High Voltage During Programming or Verify | $V_{DD} - 1.0$ | – | V_{DD} | V | |
| Flash _{ENPB} | Flash Endurance (per block) | 50,000 | – | – | – | Erase/write cycles per block. |
| Flash _{ENT} | Flash Endurance (total) ^a | 1,800,000 | – | – | – | Erase/write cycles. |
| Flash _{DR} | Flash Data Retention | 10 | – | – | Years | |

- a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Note See the individual user module data sheets for information on maximum frequencies for user modules.

Table 23. AC Chip-Level Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------------|---|------|--------|-----------------------|-------|---|
| F _{IMO24} | Internal Main Oscillator Frequency for 24 MHz | 23.4 | 24 | 24.6 ^{a,b,c} | MHz | Trimmed for 5V or 3.3V operation using factory trim values. See the figure on page 19. SLIMO Mode = 0. |
| F _{IMO6} | Internal Main Oscillator Frequency for 6 MHz | 5.75 | 6 | 6.35 ^{a,b,c} | MHz | Trimmed for 5V or 3.3V operation using factory trim values. See the figure on page 19. SLIMO Mode = 1. |
| F _{CPU1} | CPU Frequency (5V Nominal) | 0.93 | 24 | 24.6 ^{a,b} | MHz | |
| F _{CPU2} | CPU Frequency (3.3V Nominal) | 0.93 | 12 | 12.3 ^{b,c} | MHz | |
| F _{48M} | Digital PSoc Block Frequency | 0 | 48 | 49.2 ^{a,b,d} | MHz | Refer to the AC Digital Block Specifications below. |
| F _{24M} | Digital PSoc Block Frequency | 0 | 24 | 24.6 ^{b,d} | MHz | |
| F _{32K1} | Internal Low Speed Oscillator Frequency | 15 | 32 | 64 | kHz | |
| F _{32K2} | External Crystal Oscillator | – | 32.768 | – | kHz | Accuracy is capacitor and crystal dependent. 50% duty cycle. |
| F _{PLL} | PLL Frequency | – | 23.986 | – | MHz | A multiple (x732) of crystal frequency. |
| Jitter24M2 | 24 MHz Period Jitter (PLL) | – | – | 600 | ps | |
| T _{PLLSLEW} | PLL Lock Time | 0.5 | – | 10 | ms | |
| T _{PLLSLEWLOW} | PLL Lock Time for Low Gain Setting | 0.5 | – | 50 | ms | |
| T _{OS} | External Crystal Oscillator Startup to 1% | – | 250 | 500 | ms | |
| T _{OSACC} | External Crystal Oscillator Startup to 100 ppm | – | 300 | 600 | ms | The crystal oscillator frequency is within 100 ppm of its final value by the end of the T _{OSACC} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ V _{dd} ≤ 5.5V, -40 °C ≤ T _A ≤ 85 °C. |
| Jitter32k | 32 kHz Period Jitter | – | 100 | – | ns | |
| T _{XRST} | External Reset Pulse Width | 10 | – | – | μs | |
| DC24M | 24 MHz Duty Cycle | 40 | 50 | 60 | % | |
| Step24M | 24 MHz Trim Step Size | – | 50 | – | kHz | |
| F _{out48M} | 48 MHz Output Frequency | 46.8 | 48.0 | 49.2 ^{a,c} | MHz | Trimmed. Utilizing factory trim values. |
| Jitter24M1 | 24 MHz Period Jitter (IMO) | – | 600 | – | ps | |
| F _{MAX} | Maximum frequency of signal on row input or row output. | – | – | 12.3 | MHz | |
| T _{RAMP} | Supply Ramp Time | 0 | – | – | μs | |

a. 4.75V < V_{dd} < 5.25V.

b. Accuracy derived from Internal Main Oscillator with appropriate trim for V_{dd} range.

c. 3.0V < V_{dd} < 3.6V. See Application Note AN2012 "Adjusting PSoc Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.

d. See the individual user module data sheets for information on maximum frequencies for user modules.

Figure 6. PLL Lock Timing Diagram

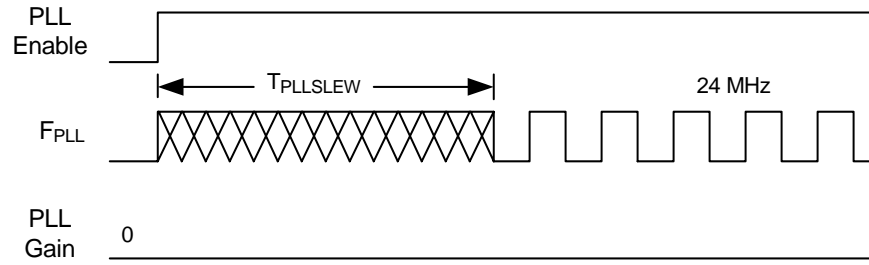


Figure 7. PLL Lock for Low Gain Setting Timing Diagram

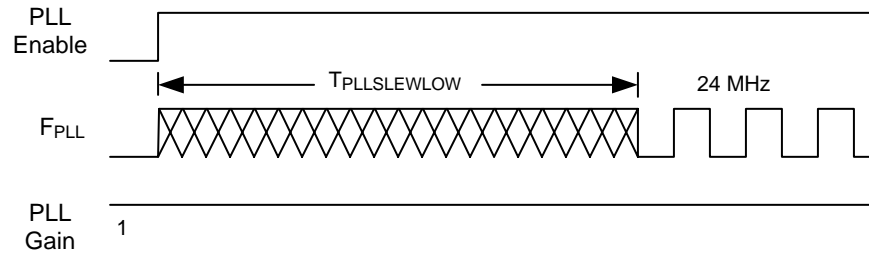


Figure 8. External Crystal Oscillator Startup Timing Diagram

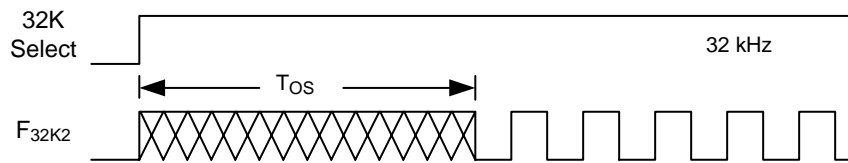


Figure 9. 24 MHz Period Jitter (IMO) Timing Diagram

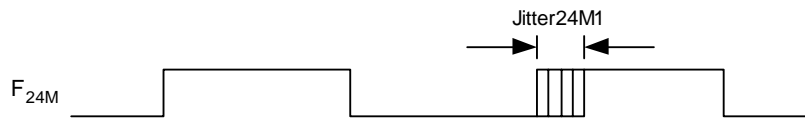
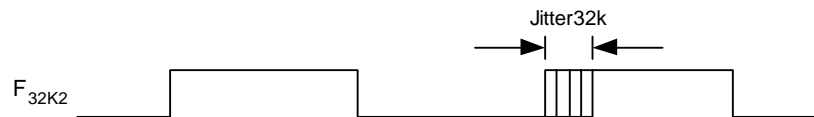


Figure 10. 32 kHz Period Jitter (ECO) Timing Diagram



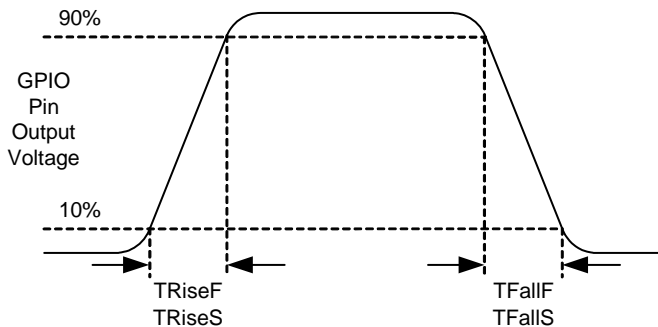
AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 24. AC GPIO Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|--------------|---|-----|-----|------|-------|--------------------------------|
| F_{GPIO} | GPIO Operating Frequency | 0 | – | 12.3 | MHz | Normal Strong Mode |
| TR_{riseF} | Rise Time, Normal Strong Mode, Clload = 50 pF | 3 | – | 18 | ns | Vdd = 4.75 to 5.25V, 10% - 90% |
| TF_{fallF} | Fall Time, Normal Strong Mode, Clload = 50 pF | 2 | – | 18 | ns | Vdd = 4.75 to 5.25V, 10% - 90% |
| TR_{riseS} | Rise Time, Slow Strong Mode, Clload = 50 pF | 10 | 27 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |
| TF_{fallS} | Fall Time, Slow Strong Mode, Clload = 50 pF | 10 | 22 | – | ns | Vdd = 3 to 5.25V, 10% - 90% |

Figure 11. GPIO Timing Diagram



AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 25. 5V AC Operational Amplifier Specifications

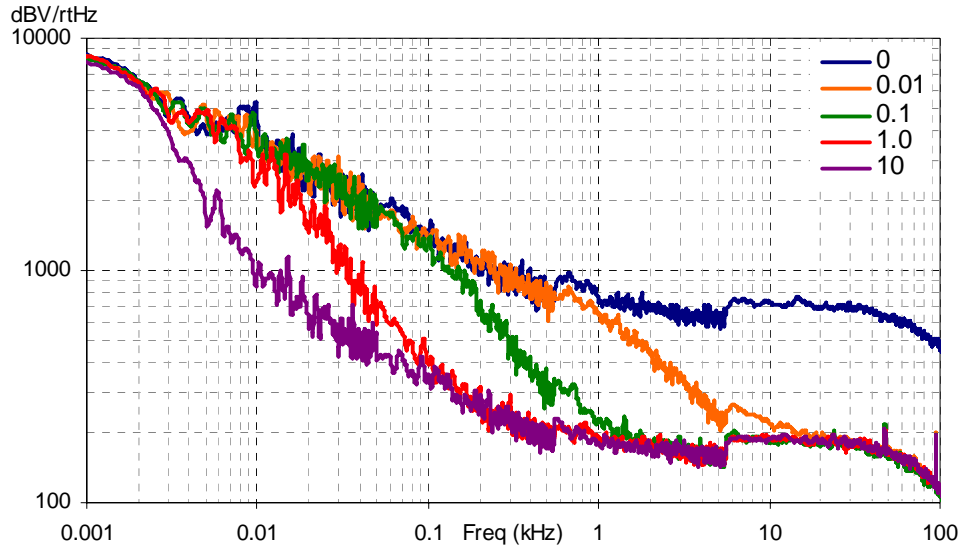
| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|--|------|-----|------|----------|-------|
| T _{ROA} | Rising Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | – | – | 3.9 | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | |
| T _{SOA} | Falling Settling Time to 0.1% for a 1V Step (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | – | – | 5.9 | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.92 | μs | |
| SR _{ROA} | Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | 0.15 | – | – | V/μs | |
| | Power = Medium, Opamp Bias = High | 1.7 | – | – | V/μs | |
| SR _{FOA} | Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | 0.01 | – | – | V/μs | |
| | Power = Medium, Opamp Bias = High | 0.5 | – | – | V/μs | |
| BW _{OA} | Gain Bandwidth Product | | | | | |
| | Power = Low, Opamp Bias = Low | 0.75 | – | – | MHz | |
| | Power = Medium, Opamp Bias = High | 3.1 | – | – | MHz | |
| E _{NOA} | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 100 | – | nV/rt-Hz | |

Table 26. 3.3V AC Operational Amplifier Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|--|------|-----|------|----------|-------|
| T _{ROA} | Rising Settling Time to 0.1% of a 1V Step (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | – | – | 3.92 | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | |
| T _{SOA} | Falling Settling Time to 0.1% of a 1V Step (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | – | – | 5.41 | μs | |
| | Power = Medium, Opamp Bias = High | – | – | 0.72 | μs | |
| SR _{ROA} | Rising Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | 0.31 | – | – | V/μs | |
| | Power = Medium, Opamp Bias = High | 2.7 | – | – | V/μs | |
| SR _{FOA} | Falling Slew Rate (20% to 80%) of a 1V Step (10 pF load, Unity Gain) | | | | | |
| | Power = Low, Opamp Bias = Low | 0.24 | – | – | V/μs | |
| | Power = Medium, Opamp Bias = High | 1.8 | – | – | V/μs | |
| BW _{OA} | Gain Bandwidth Product | | | | | |
| | Power = Low, Opamp Bias = Low | 0.67 | – | – | MHz | |
| | Power = Medium, Opamp Bias = High | 2.8 | – | – | MHz | |
| E _{NOA} | Noise at 1 kHz (Power = Medium, Opamp Bias = High) | – | 100 | – | nV/rt-Hz | |

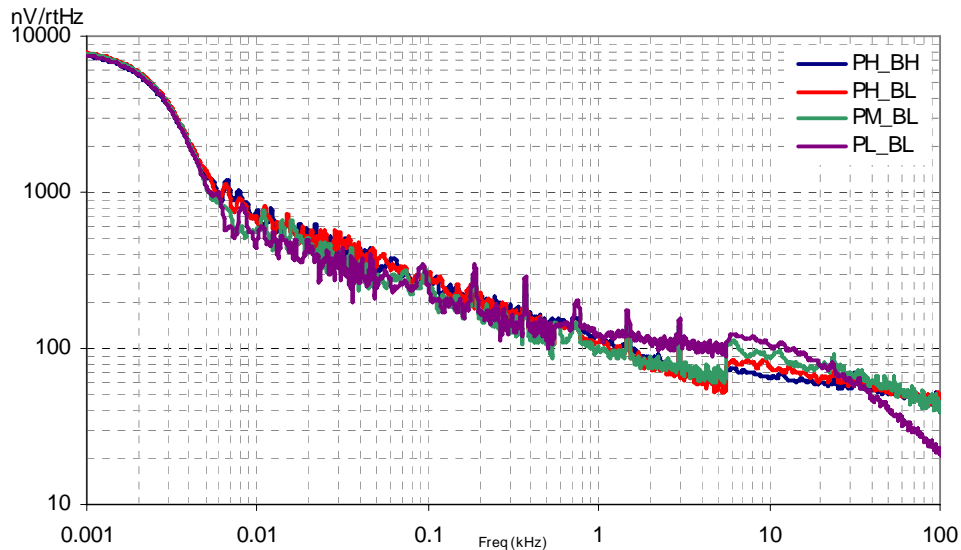
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 12. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 13. Typical Opamp Noise



AC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 2.4V to 3.0V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 27. AC Low Power Comparator Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|------------|-------------------|-----|-----|-----|---------------|---|
| T_{RLPC} | LPC response time | - | - | 50 | μs | ≥ 50 mV overdrive comparator reference set within V_{REFLPC} . |

AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 28. AC Digital Block Specifications

| Function | Description | Min | Typ | Max | Units | Notes |
|-------------------|---|-----------------|-----|------|-------|---|
| All Functions | Maximum Block Clocking Frequency (> 4.75V) | | | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| | Maximum Block Clocking Frequency (< 4.75V) | | | 24.6 | MHz | 3.0V < Vdd < 4.75V. |
| Timer | Capture Pulse Width | 50 ^a | – | – | ns | |
| | Maximum Frequency, No Capture | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| | Maximum Frequency, With Capture | – | – | 24.6 | MHz | |
| Counter | Enable Pulse Width | 50 ^a | – | – | ns | |
| | Maximum Frequency, No Enable Input | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| | Maximum Frequency, Enable Input | – | – | 24.6 | MHz | |
| Dead Band | Kill Pulse Width: | | | | | |
| | Asynchronous Restart Mode | 20 | – | – | ns | |
| | Synchronous Restart Mode | 50 ^a | – | – | ns | |
| | Disable Mode | 50 ^a | – | – | ns | |
| | Maximum Frequency | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| CRCPRS (PRS Mode) | Maximum Input Clock Frequency | – | – | 49.2 | MHz | 4.75V < Vdd < 5.25V. |
| CRCPRS (CRC Mode) | Maximum Input Clock Frequency | – | – | 24.6 | MHz | |
| SPIIM | Maximum Input Clock Frequency | – | – | 8.2 | MHz | Maximum data rate at 4.1 MHz due to 2 x over clocking. |
| SPIS | Maximum Input Clock Frequency | – | – | 4.1 | ns | |
| | Width of SS_ Negated Between Transmissions | 50 ^a | – | – | ns | |
| Transmitter | Maximum Input Clock Frequency Vdd ≥ 4.75V, 2 Stop Bits | – | – | 24.6 | MHz | Maximum data rate at 3.08 MHz due to 8 x over clocking. |
| | | – | – | 49.2 | MHz | Maximum data rate at 6.15 MHz due to 8 x over clocking. |
| Receiver | Maximum Input Clock Frequency Vdd ≥ 4.75V, 2 Stop Bits | – | – | 24.6 | MHz | Maximum data rate at 3.08 MHz due to 8 x over clocking. |
| | | – | – | 49.2 | MHz | Maximum data rate at 6.15 MHz due to 8 x over clocking. |

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 29. 5V AC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|---|------|-----|-----|-------|-------|
| T _{ROB} | Rising Settling Time to 0.1%, 1V Step, 100pF Load | | | | | |
| | Power = Low | – | – | 4 | μs | |
| | Power = High | – | – | 4 | μs | |
| T _{SOB} | Falling Settling Time to 0.1%, 1V Step, 100pF Load | | | | | |
| | Power = Low | – | – | 3.4 | μs | |
| | Power = High | – | – | 3.4 | μs | |
| SR _{ROB} | Rising Slew Rate (20% to 80%), 1V Step, 100pF Load | | | | | |
| | Power = Low | 0.5 | – | – | V/μs | |
| | Power = High | 0.5 | – | – | V/μs | |
| SR _{FOB} | Falling Slew Rate (80% to 20%), 1V Step, 100pF Load | | | | | |
| | Power = Low | 0.55 | – | – | V/μs | |
| | Power = High | 0.55 | – | – | V/μs | |
| BW _{OB} | Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100pF Load | | | | | |
| | Power = Low | 0.8 | – | – | MHz | |
| | Power = High | 0.8 | – | – | MHz | |
| BW _{OB} | Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100pF Load | | | | | |
| | Power = Low | 300 | – | – | kHz | |
| | Power = High | 300 | – | – | kHz | |

Table 30. 3.3V AC Analog Output Buffer Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|-------------------|---|-----|-----|-----|-------|-------|
| T _{ROB} | Rising Settling Time to 0.1%, 1V Step, 100pF Load | | | | | |
| | Power = Low | – | – | 4.7 | μs | |
| | Power = High | – | – | 4.7 | μs | |
| T _{SOB} | Falling Settling Time to 0.1%, 1V Step, 100pF Load | | | | | |
| | Power = Low | – | – | 4 | μs | |
| | Power = High | – | – | 4 | μs | |
| SR _{ROB} | Rising Slew Rate (20% to 80%), 1V Step, 100pF Load | | | | | |
| | Power = Low | .36 | – | – | V/μs | |
| | Power = High | .36 | – | – | V/μs | |
| SR _{FOB} | Falling Slew Rate (80% to 20%), 1V Step, 100pF Load | | | | | |
| | Power = Low | .4 | – | – | V/μs | |
| | Power = High | .4 | – | – | V/μs | |
| BW _{OB} | Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100pF Load | | | | | |
| | Power = Low | 0.7 | – | – | MHz | |
| | Power = High | 0.7 | – | – | MHz | |
| BW _{OB} | Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100pF Load | | | | | |
| | Power = Low | 200 | – | – | kHz | |
| | Power = High | 200 | – | – | kHz | |

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 31. 5V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|------------------------|-------|-----|------|-------|-------|
| F _{OSCEXT} | Frequency | 0.093 | – | 24.6 | MHz | |
| – | High Period | 20.6 | – | 5300 | ns | |
| – | Low Period | 20.6 | – | – | ns | |
| – | Power Up IMO to Switch | 150 | – | – | μs | |

Table 32. 3.3V AC External Clock Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|---|-------|-----|------|-------|---|
| F _{OSCEXT} | Frequency with CPU Clock divide by 1 | 0.093 | – | 12.3 | MHz | Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements. |
| F _{OSCEXT} | Frequency with CPU Clock divide by 2 or greater | 0.186 | – | 24.6 | MHz | If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met. |
| – | High Period with CPU Clock divide by 1 | 41.7 | – | 5300 | ns | |
| – | Low Period with CPU Clock divide by 1 | 41.7 | – | – | ns | |
| – | Power Up IMO to Switch | 150 | – | – | μs | |

AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 33. AC Programming Specifications

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---------------------|--|-----|-----|-----|-------|-----------------------------|
| T _{RSCLK} | Rise Time of SCLK | 1 | – | 20 | ns | |
| T _{FSCLK} | Fall Time of SCLK | 1 | – | 20 | ns | |
| T _{SSCLK} | Data Set up Time to Falling Edge of SCLK | 40 | – | – | ns | |
| T _{HSCLK} | Data Hold Time from Falling Edge of SCLK | 40 | – | – | ns | |
| F _{SCLK} | Frequency of SCLK | 0 | – | 8 | MHz | |
| T _{ERASEB} | Flash Erase Time (Block) | – | 10 | – | ms | |
| T _{WRITE} | Flash Block Write Time | – | 10 | – | ms | |
| T _{DSCLK} | Data Out Delay from Falling Edge of SCLK | – | – | 45 | ns | V _{dd} > 3.6 |
| T _{DSCLK3} | Data Out Delay from Falling Edge of SCLK | – | – | 50 | ns | 3.0 ≤ V _{dd} ≤ 3.6 |

AC I²C Specifications

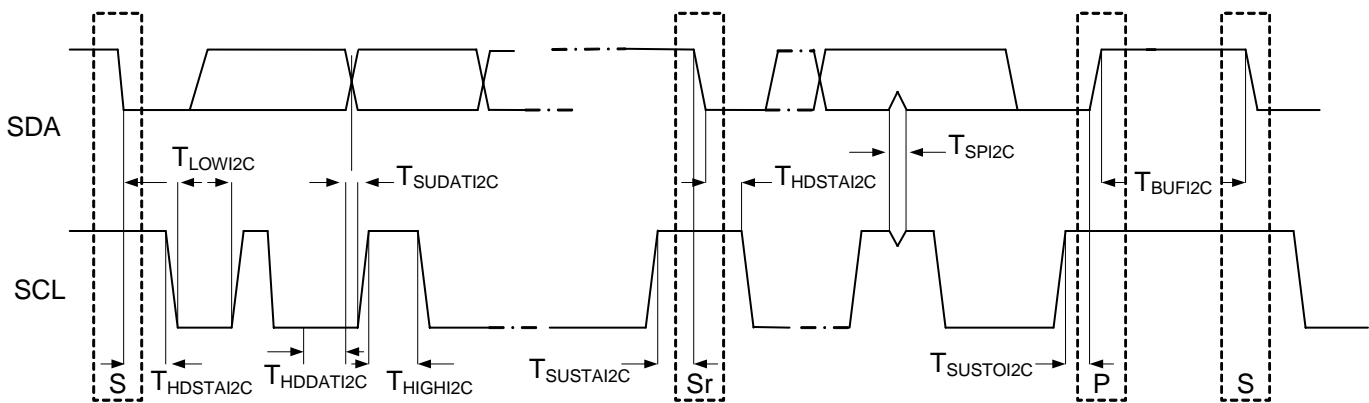
The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 34. AC Characteristics of the I²C SDA and SCL Pins

| Symbol | Description | Standard Mode | | Fast Mode | | Units | Notes |
|-----------------------|--|---------------|-----|------------------|-----|-------|-------|
| | | Min | Max | Min | Max | | |
| F _{SCL I2C} | SCL Clock Frequency | 0 | 100 | 0 | 400 | kHz | |
| T _{HDSTAI2C} | Hold Time (repeated) START Condition. After this period, the first clock pulse is generated. | 4.0 | – | 0.6 | – | μs | |
| T _{LOWI2C} | LOW Period of the SCL Clock | 4.7 | – | 1.3 | – | μs | |
| T _{HIGHI2C} | HIGH Period of the SCL Clock | 4.0 | – | 0.6 | – | μs | |
| T _{SUSTAI2C} | Set-up Time for a Repeated START Condition | 4.7 | – | 0.6 | – | μs | |
| T _{HDDATI2C} | Data Hold Time | 0 | – | 0 | – | μs | |
| T _{SUDATI2C} | Data Set-up Time | 250 | – | 100 ^a | – | ns | |
| T _{SUSTOI2C} | Set-up Time for STOP Condition | 4.0 | – | 0.6 | – | μs | |
| T _{BUFI2C} | Bus Free Time Between a STOP and START Condition | 4.7 | – | 1.3 | – | μs | |
| T _{SPI2C} | Pulse Width of spikes are suppressed by the input filter. | – | – | 0 | 50 | ns | |

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{\text{SU, DAT}} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{\text{max}} + t_{\text{SU, DAT}} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus



Packaging Information

This section illustrates the packaging specifications for the CY8CLED16 EZ-Color device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

Packaging Dimensions

Figure 15. 28-Lead (210-Mil) SSOP

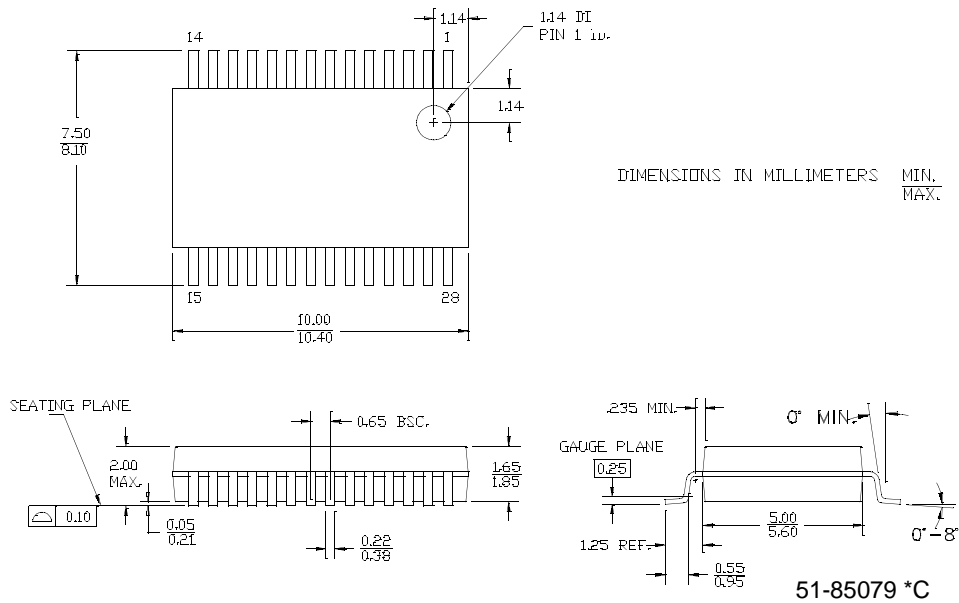


Figure 16. 48-Lead (300-Mil) SSOP

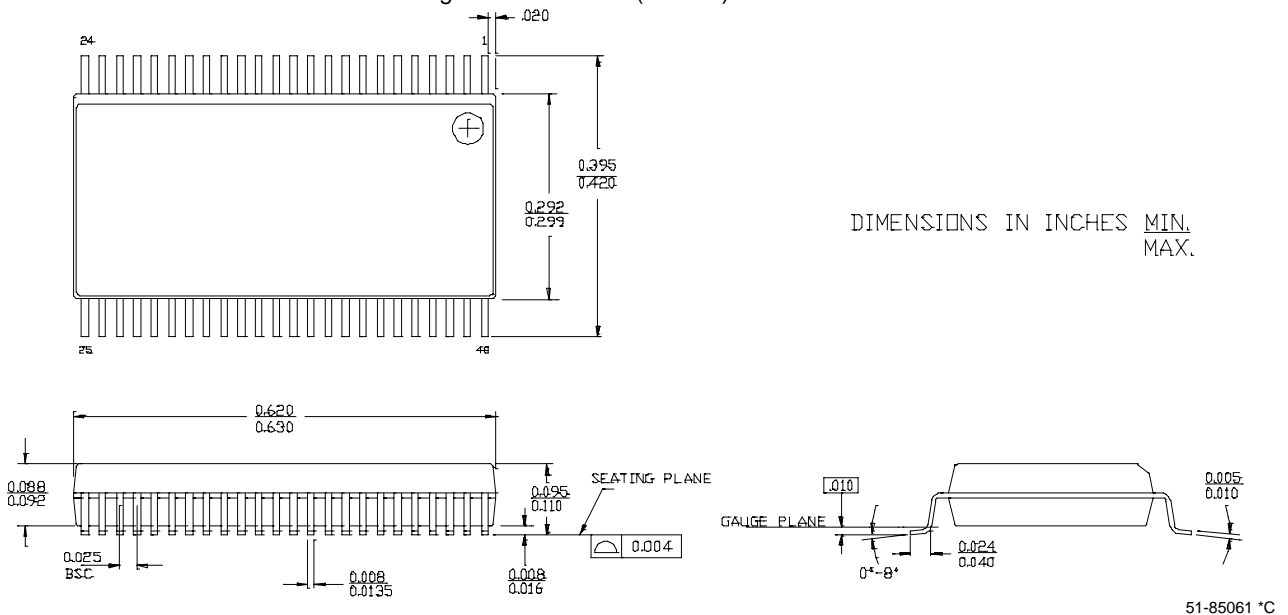
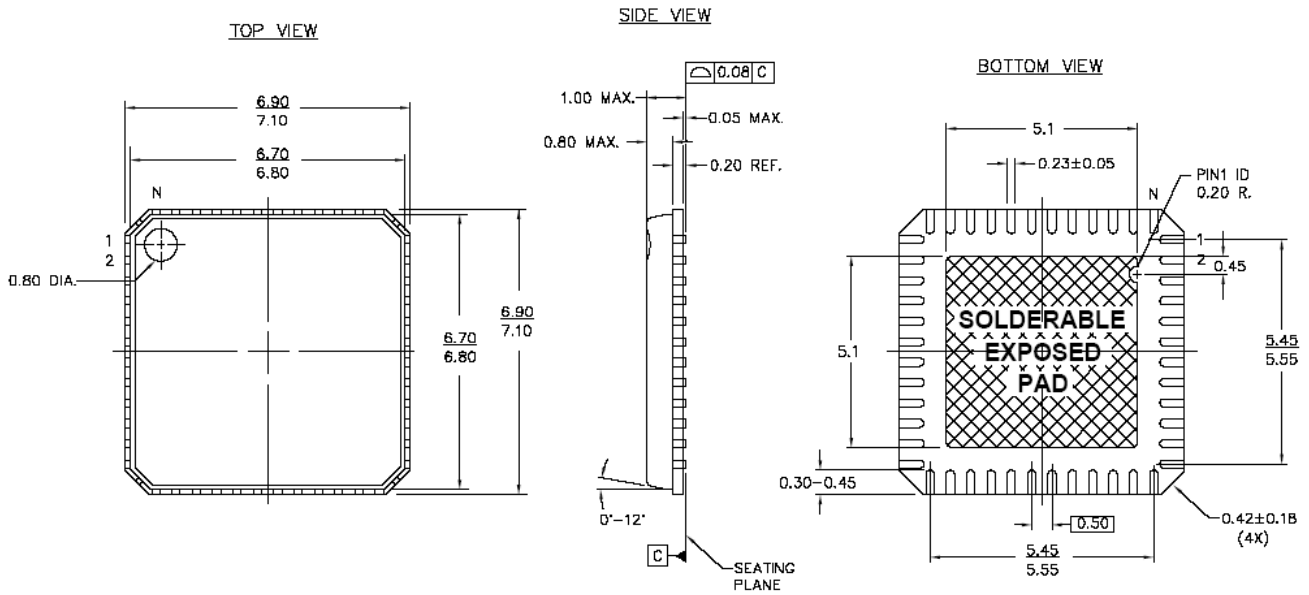



Figure 17. 48-Lead (7x7 mm) QFN



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.13g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

| PART # | DESCRIPTION |
|--------|-------------|
| LF48A | STANDARD |
| LY48A | LEAD FREE |

001-12919 *A

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Important Note Pinned vias for thermal conduction are not required for the low-power PSoC device.

Thermal Impedances

Table 35. Thermal Impedances per Package

| Package | Typical θ_{JA} * |
|----------|-------------------------|
| 28 SSOP | 94 °C/W |
| 48 SSOP | 69 °C/W |
| 48 QFN** | 28 °C/W |

* $T_J = T_A + POWER \times \theta_{JA}$

** To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

Capacitance on Crystal Pins

Table 36. Typical Package Capacitance on Crystal Pins

| Package | Package Capacitance |
|---------|---------------------|
| 28 SSOP | 2.8 pF |
| 48 SSOP | 3.3 pF |
| 48 QFN | 1.8 pF |

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 37. Solder Reflow Peak Temperature

| Package | Minimum Peak Temperature* | Maximum Peak Temperature |
|---------|---------------------------|--------------------------|
| 28 SSOP | 240°C | 260°C |
| 48 SSOP | 220°C | 260°C |
| 48 QFN | 220°C | 260°C |

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Development Tool Selection

Software

This section presents the development tools available for all current PSoC device families including the CY8CLED16 EZ-Color family.

PSoC Express™

As the newest addition to the PSoC development software suite, PSoC Express is the first visual embedded system design tool that allows a user to create an entire PSoC project and generate

a schematic, BOM, and data sheet without writing a single line of code. Users work directly with application objects such as LEDs, switches, sensors, and fans. PSoC Express is available free of charge at <http://www.cypress.com/psocexpress>.

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for half a decade. PSoC Designer is available free of charge at <http://www.cypress.com/psocdesigner>.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com/psocprogrammer>.

CY3202-C iMAGEcraft C Compiler

CY3202 is the optional upgrade to PSoC Designer that enables the iMAGEcraft C compiler. It can be purchased from the Cypress Online Store. At <http://www.cypress.com>, click the Online Store shopping cart icon at the bottom of the web page, and click *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

CY3261A-RGB EZ-Color RGB Kit

The CY3261A-RGB board is a preprogrammed HB LED color mix board with seven pre-set colors using the CY8CLED16 EZ-Color HB LED Controller. The board is accompanied by a CD containing the color selector software application, PSoC Express 3.0 Beta 2, PSoC Programmer, and a suite of documents, schematics, and firmware examples. The color selector software application can be installed on a host PC and is used to control the EZ-Color HB LED controller using the included USB cable. The application enables you to select colors via a CIE 1931 chart or by entering coordinates. The kit includes:

- Training Board (CY8CLED16)
- One mini-A to mini-B USB Cable
- PSoC Express CD-ROM
- Design Files and Application Installation CD-ROM

To program and tune this kit via PSoC Express 3.0 you must use a Mini Programmer Unit (CY3217 Kit) and a CY3240-I2CUSB kit.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD

■ Getting Started Guide

■ USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 38. Emulation and Programming Accessories

| Part # | Pin Package | Flex-Pod Kit ^a | Foot Kit ^b | Adapter ^c |
|------------------|-------------|---------------------------|-----------------------|--|
| CY8CLED16-28PVXI | 28 SSOP | CY3250-29XXX | CY3250-28 SSOP-FK | Adapters can be found at http://www.emulation.com . |
| CY8CLED16-48PVXI | 48 SSOP | CY3250-29XXX | CY3250-48 SSOP-FK | |
| CY8CLED16-48LFXI | 48 QFN | CY3250-29XXX QFN | CY3250-48 QFN-FK | |

- a. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
- b. Foot kit includes surface mount feet that can be soldered to the target PCB.
- c. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

3rd-Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under DESIGN RESOURCES >> Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at <http://www.cypress.com/an2323>.

Ordering Information

Key Device Features

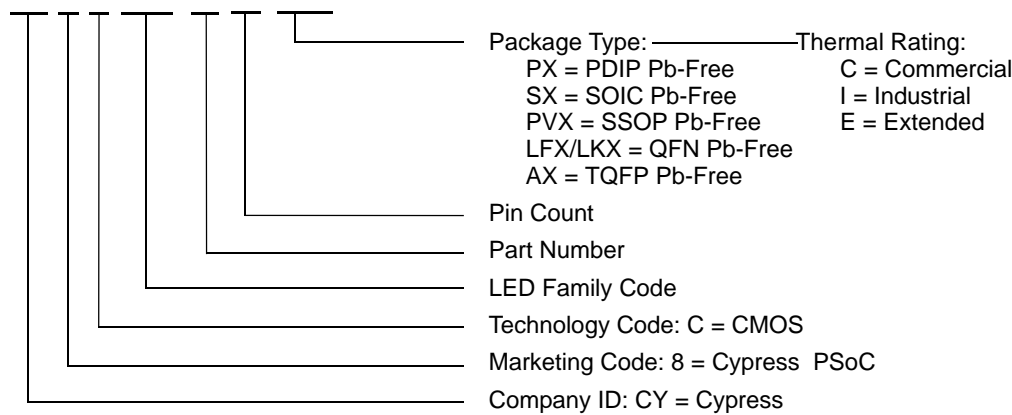
The following table lists the CY8CLED16 EZ-Color devices' key package features and ordering codes.

Table 39. Device Key Features and Ordering Information

| Package | Ordering Code | Flash (Bytes) | RAM (Bytes) | Switch Mode Pump | Temperature Range | Digital PSoC Blocks | Analog PSoC Blocks | Digital IO Pins | Analog Inputs | Analog Outputs | XRES Pin |
|---------------------------------------|-------------------|---------------|-------------|------------------|-------------------|---------------------|--------------------|-----------------|---------------|----------------|----------|
| 28 Pin (210 Mil) SSOP | CY8CLED16-28PVXI | 32K | 2K | Yes | -40C to +85C | 16 | 12 | 24 | 12 | 4 | Yes |
| 28 Pin (210 Mil) SSOP (Tape and Reel) | CY8CLED16-28PVXIT | 32K | 2K | Yes | -40C to +85C | 16 | 12 | 24 | 12 | 4 | Yes |
| 48 Pin (300 Mil) SSOP | CY8CLED16-48PVXI | 32K | 2K | Yes | -40C to +85C | 16 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin (300 Mil) SSOP (Tape and Reel) | CY8CLED16-48PVXIT | 32K | 2K | Yes | -40C to +85C | 16 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin QFN | CY8CLED16-48LFXI | 32K | 2K | Yes | -40C to +85C | 16 | 12 | 44 | 12 | 4 | Yes |
| 48 Pin QFN (Tape and Reel) | CY8CLED16-48LFXIT | 32K | 2K | Yes | -40C to +85C | 16 | 12 | 44 | 12 | 4 | Yes |

Ordering Code Definitions

CY 8 C LED xx - xx xxxx



Document History

Table 40. CY8CLED16 Data Sheet Revision History

| Document Title: CY8CLED16 EZ-Color HB LED Controller | | | | |
|---|---------|----------------------|------------------|-----------------------------|
| Document Number: 001-13105 | | | | |
| Revision | ECN # | Issue Date | Origin of Change | Description of Change |
| ** | 1148504 | See ECN | SFVTMP3 | New document (revision **). |
| | | | | |
| Distribution: External/Public | | Posting: None | | |

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