FAIRCHILD

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Single-Channel: 6N135M, 6N136M, HCPL4503M
Dual-Channel: HCPL2530M, HCPL2531M
High Speed Transistor Optocouplers

Features

- High Speed –1 MBit/s
- Superior CMR – 10 kV/µs
- Dual-Channel: HCPL2530M, HCPL2531M
- CTR Guaranteed 0°C to 70°C
- U.L. Recognized (File # E90700, Vol. 2)
- DIN EN/IEC60747-5-5
  - Ordering Option 'V', e.g., 6N135VM
- 5,000 V_{RMS} (1 Minute) Isolation Rating
- Superior CMR of 15,000 V/µs Minimum (HCPL4503M)
- No Base Connection for Improved Noise Immunity (HCPL4503M)

Applications

- Line Receivers
- Pulse Transformer Replacement
- Output Interface to CMOS-LSTTL-TTL
- Wide-Bandwidth Analog Coupling

Description

The HCPL4503M, 6N135M, 6N136M, HCPL2530M, and HCPL2531M optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

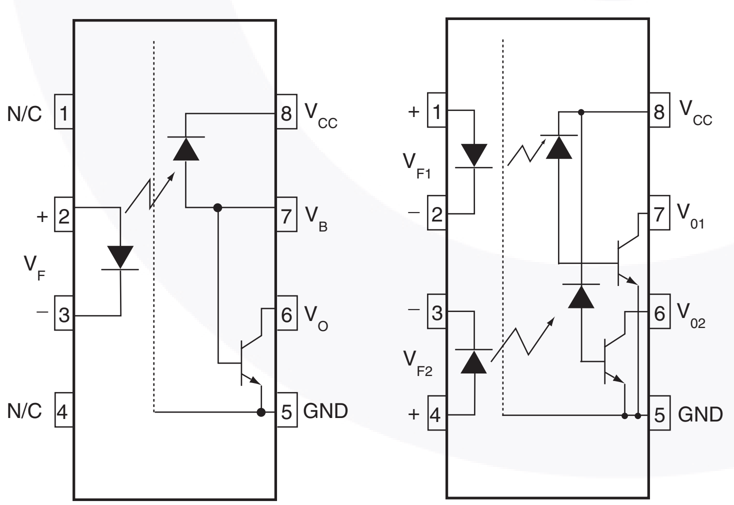
The HCPL4503M has no internal connection to the phototransistor base for improved noise immunity.

An internal noise shield provides superior common mode rejection of up to 50,000 V/µs.

Related Resources

- www.fairchildsemi.com/products/opto/
- www.fairchildsemi.com/pf/HC/HCPL0500.html
- www.fairchildsemi.com/pf/FO/FODM452.html
- www.fairchildsemi.com/pf/FO/FOD050L.html

Schematics



6N135M, 6N136M, HCPL4503M

HCPL2530M/HCPL2531M

Pin 7 is not connected in the HCPL4503M

Figure 1. Schematics

Package Outlines

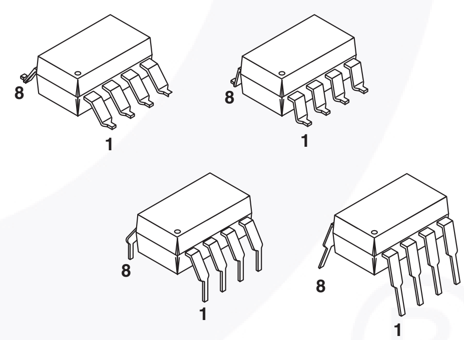


Figure 2. Package Outlines

Safety and Insulation Ratings for 8-Pin DIP White

As per DIN EN/IEC 60747-5-5. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Mains Voltage < 150 V_{RMS}		I–IV		
	For Rated Mains Voltage < 300 V_{RMS}		I–IV		
	For Rated Mains Voltage < 450 V_{RMS}		I–III		
	For Rated Mains Voltage < 600 V_{RMS}		I–III		
	Climatic Classification		40/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V_{PR}	Input to Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	1,669			
	Input to Output Test Voltage, Method a, V_{IORM} x 1.5 = V_{PR}, Type and Sample Test with t_m = 60 s, Partial Discharge < 5 pC	1,335			
V_{IORM}	Max Working Insulation Voltage	890			V_{PEAK}
V_{IOTM}	Highest Allowable Over Voltage	6,000			V_{PEAK}
	External Creepage	8.0			mm
	External Clearance	7.4			mm
	External Clearance (for Option T, 0.4” Lead Spacing)	10.16			mm
	Insulation Thickness	0.5			mm
	Safety Limit Values, Maximum Values Allowed in the Event of a Failure				
T_S	Case Temperature	150			°C
$I_{S,INPUT}$	Input Current	200			mA
$P_{S,OUTPUT}$	Output Power (Duty Factor ≤ 2.7%)	300			mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9			Ω

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Value	Units
T_{STG}	Storage Temperature		-40 to +125	°C
T_{OPR}	Operating Temperature		-40 to +100	°C
T_{SOL}	Lead Solder Temperature		260 for 10 s	°C
EMITTER				
I_F (avg)	DC/Average Forward Input Current Each Channel[(1)]		25	mA
I_F (pk)	Peak Forward Input Current Each Channel[(2)]	50% Duty Cycle, 1 ms P.W.	50	mA
I_F (trans)	Peak Transient Input Current Each Channel	≤ 1 µs P.W., 300 pps	1.0	A
V_R	Reverse Input Voltage Each Channel		5	V
P_D	Input Power Dissipation Each Channel[(3)]	6N135M, 6N136M, and HCPL4503M	45	mW
		HCPL2530M and HCPL2531M		
DETECTOR				
I_O (avg)	Average Output Current Each Channel		8	mA
I_O (pk)	Peak Output Current Each Channel		16	mA
V_{EBR}	Emitter-Base Reverse Voltage	6N135M and 6N136M	5	V
V_{CC}	Supply Voltage		-0.5 to 30	V
V_O	Output Voltage		-0.5 to 20	V
I_B	Base Current	6N135M and 6N136M	5	mA
PD	Output Power Dissipation Each Channel[(4)]	6N135M, 6N136M, and HCPL4503M	100	mW
		HCPL2530M and HCPL2531M	35	mW

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C.

Electrical Characteristics

T_A = 0°C to 70°C unless otherwise specified. Typical value is measured at T_A = 25ºC and V_{CC} = 5.0 V.

Individual Component Characteristics

Symbol	Parameter	Test Conditions	Device	Min.	Typ.	Max.	Unit
EMITTER							
V_F	Input Forward Voltage	I_F = 16 mA, T_A = 25°C	All		1.45	1.7	V
		I_F = 16 mA	All			1.8	
B_{VR}	Input Reverse Breakdown Voltage	I_R = 10 µA	All	5.0	21		V
$\Delta V_F / \Delta T_A$	Temperature Coefficient of Forward Voltage	I_F = 16 mA	All		-1.7		mV/°C
DETECTOR							
I_{OH}	Logic High Output Current	I_F = 0 mA, V_O = V_{CC} = 5.5 V, T_A = 25°C	All		0.0007	0.5	µA
		I_F = 0 mA, V_O = V_{CC} = 15 V, T_A = 25°C	6N135M 6N136M HCPL4503M		0.0019	1	
		I_F = 0 mA, V_O = V_{CC} = 15 V	All			50	
I_{CCL}	Logic Low Supply Current	I_F = 16 mA, V_O = Open, V_{CC} = 15 V	6N135M 6N136M HCPL4503M		163	200	µA
		I_{F1} = I_{F2} = 16 mA, V_O = Open, V_{CC} = 15 V	HCPL2530M HCPL2531M			400	
I_{CCH}	Logic High Supply Current	I_F = 0 mA, V_O = Open, V_{CC} = 15 V, T_A = 25°C	6N135M 6N136M HCPL4503M		0.0002	1	µA
		I_F = 0 mA, V_O = Open, V_{CC} = 15 V	6N135M 6N136M HCPL4503M		0.0004	2	
		I_F = 0 mA, V_O = Open, V_{CC} = 15 V	HCPL2530M HCPL2531M			4	

Electrical Characteristics (Continued)

T_A = 0 to 70°C unless otherwise specified. Typical value is measured at T_A = 25ºC and V_{CC} = 5.0 V.

Transfer Characteristics

Symbol	Parameter	Test Conditions		Device	Min.	Typ.	Max.	Unit
COUPLED								
CTR	Current Transfer Ratio[5]	I_F = 16 mA, V_O = 0.4 V, V_{CC} = 4.5 V, T_A = 25°C		6N135M	7	38	50	%
				HCPL2530M				
				6N136M HCPL4503M	19	38	50	%
				HCPL2531M				
		I_F = 16 mA, V_{CC} = 4.5 V	V_{OL} = 0.4 V	6N135M	5			%
			V_{OL} = 0.5 V	HCPL2530M				
			V_{OL} = 0.4 V	6N136M HCPL4503M	15			%
			V_{OL} = 0.5 V	HCPL2531M				
V_{OL}	Logic LOW Output Voltage	I_F = 16 mA, I_O = 1.1 mA, V_{CC} = 4.5 V, T_A = 25°C		6N135M		0.12	0.4	V
				HCPL2530M			0.5	
		I_F = 16 mA, I_O = 3 mA, V_{CC} = 4.5 V, T_A = 25°C		6N136M HCPL4503M		0.20	0.4	
				HCPL2531M			0.5	
		I_F = 16 mA, I_O = 0.8 mA, V_{CC} = 4.5 V		6N135M		0.11	0.5	
				HCPL2530M				
		I_F = 16 mA, I_O = 2.4 mA, V_{CC} = 4.5 V		HCPL4503M		0.18	0.5	
				HCPL2531M				

Note:

5. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.

Electrical Characteristics (Continued)

T_A = 0 to 70°C unless otherwise specified. Typical values are measured at T_A = 25°C and V_{CC} = 5V.

Switching Characteristics (V_{CC} = 5V)

Symbol	Parameter	Test Conditions	Device	Min.	Typ.	Max.	Unit
t_{PHL}	Propagation Delay Time to Logic LOW	T_A = 25°C, R_L = 4.1 kΩ, I_F = 16 mA(6) (Figure 15)	6N135M		0.23	1.5	µs
			HCPL2530M				
		R_L = 1.9 kΩ, I_F = 16 mA, T_A = 25°C(7) (Figure 15)	6N136M HCPL4503M		0.25	0.8	µs
			HCPL2531M				
		R_L = 4.1 kΩ, I_F = 16 mA(6) (Figure 15)	6N135M HCPL2530M			2.0	µs
		R_L = 1.9 kΩ, I_F = 16 mA(7) (Figure 15)	6N136M HCPL4503M HCPL2531M			1.0	µs
t_{PLH}	Propagation Delay Time to Logic HIGH	T_A = 25°C, (R_L = 4.1 kΩ, I_F = 16 mA(6) (Figure 15)	6N135M		0.45	1.5	µs
			HCPL2530M				
		R_L = 1.9 kΩ, I_F = 16 mA(7), T_A = 25°C (Figure 15)	6N136M HCPL4503M		0.26	0.8	µs
			HCPL2531M				
		R_L = 4.1 kΩ, I_F = 16 mA(6) (Figure 15)	6N135M HCPL2530M			2.0	µs
		R_L = 1.9 kΩ, I_F = 16 mA(7) (Figure 15)	6N136M HCPL4503M HCPL2531M			1.0	µs
$\|CM_H\|$	Common Mode Transient Immunity at Logic High	I_F = 0 mA, V_{CM} = 10 V_{P-P}, R_L = 4.1 kΩ, T_A = 25°C(8) (Figure 16)	6N135M HCPL2530M		10,000		V/µs
		I_F = 0 mA, V_{CM} = 10 V_{P-P}, R_L = 1.9 kΩ, T_A = 25°C(8) (Figure 16)	6N136M HCPL2531M		10,000		V/µs
		I_F = 0 mA, V_{CM} = 1,500 V_{P-P}, R_L = 1.9 kΩ, T_A = 25°C(8) (Figure 16)	HCPL4503M	15,000	50,000		
$\|CM_L\|$	Common Mode Transient Immunity at Logic Low	I_F = 16 mA, V_{CM} = 10 V_{P-P}, R_L = 4.1 kΩ, T_A = 25°C(8) (Figure 16)	6N135M HCPL2530M		10,000		V/µs
		I_F = 16 mA, V_{CM} = 10 V_{P-P}, R_L = 1.9 kΩ(8) (Figure 16)	6N136M HCPL2531M		10,000		V/µs
		I_F = 0 mA, V_{CM} = 1,500 V_{P-P}, R_L = 1.9 kΩ, T_A = 25°C(8) (Figure 16)	HCPL4503M	15,000	50,000		

Notes:

6. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
7. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and 5.6 kΩ pull-up resistor.
8. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O > 2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O < 0.8 V).

Electrical Characteristics (Continued)

T_A = 0 to 70°C unless otherwise specified. Typical values are measured at T_A = 25°C and V_{CC} = 5 V.

Isolation Characteristics

Symbol	Characteristics	Test Conditions	Min.	Typ.	Max.	Unit
V_{ISO}	Withstand Insulation Test Voltage	RH ≤ 50%, T_A = 25°C, I_{I-O} ≤ 10 µA, t = 1 minute, f = 50 Hz(9)(11)	5,000			V_{RMS}
R_{I-O}	Resistance (Input to Output)	V_{I-O} = 500 VDC(9)		10^{11}		Ω
C_{I-O}	Capacitance (Input to Output)	f = 1 MHz, V_{I-O} = 0V (9)		1		pF
I_{I-I}	Input-Input Insulation Leakage Current	RH ≤ 45%, V_{I-I} = 500 VDC(10) t = 5 s, (HCPL2530M/2531M only)		< 1		nA
R_{I-I}	Input-Input Resistance	V_{I-I} = 500 VDC(10) (HCPL2530M/2531M only)		10^{12}		Ω
C_{I-I}	Input-Input Capacitance	f = 1 MHz(10) (HCPL2530M/2531M only)		0.2		pF

Notes:

9. Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.
10. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
11. 5,000 V_{RMS} for 1 minute duration is equivalent to 6,000 V_{RMS} for 1 second duration.

Typical Performance Curves

For single-channel devices; 6N135M, 6N136M, and HCPL4503M.

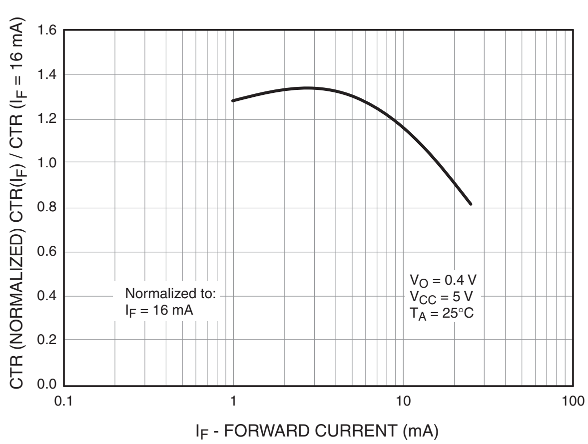


Figure 3. Normalized CTR vs. Forward Current

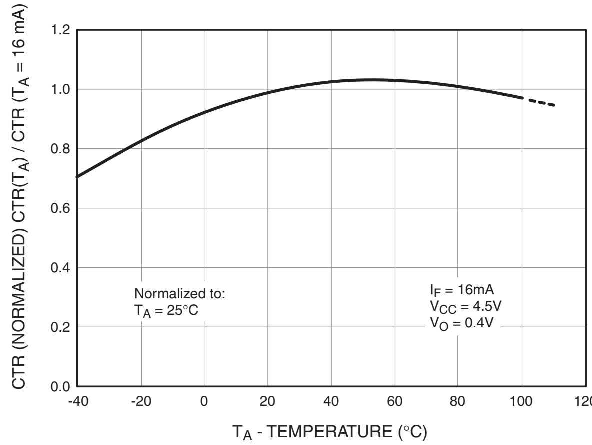


Figure 4. Normalized CTR vs. Temperature

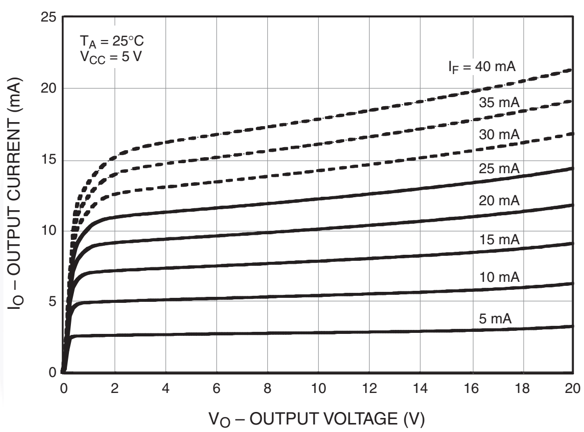


Figure 5. Output Current vs. Output Voltage

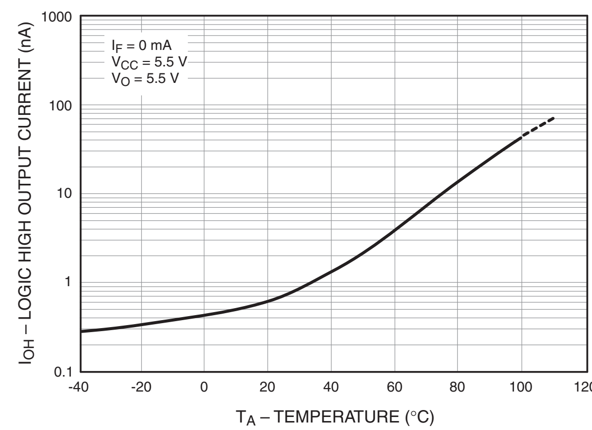


Figure 6. Logic High Output Current vs. Temperature

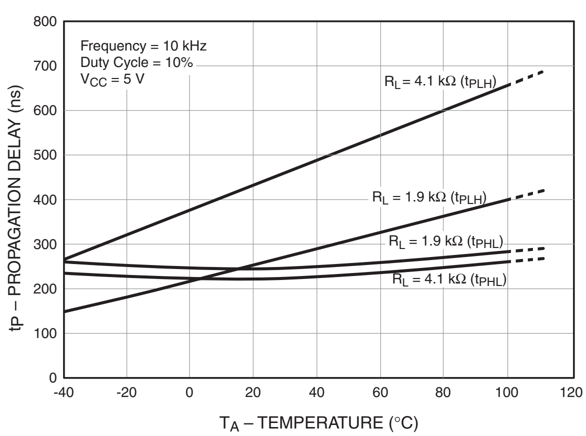


Figure 7. Propagation Delay vs. Temperature

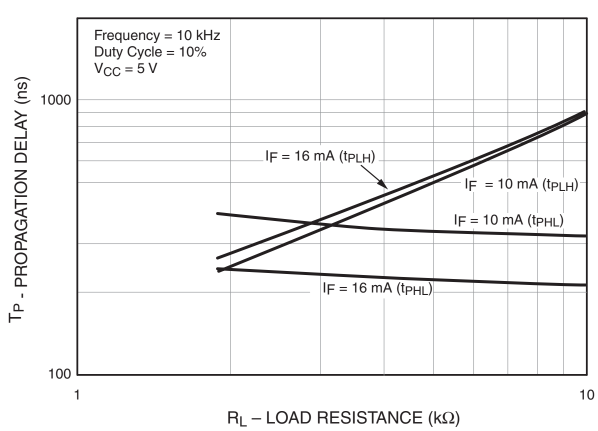


Figure 8. Propagation Delay vs. Load Resistance

Typical Performance Curves (Continued)

For dual-channel devices; HCPL2530M and HCPL2531M.

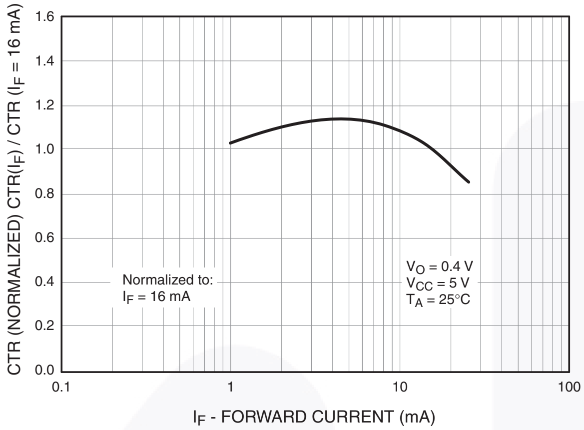


Figure 9. Normalized CTR vs. Forward Current

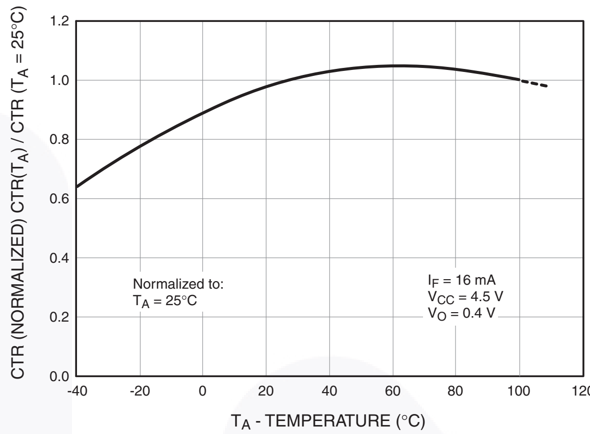


Figure 10. Normalized CTR vs. Temperature

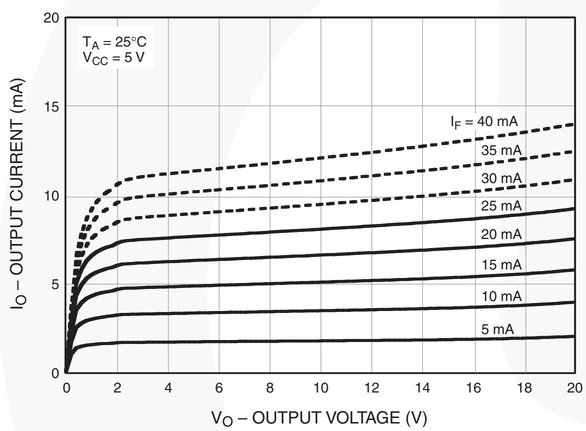


Figure 11. Output Current vs. Output Voltage

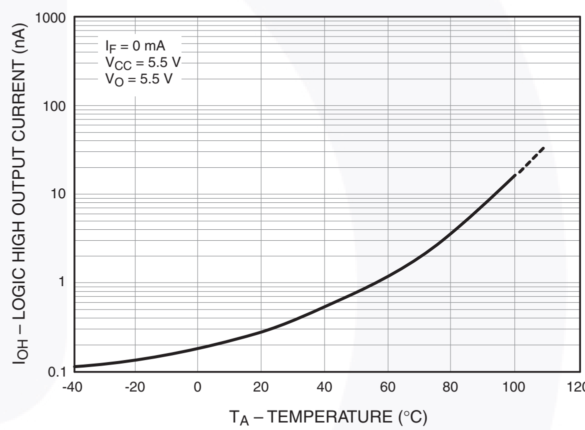


Figure 12. Logic High Output Current vs. Temperature

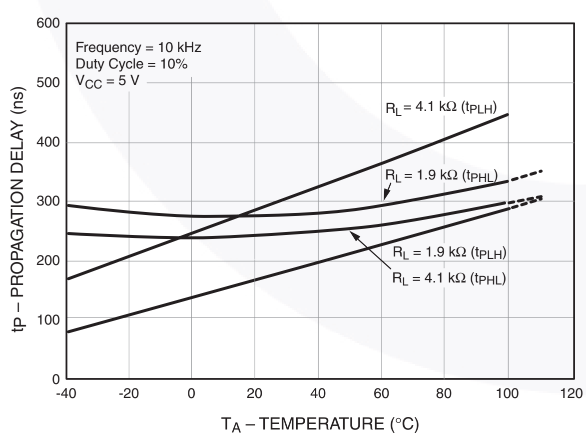


Figure 13. Propagation Delay vs. Temperature

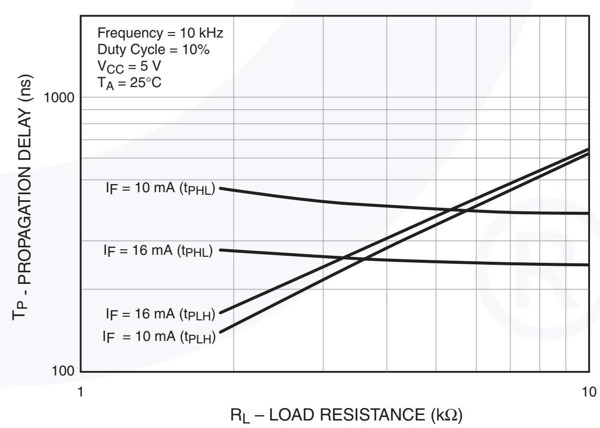


Figure 14. Propagation Delay vs. Load Resistance

Test Circuits

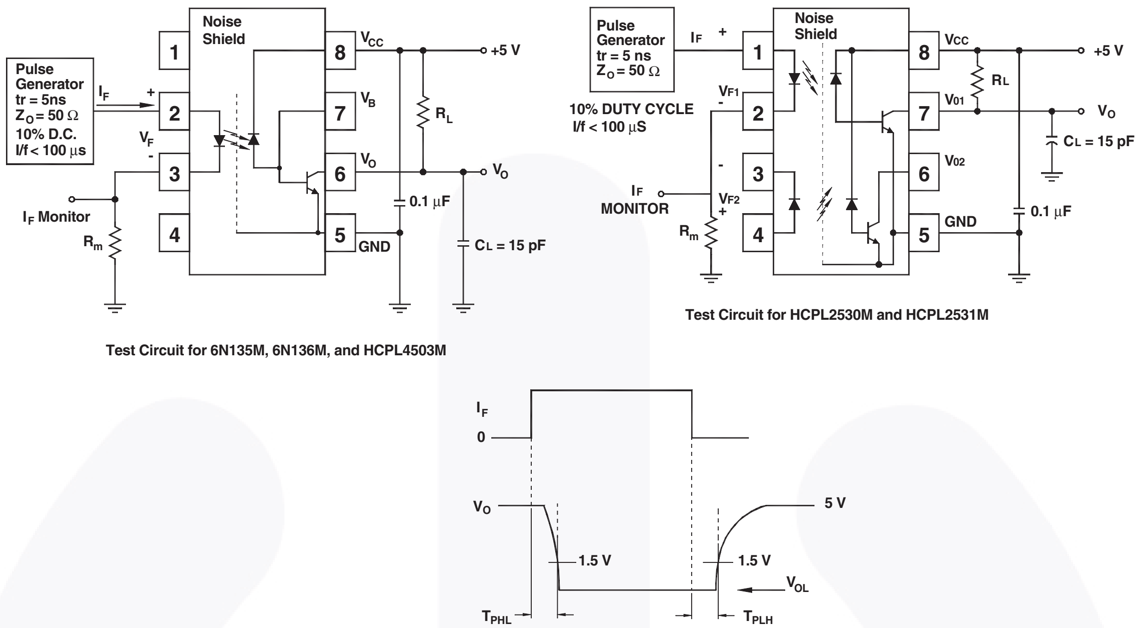


Figure 15. Switching Time Test Circuit

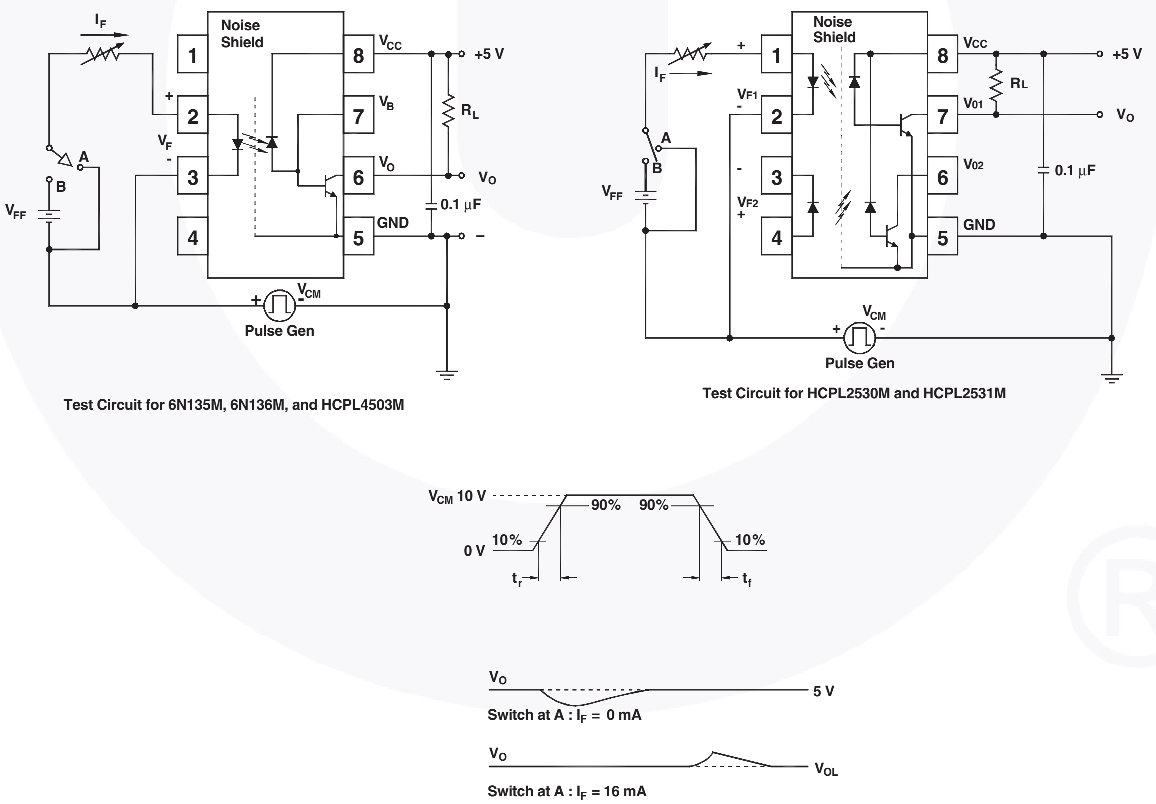
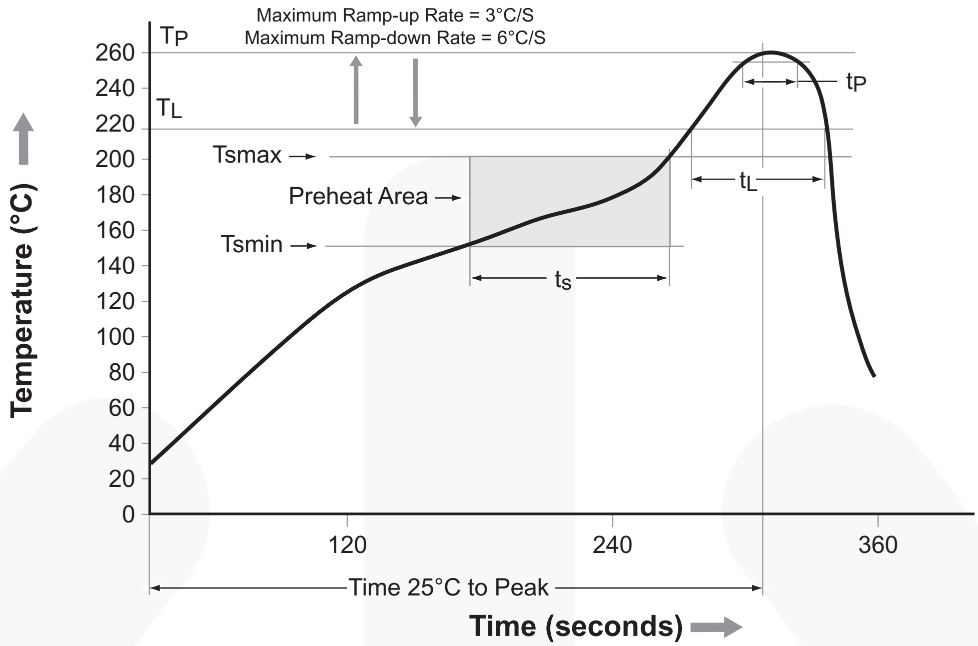


Figure 16. Common Mode Immunity Test Circuit

Reflow Profile



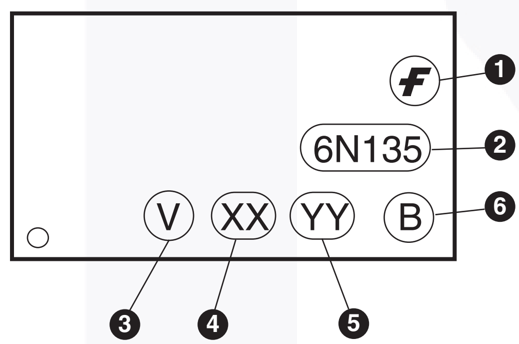
Profile Freature	Pb-Free Assembly Profile
Temperature Min. (Tsmin)	150°C
Temperature Max. (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60 to 120 s
Ramp-up Rate (t_L to t_P)	3°C/second maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 to 150 s
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 s
Ramp-down Rate (T_P to T_L)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

Figure 17. Relow Profile

Ordering Information

Part Number	Package	Packing Method
6N135M	DIP 8-Pin	Tube (50 units per tube)
6N135SM	SMT 8-Pin (Lead Bend)	Tube (50 units per tube)
6N135SDM	SMT 8-Pin (Lead Bend)	Tape and Reel (1,000 units per reel)
6N135VM	DIP 8-Pin, DIN EN/IEC 60747-5-5 option	Tube (50 units per tube)
6N135SVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option	Tube (50 units per tube)
6N135SDVM	SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 option	Tape and Reel (1,000 units per reel)
6N135TVM	DIP 8-Pin, 0.4” Lead Spacing, DIN EN/IEC 60747-5-5 option	Tube (50 units per tube)
6N135TSVM	SMT 8-Pin, 0.4” Lead Spacing, DIN EN/IEC 60747-5-5 option	Tube (50 units per tube)
6N135TSR2VM	SMT 8-Pin, 0.4” Lead Spacing, DIN EN/IEC 60747-5-5 option	Tape and Reel (700 units per reel)

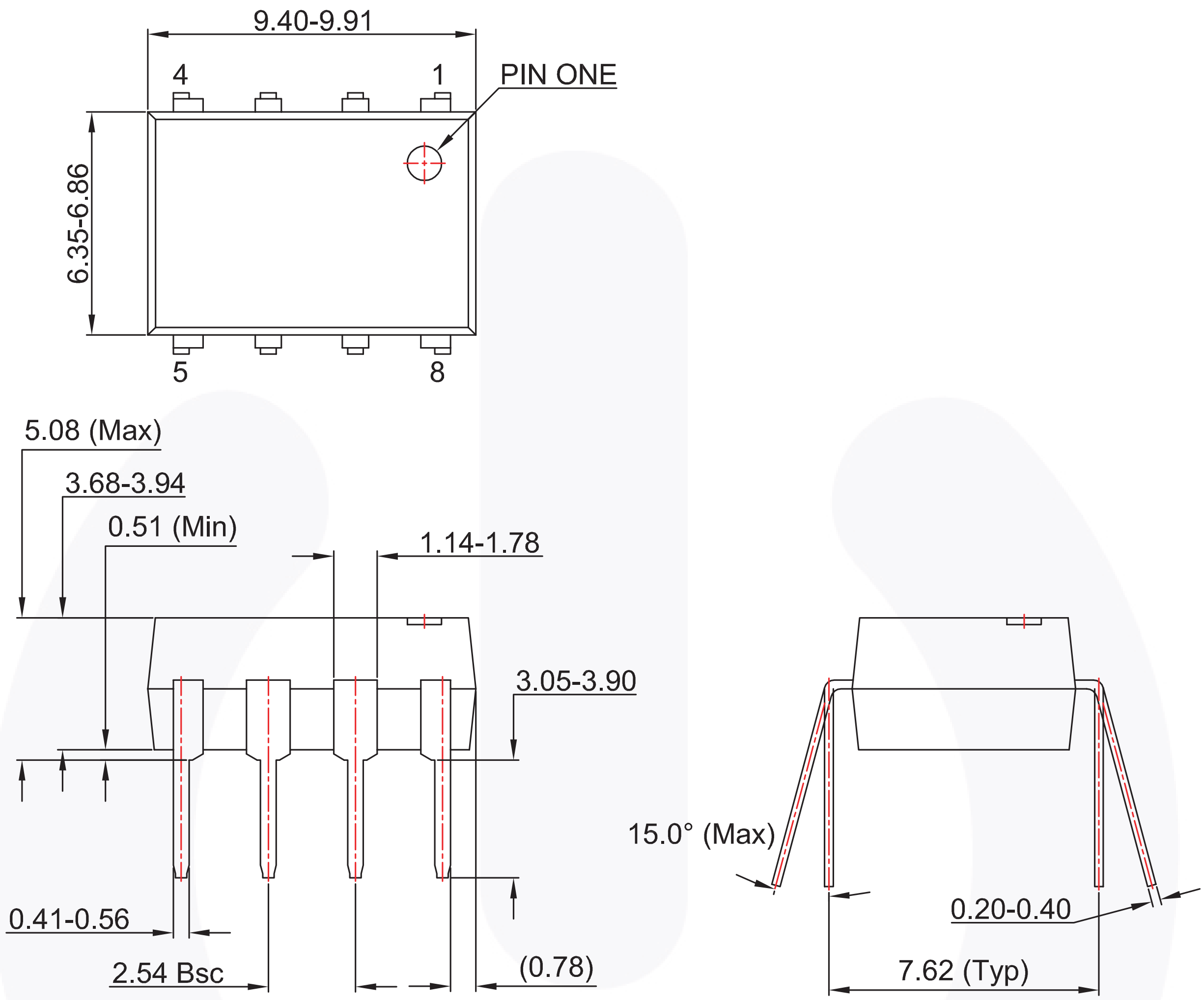
Marking Information



Definitions	
1	Fairchild logo
2(1)	Device number
3	DIN EN/IEC60747-5-5 mark (Note: Only appears on parts ordered with this option – See order entry table)
4	Two-digit year code, e.g., ‘08’
5	Two-digit work week ranging from ‘01’ to ‘53’
6	Assembly package code

Notes:
1. ‘HCPL’ devices are marked with only the numeric characters (for example, HCPL4503M is marked as ‘4503’).
2. The ‘M’ suffix is an ordering identifier only. It is used to indicated the white package version. The ‘M’ does no appear in the top mark.

Package Dimensions



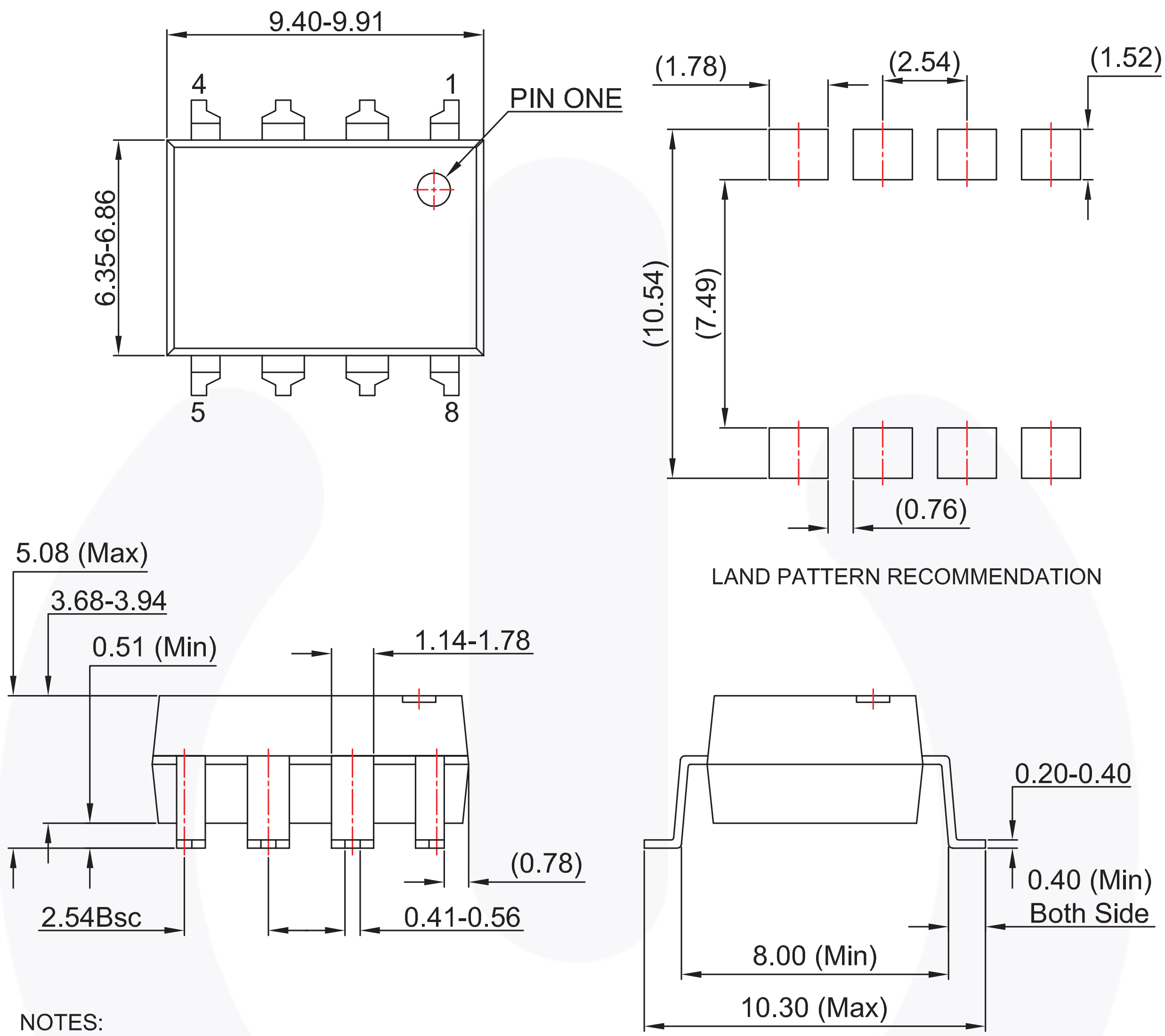
NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION
D) DRAWING FILENAME AND REVSION: MKT-N08GREV6.

Figure 18. 8-Pin DIP Through Hole

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings: http://www.fairchildsemi.com/dwg/N0/N08G.pdf.

Package Dimensions (Continued)



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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH, AND TIE BAR EXTRUSION
D) DRAWING FILENAME AND REVSION: MKT-N08HREV6.

Figure 19. 8-Pin DIP Surface Mount (Option S)

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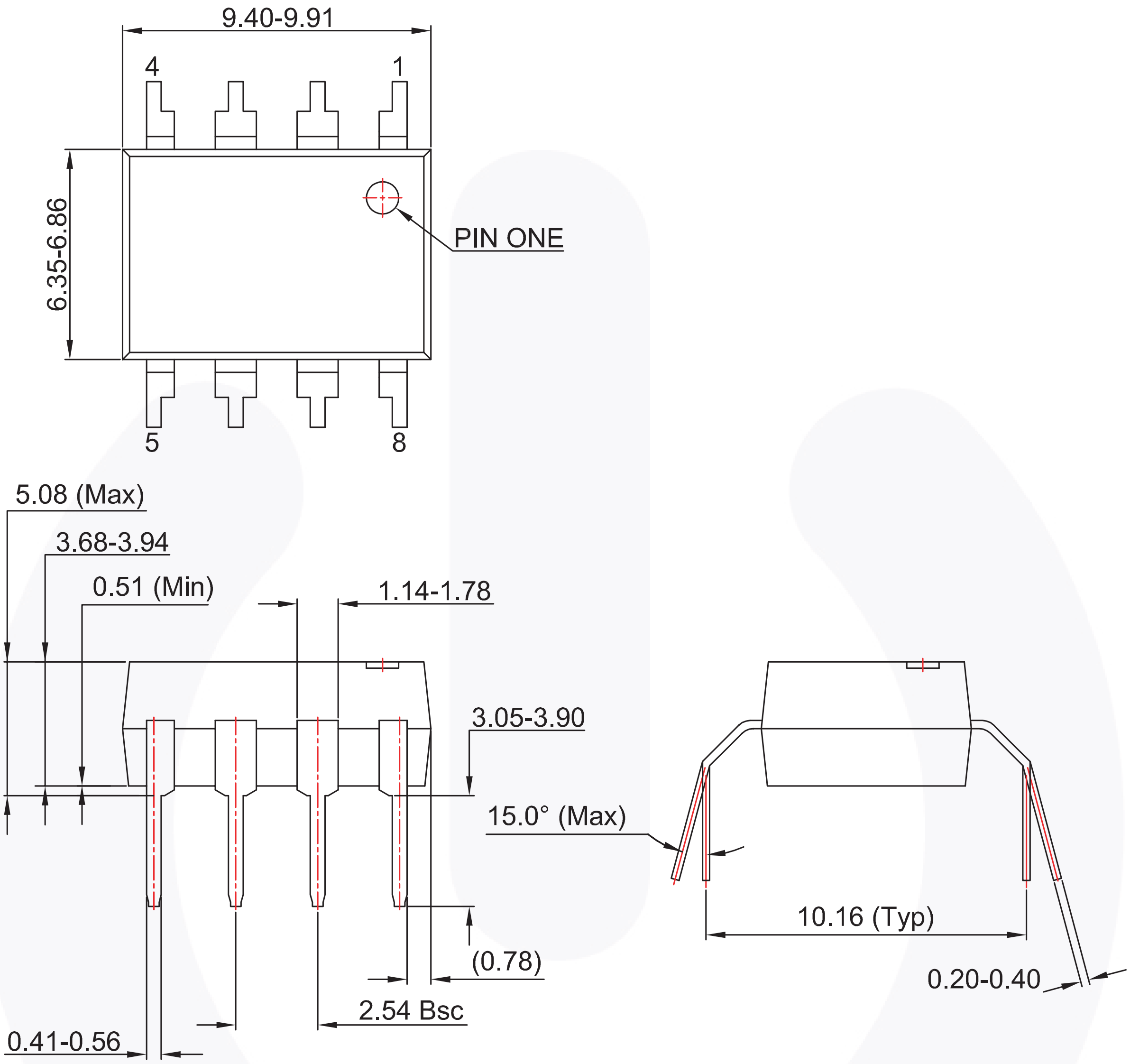
Package Dimensions (Continued)



NOTES:

A) NO STANDARD APPLIES TO THIS PACKAGE

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

D) DRAWING FILENAME AND REVSION: MKT-N08AREV6.

Figure 20. 8-Pin DIP Through Hole 0.4" Lead Spacing (Option T)

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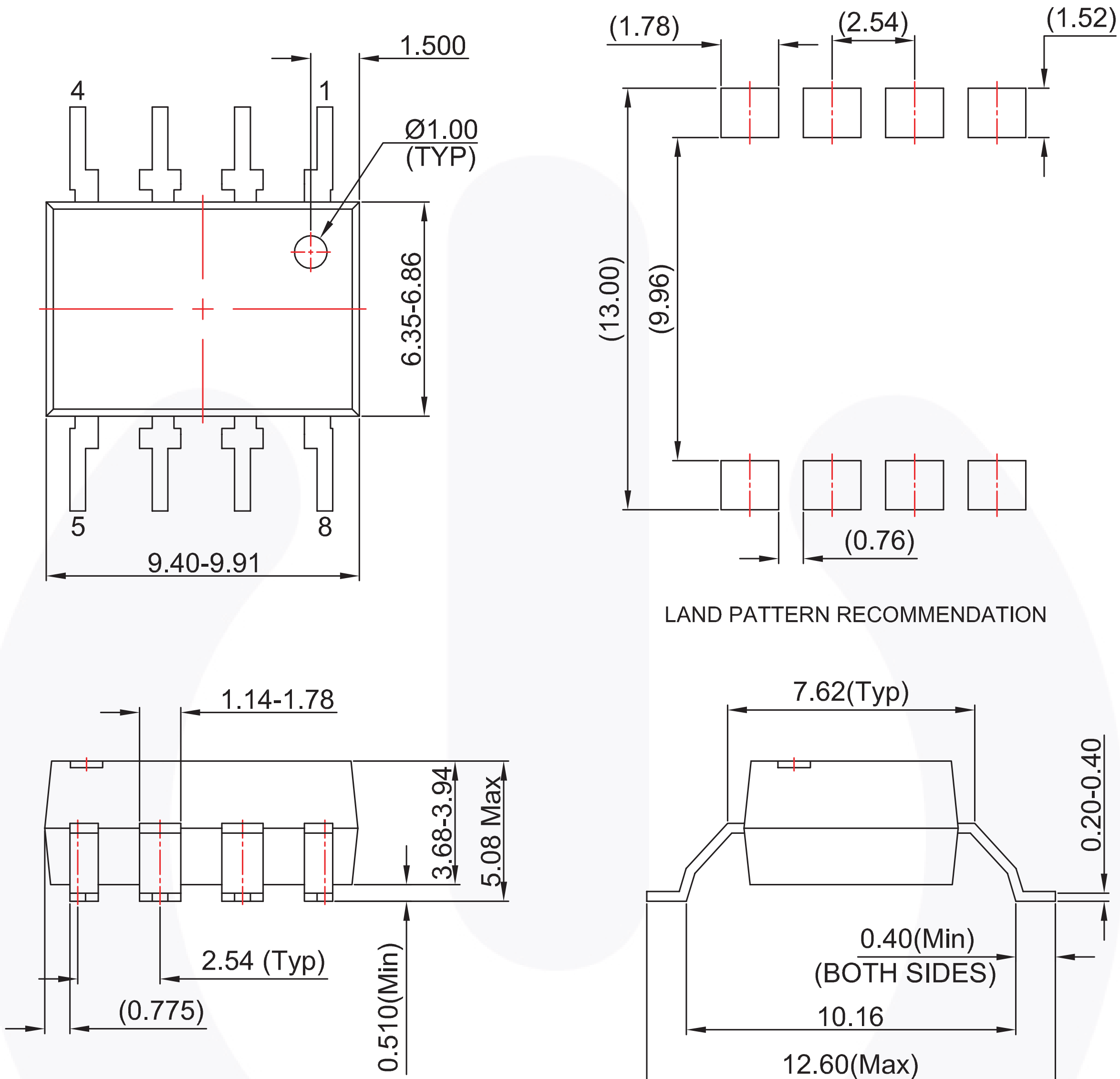
Package Dimensions (Continued)



NOTES:

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Figure 21. 8-Pin DIP Surface Mount 0.4" Lead Spacing (Option TS)

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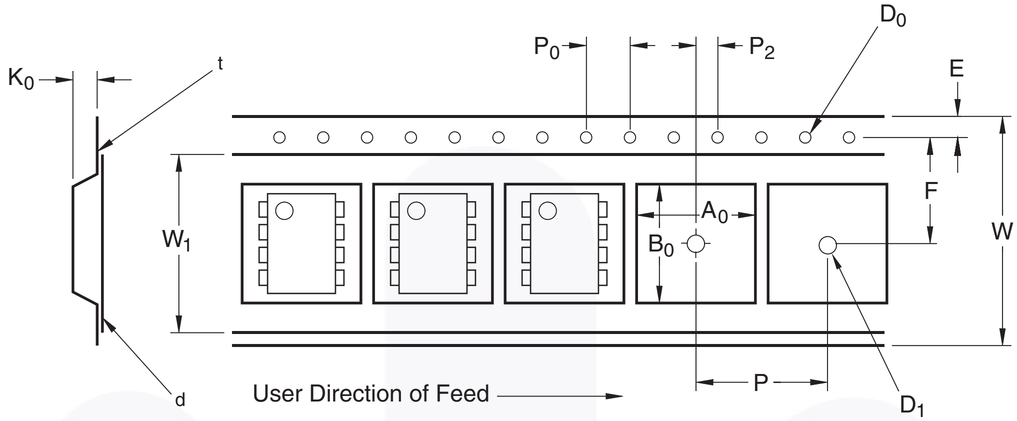
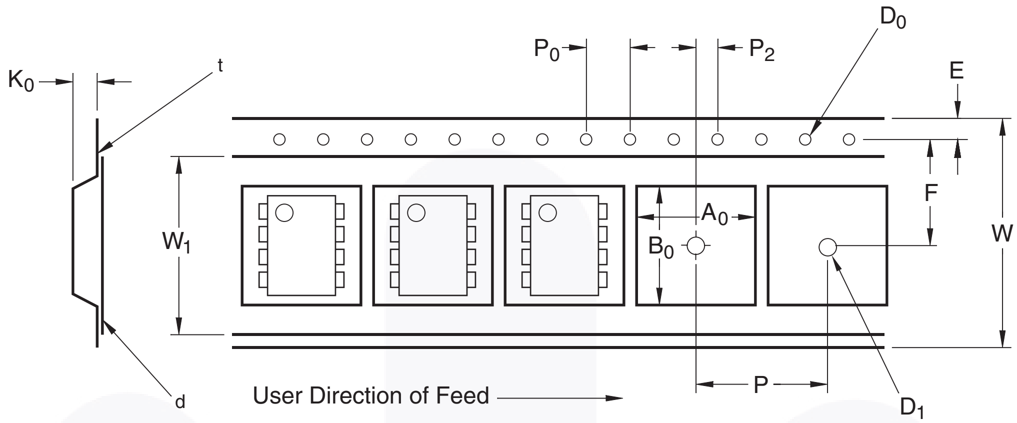
Carrier Tape Specifications (Option SD)



Symbol	Description	Dimension in mm
W	Tape Width	16.0 ± 0.3
t	Tape Thickness	0.30 ± 0.05
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	7.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	12.0 ± 0.1
A_0	Pocket Dimensions	10.30 ±0.20
B_0		10.30 ±0.20
K_0		4.90 ±0.20
W_1	Cover Tape Width	13.2 ± 0.2
d	Cover Tape Thickness	0.1 Maximum
	Maximum Component Rotation or Tilt	10°
R	Minimum Bending Radius	30

Carrier Tape Specifications (Option TSR2)



Symbol	Description	Dimension in mm
W	Tape Width	24.0 ± 0.3
t	Tape Thickness	0.40 ± 0.1
P_0	Sprocket Hole Pitch	4.0 ± 0.1
D_0	Sprocket Hole Diameter	1.55 ± 0.05
E	Sprocket Hole Location	1.75 ± 0.10
F	Pocket Location	11.5 ± 0.1
P_2		2.0 ± 0.1
P	Pocket Pitch	16.0 ± 0.1
A_0	Pocket Dimensions	12.80 ± 0.1
B_0		10.35 ± 0.1
K_0		5.7 ±0.1
W_1	Cover Tape Width	21.0 ± 0.1
d	Cover Tape Thickness	0.1 Maximum
	Maximum Component Rotation or Tilt	10°
R	Minimum Bending Radius	30

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Definition of Terms

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