

Advance Information

Single-Wire CAN Transceiver

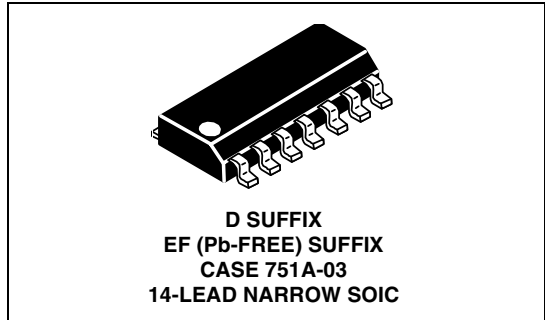
The 33897 is intended to be used as the physical interface in an SWCAN (Single-Wire Controller Area Network) application. It supports both the standard 33.333 kbps communications rate and the high-speed service rate of 83.333 kbps. The modes (speed, high-voltage wake-up [HVWU], and sleep) are controlled by the state of two input pins for easy MCU interfacing.

Features

- 33.33 kbps Data Rate with Loading per J2411
- Waveshaping for Low EMI
- High-Speed Mode up to 83.33 kbps
- Responds to High-Voltage Wake-up
- CNTL Output to External Regulator for Bus-Controlled Module Wake-up
- Built-In Delay Timers to Allow MCU-Required Wake-up Timing
- Detects and Automatically Handles Loss of Ground
- Extended Frame Tolerance
- Worst-Case Sleep Mode Current of Only 80  $\mu$ A
- Current Limit Prevents Damage Due to Bus Shorts
- Built-In Thermal Shutdown on Bus Output
- Protected Against Vehicular Electrical Transients
- Undervoltage Lockout Prevents False Data with Low Battery
- Designed to Meet GMW3089V2.3 Requirements
- Pb-Free Packaging Designated by Suffix Code EF

33897

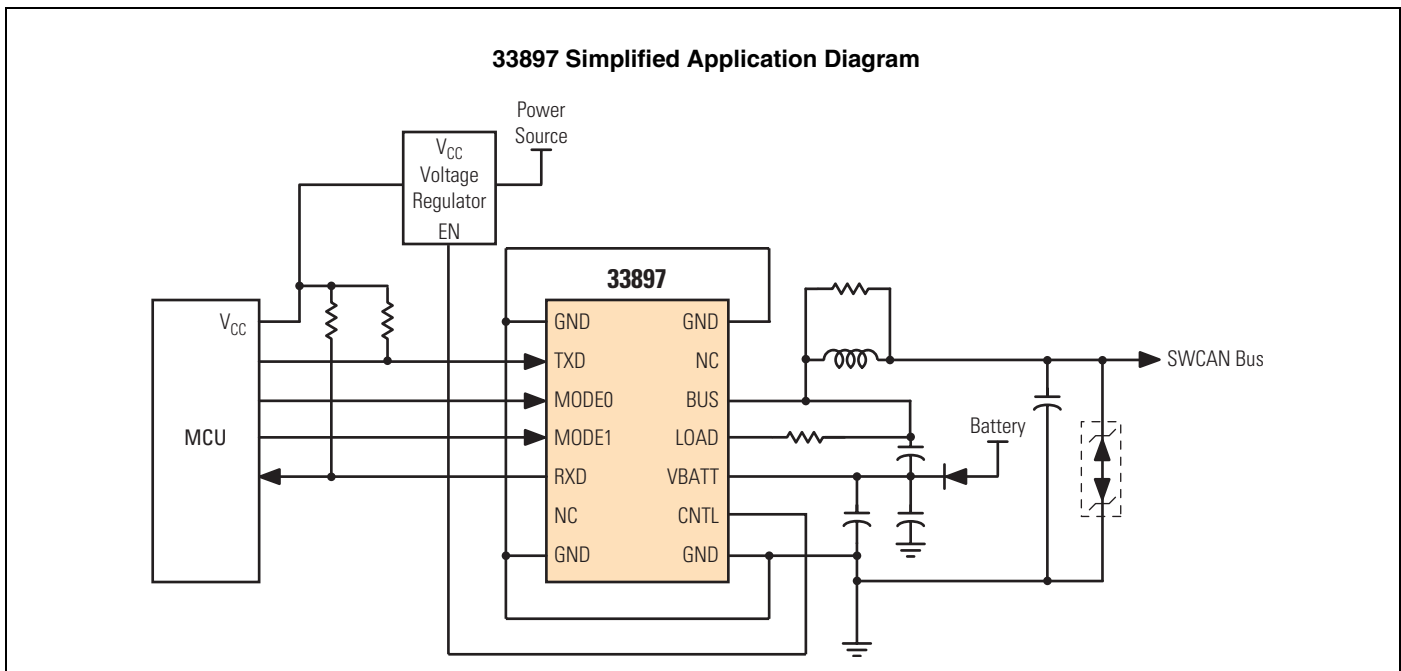
SINGLE-WIRE CAN TRANSCEIVER



ORDERING INFORMATION

Device	Temperature Range (T <sub>A</sub> )	Package
PC33897D/R2	-40°C to 125°C	14 SOICN
PC33897EF/R2		

Freescale Semiconductor, Inc.



This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

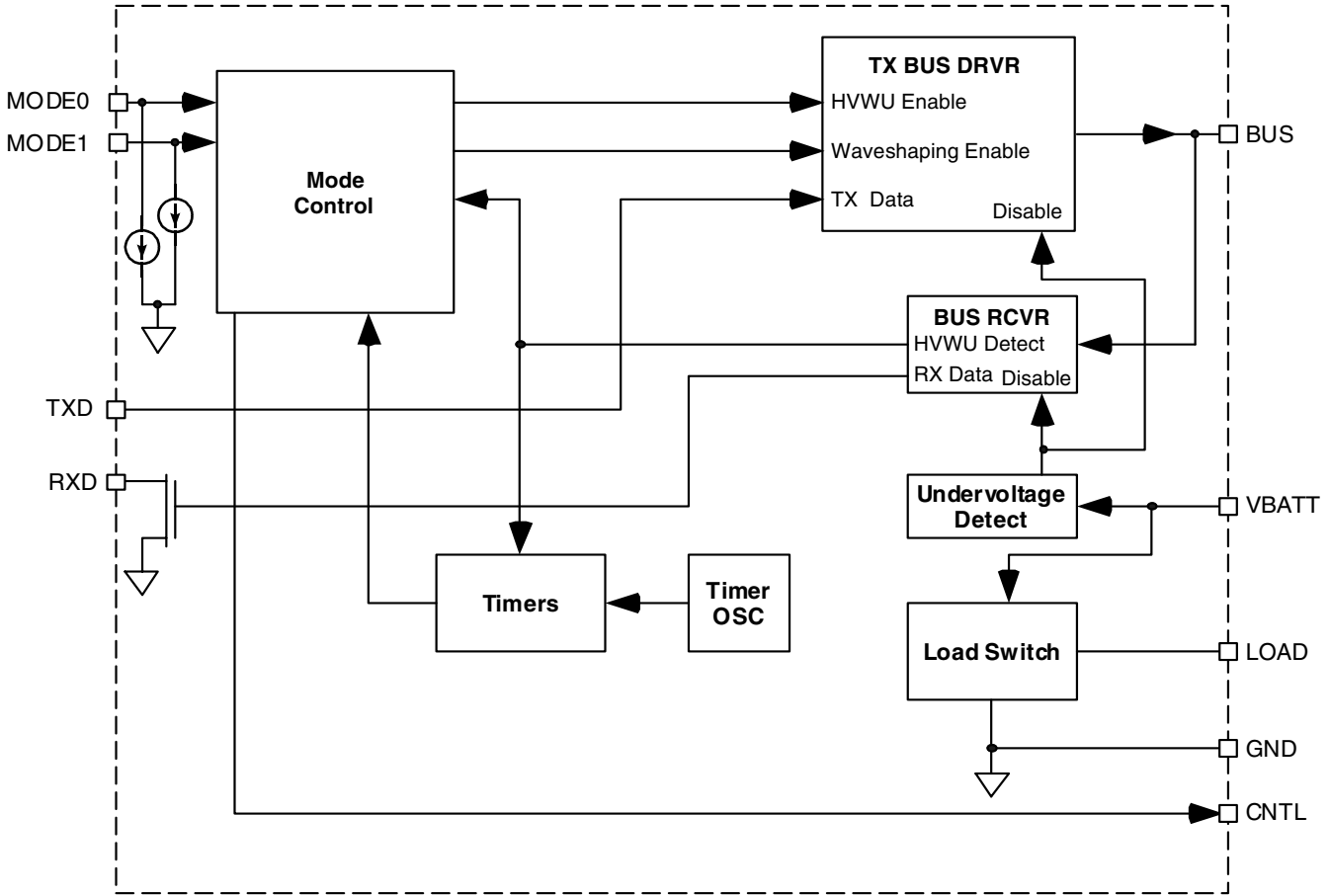
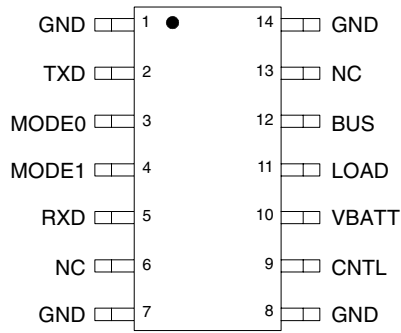


Figure 1. 33897 Simplified Internal Block Diagram



## PIN FUNCTION DESCRIPTION

Pin	Pin Name	Formal Name	Definition
1, 7, 8, 14	GND	Ground	Electrical Common Ground and Heat removal. A good thermal path will also reduce the die temperature.
2	TXD	Transmit Data	Data input here will appear on the BUS pin. A logic "0" will assert the bus, a "1" will go to the recessive state.
3, 4	MODEn	Mode Control	These pins control Sleep Mode, Transmit Level, and Speed. They have weak pull-downs.
5	RXD	Receive Data	Open drain output of the data on BUS. A recessive bus = "1", dominant = "0". An external pull-up is required.
6, 13	NC	No connect	No internal connection to this pin.
9	CNTL	Control	Provides a battery-level logic signal.
10	VBATT	Battery	Power input. An external diode is needed for reverse battery protection.
11	LOAD	Load	The external bus load resistor connects here to prevent bus pull-up in the case of loss of module ground.
12	BUS	Bus	This pin connects to the bus through external components.

## MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted.

Rating	Symbol	Value	Unit
Supply Voltage	$V_{BATT}$	-0.3 to 40	V
Input Logic Voltage	$V_{IN}$	-0.3 to 7.0	V
RXD	$V_{RXD}$	-0.3 to 7.0	V
CNTL	$V_{CNTL}$	-0.3 to 40	V
ESD Voltage			V
Human Body Model (Note 1)	$V_{ESD1}$	±2000	
Machine Model (Note 2)	$V_{ESD2}$	±200	
Storage Temperature	$T_{STG}$	-55 to 150	°C
Operating Ambient Temperature	$T_A$	-40 to 125	°C
Operating Junction Temperature	$T_J$	-40 to 150	°C
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	150	°C/W
Terminal Soldering Temperature (Note 3)	$T_{SOLDER}$		°C
D Suffix		245	
EF (Pb-Free) Suffix		260	

### Notes

- ESD1 testing is performed in accordance with the Human Body Model ( $C_{ZAP}=100$  pF,  $R_{ZAP}=1500$   $\Omega$ ).
- ESD2 testing is performed in accordance with the Machine Model ( $C_{ZAP}=200$  pF,  $R_{ZAP}=0$   $\Omega$ ).
- Terminal soldering temperature limit is for 10 second maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

## STATIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  unless otherwise noted. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>LOGIC I/O</b>					
Logic Input Low Level (MODE0, MODE1, and TXD) $5.0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$V_{\text{IL}}$	0	–	0.8	V
Logic Input High Level (MODE0, MODE1, and TXD) $5.0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$V_{\text{IH}}$	2.0	–	–	V
Mode Pin Pull-Down Current (MODE0 and MODE1) Pin Voltage = 0.8 V, $5.0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$I_{\text{PD}}$	10	–	50	$\mu\text{A}$
Receiver Output Low $I_{\text{IN}} = 2.0\text{ mA}$ , $5.0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$V_{\text{OL}}$	0	–	0.45	V
CNTL Output Low $I_{\text{IN}} = 5.0\text{ }\mu\text{A}$ , $5.0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$V_{\text{OLCNTL}}$	0	–	0.8	V
CNTL Output High $I_{\text{OUT}} = 180\text{ }\mu\text{A}$ , $5.0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$V_{\text{OHCNTL}}$	$V_{\text{BATT}} - 0.8$	–	$V_{\text{BATT}}$	V

## GENERAL

Passive Out BUS Leakage					$\mu\text{A}$
Passive In $0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$ , $-1.5\text{ V} \leq V_{\text{BUS}} < 0\text{ V}$	$I_{\text{LEAK}}$	10	–	-10	
Active In $0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$ , $0\text{ V} < V_{\text{BUS}} \leq 12.5\text{ V}$	$I_{\text{LKAI}}$	10	–	-10	
BUS Leakage During Loss of Module Ground (Note 4) $0\text{ V} \leq V_{\text{BATT}} \leq 18\text{ V}$	$I_{\text{BLKLOG}}$	10	–	-10	
Quiescent Current					
Sleep $5.0\text{ V} \leq V_{\text{BATT}} \leq 13\text{ V}$ (Note 5)	$I_{\text{QSLP}}$	0	45	80	$\mu\text{A}$
Awake with Transmitter Disabled $5.0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$I_{\text{QATDIS}}$	0	–	4.0	mA
Awake with Transmitter Enabled $5.0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$I_{\text{QATEN}}$	0	–	9.0	mA
Undervoltage Shutdown	$V_{\text{BATTUV}}$	2.5	4.8	5.0	V
Undervoltage Hysteresis	$V_{\text{UVHYS}}$	0	–	0.5	V

### Notes

4. BUS pin is at system ground voltage.
5. After  $t_{\text{CNTLFDLY}}$ .

## STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  unless otherwise noted. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>GENERAL (continued)</b>					
LOAD Voltage Rise (Note 6) Normal Speed and Voltage Mode, Transmit High-Voltage Mode, Transmit High-Speed Mode $I_{IN} = 1.0 \text{ mA}$ , $5.0 \text{ V} \leq V_{BATT} \leq 26.5 \text{ V}$ Sleep Mode (Note 8) $I_{IN} = 7.0 \text{ mA}$ Loss of Battery $I_{IN} = 7.0 \text{ mA}$	$V_{LDRISE}$	0	–	0.1	V
LOAD Leakage During Loss of Module Ground (Note 7) $0 \text{ V} \leq V_{BATT} \leq 18 \text{ V}$	$I_{LDLEAK}$	0	–	-90	$\mu\text{A}$

## TRANSMITTER

High-Voltage Wake-up Mode Output High Voltage $12 \text{ V} \leq V_{BATT} \leq 26.5 \text{ V}$ , $200 \Omega \leq R_L \leq 3332 \Omega$ $5.0 \text{ V} \leq V_{BATT} < 12 \text{ V}$ , $200 \Omega \leq R_L \leq 3332 \Omega$	$V_{HVWUOHF}$ $V_{HVWUOHO}$	9.7 Lesser of $V_{BATT} - 1.5$ or 9.7	– –	12.5 $V_{BATT}$	V
High-Speed Mode Output High Voltage $8.0 \text{ V} \leq V_{BATT} \leq 16 \text{ V}$ , $75 \Omega \leq R_L \leq 135 \Omega$	$V_{OHHS}$	4.2	–	5.1	V
Normal Mode Output High Voltage $6.0 \text{ V} \leq V_{BATT} \leq 26.5 \text{ V}$ , $200 \Omega \leq R_L \leq 3332 \Omega$ $5.0 \text{ V} \leq V_{BATT} < 6.0 \text{ V}$ , $200 \Omega \leq R_L \leq 3332 \Omega$	$V_{NOHF}$ $V_{NOHO}$	4.4 Lesser of $V_{BATT} - 1.6$ or 4.4	– –	5.1 Lesser of $V_{BATT}$ or 5.1	V
BUS Low Voltage $5.0 \text{ V} \leq V_{BATT} \leq 26.5 \text{ V}$ , $200 \Omega \leq R_L \leq 3332 \Omega$	$V_{OL}$	-0.2	–	0.2	V
Short Circuit BUS Output Current Dominant State, $5.0 \text{ V} \leq V_{BATT} \leq 26.5 \text{ V}$	$I_{BSC}$	-150	–	-350	mA
Thermal Shutdown (Note 8), (Note 9) $5.0 \text{ V} \leq V_{BATT} \leq 26.5 \text{ V}$	$T_{SD}$	150	–	190	$^{\circ}\text{C}$
Thermal Shutdown Hysteresis (Note 8) $5.0 \text{ V} \leq V_{BATT} \leq 26.5 \text{ V}$	$T_{SDHYS}$	10	–	20	$^{\circ}\text{C}$

### Notes

6. GMW3089V2.3 specifies the maximum load voltage rise to be 0.1 V whenever module battery is intact, including when in Sleep mode. The maximum load voltage rise of 1.0 V in Sleep mode is a GM-approved exception to GMW3089V2.3.
7. LOAD pin is at system ground voltage.
8. Guaranteed by design but not production tested.
9. Thermal shutdown causes the BUS output driver to be disabled.

# Freescale Semiconductor, Inc.

## STATIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  unless otherwise noted. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>RECEIVER</b>					
Input Threshold					V
Awake $5.0\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$V_{\text{BIA}}$	2.0	–	2.2	
Sleep $12\text{ V} \leq V_{\text{BATT}} \leq 26.5\text{ V}$	$V_{\text{BISF}}$	6.6	–	7.9	
Sleep $5.0\text{ V} \leq V_{\text{BATT}} < 12\text{ V}$	$V_{\text{BISO}}$	Lesser of 6.6 V or $V_{\text{BATT}} - 4.3$	–	Lesser of 7.9 V or $V_{\text{BATT}} - 3.25$	

## DYNAMIC ELECTRICAL CHARACTERISTICS

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  unless otherwise noted. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
<b>TRANSMITTER</b>					
Normal Speed Rising Output Delay $200\ \Omega \leq R_L \leq 3332\ \Omega$ , $1.0\ \mu\text{s} \leq \text{Load Time Constant} \leq 4.0\ \mu\text{s}$ Measured from TXD = $V_{IL}$ to $V_{BUS}$ as follows: Max Time to $V_{BUSMOD} = 3.7\ \text{V}$ , $6.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ (Note 10) Min Time to $V_{BUSMOD} = 1.0\ \text{V}$ , $6.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ (Note 10) Max Time to $V_{BUSMOD} = 2.7\ \text{V}$ , $V_{BATT} = 5.0\ \text{V}$ (Note 10) Min Time to $V_{BUSMOD} = 1.0\ \text{V}$ , $V_{BATT} = 5.0\ \text{V}$ (Note 10)	$t_{DLYNORMRO}$	2.0	–	6.3	$\mu\text{s}$
Normal Speed Falling Output Delay $200\ \Omega \leq R_L \leq 3332\ \Omega$ , $1.0\ \mu\text{s} \leq \text{Load Time Constant} \leq 4.0\ \mu\text{s}$ Measured from TXD = $V_{IH}$ to $V_{BUS}$ as follows: Max Time to $V_{BUSMOD} = 1.0\ \text{V}$ , $6.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ (Note 10) Min Time to $V_{BUSMOD} = 3.7\ \text{V}$ , $6.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ (Note 10) Max Time to $V_{BUSMOD} = 1.0\ \text{V}$ , $V_{BATT} = 5.0\ \text{V}$ (Note 10) Min Time to $V_{BUSMOD} = 2.7\ \text{V}$ , $V_{BATT} = 5.0\ \text{V}$ (Note 10)	$t_{DLYNORMFO}$	1.8	–	8.5	$\mu\text{s}$
High-Speed Rising Output Delay $75\ \Omega \leq R_L \leq 135\ \Omega$ , $0\ \mu\text{s} \leq \text{Load Time Constant} \leq 1.5\ \mu\text{s}$ , $8.0\ \text{V} \leq V_{BATT} \leq 16\ \text{V}$ Measured from TXD = $V_{IL}$ to $V_{BUS}$ as follows: Max Time to $V_{BUS} = 3.7\ \text{V}$ (Note 11) Min Time to $V_{BUS} = 1.0\ \text{V}$ (Note 11)	$t_{DLYHSRO}$	0.1	–	2.0	$\mu\text{s}$
High-Speed Falling Output Delay $75\ \Omega \leq R_L \leq 135\ \Omega$ , $0\ \mu\text{s} \leq \text{Load Time Constant} \leq 1.5\ \mu\text{s}$ , $8.0\ \text{V} \leq V_{BATT} \leq 16\ \text{V}$ Measured from TXD = $V_{IH}$ to $V_{BUS}$ as follows: Max Time to $V_{BUS} = 1.0\ \text{V}$ (Note 11) Min Time to $V_{BUS} = 3.7\ \text{V}$ (Note 11)	$t_{DLYHSFO}$	0.04	–	3.0	$\mu\text{s}$

**Notes**

10.  $V_{BUSMOD}$  is the voltage at the BUSMOD node in [Figure 2](#), page 10.
11.  $V_{BUS}$  is the voltage at the BUS pin in [Figure 3](#), page 10.



## DYNAMIC ELECTRICAL CHARACTERISTICS (continued)

Characteristics noted under conditions  $-40^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$  unless otherwise noted. Voltages are relative to GND unless otherwise noted. All positive currents are into the pin. All negative currents are out of the pin.

Characteristic	Symbol	Min	Typ	Max	Unit
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### TRANSMITTER (continued)

High-Voltage Rising Output Delay $200\ \Omega \leq R_L \leq 3332\ \Omega$ , $1.0\ \mu\text{s} \leq \text{Load Time Constance} \leq 4.0\ \mu\text{s}$ Measured from $V_{IL}$ to $V_{BUS}$ as follows: Max Time to $V_{BUSMOD} = 3.7\ \text{V}$ , $6.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ (Note 12) Min Time to $V_{BUSMOD} = 1.0\ \text{V}$ , $6.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ (Note 12) Max Time to $V_{BUSMOD} = 9.4\ \text{V}$ , $12.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ (Note 12)	$t_{DLYHVRO}$	2.0 2.0 2.0	– – –	6.3 6.3 18	$\mu\text{s}$
High-Voltage Falling Output Delay $200\ \Omega \leq R_L \leq 3332\ \Omega$ , $1.0\ \mu\text{s} \leq \text{Load Time Constance} \leq 4.0\ \mu\text{s}$ , $12.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ Measured from $V_{IH}$ to $V_{BUS}$ as follows: Max Time to $V_{BUSMOD} = 1.0\ \text{V}$ (Note 12) Min Time to $V_{BUSMOD} = 3.7\ \text{V}$ (Note 12)	$t_{DLYHVFO}$	1.8 1.8	– –	13.7 13.7	$\mu\text{s}$

### RECEIVER

Receive Delay Time ( $5.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ ) Awake	$t_{RDLY}$	0.2	–	1.0	$\mu\text{s}$
Receive Delay Time (BUS Rising to RXD Falling, $5.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ ) Sleep	$t_{RDLYSL}$	10	–	70	$\mu\text{s}$

### LOGIC I/O

CNTL Falling Delay Time ( $5.0\ \text{V} \leq V_{BATT} \leq 26.5\ \text{V}$ )	$t_{CNTLFDLY}$	300	–	1000	ms
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#### Notes

12.  $V_{BUSMOD}$  is the voltage at the BUSMOD node in [Figure 2](#), page 10.

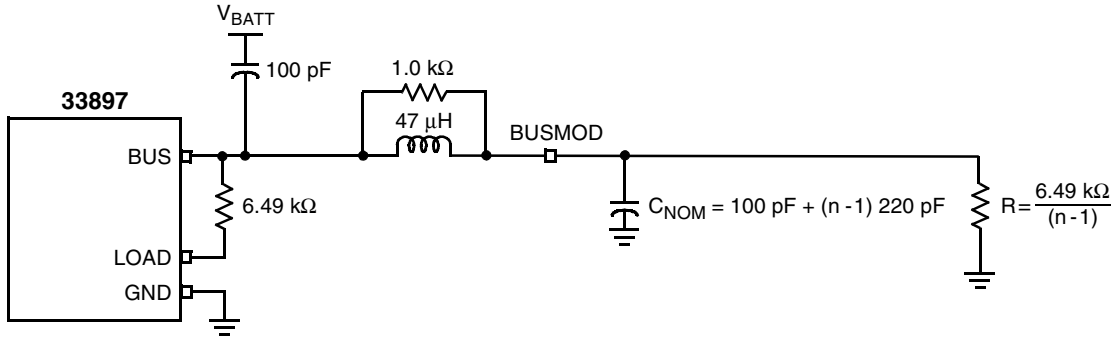


Figure 2. Transmitter Delays in Normal and High-Voltage Wake-up Modes

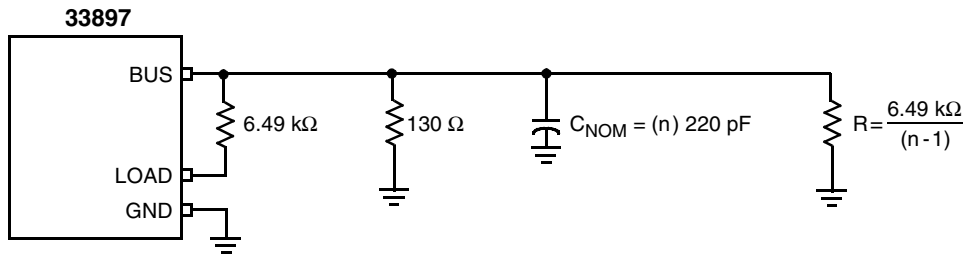


Figure 3. Transmitter Delays in High-Speed Mode

## SYSTEM/APPLICATION INFORMATION

### INTRODUCTION

The 33897 is intended for use as a physical layer device in a single-wire CAN communications bus. The communications takes place from a single pin over a single wire using a common ground for a current return path. Two data rates are available, with the high rate used for factory or assembly line communications and the lower for actual system

communications where the radiated EMI of the higher rate could be an issue.

Two pins control of the mode of operation (sleep, low-speed, high-speed, and high-voltage wake-up).

### BLOCK DIAGRAM COMPONENTS

#### Timer OSC

This circuit generates a 500 kHz signal to be used for internal logic. It is the reference for some of the required delays.

#### Timers

This circuit contains the timing logic used to hold the CNTL active for the required time after the conditions for sleep mode have been met. It is also used to keep the TXD driver active for a period of time after it has generated a passive level on the bus.

#### Mode Control

This circuit contains the control logic for the various operating modes and conditions required for the IC.

#### BUS RCVR

This circuit translates the levels on the BUS pin to a CMOS level indicating the presence of a data 0 or 1. It also determines the presence of a high-voltage wake-up (HVWU) signal that is passed to Mode Control and Timers circuits. An analog filter is used to “de-glitch” the high-voltage wake-up signal and prevent false exits from the sleep mode.

#### TX BUS DRVR

This circuit drives the BUS. It can drive it with the higher voltage wake-up signals when enabled by the Mode Control circuit. It can also provide waveshaping for reduced EMI or not provide it for the higher data rate mode. The actual data is received on TXD at CMOS logic levels, then translated by this circuit to the necessary operating voltages.

#### Undervoltage Detect

This circuit monitors internal operating voltage to assure proper operation of the part. If a low-voltage condition is detected, it sends a signal to disable the BUS RCVR and Tx BUS DRVR circuits. This prevents incorrect data from being put on the bus or sent to the MCU.

#### Load Switch

The LOAD switch provides a path for an external resistor connected to the BUS to be connected to ground. When a loss of ground is detected, this switch is opened to prevent the current that would normally be flowing to the ground from the module from going back through the load resistor and raising the bus level. The circuit is opened when the voltage between GND and VBATT becomes too low as would be the case if module ground were lost.

### OPERATION

The 33897 is intended to be used with an MCU to control its operation and to process and generate the data for the bus.

#### Ground Pins

The four ground pins are not only for electrical conduction, their number and locations at each of the four corners serve also to remove heat from the IC. The biggest benefit of this is obtained by putting a lot of copper on the PCB in this area and, if ground is an internal layer, by adding numerous plated-through connections to it with the largest diameter holes the layout can use.

#### TX Data

The data driven onto the SWCAN bus is inverted from the TXD pin. A “1” driven on TXD will result in an undriven

(recessive) state (bus at near zero volts). When the TXD pin is low, the output goes to a driven state. The voltage and waveshaping in the driven state is determined by the levels on the MODE0 and MODE1 pins (refer to [Table 1](#)).

**Table 1. Mode Control**

MODE0	MODE1	Operation
0	0	Sleep Mode
0	1	Transmit High Voltage (Wake-up)
1	0	Transmit High Speed
1	1	Normal Speed and Voltage

## Mode Control

The MODE pins control the transmitter filtering and BUS voltage and the IC sleep mode operation. [Table 1](#) shows the mode versus the logic levels on MODE0 and MODE1.

The MODE0 and MODE1 pins have a weak pull-down in the IC so that in case the pins are not driven, the device will enter the sleep mode. This is usually the situation as the MCU comes out of reset, before the driving signals have been configured as outputs.

## RX Data

The data received on the bus is translated to logic levels on this pin. This pin is a logic high when the bus is in the recessive state (near zero volts) and is low when the bus is in either the normal or high-voltage dominant state.

This is an open-drain type of output that requires an external resistor to pull it up. When the device is in sleep mode, the output will be off unless a high-voltage wake-up level is detected on the bus. If the wake-up level is detected, the output will be driven by the data on the bus. If the level of the data returns to normal level, the output will return to off after a short delay unless a non-sleep mode condition is set by the MCU.

## LOAD Switch

This switch is on in all operating modes unless a loss of ground is detected. If this happens, the switch is opened and the resistor normally attached to its pin will be no longer pass current to or from the bus.

## CNTL Output

This logic level signal is used to control a  $V_{CC}$  regulator. When the output is low, the  $V_{CC}$  regulator is expected to shutdown. This is normally used to shut down the MCU and all the devices powered by  $V_{CC}$  when the IC is in sleep mode. This is done to save power. When the part is taken out of the sleep mode by the higher-than-normal bus voltage, this pin is asserted high and the  $V_{CC}$  regulator brings its output up to the regulated level. This starts the MCU, which controls the mode of the IC. The MCU must change the mode signals to non-sleep mode levels in order to keep this pin from going low. There is a delay to allow the MCU to fully wake up and take control after the high-voltage signaling is removed before the level on this output returns low. After a delay time, even if the bus is at high voltage, the IC will return to sleep mode if both MODE pins are low.

## VBATT Input

This power input is not reverse battery protected and should use an external diode to protect it from damage owing to reverse battery if this protection is desired. The voltage drop of the diode must be taken into consideration when the operating range of the system is being determined. This diode is generally used to protect the entire module from reverse battery and should be selected accordingly.

## BUS I/O

This input/output may require ESD and/or EMI external circuitry. A set of components is shown in the Simplified Application Diagram on the front of this datasheet. The value of the capacitor should be adjusted downward in direct proportion to the added capacitance of the ESD or EMI circuits. The series resistance of the inductor should be kept below  $3.5 \Omega$  to prevent its voltage drop from significantly degrading system noise margins.

APPLICATIONS

Figure 4 shows a typical application schematic for the 33897.

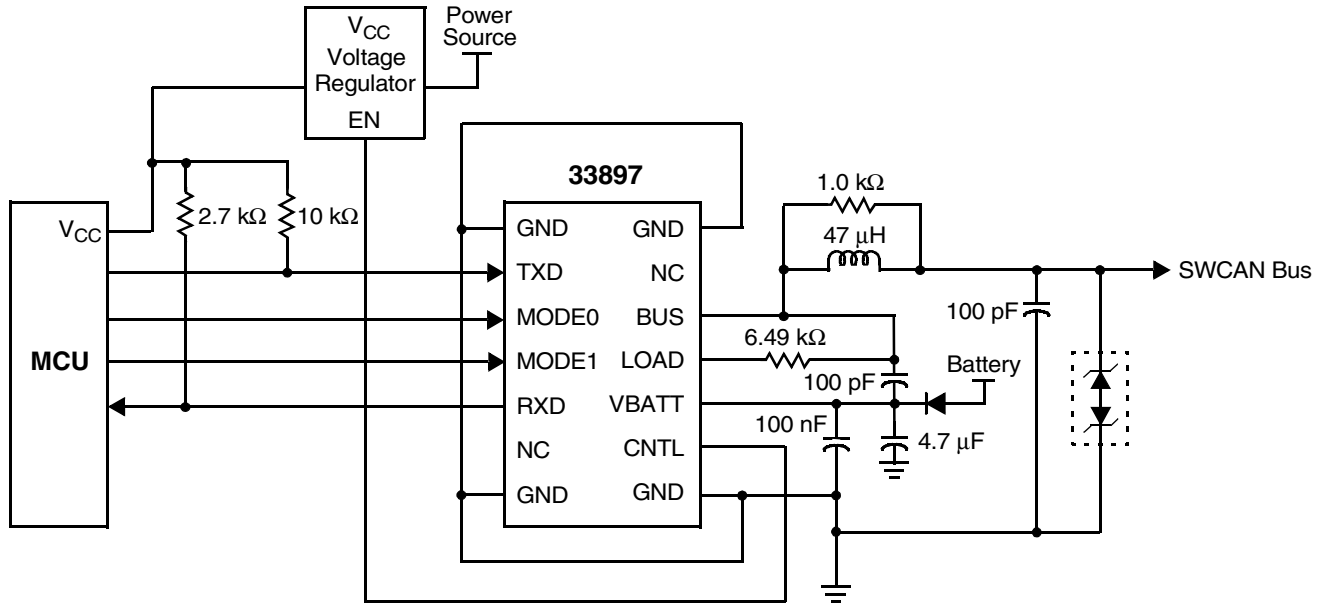


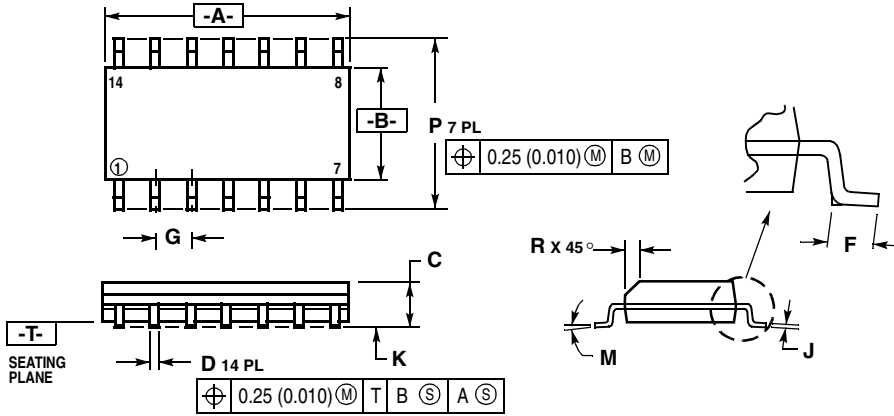
Figure 4. 33897 Typical Application Schematic

PACKAGE DIMENSIONS

D SUFFIX  
 EF (Pb-FREE) SUFFIX  
 14-LEAD SOICN  
 PLASTIC PACKAGE  
 CASE 751A-03  
 ISSUE F

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

Freescale Semiconductor, Inc.

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