NAND Controller
GLS55VD031

Data Sheet

FEATURES:

- **Industry Standard ATA/IDE Bus Interface**
  - Host Interface: 16-bit access
  - Supports up to PIO Mode-6
  - Supports up to Multi-word DMA Mode-4
  - Supports up to Ultra DMA Mode-5
- **Interface for Standard NAND Flash Media**
  - Flash Media Interface: Single or Dual 8-bit access
    - Supports up to 8 flash media devices directly
    - Supports up to 64 flash media devices with external decoding logic
  - Supports Single-Level Cell (SLC) or Multi-Level Cell (MLC) flash media
    - 2 KByte and 4 KByte program page size
    - 8 KByte program page size (SLC, single channel only)
- **Low Power, 3V Power Supply and NAND flash interface**
- **3V host interface**
- **Low Power Operation:**
  - Active mode: 25 mA (3V) (typical)
  - Sleep mode: 65 µA (3V) (typical)
- **Power Management Unit**
  - Immediate disabling of unused circuitry without host intervention
  - Zero wake-up latency
- **Expanded Data Protection**
  - WP#/PD# pin configurable by firmware for prevention of data overwrites
  - Added data security through user-selectable protection zones
- **20-byte Unique ID for Enhanced Security**
  - User-Programmable 10-byte ID
- **Programmable, Multitasking NAND Interface**
- **Firmware Storage in Embedded SuperFlash**
- **Pre-programmed Embedded Firmware**
  - Performs self-initialization on first system Power-on
  - Executes industry standard ATA/IDE commands
  - Implements advanced wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
- **Built-in Hardware ECC**
  - Corrects up to 8 random bits of error per 512-byte sector
- **Built-in Internal System Clock**
- **Multi-tasking Technology enables Fast Sustained Write Performance (Host to Flash)**
  - Supports up to 30 MByte/sec
- **Fast Sustained Read Performance (Flash to Host)**
  - Up to 40 MByte/sec
- **Automatic Recognition and Initialization of Flash Media Devices**
  - Seamless integration into a standard SMT manufacturing process
  - 5 sec. (typical) for flash drive recognition and setup
- **Commercial and Industrial Temperature Ranges**
  - 0°C to 70°C for commercial operation
  - -40°C to +85°C for industrial operation
- **Packages Available**
  - 100-lead TQFP – 14mm x 14mm x 1.10mm
  - 85-ball VFBGA – 6mm x 6mm x 0.86mm

PRODUCT DESCRIPTION

The NAND Controller is the heart of a high-performance, flash media-based data storage system. The NAND Controller recognizes the control, address, and data signals on the ATA/IDE bus and translates them into memory accesses to the standard NAND-type flash media. The GLS55VD031 device supports Single-Level Cell (SLC) and Multi-Level Cell (MLC) flash media. This technology is ideal for solid-state mass storage applications offering, expanded functionality while enabling smaller, lighter designs with lower power consumption.

The ATA/IDE interface is widely used in such products as portable and desktop computers, digital cameras, multimedia players, music players, handheld data collection scanners, PDAs, handy terminals, personal communicators, audio recorders, monitoring devices, global positioning systems, and set-top boxes. The Greenliant NAND Controller supports standard ATA/IDE protocol with up to PIO Mode-6, Multi-word DMA Mode-4, and Ultra DMA Mode-5 interface.

The NAND Controller uses Greenliant proprietary SuperFlash memory technology and is factory pre-programmed with an embedded flash file system. Upon initial power-on,

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the NAND Controller recognizes attached flash media devices, sets up a bad block table, executes all necessary handshaking routines for flash media support, and performs the low-level format.

The entire set up process typically takes about 3 sec plus 0.5 sec for each GByte of drive capacity. A 16 GByte flash drive is fully initialized in about 11 seconds.

For added manufacturing flexibility, system debug, re-initialization, and user customization is accomplished through the ATA/IDE interface.

The GLS55VD031 offers sustained read and write performance up to 40 MB/sec; and directly supports up to 8 flash media devices or, through simple decoding logic, supports up to 64 flash media devices.

For confidential information stored in the flash media, the GLS55VD031 provides exceptional security protection. Four password-protected, protection zones can be set to Read/Write, Read-only, or Hidden (Read-disabled). The NAND Controller also provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites

The GLS55VD031 is available in an industry-standard, 100-lead TQFP package or an 85-ball VFBGA package for easy integration into an SMT manufacturing process.

GENERAL DESCRIPTION

The NAND Controller contains a microcontroller and embedded flash file system integrated in TQFP and VFBGA packages. Refer to Figure 1 for the NAND Controller block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

Performance-optimized NAND Controller

The heart of the flash drive is the NAND Controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the NAND Controller's operation.

Microcontroller Unit (MCU)

The MCU translates ATA/IDE commands into data and control signals required for flash media operation.

Internal Direct Memory Access (DMA)

The NAND Controller uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

Power Management Unit (PMU)

The power management unit controls the power consumption of the NAND Controller. The PMU dramatically reduces the power consumption of the NAND Controller by putting the part of the circuitry that is not in operation into sleep mode. The PMU is designed so that it has zero wake-up latency.

SRAM Buffer

A key contributor to the NAND Controller performance is an SRAM buffer. The buffer optimizes the host's data transfer to and from the flash media.

Embedded Flash File System

The embedded flash file system is an integral part of the NAND Controller. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads.
2. Provides advanced flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media.
3. Keeps track of data file structures.
4. Manages system security for the selected protection zones.

Error Correction Code (ECC)

The NAND Controller utilizes BCH Error detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to eight random single-bit errors for each 512-byte block of data.

High performance is achieved through hardware-based error detection and correction.

Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed to provide trace information during debugging processes.To aid in validation, always provide the SCI access to PCB design.

Programmable, Multi-tasking NAND Interface

The multi-tasking interface enables fast, sustained write performance by allowing multiple Read, Program, and Erase operations to multiple flash media devices. The ease with which the NAND interface can be programmed enables the quick support of new NAND devices.

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FUNCTIONAL BLOCKS

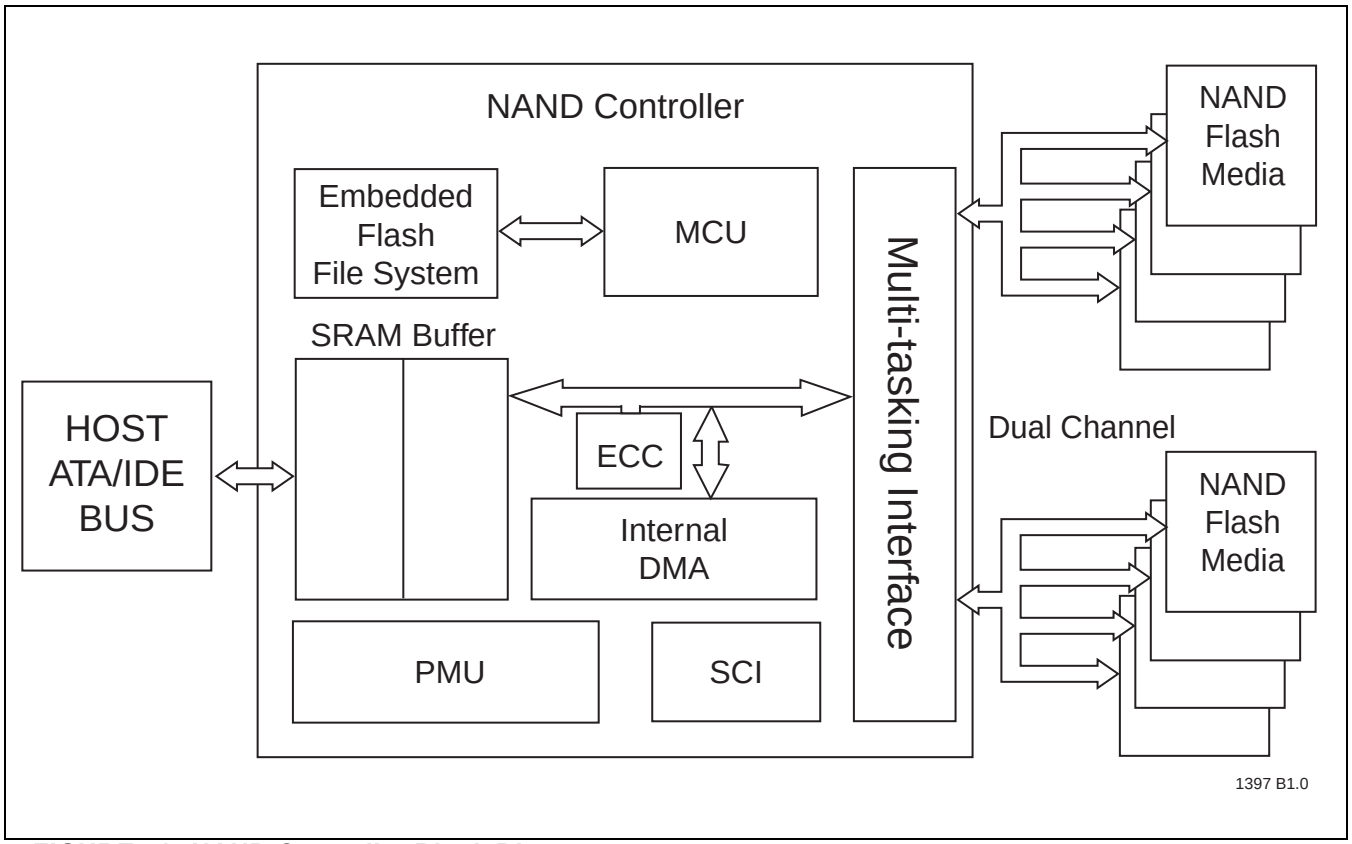
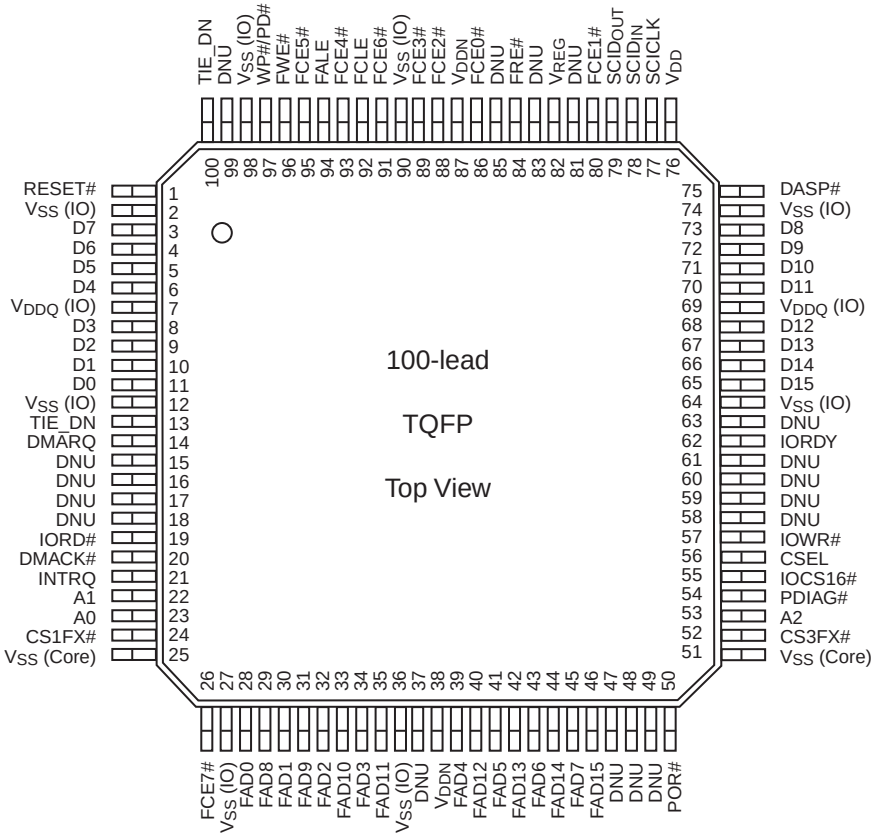


FIGURE 1: NAND Controller Block Diagram

PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 2. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the NAND Controller sources are outputs.

The NAND Controller functions in ATA mode, which is compatible with IDE hard disk drives.



Note: DNU means Do Not Use, must be left unconnected.

1397 100-tqfp P1.1

FIGURE 2: Pin Assignments for 100-lead TQFP (TQW)

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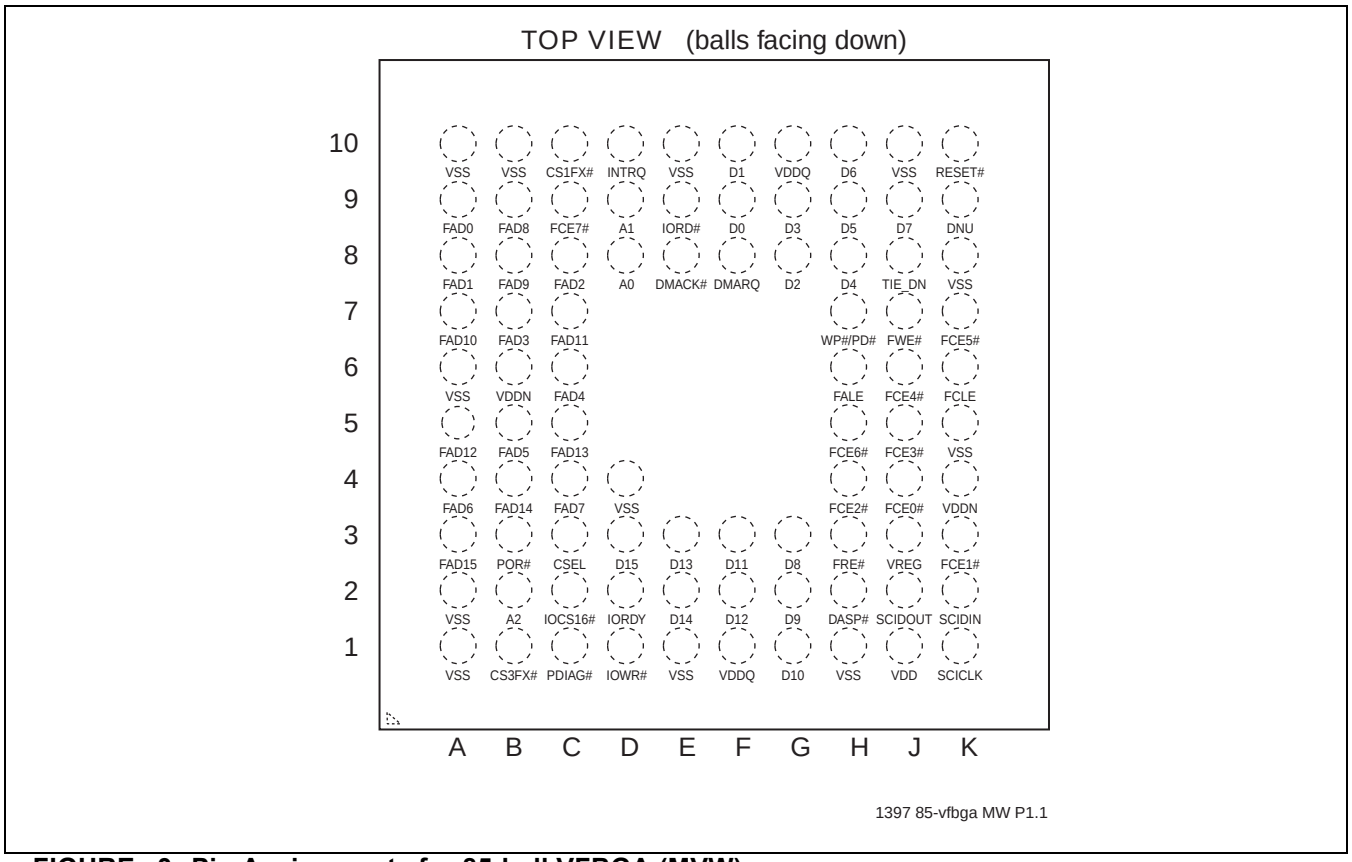

FIGURE 3: Pin Assignments for 85-ball VFBGA (MVW)

TABLE 1: Pin Assignments (1 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin Type	I/O Type[1]	Name and Functions
Host Interface					
A2	53	B2	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	22	D9			
A0	23	D8			
D15	65	D3	I/O	I1Z/O1	D[15:0] Data bus
D14	66	E2			
D13	67	E3			
D12	68	F2			
D11	70	F3			
D10	71	G1			
D9	72	G2			
D8	73	G3			
D7	3	J9			
D6	4	H10			
D5	5	H9			
D4	6	H8			
D3	8	G9			
D2	9	G8			
D1	10	F10			
D0	11	F9			
DMACK#	20	E8	I	I2U	DMA Acknowledge - input from host
DMARQ	14	F8	O	O1	DMA Request to host
IORDY	62	D2	O	O1	IORDY: When in PIO mode, the device is not ready to respond to a data transfer request, this signal is negated to extend the Host transfer cycle after from the assertion of DIOR- or DIOW-. However, this signal is never negated by the controller.
					DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the device to indicate that the device is ready to receive Ultra DMA data-out bursts. The device may negate DDMARDY to pause an Ultra DMA transfer.
					DSTROBE: When Ultra DMA mode DMA Read is active, this signal is the data-in strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-in burst.
CS1FX#	24	C10	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	52	B1			CS3FX# is used to select the Alternate Status register and the Device Control register.
CSEL	56	C3	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.

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TABLE 1: Pin Assignments (Continued) (2 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin Type	I/O Type[1]	Name and Functions
IORD#	19	E9	I	I2Z	IORD#: This is an I/O Read strobe generated by the host. While Ultra DMA mode is not active, this signal gates I/O data from the device.
					HDMARDY#: When Ultra DMA mode DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data in bursts. The host may negate HDMARDY# to pause an Ultra DMA transfer.
					HSTROBE: When Ultra DMA mode DMA Write is active, this signal is the data out strobe generated by the host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data out burst.
IOWR#	57	D1	I	I2Z	This is an I/O Write strobe generated by the host. When Ultra DMA is not active, this signal clocks I/O into the device.
					When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst
IOCS16#	55	C2	O	O2	This output signal is asserted low when the device is indicating a word data transfer cycle.
INTRQ	21	D10	O	O1	This signal is the active high Interrupt Request to the host.
PDIAG#	54	C1	I/O	I1U/O1	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	75	H2	I/O	I1U/O3	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	1	K10	I	I2U	This input pin is the active low hardware reset from the host.
Flash Media Interface (3v)					
FRE#	84	H3	O	O7	Active Low Flash Media Chip Read
FWE#	96	J7			Active Low Flash Media Chip Write
FCLE	92	K6	O	O6	Active High Flash Media Chip Command Latch Enable
FALE	94	H6			Active High Flash Media Chip Address Latch Enable
FAD15	46	A3	I/O	I3U/O6	Flash Media Chip High Byte Address/Data Bus pins
FAD14	44	B4			
FAD13	42	C5			
FAD12	40	A5			
FAD11	35	C7			
FAD10	33	A7			
FAD9	31	B8			
FAD8	29	B9			

TABLE 1: Pin Assignments (Continued) (3 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin Type	I/O Type[1]	Name and Functions
FAD7	45	C4	I/O	I3U/O6	Flash Media Chip Low Byte Address/Data Bus pins
FAD6	43	A4			
FAD5	41	B5			
FAD4	39	C6			
FAD3	34	B7			
FAD2	32	C8			
FAD1	30	A8			
FAD0	28	A9			
FCE7#	26	C9	O	O4	Active Low Flash Media Chip Enable pin
FCE6#	91	H5			
FCE5#	95	K7			
FCE4#	93	J6			
FCE3#	89	J5			
FCE2#	88	H4			
FCE1#	80	K3			
FCE0#	86	J4			
$SCID_{OUT}$	79	J2	O	O5	SCI interface data output
$SCID_{IN}$	78	K2	I	I3U	SCI interface data input
SCICLK	77	K1	I	I3U	SCI interface clock
WP#/PD#	97	H7	I	I3U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.
Miscellaneous					
V_{SS} (IO)	2 12 27 36 64 74 90 98	A2, A6 A10 D4 E1 E10 H1 J10 K5 K8	PWR		Ground for I/O
V_{SS} (Core)	25 51	A1 B10	PWR		Ground for Core
V_{DDN} (IO)	38 87	B6 K4	PWR		3V For Media Interface and SCI
V_{DD}	76	J1	PWR		3V Core Power Supply
V_{DDQ} (IO)	7 69	F1 G10	PWR		3V for Host interface
V_{REG}	82	J3	O		External capacitor pin. Connect to external 4.7 uF capacitor.
POR#	50	B3	I	Analog Input[2]	Power-on Reset (POR). Active Low, 3V input

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TABLE 1: Pin Assignments (Continued) (4 of 4)

Symbol	Pin No. 100-TQFP	Pin No. 85-VFBGA	Pin Type	I/O Type[1]	Name and Functions
T_{IE}_DN	13, 100	J8			Pin needs to be connected to V_{SS}.
DNU[3]	15 16 17 18 37 47 48 49 58 59 60 61 63 81 83 85, 99	K9			Do Not Use, must be left unconnected.

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1. See “Electrical Specifications” on page 35. for I/O type description.
2. Analog input for supply voltage detection
3. All DNU pins should not be connected.

CAPACITY SPECIFICATION

Table 2 shows the default capacity. To change the default settings, update the drive ID table (see Table 8). If the total number of bytes is less than the default, the remaining space could be used as spares to increase the flash drive endurance. When the total flash drive capacity exceeds the total default number of bytes, the flash drive endurance is reduced.

TABLE 2: Default ATA Flash Drive Settings

Capacity[1]	Total Bytes	Cylinders[2]	Heads[2]	Sectors[2]	Max LBA
1 GB	1,024,966,656	1986	16	63	2,001,888
2 GB	2,048,385,024	3969	16	63	4,000,752
4 GB	4,096,253,952	7937	16	63	8,000,496
6 GB	6,001,164,288	11628	16	63	11,721,024
8 GB	8,001,552,384	15504	16	63	15,628,032
16 GB	16,013,942,784	31029	16	63	31,277,232
32 GB	32,017,047,552	62037	16	63	62,533,296
48 GB	48,020,152,320	93045	16	63	93,754,080
64 GB	64,023,257,088	124053	16	63	125,045,424
96 GB	96,029,466,624	186069	16	63	187,557,552
128 GB	128,035,676,160	248085	16	63	250,069,680

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1. These flash drive capacities can only be manufactured by using the specified version of the NAND Controller.
2. Cylinders, Heads, and Sectors can be re-configured from the default settings during the manufacturing process.

Functional Specifications

Table 3 shows the performance and the maximum capacity supported by GLS55VD031.

TABLE 3: Functional Specification of GLS55VD031

Functions	GLS55VD031
NAND Controller Supported Capacity	up to 128 GB
NAND Controller Performance-Sustained Write speed	Up to 30 MB/sec
NAND Controller Performance-Sustained Read speed	Up to 40 MB/sec

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MANUFACTURING SUPPORT

The NAND Controller firmware contains a list of supported standard NAND flash media devices. Upon initial Power-on, the controller scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices in the NAND controller, the controller performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format. For Power-up timing specifications, please refer to Table 13.

Please contact Greenliant for the most current list of supported NAND Flash media devices.

In the event that the NAND flash media device ID is not recognized by the NAND Controller, the user has an option of adding this device to the controller device table through the manufacturing interface provided by Greenliant. Please contact Greenliant for the NAND Controller manufacturing interface software. If the drive initialization fails, and a visual inspection is unable to determine the problem, the GLS55VD031 NAND Controller provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

ATA/IDE Interface

The NAND Controller interface can be used for manufacturing support. Greenliant provides an example of a DOS-based solution (an executable routine downloadable from www.greenliant.com) for manufacturing debug and rework.

Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can report manufacturing errors. The SCI consists of 3 active signals: $SCID_{OUT}$, $SCID_{IN}$, and SCICLK.

SECURITY FEATURES

The GLS55VD031 NAND Controller offers added data protection for applications where data security is of the utmost importance. The secure features are:

1. Protection zones - Customer can enable up to 4 independent protection zones, with two options: Read-only or Hidden (Read and Write protected) within each protected zone. If protection zones are not enabled the data is unprotected (default configuration).
2. Password protection - Accessing information within the protected zones can be only achieved through a customer-unique password.
3. Purge command - The system can issue a Purge command to erase all information stored in the flash media.

CONFIGURABLE WRITE PROTECT/POWER-DOWN MODES

The WP#/PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP#/PD#-Mode, explained in Section .

Once the mode is set with this command, the pin will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

Write Protect Mode

When the WP#/PD# pin is configured in the Write Protect mode, the pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, the WP#/PD# pin should be asserted prior to issuing the destructive commands: Erase-Sector, Format-Track, Write-DMA, Write-Long-Sector, Write-Multiple, Write-Multiple-without-Erase, Write-Sector(s), Write-Sector-without-Erase, or Write-Verify. This will force the NAND Controller to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

Power-down Mode

When the WP#/PD# is configured in the Power-down mode, if the pin is asserted during a command, the NAND Controller completes the current command and returns to the standby mode immediately to save power. Afterwards, the device will not accept any other commands. Only a Power-on Reset (POR) or hardware reset will bring the device to normal operation with the WP#/PD# pin de-asserted.

POWER-ON AND BROWN-OUT RESET CHARACTERISTICS

Power-on and Brown-out Reset circuitry reset the device to a known state. Power-on Reset asserts when the device is turned on. Brown-out Reset asserts when the detected voltage falls below an acceptable level. For more information about the Power-on and Brown-out Reset timing, see Figure 4 and Table 4.

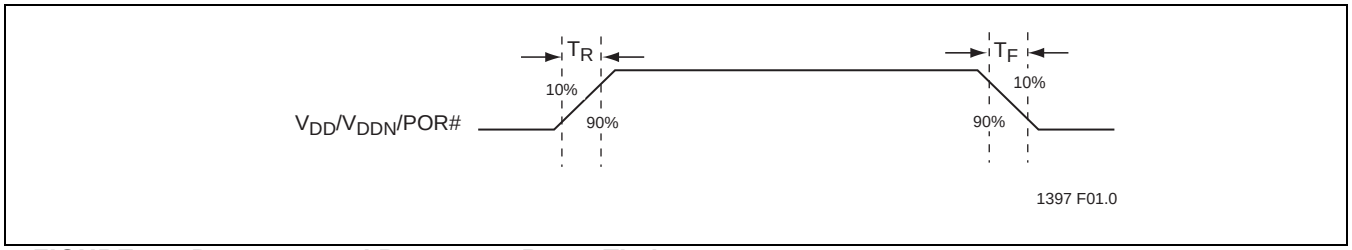

FIGURE 4: Power-on and Brown-out Reset Timing

TABLE 4: Power-on and Brown-out Reset Timing

Item	Symbol	Min	Max	Units
V_{DD}/V_{DDN}/POR# Rise Time[1]	T_R		250	ms
V_{DD}/V_{DDN}/POR# Fall Time[2]	T_F		250	ms

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1. V_{DD} Rise Time should be faster than or equal to POR# Rise Time.
2. V_{DD} Fall Time should be slower than or equal to POR# Fall Time.

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I/O TRANSFER FUNCTION

The default operation for the NAND Controller is 16-bit. However, if the host issues a Set-Feature command to enable 8-bit mode, the NAND Controller permits 8-bit data access.

The following table defines the function of various operations.

TABLE 5: I/O Function

Function Code	CS3FX#	CS1FX#	A0-A2	IORD#	IOWR#	D15-D8	D7-D0
Invalid Mode	V_{IL}	V_{IL}	X	X	X	Undefined	Undefined
Standby Mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	X	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	In[1]	In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Out[1]	Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	X	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out

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1. If 8-bit data transfer mode is enabled.
In 8-bit data transfer mode, High Byte is undefined for Data Out. For Data In, X can be V_{IH} or V_{IL}, but no other value.

SOFTWARE INTERFACE

NAND Controller Drive Register Set Definitions and Protocol

This section defines the drive registers for the NAND Controller and the protocol used to address them.

NAND Controller Addressing

The I/O decoding for a NAND Controller is shown in Table 6.

TABLE 6: Task File Registers

CS3FX#	CS1FX#	A2	A1	A0	Registers	
					IORD# = 0 (IOWR#=1)	IOWR# = 0 (IORD#=1)
1	0	0	0	0	Data (Read)	Data (Write)
1	0	0	0	1	Error	Feature
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector Number (LBA 7-0)	Sector Number (LBA 7-0)
1	0	1	0	0	Cylinder Low (LBA 15-8)	Cylinder Low (LBA 15-8)
1	0	1	0	1	Cylinder High (LBA 23-16)	Cylinder High (LBA 23-16)
1	0	1	1	0	Drive/Head	Drive/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alternate Status	Device Control

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NAND Controller Registers

The following section describes the hardware registers used by the host software to issue commands to the NAND Controller. These registers are often collectively referred to as the Task File registers. The registers are only selectable through CS3FX#, CS1FX#, and A_2-A_0 signals.

Data Register (Read/Write)

This 16-bit register is used to transfer data blocks between the device data buffer and the host. Data transfer can be performed in PIO mode or DMA mode.

Error Register (Read Only)

This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	Reset Value
ICRC/BBK	UNC	0	IDNF	0	ABRT	0	AMNF	0000 0000b

Symbol	Function
ICRC / BBK	This bit is set when a Bad Block is detected. During an ultra-DMA transfer, this bit is set on detection of a CRC error.
UNC	This bit is set when an Uncorrectable Error is encountered.
IDNF	The requested sector ID is in error or cannot be found.
ABRT	This bit is set if the command has been aborted because of an NAND Controller status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued. It

	is required that the host retry any media access command (such as Read-Sectors and Write-Sectors) that ends with an error condition.
AMNF	This bit is set in case of a general error.

Feature Register (Write Only)
This register provides additional command-specific parameters to the NAND Controller.

Sector Count Register
This register contains the numbers of sectors of data requested to be transferred on a Read or Write operation between the host and the NAND Controller. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

Sector Number (LBA 7-0) Register
This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any NAND Controller data access for the subsequent command.

Cylinder Low (LBA 15-8) Register
This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of the Logical Block Address.

Cylinder High (LBA 23-16) Register
This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

Drive/Head (LBA 27-24) Register
The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
1	LBA	1	DRV	HS3	HS2	HS1	HS0	**1010 0000b**

Symbol	**Function**
LBA	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block mode, the Logical Block Address is interpreted as follows: LBA7-LBA0: Sector Number register D7-D0. LBA15-LBA8: Cylinder Low register D7-D0. LBA23-LBA16: Cylinder High register D7-D0. LBA27-LBA24: Drive/Head register bits HS3-HS0.
DRV	DRV is the drive number. When DRV=0 (Master), Master is selected. When DRV=1 (Slave), Slave is selected.
HS3	When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
HS2	When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
HS1	When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
HS0	When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

Status & Alternate Status Registers (Read Only)

These registers return the NAND Controller status when read by the host. Reading the Status register does clear a pending interrupt while reading the alternate Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0	Reset Value
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR	1000 0000b

Symbol	Function
BUSY	The busy bit is set when the NAND Controller has access to the command buffer and registers and the host is locked out from accessing the Command register and buffer. No other bits in this register are valid when this bit is set to a 1.
RDY	RDY indicates whether the device is capable of performing NAND Controller operations. This bit is cleared at power up and remains cleared until the NAND Controller is ready to accept a command.
DWF	This bit, if set, indicates a write fault has occurred.
DSC	This bit is set when the NAND Controller is ready.
DRQ	The Data-Request bit is set when the NAND Controller requires that information be transferred either to or from the host through the Data register.
CORR	This bit is set when a correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector Read operation.
ERR	This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is required that the host retry any media access command (such as Read-Sectors and Write-Sectors) that end with an error condition.

Device Control Register (Write Only)

This register is used to control the NAND Controller interrupt request and to issue a software reset. This register can be written to even if the device is busy. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	Reset Value
X	X	X	X	1	SW Rst	-IEn	0	0000 1000b

Symbol	Function
SW Rst	This bit is set to 1 in order to force the NAND Controller to perform a software Reset operation. The chip remains in reset until this bit is reset to '0.'
-IEn	0: The Interrupt Enable bit enables interrupts 1: Interrupts from the NAND Controller are disabled This bit is set to 0 at Power-on and Reset.

Command Register (Write Only)

This register contains the command code being sent to the drive. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are listed in Table 7.

Data Sheet

NAND Controller Command Description

This section defines the software requirements and the format of the commands the host sends to the NAND Controller. Commands are issued to the NAND Controller by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. With the exception of commands listed in Sections -, NAND Controller complies with ATA-6 Specifications.

NAND Controller Command Set

Table 7 summarizes the NAND Controller command set.

TABLE 7: NAND Controller Command Set (1 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Check-Power-Mode	E5H or 98H	-	-	-	-	D[8]	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Flush-Cache	E7H	-	-	-	-	D	-
Format-Track	50H	-	Y[7]	-	Y	Y[8]	Y
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Security-Disable-Password	F6H	-	-	-	-	D	-
Security-Erase-Prepare	F3H	-	-	-	-	D	-
Security-Erase-Unit	F4H	-	-	-	-	D	-
Security-Freeze-Lock	F5H	-	-	-	-	D	-
Security-Set-Password	F1H	-	-	-	-	D	-
Security-Unlock	F2H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y	-	-	-	D	-
SMART	B0H	Y	Y	Y	Y	D	-
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Set-WP#/PD#-Mode	8BH	Y	-	-	-	D	-
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-
Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y

TABLE 7: NAND Controller Command Set (Continued) (2 of 2)

Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
Write-Verify	3CH	-	Y	Y	Y	Y	Y

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1.FR - Features register
2.SC - Sector Count register
3.SN - Sector Number register
4.CY - Cylinder registers
5.DH - Drive/Head register
6.LBA - Logical Block Address mode supported (see command descriptions for use)
7.Y - The register contains a valid parameter for this command.
8.For the Drive/Head register:Y means both the NAND Controller and Head parameters are used;
D means only the NAND Controller parameter is valid and not the Head parameter.

Identify-Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the NAND Controller. This command has the same protocol as the Read-Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 8. All reserved bits or words are zero. Table 8 gives the definition for each field in the Identify-Drive information.

Data Sheet

TABLE 8: Identify-Drive Information (1 of 2)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit
1	bbbbH[2]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[2]	2	Default number of heads
4	0000H	2	Reserved
5	0000H	2	Reserved
6	bbbbH[2]	2	Default number of sectors per track
7-8	bbbbH[3]	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	xxxxH	2	Vendor Unique
10-14	eeeeH[4]	10	User-programmable serial number in ASCII
15-19	ddddH[5]	10	Greenliant preset, unique ID in ASCII
20	0002H	2	Buffer type
21	xxxxH	2	Vendor Unique
22	xxxxH	2	Vendor Unique
23-26	aaaaH[6]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	ccccH[7]	40	User Definable Model number
47	8000	2	Maximum number of sectors on Read/Write-Multiple command
48	0000H	2	Reserved
49	0B00H	2	Capabilities
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	0007H	2	Translation parameters are valid
54	nnnnH	2	Current numbers of cylinders
55	nnnnH	2	Current numbers of heads
56	nnnnH	2	Current sectors per track
57-58	nnnnH	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010X	2	Multiple sector setting
60-61	nnnnH	4	Total number of sectors addressable in LBA mode
62	0000H	2	Reserved
63	0x07H	2	DMA data transfer is supported in NAND Controller
64	0003H	2	Advanced PIO Transfer mode supported
65	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
66	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
67	0078H	2	PIO Mode-4 supported
68	0078H	2	PIO Mode-4 supported
69-79	0000H	22	Reserved
80	007EH	2	ATA/ATAPI major version number
81	0019H	2	ATA/ATAPI minor version number
82	706BH	2	Features/command sets supported
83	4008H	2	Features/command sets supported
84	4000H	2	Features/command sets supported
85-87	xxxxH	6	Features/command sets enabled
88	xx3FH	2	UDMA modes

TABLE 8: Identify-Drive Information (Continued) (2 of 2)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
89	xxxxH	2	Time required for security erase unit completion
90	xxxxH	2	Time required for enhanced security erase unit completion
91-92	0000H	4	Reserved
93	bbbbH	2	Hardware reset result
94-127	0000H	66	Reserved
128	xxxxH	2	Security Status
129-159	0000H	62	Vendor unique bytes
160-162	0000H	6	Reserved
163	xx2H	2	CF Advanced True IDE Timing Mode capabilities and settings
164-254	0000H	182	Reserved
255	bbA5H	2	Integrity word [15-8 Checksum, 7-0 Signature (A5H)]

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1. XXXX = Don't care. This field is subject to change by the host or the device.
2. bbbb - default value set by controller. The selections could be user programmable.
3. n - calculated data based on product configuration
4. eeee - the default value is '0000000000'
5. dddd - unique number of each device
6. aaaa - any unique Greenliant firmware revision
7. cccc - default value is "xxxMB NAND" or "xxxGB NAND" where xxx is the flash drive capacity. The user has an option to change the model number during manufacturing.

Word 0: General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

Word 7-8: Number of Sectors

This field contains the number of sectors per NAND Controller. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

Word 10-19: Serial Number

The contents of this field are right justified and padded with spaces (20H). The right-most ten bytes are a Greenliant preset, unique ID. The left-most ten bytes are a user-programmable value with a default value of spaces.

Word 20: Buffer Type

This field defines the buffer capability:

0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the NAND Controller.

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Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

Word 27-46: Model Number

This field is reserved for the model number for this product.

Word 47: Read-/Write-Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands.

Word 49: Capabilities

Bit	Function
13	Standby Timer 0: forces sleep mode when host is inactive.
11	IORDY Support 1: NAND Controller supports PIO Mode-4.
9	LBA support 1: NAND Controller supports LBA mode addressing.
8	DMA Support 1: DMA mode is supported.

Word 51: PIO Data Transfer Cycle Timing Mode

This field defines the mode for PIO data transfer. NAND Controller supports up to PIO Mode-4.

Word 53: Translation Parameters Valid

Bit	Function
0	1: words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: words 64-70 are valid to support PIO Mode-3 and 4.
2	1: words 88 are valid to support Ultra DMA data transfer.

Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Word 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

Word 59: Multiple Sector Setting

This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for Read/Write Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that Read/Write Multiple commands are not valid.

Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the NAND Controller in LBA mode only.

Word 63: Multi-word DMA Transfer Mode

This field identifies the multi-word DMA transfer modes supported by the NAND Controller and indicates the mode that is currently selected. Only one DMA mode can be selected at any given time.

Bit	Function
15-11	Reserved
10	Multi-word DMA mode 2 selected 1: Multi-word DMA mode 2 is selected and bits 8 and 9 are cleared to 0 0: Multi-word DMA mode 2 is not selected.
9	Multi-word DMA mode 1 selected 1: Multi-word DMA mode 1 is selected and 8 and 10 should be cleared to 0. 0: Multi-word DMA mode 1 is not selected.
8	Multi-word DMA mode 0 selected 1: Multi-word DMA mode 0 is selected and bits 9 and 10 are cleared to 0. 0: Multi-word DMA mode 0 is not selected.
7-3	Reserved
2	Multi-word DMA mode 2 supported 1: Multi-word DMA mode 2 and below are supported and Bits 0 and 1 are set to 1.
1	Multi-word DMA mode 1 supported 1: Multi-word DMA mode 1 and below are supported.
0	Multi-word DMA mode 0 supported 1: Multi-word DMA mode 0 is supported.

Word 64: Advanced PIO Data Transfer Mode

Bits (7:0) is defined as the PIO data and register transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bits (7:2) are Reserved for future PIO modes.

Bit	Function
0	1: NAND Controller supports PIO Mode-3.
1	1: NAND Controller supports PIO Mode-4.

Word 65: Minimum Multi-word DMA Transfer Cycle Time Per Word

This field defines the minimum Multi-word DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the NAND Controller supports when performing Multi-word DMA transfers on a per word basis. Greenliant's NAND Controller supports up to Multi-word DMA Mode-2, so this field is set to 120ns.

Word 66: Device Recommended Multi-word DMA Cycle Time

This field defines the NAND Controller recommended Multi-word DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the NAND Controller may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. NAND Controller supports up to Multi-word DMA Mode-2, so this field is set to 120 ns.

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Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one.The NAND Controller's minimum cycle time is 120 ns. A value of 0078H is reported.

Word 68: Minimum PIO Transfer Cycle Time With IORDY

This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. The NAND Controller's minimum cycle time is 120 ns, e.g., PIO Mode-4. A value of 0078H is reported.

Word 80: Major Version Number

If not 0000H or FFFFH, the device claims compliance with the major version(s) as indicated by bits (6:1) being set to one. Since ATA standards maintain downward compatibility, a device may set more than one bit. GLS55VD031 supports ATA-1 to ATA-6.

Word 81: Minor Version Number

If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 should be 0000H or FFFFH.

A value of 0019H reported in word 81 indicates ATA/ATAPI-6 T13 1410D revision 3a guided the implementation.

Words 82-84: Features/command sets supported

Words 82, 83, and 84 indicate the features and command sets supported. A value of 706BH is reported.

Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	0: Host Protected Area feature set is not supported
9	0: Device Reset command is not supported
8	0: Service interrupt is not supported
7	0: Release interrupt is not supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	1: Security Mode feature set is supported
0	1: SMART feature set is supported

Word 83

The values in this word should not be depended on by host implementers.

Bit	Function

15	0: Provides indication that the features/command sets supported words are not valid
14	1: Provides indication that the features/command sets supported words are valid
13-11	0: Reserved
9	0: Reserved
8	0: Set-Max security extension is not supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	1: Advanced Power Management feature set is supported
2	0: CFA feature set is not supported
1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	0: Download Microcode command is not supported

Word 84

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

Words 85-87: Features/command sets enabled

Words 85, 86, and 87 indicate features/command sets enabled.
The host can enable/disable the features or command set only if they are supported in Words 82-84.

Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled 1: NOP command is enabled
13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled
12	0:Write Buffer command is not enabled 1: Write Buffer command is enabled
11	0: Obsolete
10	1: Host Protected Area feature set is enabled
9	0: Device Reset command is not enabled
8	0: Service interrupt is not enabled
7	0: Release interrupt is not enabled
6	0: Look-ahead is not enabled 1: Look-ahead is enabled
5	0: Write cache is not enabled 1: Write cache is enabled
4	0: Packet Command feature set is not enabled
3	0: Power Management feature set is not enabled 1: Power Management feature set is enabled
2	0: Removable Media feature set is not enabled

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1	0: Security Mode feature set has not been enabled via the Security Set Password command 1: Security Mode feature set has been enabled via the Security Set Password command
0	0: SMART feature set is not enabled

Word 86

Bit	**Function**
15-9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not enabled
3	0: Advanced Power Management feature set is not enabled
2	0: CFA feature set is disabled
1	0: Read DMA Queued and Write DMA Queued commands are not enabled
0	0: Download Microcode command is not enabled

Word 87

The values in this word should not be depended on by host implementers.

Bit	**Function**
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

Word 88

Bit	**Function**
15-14	Reserved
13	1: Ultra DMA mode 5 selected 0: Ultra DMA mode 5 not selected
12	1: Ultra DMA mode 4 selected 0: Ultra DMA mode 4 not selected
11	1: Ultra DMA mode 3 selected 0: Ultra DMA mode 3 not selected
10	1: Ultra DMA mode 2 selected 0: Ultra DMA mode 2 not selected
9	1: Ultra DMA mode 1 selected 0: Ultra DMA mode 1 not selected
8	1: Ultra DMA mode 0 selected 0: Ultra DMA mode 0 not selected
7-6	Reserved
5	1: Ultra DMA mode 5 and below supported
4	1: Ultra DMA mode 4 and below supported
3	1: Ultra DMA mode 3 and below supported
2	1: Ultra DMA mode 2 and below supported
1	1: Ultra DMA mode 1 and below supported
0	1: Ultra DMA mode 0 supported

Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 93: Hardware reset result

Bit **Function**

The contents of bits (12:0) of this word will change only during the execution of the hardware reset.

15 Shall be cleared to zero

14 Shall be set to one

13 1: Device detected CBLID - above VIH

0: Device detected CBLIP - below VIL

12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:

12 Reserved.

11 0: Device 1 did not assert PDIAG-.

1: Device 1 asserted PDIAG-.

10-9 These bits indicate how Device 1 determined the device number:

00: Reserved.

01: A jumper was used.

10: The CSEL signal was used.

11: Some other method was used or the method is unknown.

8 Shall be set to one.

7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:

7 Reserved.

6 0: Device 0 does not respond when Device 1 is selected.

1: Device 0 responds when Device 1 is selected.

5 0: Device 0 did not detect the assertion of DASP-.

1: Device 0 detected the assertion of DASP-.

4 0: Device 0 did not detect the assertion of PDIAG-.

1: Device 0 detected the assertion of PDIAG-.

3	0: Device 0 failed diagnostics. 1: Device 0 passed diagnostics.
2-1	These bits indicate how Device 0 determined the device number: 00: Reserved. 01: A jumper was used. 10: The CSEL signal was used. 11: Some other method was used or the method is unknown.
0	Shall be set to one.

Word 128: Security Status

Bit	Function
8	Security Level 1: Security mode is enabled and the security level is maximum 0: and security mode is enabled, indicates that the security level is high
5	Enhanced security erase unit feature supported 1: Enhanced security erase unit feature set is supported
4	Expire 1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a Power-on reset or hard reset
3	Freeze 1: Security is frozen
2	Lock 1: Security is locked
1	Enable/Disable 1: Security is enabled 0: Security is disabled
0	Capability 1: NAND Controller supports security mode feature set 0: NAND Controller does not support security mode feature set

Word 163: CF Advanced True IDE Timing Mode Capabilities and Settings

This word describes the capabilities and current settings for CF modes utilizing the True IDE interface.

Four separate fields determine support and selection options in the Advanced PIO and Advanced Multiword DMA timing modes. For information on the older modes, see “Word 63: Multi-word DMA Transfer Mode” on page 23. and “Word 64: Advanced PIO Data Transfer Mode” on page 23.. When the Identity drive command executes, the device returns 0492H.

Bit	Function
2-0	Advanced True IDE PIO Mode Support Indicates the maximum True IDE PIO mode supported by the card

Value	Time
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

5-3 Advanced True IDE Multiword DMA Mode Support
Indicates the maximum True IDE Multiword DMA mode supported by the card

Value	Time
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

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8-6 Advanced True IDE PIO Mode Selected
Indicates the current True IDE PIO mode selected on the card

Value	Time
0	Specified in word 64
1	PIO Mode 5
2	PIO Mode 6
3-7	Reserved

11-9 Advanced True IDE Multiword DMA Mode Selected
Indicates the current True IDE Multiword DMA mode selected on the card

Value	Time
0	Specified in word 63
1	Multiword DMA Mode 3
2	Multiword DMA Mode 4
3-7	Reserved

15-12 Reserved

Set-Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 9 defines all features that are supported.

Word 255: Integrity Word

The use of this word is optional. If bits (7:0) of this word contain the signature A5h, bits (15:8) contain the data structure checksum. The data structure checksum is the two's complement of the sum of all bytes in words(254:0) and the byte consisting of bits (7:0) in word 255. Each byte shall be added with unsigned arithmetic, and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct.

TABLE 9: Features Supported

Feature	Operation
01H	Enable 8-bit data transfers.
02H	Enable Write cache
03H	Set transfer mode based on value in Sector Count register. Table 10 defines the values.
09H	Enable Extended Power Operations
55H	Disable Read Look Ahead.
66H	Disable Power-on Reset (POR) establishment of defaults at software reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
82H	Disable Write Cache
89H	Disable Extended Power operations
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
AAH	Enable Read-Look-Ahead
CCH	Enable Power-on Reset (POR) establishment of defaults at software reset.

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Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D_7-D_0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 02H and 82H allow the host to enable or disable write cache in the NAND Controllers that implement write cache. When the subcommand Disable-Write-Cache is issued, the NAND Controller should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

Feature 55H is the default feature for the NAND Controller. Therefore, the host does not have to issue Set-Features command with this feature unless it is necessary for compatibility reasons.

Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

TABLE 10: Transfer Mode Values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Multi-word DMA mode	00100b	mode[1]
Ultra-DMA mode	01000b	mode[1]
Reserved	Other	N/A

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1. Mode = transfer mode number, all other values are not valid

Data Sheet

Idle - 97H or E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the NAND Controller to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic Power-down mode is enabled. If the sector count is zero, the automatic Power-down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

Set-Sleep-Mode - 99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99H or E6H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the NAND Controller to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

Set-WP#/PD#-Mode - 8BH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	8BH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	6EH							
Cyl Low (4)	44H							
Sec Num (3)	72H							
Sec Cnt (2)	50H							
Feature (1)	55H or AAH							

This command configures the WP#/PD# pin for either the Write Protect mode or the Power-down mode. When the host sends this command to the device with the value AAH in the feature register, the WP#/PD# pin is configured for the Write Protect mode described in Section . The Write Protect mode is the factory default setting. When the host sends this command to the device with the value 55H in the feature register, WP#/PD# is configured for the Power-down mode.

All values in the C/D/H register, the Cylinder Low register, the Cylinder High register, the Sector Number register, the Sector Count register, and the Feature register need to match the values shown above, otherwise, the command will be treated as an invalid command.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

Data Sheet

Error Posting

The following table summarizes the valid status and error values for the NAND Controller command set.

TABLE 11: Error and Status Register[1]

Command	Error Register					Status Register				
	ICRC/ BBK	UNC	IDNF	ABRT	AMNF	RDY	DWF	DSC	CORR	ERR
Check-Power-Mode				V		V	V	V		V
Execute-Drive-Diagnostic[2]						V		V		V
Flush-Cache				V		V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
Initialize-Drive-Parameters						V		V		V
NOP				V		V	V			V
Read-Buffer				V		V	V	V		V
Read-DMA	V	V	V	V	V	V	V	V	V	V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Security-Disable-Password				V		V	V	V		V
Security-Erase-Prepare				V		V	V	V		V
Security-Erase-Unit				V		V	V	V		V
Security-Freeze-Lock				V		V	V	V		V
Security-Set-Password				V		V	V	V		V
Security-Unlock				V		V	V	V		V
Seek			V	V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Multiple-Mode				V		V	V	V		V
Set-Sleep-Mode				V		V	V	V		V
Set-WP#/PD#-Mode				V		V		V		V
SMART				V		V		V		V
Standby				V		V	V	V		V
Standby-Immediate				V		V	V	V		V
Write-Buffer				V		V	V	V		V
Write-DMA	V		V	V	V	V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Verify	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

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1. The host is required to reissue any media access command (such as Read-Sector and Write Sector) that ends with an error condition.
2. See Table 8
   V = valid on this command.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D.C. Voltage on Pins[1] I3, O4, O5, O6, and O7 to Ground Potential . . . . . -0.5V to V_{DDN}+0.5V
Transient Voltage (<20 ns) on Pins[1] I3, O4, O5, O6, and O7 to Ground Potential . . . . . -2.0V to V_{DDN}+2.0V
D.C. Voltage on Pins[1] I1, I2, O1, O2, and O3 to Ground Potential . . . . . -0.5V to V_{DDQ}+0.5V
Transient Voltage (<20 ns) on Pins[1] I1, I2, O1, O2, and O3 to Ground Potential . . . . . -2.0V to V_{DDQ}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Through Hole Lead Soldering Temperature (10 Seconds) . . . . . 300°C
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. Please refer to Table 1 for pin assignment information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

TABLE 12: Absolute Maximum Power Pin Stress Ratings

Parameter	Symbol	Conditions
Input Power	$V_{DDQ}/V_{DDN}/V_{DD}$	-0.3V min to 4.0V max
Voltage on any flash media interface pin with respect to V_{SS}		-0.5V min to V_{DD} + 0.5V max
Voltage on all other pins with respect to V_{SS}		-0.5V min to V_{DDQ} + 0.5V max

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Operating Range

Range	Ambient Temperature	V_{DD}/V_{DDN}=3V	V_{DDQ}=3V
Commercial	0°C to +70°C	2.7-3.6V	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V	2.7-3.6V

AC Conditions of Test

Input Rise/Fall Time . . . . . 5 ns
Output Load (FRE#, FWE#) . . . . . C_L = 100 pF
Output Load (all others) . . . . . C_L = 80 pF
See Figure 5

Note: All AC specifications are guaranteed by design.

TABLE 13: Recommended System Power-on Timing

Symbol	Parameter		Typical	Maximum	Units
$T_{PU-INITIAL}$	Drive Initialization to Ready		3 sec + (0.5 sec/ GByte)	100	sec
$T_{PU-READY1}$[1]	GLS55VD031:	Host Power-on/Reset to Ready Operation	200	1000	ms
$T_{PU-WRITE1}$[1]	GLS55VD031:	Host Power-on/Reset to Write Operation	200	1000	ms

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Data Sheet

TABLE 14: Capacitance (Ta = 25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	9 pF

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 15: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

DC Characteristics

TABLE 16: DC Characteristics for Media Interface

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH3}	I3	Input Voltage	2.0		V	V_{DDN}=V_{DDN} Max
V_{IL3}				0.8	V	V_{DDN}=V_{DDN} Min
I_{IL3}	I3Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDN}, V_{DDN} = V_{DDN} Max
I_{U3}	I3U	Input Pull-Up Current	-175	-15	uA	V_{IN} = GND, V_{DDN} = V_{DDN} Max
V_{OH4}	O4	Output Voltage	2.2		V	I_{OH4}=I_{OH4} Min
V_{OL4}				0.4	V	I_{OL4}=I_{OL4} Max
I_{OH4}		Output Current	-2		mA	V_{DDN}=V_{DDN} Min
I_{OL4}				2	mA	V_{DDN}=V_{DDN} Min
V_{OH5}	O5	Output Voltage	2.2		V	I_{OH5}=I_{OH5} Min
V_{OL5}				0.4	V	I_{OL5}=I_{OL5} Max
I_{OH5}		Output Current	-4		mA	V_{DDN}=V_{DDN} Min
I_{OL5}				4	mA	V_{DDN}=V_{DDN} Min
V_{OH7}	O6	Output Voltage	2.2		V	I_{OH7}=I_{OH7} Min
V_{OL7}				0.4	V	I_{OL7}=I_{OL7} Max
I_{OH7}		Output Current	-3.5		mA	V_{DDN}=V_{DDN} Min
I_{OL7}				3.5	mA	V_{DDN}=V_{DDN} Min
V_{OH8}	O7	Output Voltage	2.2		V	I_{OH8}=I_{OH8} Min
V_{OL8}				0.4	V	I_{OL8}=I_{OL8} Max
I_{OH8}		Output Current	-6		mA	V_{DDN}=V_{DDN} Min
I_{OL8}				6	mA	V_{DDN}=V_{DDN} Min

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TABLE 17: DC Characteristics for Host Interface V_{DDQ} = 3V

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH1} V_{IL1}	I1	Input Voltage	2.0 	 0.8	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL1}	I1Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U1}	I1U	Input Pull-Up Current	-175	-15	uA	V_{IN} = GND, V_{DDQ} = V_{DDQ} Max
V_{T+2} V_{T-2}	I2	Input Voltage Schmitt Trigger	 0.8	2.0 	V	V_{DDQ}=V_{DDQ} Max V_{DDQ}=V_{DDQ} Min
I_{IL2}	I2Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U2}	I2U	Input Pull-Up Current	-175	-15	uA	V_{IN} = GND, V_{DDQ} = V_{DDQ} Max
V_{OH1} V_{OL1}	O1	Output Voltage	2.2 	 0.4	V	I_{OH1}=I_{OH1} Min I_{OL1}=I_{OL1} Max
I_{OH1}		Output Current	-4		mA	V_{DDQ}=V_{DDQ} Min
I_{OL1}		Output Current		4	mA	V_{DDQ}=V_{DDQ} Min
V_{OH2} V_{OL2}	O2	Output Voltage	2.2 	 0.4	V	I_{OH2}=I_{OH2} Min I_{OL2}=I_{OL2} Max
I_{OH2}		Output Current	-6		mA	V_{DDQ}=V_{DDQ} Min
I_{OL2}		Output Current		6	mA	V_{DDQ}=1V_{DDQ} Min
V_{OH3} V_{OL3}	O3	Output Voltage for DASP# pin	2.2 	 0.4	V	I_{OH6}=I_{OH6} Min I_{OL6}=I_{OL6} Max
I_{OH3}		Output Current for DASP# pin	-4		mA	V_{DDQ}=V_{DDQ} Min
I_{OL3}		Output Current for DASP# pin		12	mA	V_{DDQ}=V_{DDQ} Min

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TABLE 18: Power Consumption

Symbol	Type	Parameter	Min	Max	Units	Conditions
I_{DD}[1,2]	PWR	Power supply current		55	mA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max
I_{SP}	PWR	Sleep/Standby/Idle current		200	µA	V_{DD}=V_{DD} Max; V_{DDQ}=V_{DDQ} Max

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1. Sequential data transfer for 1 sector read data from host interface and write data to media.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Data Sheet

AC Characteristics

AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 5: AC Input/Output Reference Waveforms

Media Side Interface Timing Specifications

TABLE 19: GLS55VD031 Timing Specifications

Symbol	Parameter	Min	Max	Units
T_{CLS}	FCLE Setup Time	15	-	ns
T_{CLH}	FCLE Hold Time	15	-	ns
T_{CS}	FCE# Setup Time	30	-	ns
T_{CH}	FCE# Hold Time for Command/Data Write Cycle	15	-	ns
T_{CHR}	FCE# Hold Time for Sequential Read Last Cycle	-	40	ns
T_{WP}	FWE# Pulse Width	15	-	ns
T_{WH}	FWE# High Hold Time	10	-	ns
T_{WC}	Write Cycle Time	30	-	ns
T_{ALS}	FALE Setup Time	15	-	ns
T_{ALH}	FALE Hold Time	15	-	ns
T_{DS}	FAD[15:0] Setup Time	15	-	ns
T_{DH}	FAD[15:0] Hold Time	10	-	ns
T_{RP}	FRE# Pulse Width	15	-	ns
T_{RR}	Ready to FRE# Low	20	-	ns
T_{REA}	FRE# Data Setup Time	-	20	ns
T_{RC}	Read Cycle Time	30	-	ns
T_{REH}	FRE# High Hold Time	10	-	ns
T_{RHZ}	FRE# High to Data Hi-Z	-	100	ns

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Note: All AC specifications are guaranteed by design.

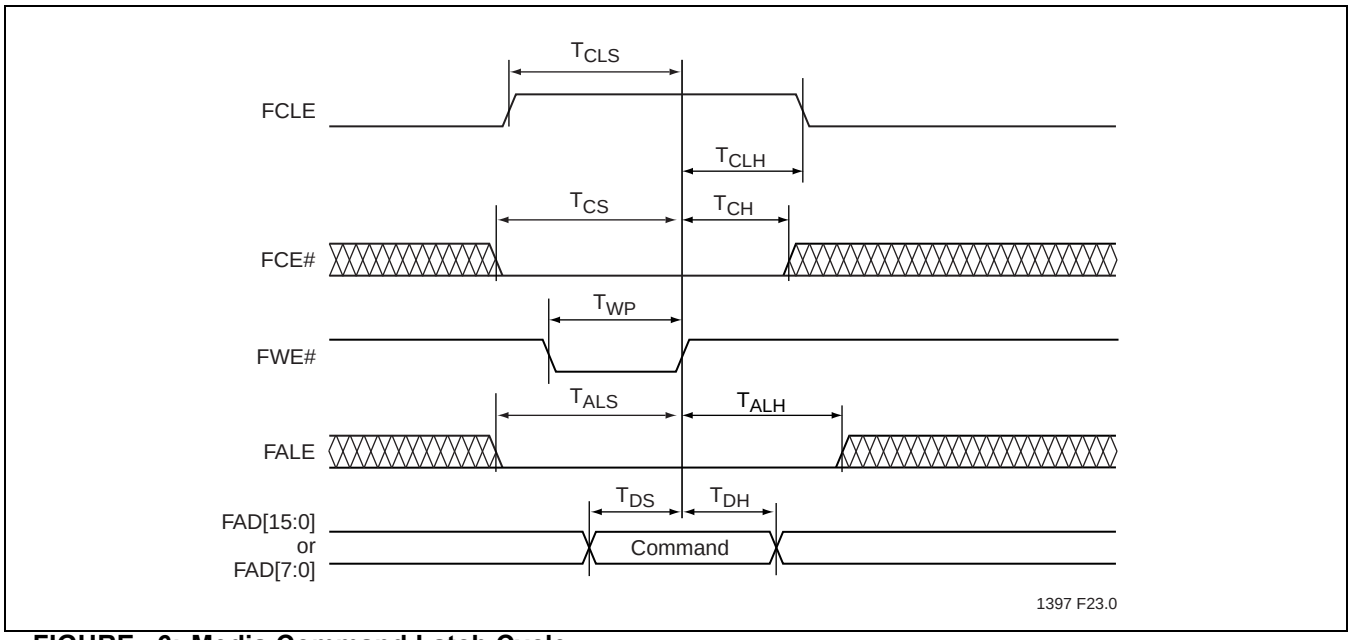


FIGURE 6: Media Command Latch Cycle

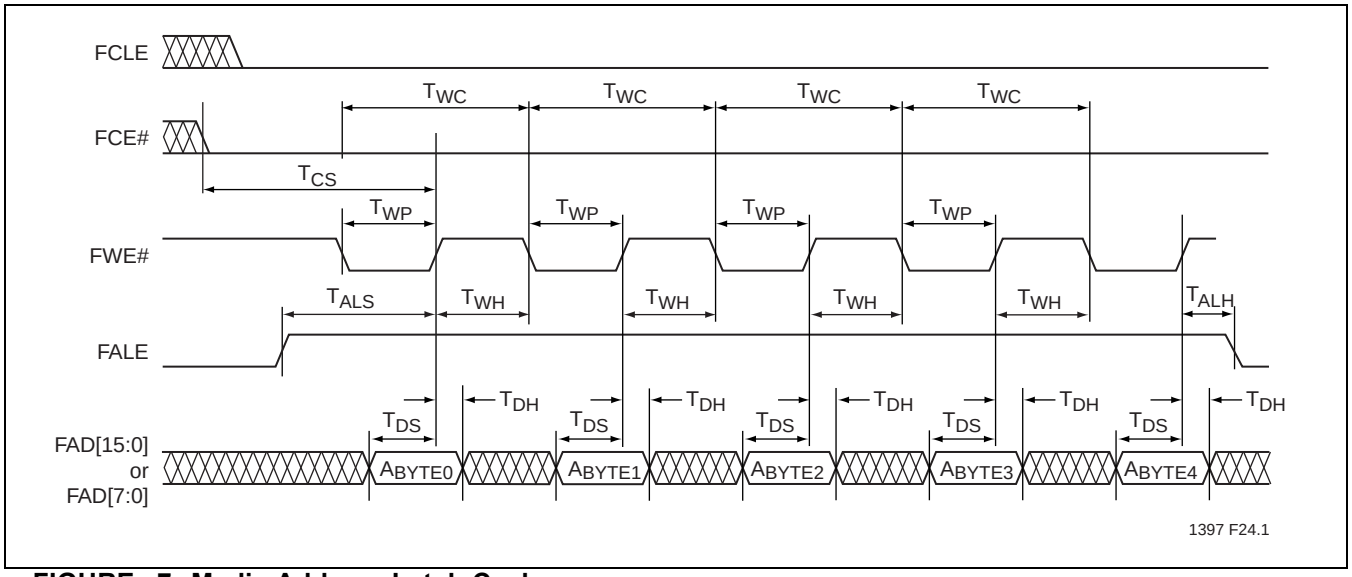


FIGURE 7: Media Address Latch Cycle

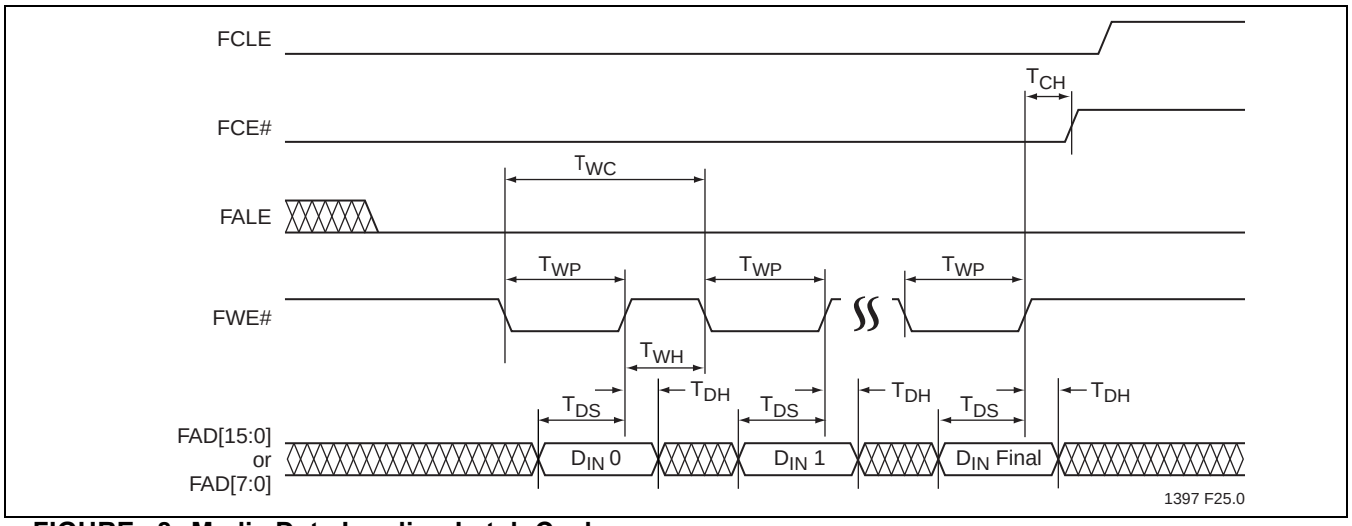


FIGURE 8: Media Data Loading Latch Cycle

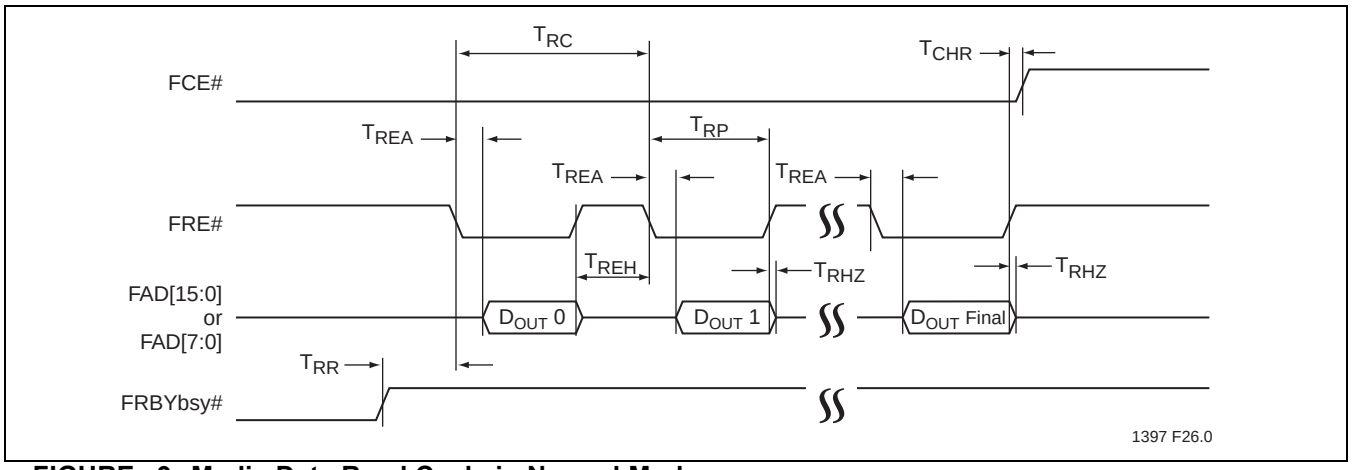


FIGURE 9: Media Data Read Cycle in Normal Mode

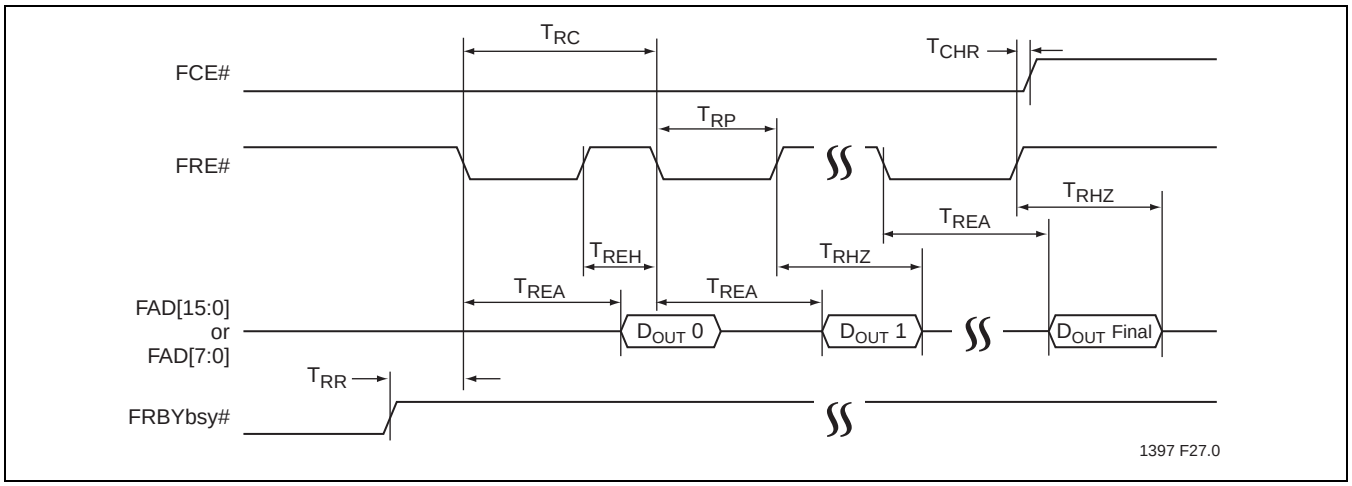
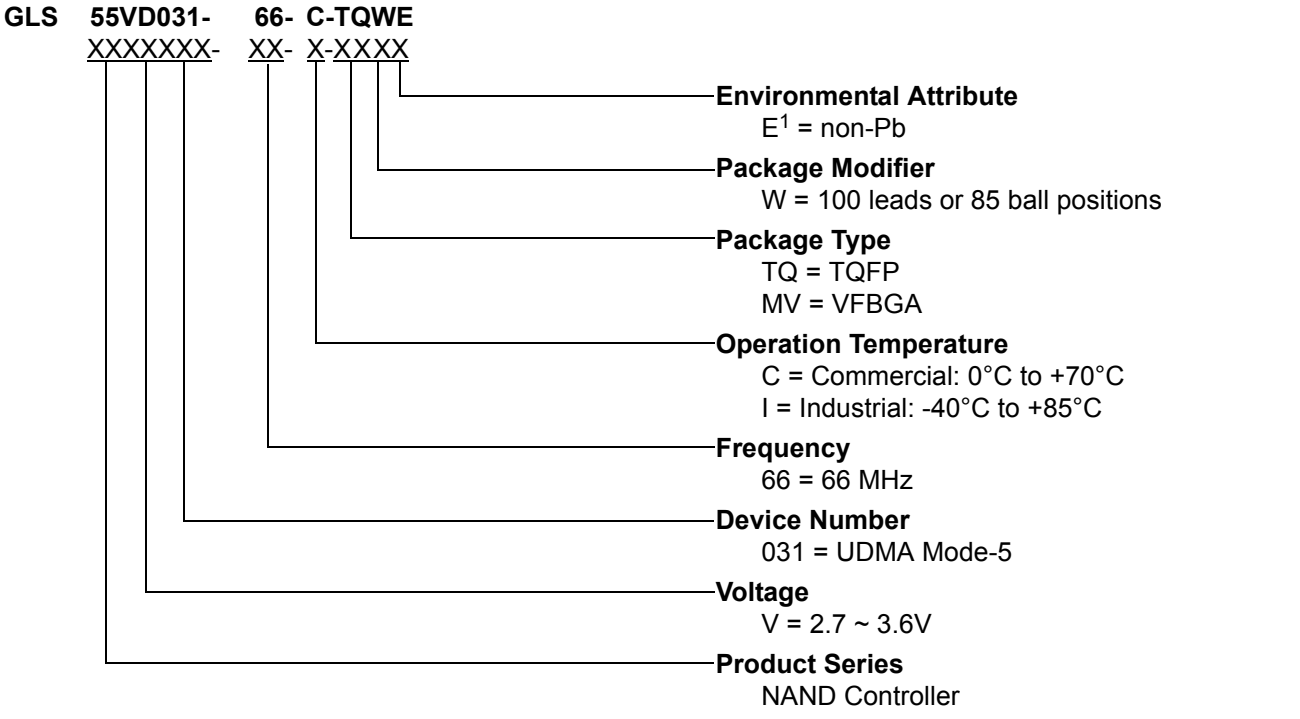


FIGURE 10: Media Data Read Cycle in EDO Mode

Data Sheet

PRODUCT ORDERING INFORMATION



1 Environmental suffix "E" denotes non-Pb solder. Greenliant non-Pb solder devices are "RoHS Compliant".

Valid Combinations

Valid combinations for GLS55VD031

GLS55VD031-66-C-TQWE

GLS55VD031-66-I-TQWE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Greenliant sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGING DIAGRAM

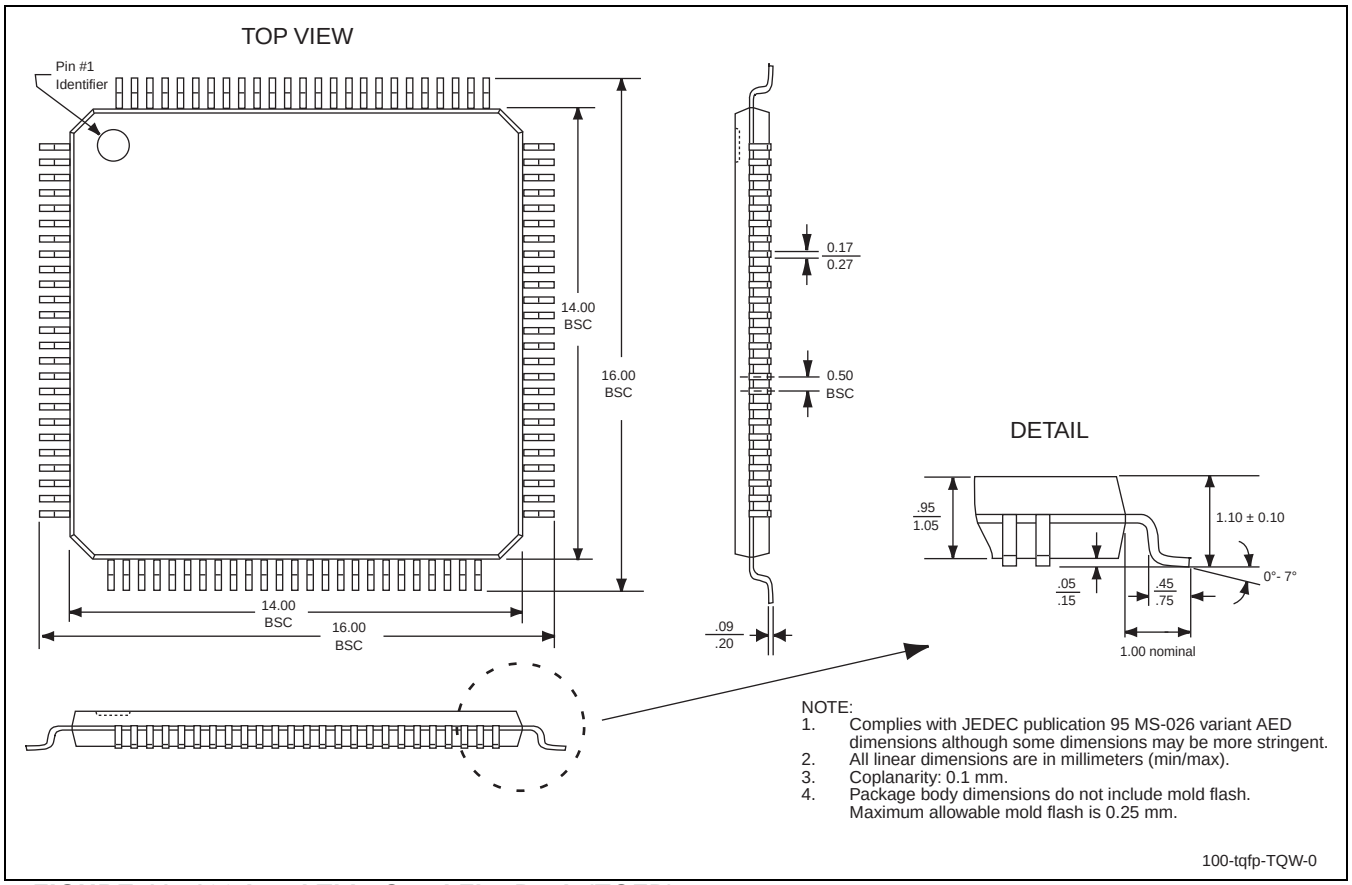
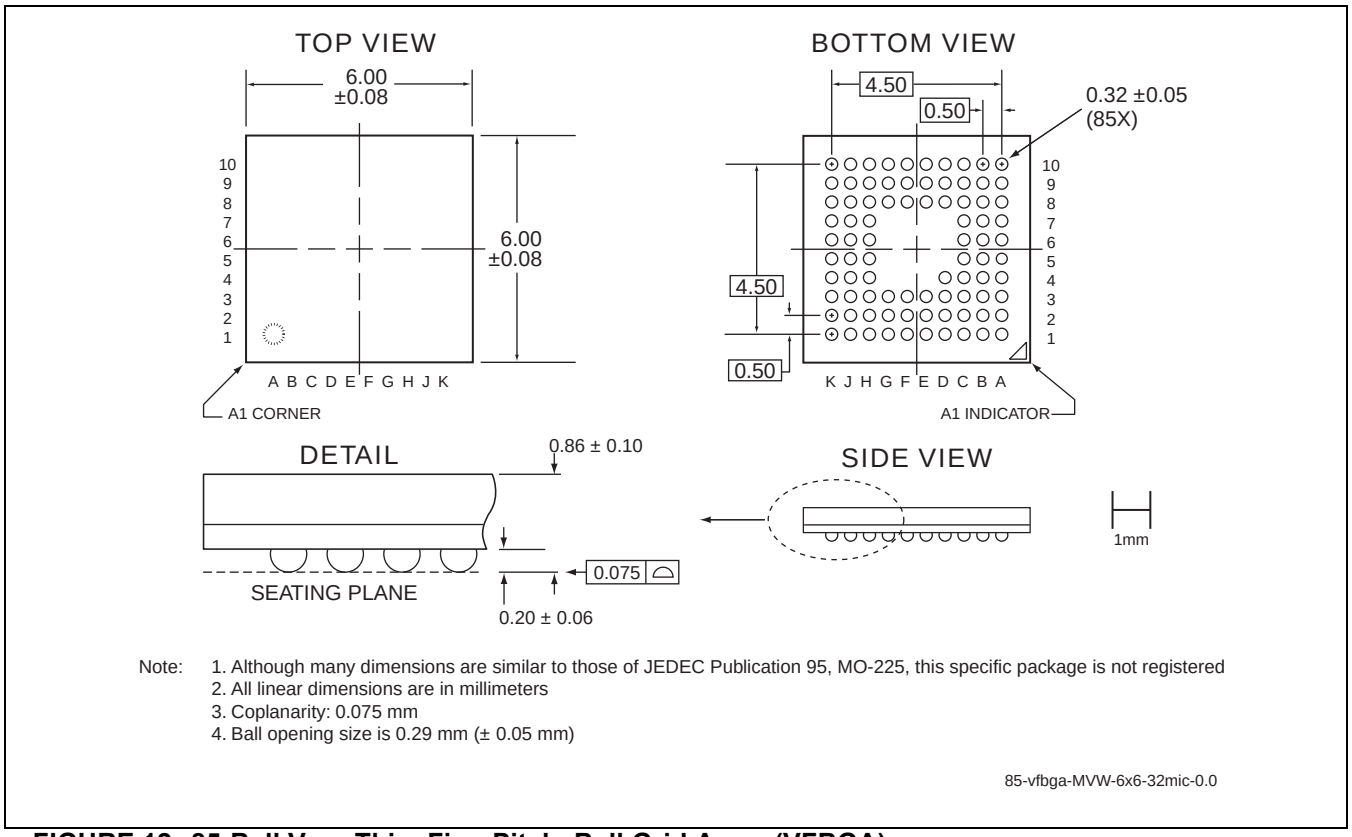


FIGURE 11: 100-Lead Thin Quad Flat Pack (TQFP)
Greenliant Package Code: TQW



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-225, this specific package is not registered
2. All linear dimensions are in millimeters
3. Coplanarity: 0.075 mm
4. Ball opening size is 0.29 mm (± 0.05 mm)

85-vfbga-MVW-6x6-32mic-0.0

FIGURE 12: 85-Ball Very-Thin, Fine-Pitch, Ball Grid Array (VFBGA)
Greenliant Package Code: MVW

Revision History

Number	Description	Date
00	• Initial Release Data Sheet	Dec 2008
01	• Globally changed product name from ATA Flash Disk to NAND Controller • Globally changed product number from SST55LD031 to SST55VD031 • Removed 1.8V reference globally • Changed 3.3V to 3V globally • Changed sustained Write performance from 40 MByte/sec to 30 MByte/sec globally • Edited pin assignments Figure 2, Figure 3, and Table 1 on page 7 • Edited Default ATA Flash Drive Settings Table 2 on page 11 • Removed External Clock Interface section • Edited Electrical Specification and Operating Range on page 34 • Edited Table 16 on page 36 • Edited Table 17 on page 37 • Edited Table 19 on page 38 • Edited Figure 9 on page 38 • Added Figure 10 on page 38 • Included“Word 255: Integrity Word” on page 30.	Jun 2009
02	• Changed status from Preliminary Specification to Data Sheet.	Jul 2009
03	• Revised IDD and ISP by updating Tables 17 and 18	Aug 2009
04	• Transferred from SST to Greenliant. Removed GLS55VD031-66-C-MVWE due to EOL.	May 2010

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