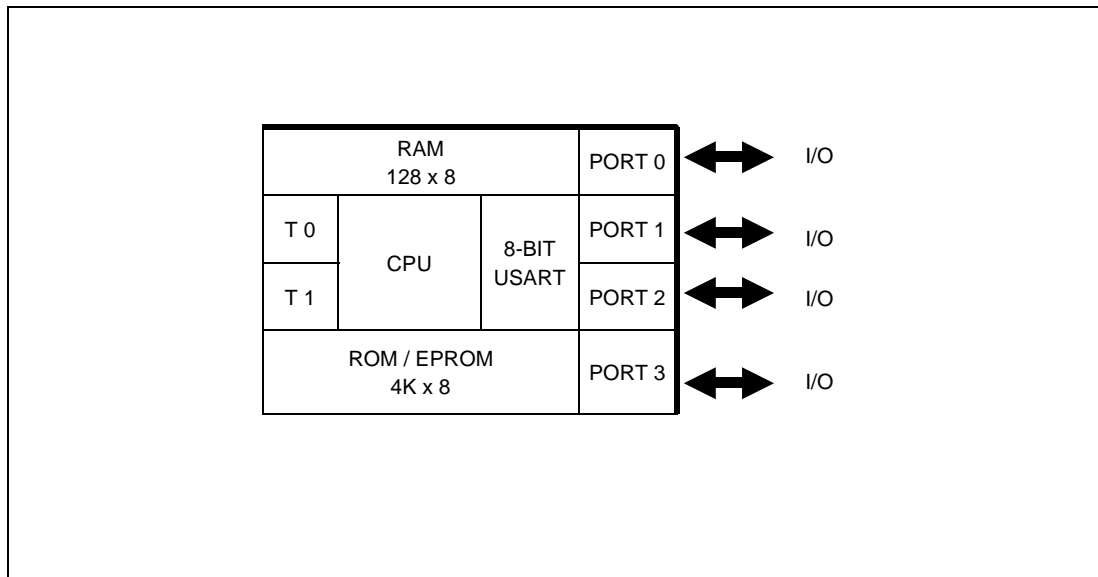


GMS90C31/51/31B/51B, GMS97C51 GMS90L31/51/31B/51B, GMS97L51 (Low voltage versions)

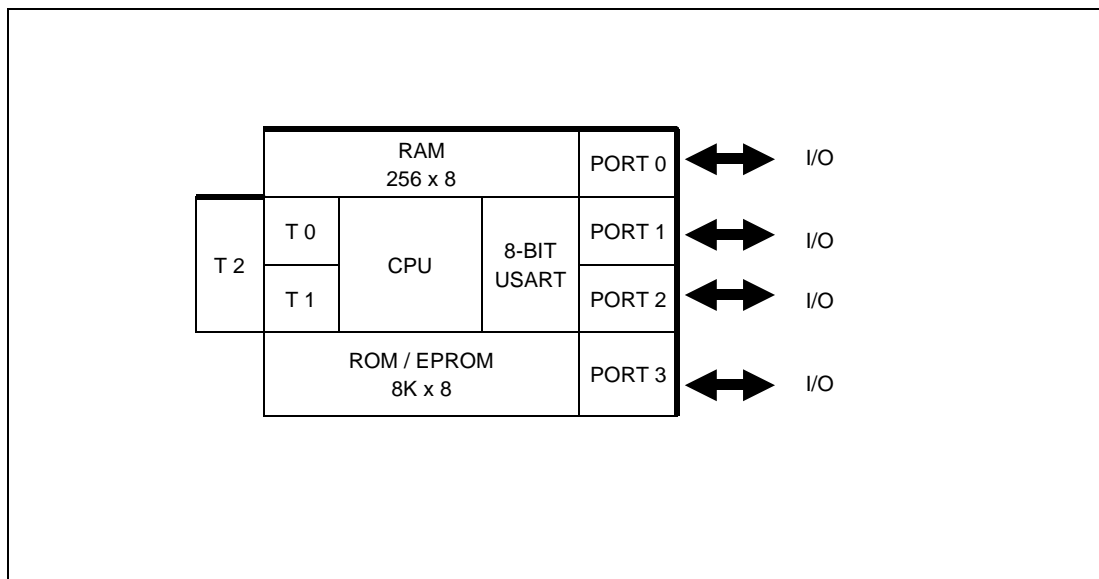
- Fully compatible to standard MCS-51 microcontroller
- Versions for 12/24/40 MHz operating frequency (90C31/51)
Versions for 12/24/33 MHz operating frequency (90C31B/51B, 97C51)
Low voltage versions are available 12MHz only
- 4K x 8 (EP)ROM
- 128 x 8 RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Two 16-bit Timers / Counters
- USART
- Five interrupt sources, two priority levels
- Power saving Idle and power down mode
- Quick pulse programming algorithm (in the OTP devices)
- 2-level program memory lock (in the OTP devices)
- 2.7Volt low voltage version available
- P-DIP-40, P-LCC-44, P-MQFP-44 package



Block Diagram

GMS90C32/52/32B/52B, GMS97C52
GMS90L32/52/32B/52B, GMS97L52 (Low voltage versions)

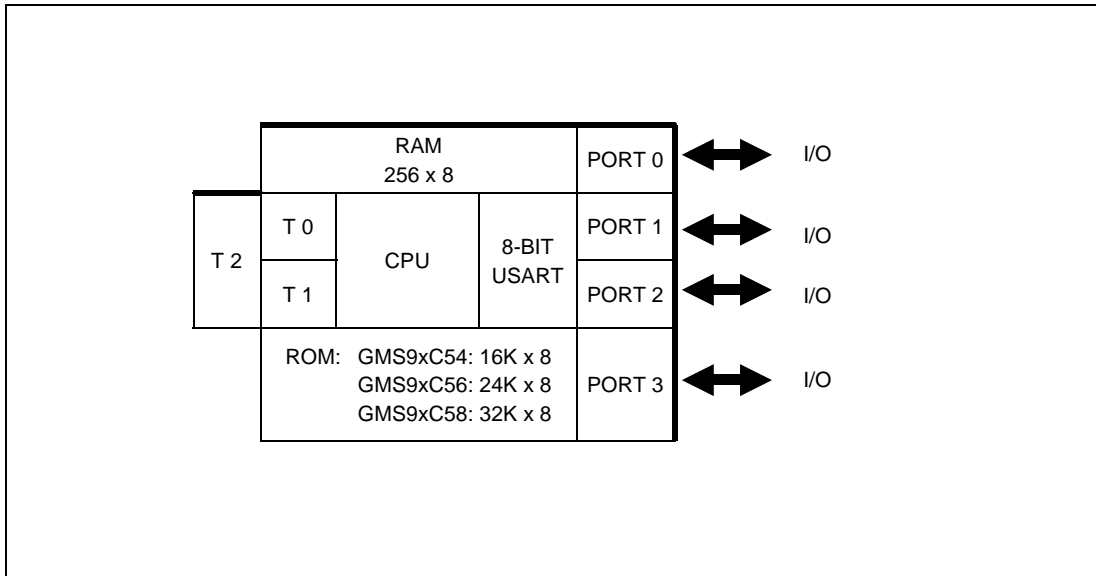
- Fully compatible to standard MCS-51 microcontroller
- Versions for 12/24/40 MHz operating frequency (90C32/52)
 Versions for 12/24/33 MHz operating frequency (90C32B/52B, 97C52)
 Low voltage versions are available 12MHz only
- 8K x 8 (EP)ROM
- 256 x 8 RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer2 with up/down counter feature)
- USART
- Six interrupt sources, two priority levels
- Power saving Idle and power down mode
- Quick pulse programming algorithm (in the OTP devices)
- 2-level program memory lock (in the OTP devices)
- 2.7Volt low voltage version available
- P-DIP-40, P-LCC-44, P-MQFP-44 package



Block Diagram

**GMS90C54/56/58, GMS97C54/56/58
GMS90L54/56/58, GMS97L54/56/58 (Low voltage versions)**

- Fully compatible to standard MCS-51 microcontroller
- Versions for 12/24/33 MHz operating frequency
Low voltage versions are available 12MHz only
- 16K/24K/32K bytes (EP)ROM
- 256 x 8 RAM
- 64K external program memory space
- 64K external data memory space
- Four 8-bit ports
- Three 16-bit Timers / Counters (Timer2 with up/down counter feature)
- USART
- One clock output port
- Programmable ALE pin enable / disable
- Six interrupt sources, two priority levels
- Power saving Idle and power down mode
- Quick pulse programming algorithm (in the OTP devices)
- 2-level program memory lock (in the OTP devices)
- 2.7Volt low voltage version available (with 12MHz operating frequency)
- P-DIP-40, P-LCC-44, P-MQFP-44 package



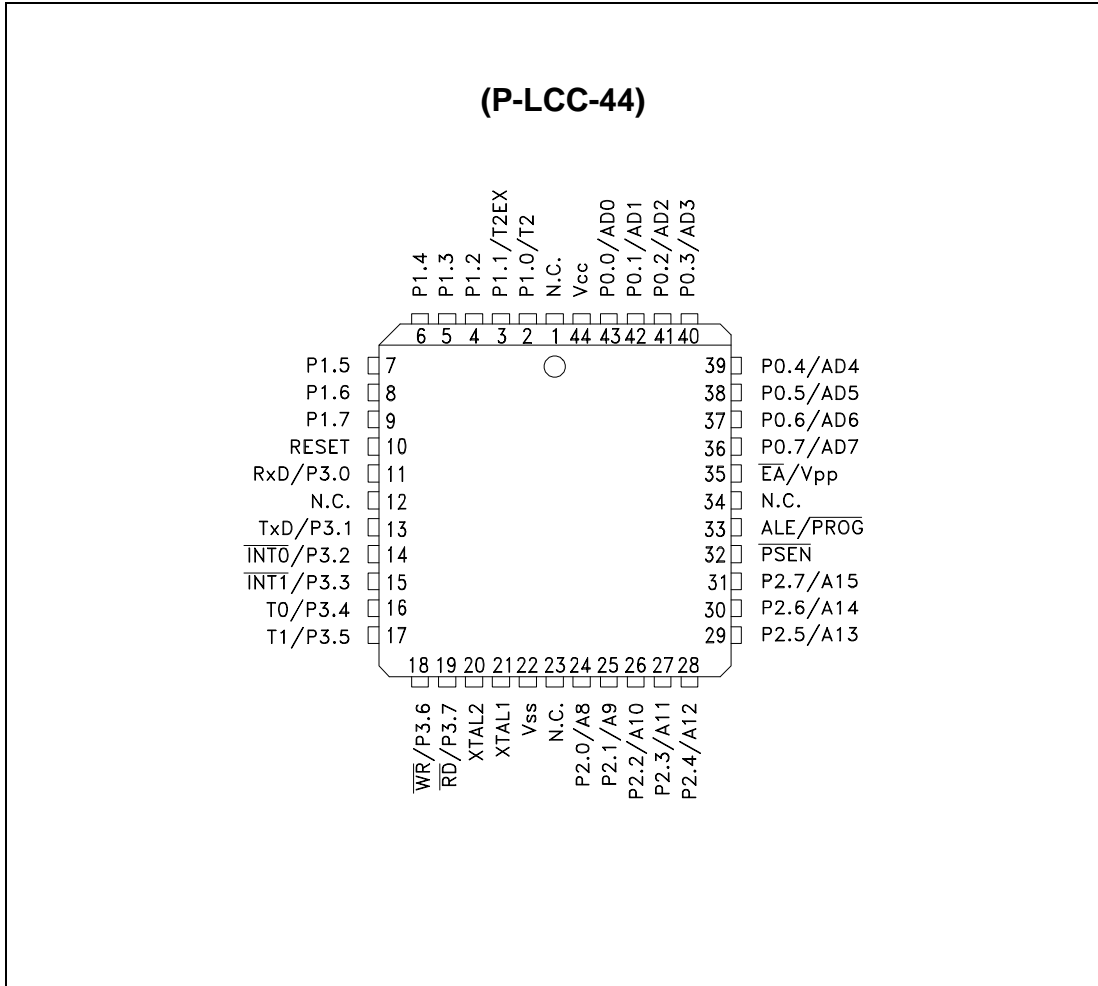
Block Diagram

GMS90 series Selection Guide

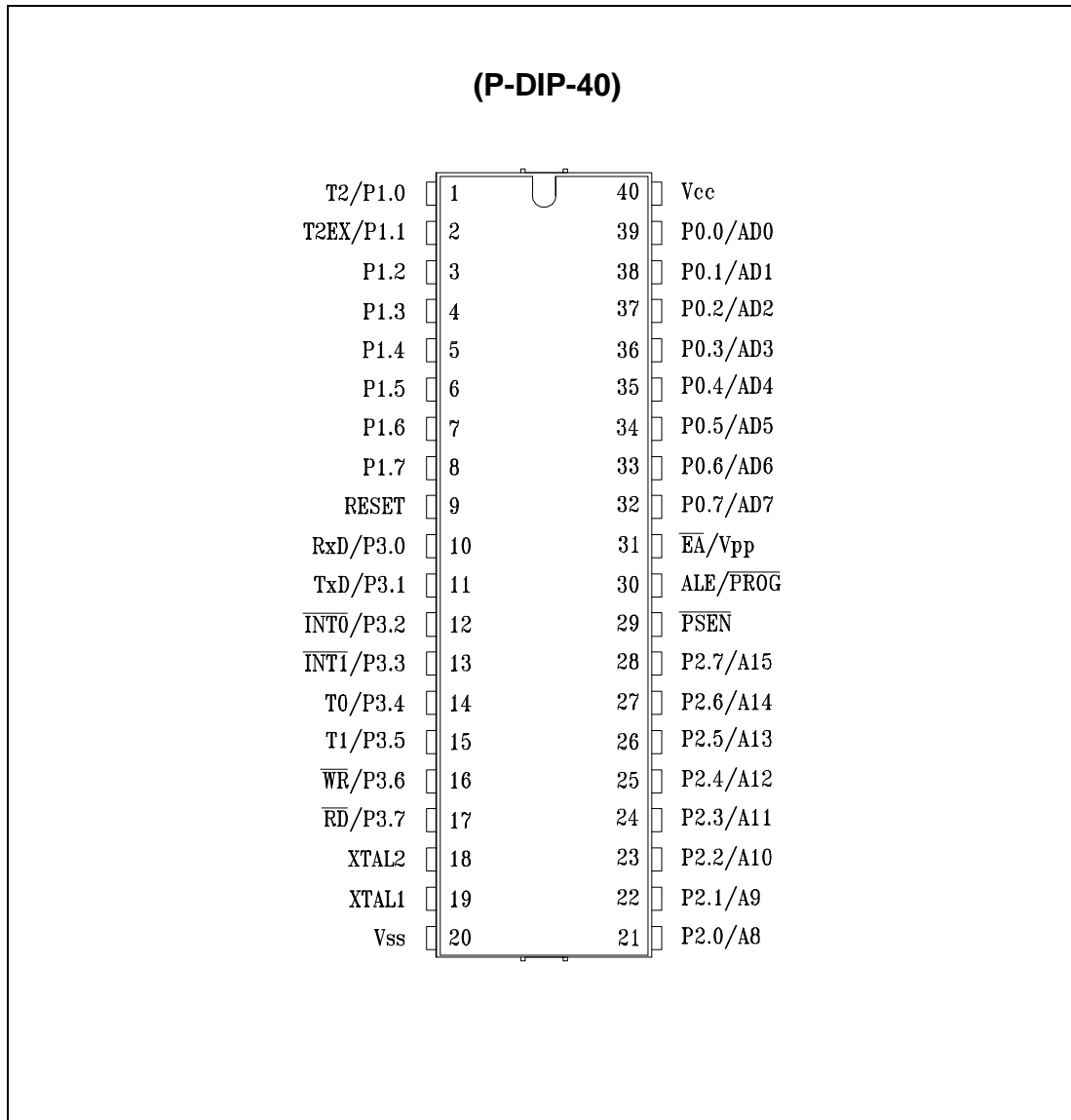
Operating voltage (V)	(EP)ROM (bytes)	RAM (bytes)	Device	Frequency (MHz)	
4.25~5.5	ROM-less	128	GMS90C31	12/24/40	
		128	GMS90C31B	12/24/33	
		256	GMS90C32	12/24/40	
		256	GMS90C32B	12/24/33	
	4K 4K 8K 8K 16K 24K 32K	128 128 256 256 256 256 256	128 128 256 256 256 256 256	GMS90C51	12/24/40
				GMS90C51B	12/24/33
				GMS90C52	12/24/40
				GMS90C52B	12/24/33
				*GMS90C54	"
				*GMS90C56	"
	4K OTP 8K OTP 16K OTP 24K OTP 32K OTP	128 256 256 256 256	128 256 256 256 256	GMS97C51	12/24/33
				GMS97C52	"
GMS97C54				"	
GMS97C56				"	
GMS97C58				"	
2.7~5.5	ROM-less	128	GMS90L31	12	
		128	GMS90L31B		
		256	GMS90L32		
		256	GMS90L32B		
	4K 4K 8K 8K 16K 24K 32K	128 128 256 256 256 256 256	128 128 256 256 256 256 256	GMS90L51	12
				GMS90L51B	
				GMS90L52	
				GMS90L52B	
				*GMS90L54	
				*GMS90L56	
	4K OTP 8K OTP 16K OTP 24K OTP 32K OTP	128 256 256 256 256	128 256 256 256 256	GMS97L51	12
				GMS97L52	
GMS97L54					
GMS97L56					
GMS97L58					

Note) * : Under development

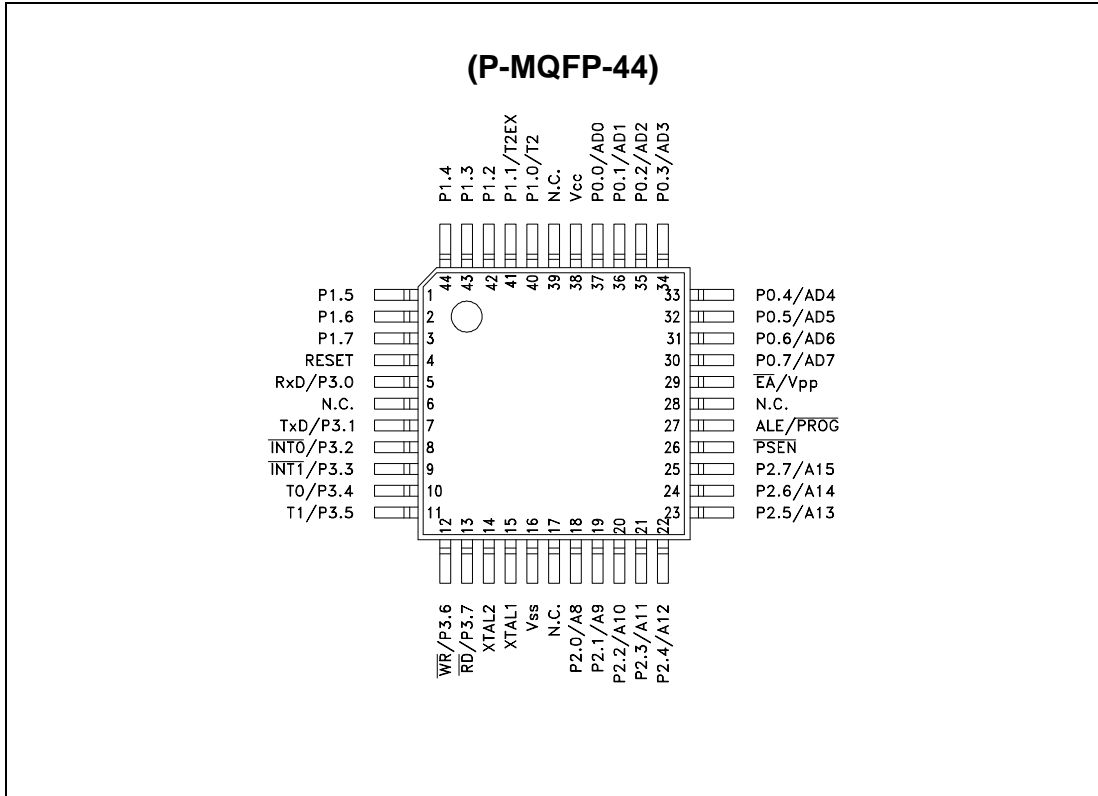
44-PLCC Pin Configuration (top view)

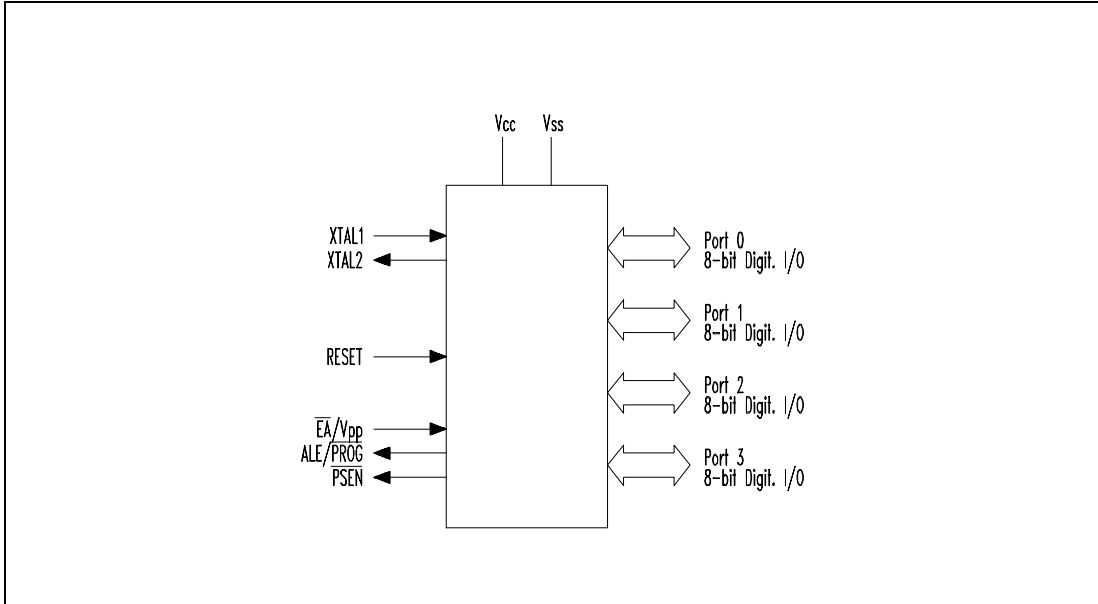


40-PDIP Pin Configuration (top view)



44-MQFP Pin Configuration (top view)





Logic Symbol

Pin Definitions and Functions

Symbol	Pin Number			Input/ Output	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
P1.0 - P1.7	2-9	1-8	40-44, 1-3	I/O	<p>Port1 Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the pull-ups (I_{IL}, in the DC characteristics). Pins P1.0 and P1.1 also. Port1 also receives the low-order address byte during program memory verification. Port1 also serves alternate functions of Timer 2.</p> <p>P1.0 / T2 : Timer/counter 2 external count input P1.1 / T2EX : Timer/counter 2 trigger input</p> <p>In GMS9xC54/56/58: P1.0 / T2, Clock Out : Timer/counter 2 external count input, Clock Out</p>
	2	1	40		
	3	2	41		
	2	1	40		
P3.0 - P3.7	11, 13-19	10-17	5, 7-13	I/O	<p>Port 3 Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 3 pins that are externally pulled low will source current because of the pull-ups (I_{IL}, in the DC characteristics). Port 3 also serves the special features of the 80C51 family, as listed below.</p> <p>P3.0 / RxD receiver data input (asynchronous) or data input output(synchronous) of serial interface 0 P3.1 / TxD transmitter data output (asynchronous) or clock output (synchronous) of the serial interface 0 P3.2 / $\overline{\text{INT0}}$ interrupt 0 input/timer 0 gate control P3.3 / $\overline{\text{INT1}}$ interrupt 1 input/timer 1 gate control P3.4 / T0 counter 0 input P3.5 / T1 counter 1 input P3.6 / $\overline{\text{WR}}$ the write control signal latches the data byte from port 0 into the external data memory P3.7 / $\overline{\text{RD}}$ the read control signal enables the external data memory to port 0</p>
	11	10	5		
	13	11	7		
	14	12	8		
	15	13	9		
	16	14	10		
	17	15	11		
	18	16	12		
	19	17	13		
	XTAL2	20	18		

Symbol	Pin Number			Input/ Output	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
XTAL1	21	19	15	I	XTAL1 Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is divided down by a divide-by-two flip-flop. Minimum and maximum high and low times as well as rise fall times specified in the AC characteristics must be observed.
P2.0 - P2.7	24-31	21-28	18-25	I/O	Port 2 Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-up resistors and can be used as inputs. As inputs, port 2 pins that are externally pulled low will source current because of the pull-ups (I_{IL} , in the DC characteristics). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 emits the contents of the P2 special function register.
$\overline{\text{PSEN}}$	32	29	26	O	The Program Store Enable The read strobe to external program memory when the device is executing code from the external program memory. $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
RESET	10	9	4	I	RESET A high level on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{CC} .

Symbol	Pin Number			Input/ Output	Function
	P-LCC-44	P-DIP-40	P-MQFP-44		
ALE / $\overline{\text{PROG}}$	33	30	27	O	<p>The Address Latch Enable / Program pulse Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming.</p> <p>In GMS9xC54/56/58: If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With this bit set, the pin is weakly pulled high. The ALE disable feature will be terminated by reset. Setting the ALE-disable bit has no affect if the microcontroller is in external execution mode.</p>
$\overline{\text{EA}}$ / V _{PP}	35	31	29	I	<p>External Access Enable / Program Supply Voltage EA must be external held low to enable the device to fetch code from external program memory locations 0000_H to FFFF_H. If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than its internal memory size. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming.</p> <p>Note; however, that if any of the Lock bits are programmed, EA will be internally latched on reset.</p>
P0.0 - P0.7	43-36	39-32	37-30	I/O	<p>Port 0 Port 0 is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1s. Port 0 also outputs the code bytes during program verification in the GMS97C5x. External pull-up resistors are required during program verification.</p>
V _{SS}	22	20	16	-	Circuit ground potential
V _{CC}	44	40	38	-	Supply terminal for all operating modes
N.C.	1,12, 23,34	-	6,17,28,39	-	No connection

Functional Description

The GMS90 series is fully compatible to the standard 8051 microcontroller family.

It is compatible with the general 8051 family. While maintaining all architectural and operational characteristics of the general 8051 family.

Figure 1 shows a block diagram of the GMS90 series

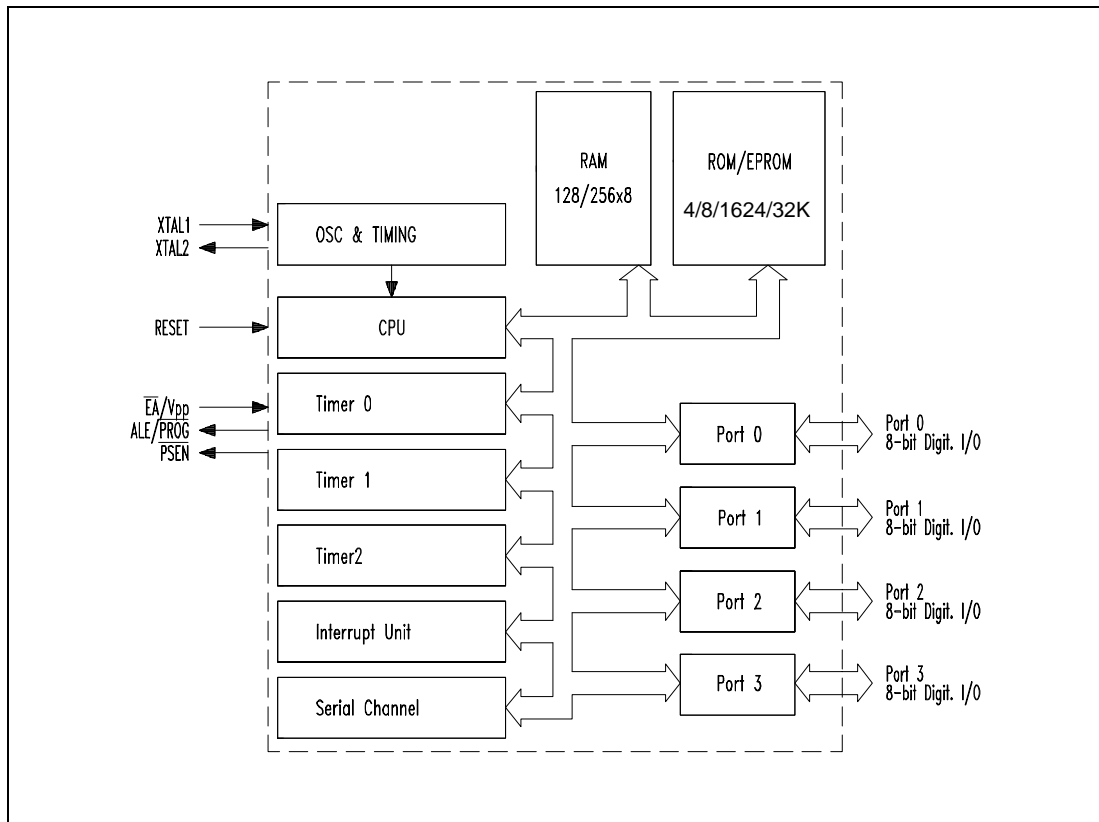


Figure 1
Block Diagram of the GMS90 series

CPU

The GMS90 series is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 12 MHz crystal, 58% of the instructions are executed in 1.0 μ s.

Special Function Register PSW

	MSB							LSB	
Bit No.	7	6	5	4	3	2	1	0	
Addr. D0 _H	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Reset value of PSW is 00H.

Bit	Function										
CY	Carry Flag										
AC	Auxiliary Carry Flag (for BCD operations)										
F0	General Purpose Flag										
<table style="display: inline-table; border: none; vertical-align: middle;"> <tr> <td style="padding-right: 20px;"><i>RS1</i></td> <td><i>RS0</i></td> </tr> <tr> <td style="padding-right: 20px;">0</td> <td>0</td> </tr> <tr> <td style="padding-right: 20px;">0</td> <td>1</td> </tr> <tr> <td style="padding-right: 20px;">1</td> <td>0</td> </tr> <tr> <td style="padding-right: 20px;">1</td> <td>1</td> </tr> </table>	<i>RS1</i>	<i>RS0</i>	0	0	0	1	1	0	1	1	Register Bank select control bits Bank 0 selected, data address 00H - 07 _H Bank 1 selected, data address 08H - 0F _H Bank 2 selected, data address 10H - 17 _H Bank 3 selected, data address 18H - 1F _H
<i>RS1</i>	<i>RS0</i>										
0	0										
0	1										
1	0										
1	1										
OV	Overflow Flag										
F1	General Purpose Flag										
P	Parity Flag Set/cleared by hardware each instruction cycle to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.										

Special Function Registers

All registers, except the program counter and the four general purpose register banks, reside in the special function register area.

The 27 special function registers (SFR) include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. There are also 128 directly addressable bits within the SFR area.

All SFRs are listed in **table 1**, **table 2**, and **table 3**.

In **table 1** they are organized in numeric order of their addresses. In **table 2** they are organized in groups which refer to the functional blocks of the GMS90 series. **Table 3** illustrates the contents of the SFRs.

Table 1

Special Function Registers in Numeric Order of their Addresses

Address	Register	Contents after Reset	Address	Register	Contents after Reset
80H	P0 ¹⁾	FFH	98H	SCON ¹⁾	00H
81H	SP	07H	99H	SBUF	XX _H ²⁾
82H	DPL	00H	9AH	reserved	XX _H ²⁾
83H	DPH	00H	9BH	reserved	XX _H ²⁾
84H	reserved	XX _H ²⁾	9CH	reserved	XX _H ²⁾
85H	reserved	XX _H ²⁾	9DH	reserved	XX _H ²⁾
86H	reserved	XX _H ²⁾	9EH	reserved	XX _H ²⁾
87H	PCON	0XXX000B ²⁾	9FH	reserved	XX _H ²⁾
88H	TCON ¹⁾	00H	A0H	P2 ¹⁾	FFH
89H	TMOD	00H	A1H	reserved	XX _H ²⁾
8AH	TL0	00H	A2H	reserved	XX _H ²⁾
8BH	TL1	00H	A3H	reserved	XX _H ²⁾
8CH	TH0	00H	A4H	reserved	XX _H ²⁾
8DH	TH1	00H	A5H	reserved	XX _H ²⁾
8E _H ³⁾	⌀ ³⁾	⌀ ³⁾	A6H	reserved	XX _H ²⁾
8FH	reserved	XX _H ²⁾	A7H	reserved	XX _H ²⁾
90H	P1 ¹⁾	FFH	A8H	IE ¹⁾	0X000000B ²⁾
91H	reserved	00H	A9H	reserved	XX _H ²⁾
92H	reserved	XX _H ²⁾	AAH	reserved	XX _H ²⁾
93H	reserved	XX _H ²⁾	ABH	reserved	XX _H ²⁾
94H	reserved	XX _H ²⁾	ACH	reserved	XX _H ²⁾
95H	reserved	XX _H ²⁾	ADH	reserved	XX _H ²⁾
96H	reserved	XX _H ²⁾	AEH	reserved	XX _H ²⁾
97H	reserved	XX _H ²⁾	AFH	reserved	XX _H ²⁾

¹⁾ : Bit-addressable Special Function Register.

²⁾ : X means that the value is indeterminate and the location is reserved.

³⁾ : The GMS9xC54/56/58 have the AUXR0 register at address 8E_H.

GMS9xC51/52

GMS9xC54/56/58

8E _H	reserved	XX _H ²⁾	8E _H	AUXR0 1)	XXXXXXXX0B ²⁾
-----------------	----------	-------------------------------	-----------------	----------	--------------------------

Special Function Registers in Numeric Order of their Addresses (continued)

Address	Register	Contents after Reset	Address	Register	Contents after Reset
B0H B1H B2H B3H B4H B5H B6H B7H	P3 ¹⁾ reserved reserved reserved reserved reserved reserved reserved	FFH XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾	D8H D9H DAH DBH DCH DDH DEH DFH	reserved reserved reserved reserved reserved reserved reserved reserved	XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾
B8H B9H BAH BBH BCH BDH BEH BFH	IP ¹⁾ reserved reserved reserved reserved reserved reserved reserved	XX00000B ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾	E0H E1H E2H E3H E4H E5H E6H E7H	ACC ¹⁾ reserved reserved reserved reserved reserved reserved reserved	00H XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾
C0H C1H C2H C3H C4H C5H C6H C7H	reserved reserved reserved reserved reserved reserved reserved reserved	XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾	E8H E9H EAH EBH ECH EDH EEH EFH	reserved reserved reserved reserved reserved reserved reserved reserved	XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾
C8H C9H ³⁾ CAH CBH CCH CDH CEH CFH	T2CON T2MOD RC2L RC2H TL2 TH2 reserved reserved	00H 3) 00H 00H 00H 00H XX _H ²⁾ XX _H ²⁾	F0H F1H F2H F3H F4H F5H F6H F7H	B ¹⁾ reserved reserved reserved reserved reserved reserved reserved	00H XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾
D0H D1H D2H D3H D4H D5H D6H D7H	PSW ¹⁾ reserved reserved reserved reserved reserved reserved reserved	00H XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾	F8H F9H FAH FBH FCH FDH FEH FFH	reserved reserved reserved reserved reserved reserved reserved reserved	XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾ XX _H ²⁾

1) : Bit-addressable Special Function Register

2) : X means that the value is indeterminate and the location is reserved

3) :

GMS9xC51/52

GMS9xC54/56/58

C9H	T2MOD	XXXXXXXX0H ²⁾	C9H	T2MOD	XXXXXXXX00B ²⁾
-----	-------	--------------------------	-----	-------	---------------------------

Table 2
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	E0H ¹⁾	00H
	B	B-Register	F0H ¹⁾	00H
	DPH	Data Pointer, High Byte	83H	00H
	DPL	Data Pointer, Low Byte	82H	00H
	PSW	Program Status Word Register	D0H ¹⁾	00H
	SP	Stack Pointer	81H	07H
Interrupt System	IE	Interrupt Enable Register	A8H ¹⁾	0X000000B ²⁾
	IP	Interrupt Priority Register	B8H ¹⁾	XX000000B ²⁾
Ports	P0	Port 0	80H ¹⁾	FFH
	P1	Port 1	90H ¹⁾	XXH ³⁾
	P2	Port 2	A0H ¹⁾	FFH
	P3	Port 3	B0H ¹⁾	FFH
Serial Channels	PCON ²⁾	Power Control Register	87H	0XXX0000B ²⁾
	SBUF	Serial Channel Buffer Reg.	99H	XXH ³⁾
	SCON	Serial Channel 0 Control Reg.	98H ¹⁾	00H
Timer 0 / Timer 1	TCON	Timer 0/1 Control Register	88H ¹⁾	00H
	TH0	Timer 0, High Byte	8CH	00H
	TH1	Timer 1, High Byte	8DH	00H
	TL0	Timer 0, Low Byte	8AH	00H
	TL1	Timer 1, Low Byte	8BH	00H
	TMOD	Timer Mode Register	89H	00H
Timer 2	T2CON	Timer 2 Control Register	C8H ¹⁾	00H
	T2MOD	Timer 2 Mode Register	C9H	00H
	RC2H	Timer 2 Reload Capture Reg., High Byte	CBH	00H
	RC2L	Timer 2 Reload Capture Reg., Low Byte	CAH	00H
	TH2	Timer 2, High Byte	CDH	00H
	TL2	Timer 2, Low Byte	CCH	00H
	AUXR0 ⁴⁾	Aux. Register 0	8EH	XXXXXXXX0B ²⁾
	Power Saving Modes	PCON	Power Control Register	87H

1) Bit-addressable Special Function register

2) This special function register is listed repeatedly since some bit of it also belong to other functional blocks

3) X means that the value is indeterminate and the location is reserved

4) : The AUXR0 is in the GMS9xC54/56/58 only.

Table 3
Contents of SFRs, SFRs in Numeric Order

Address	Register	Bit7	6	5	4	3	2	1	0
80H	P0								
81H	SP								
82H	DPL								
83H	DPH								
87H	PCON	SMOD	-	-	-	GF1	GF0	PDE	IDLE
88H	TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89H	TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0
8AH	TL0								
8BH	TL1								
8CH	TH0								
8DH	TH1								
8EH	AUXR0 ¹⁾	-	-	-	-	-	-	-	A0 ¹⁾
90H	P1								
98H	SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99H	SBUF								
A0H	P2								
A8H	IE	EA	-	ET2	ES	ET1	EX1	ET0	EX0
B0H	P3								
B8H	IP	-	-	PT2	PS	PT1	PX1	PT0	PX0
C8H	T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
C9H	T2MOD	-	-	-	-	-	-	T2OE ¹⁾	DCEN

--	--	--	--	--	--	--	--	--	--

 SFR bit and byte addressable

--	--	--	--	--	--	--	--	--	--

 SFR not bit addressable

- : this bit location is reserved

¹⁾ Only in the GMS9xC54/56/58

Table 3
Contents of SFRs, SFRs in Numeric Order (continued)

Address	Register	Bit7	6	5	4	3	2	1	0
CA _H	RC2L								
CB _H	RC2H								
CC _H	TL2								
CD _H	TH2								
D0 _H	PSW	CY	AC	F0	RS1	RS0	OV	F1	P
E0 _H	ACC								
F0 _H	B								

--	--	--	--	--	--	--	--

 SFR bit and byte addressable

--	--	--	--	--	--	--	--

 SFR not bit addressable

- : this bit location is reserved

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **table 4**:

Table 4

Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD				Input Clock	
		Gate	C/T	M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	X	X	0	0	$f_{osc} / 12 \cdot 32$	$f_{osc} / 24 \cdot 32$
1	16-bit timer/counter	X	X	0	1	$f_{osc} / 12$	$f_{osc} / 24$
2	8-bit timer/counter with 8-bit autoreload	X	X	1	0	$f_{osc} / 12$	$f_{osc} / 24$
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	X	X	1	1	$f_{osc} / 12$	$f_{osc} / 23$

In the "timer" function ($C/\bar{T} = "0"$) the register is incremented every machine cycle. therefore the count rate is $f_{osc}/12$.

In the "counter" function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is $f_{osc}/24$. External inputs INT0 and INT1 (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 2** illustrates the input clock logic.

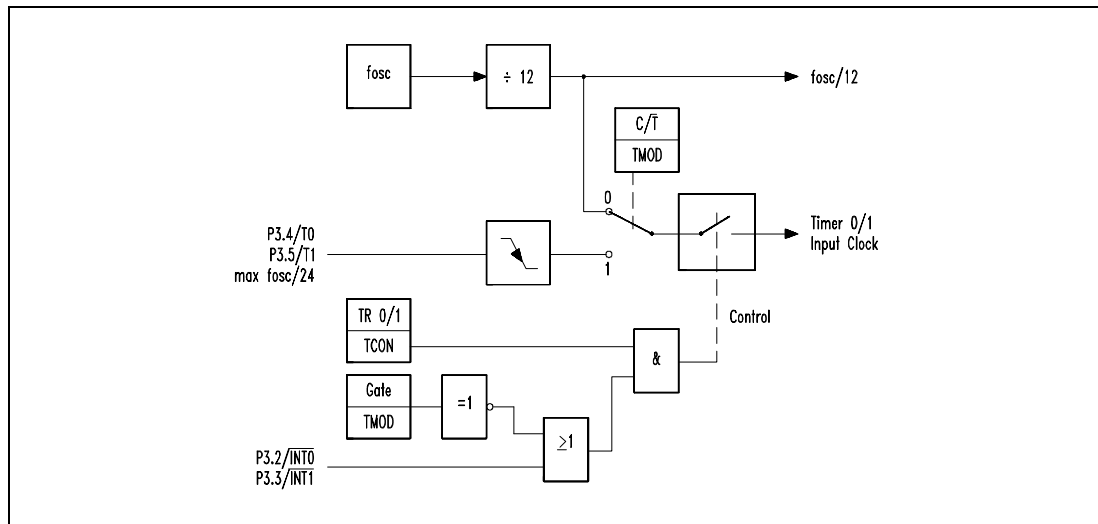



Figure 2
Timer/Counter 0 and 1 Input Clock Logic

Timer 2

Timer 2 is a 16-bit timer/Counter with an up/down count feature. It can operate either as timer or as an event counter which is selected by bit $\overline{C/T2}$ (T2CON.1). It has three operating modes as shown in table 5.

Table 5
Timer/Counter 2 Operating Modes

Mode	T2CON			T2MOD DCEN	T2CON EXEN	P1.1/ T2EX	Remarks	Input Clock	
	RxCLK or TxCLK	CP/ RL2	TR2					internal	external (P1.0/T2)
16-bit Auto- reload	0	0	1	0	0	X	reload upon overflow reload trigger (falling edge) Down counting Up counting	$f_{osc}/12$	max $f_{osc}/24$
	0	0	1	0	1	↓			
	0	0	1	1	X	0			
	0	0	1	1	X	1			
16-bit Cap- ture	0	1	1	X	0	X	16 bit Timer/ Counter (only up-counting) capture TH2, TL2, RC2H, RC2L	$f_{osc}/12$	max $f_{osc}/24$
	0	1	1	X	1	↓			
Baud Rate Gene- rator	1	X	1	X	0	X	no overflow interrupt request (TF2) extra external interrupt ("Timer 2")	$f_{osc}/2$	max $f_{osc}/24$
	1	X	1	X	1	↓			
off	X	X	0	X	X	X	Timer 2 stops	-	-

Note : ↓ =  falling edge

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **table 6**. The possible baud rates can be calculated using the formulas given in **table 7**.

Table 6
USART Operating Modes

Mode	SCON		Baud rate	Description
	SM0	SM1		
0	0	0	$f_{osc}/12$	Serial data enters and exits through RxD. TxD outputs the shift clock. 8-bit are transmitted/received (LSB first)
1	0	1	Timer 1/2 overflow rate	8-bit UART 10 bits are transmitted (through TxD) or received (RxD)
2	1	0	$f_{osc}/32$ or $f_{osc}/64$	9-bit UART 11 bits are transmitted (TxD) or received (RxD)
3	1	1	Timer 1/2 overflow rate	9-bit UART Like mode 2 except the variable baud rate

Table 7
Formulas for Calculating Baud rates

Baud Rate derived from	Interface Mode	Baud rate
Oscillator	0 2	$f_{osc}/12$ $(2^{SMOD} \cdot f_{osc})/64$
Timer 1 (16-bit timer) (8-bit timer with 8-bit autoreload)	1,3 1,3	$(2^{SMOD} \cdot \text{timer 1 overflow rate})/32$ $(2^{SMOD} \cdot f_{osc})/(32 \cdot (256 - TH1))$
Timer2	1,3	$f_{osc}/(32 \cdot (65536 - (RC2H, RC2L)))$

Interrupt System

The GMS90 series provides 5 or 6 interrupt sources with two priority levels. **Figure 3** gives a general overview of the interrupt sources and illustrates the request and control flags.

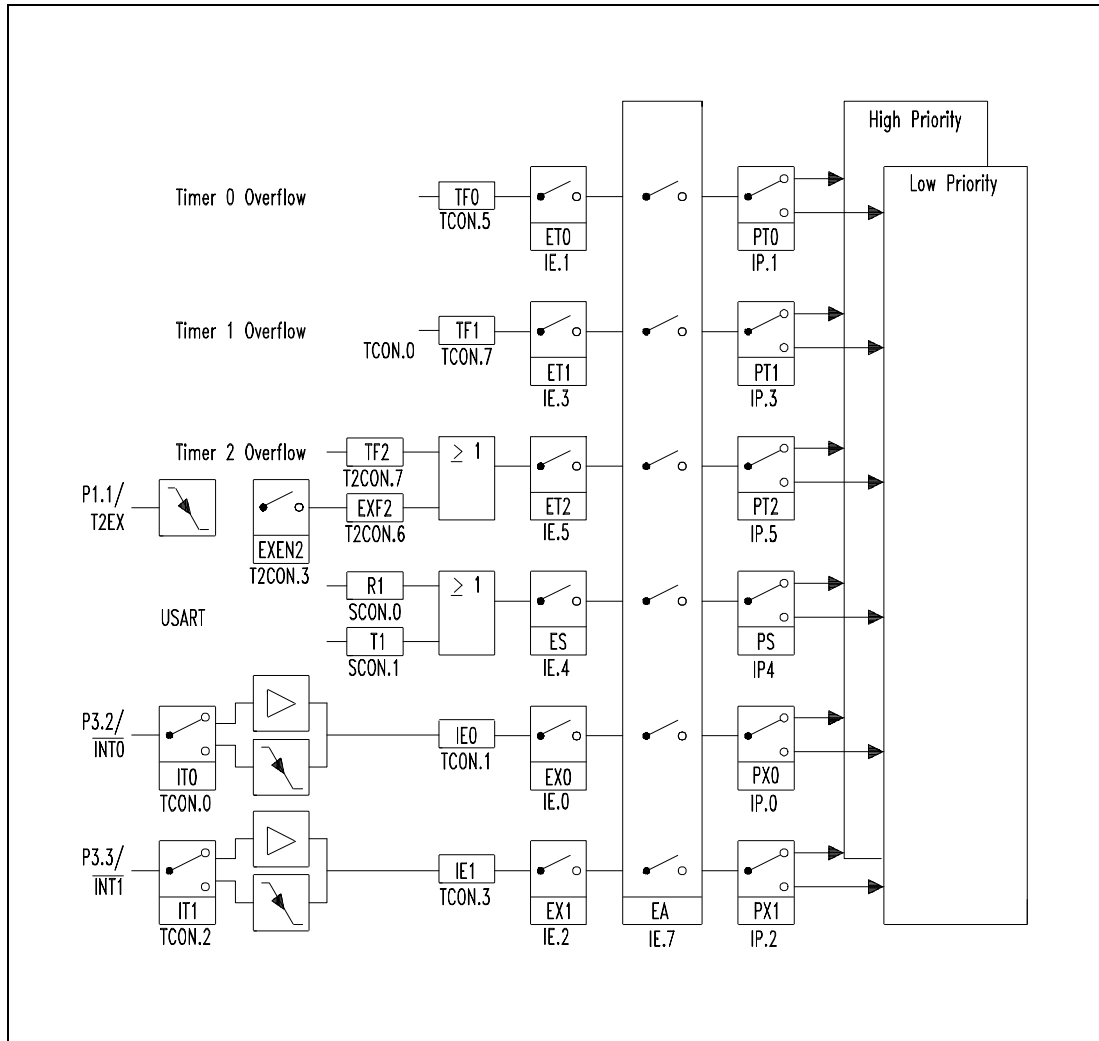


Figure 3
Interrupt Request Sources

Table 8
Interrupt Sources and their Corresponding Interrupt Vectors

Source (Request Flags)	Vector	Vector Address
RESET	RESET	0000H
IE0	External interrupt 0	0003H
TF0	Timer 0 interrupt	000BH
IE1	External interrupt 1	0013H
TF1	Timer 1 interrupt	001BH
RI + TI	Serial port interrupt	0023H
TF2 + EXF2	Timer 2 interrupt	002BH

A low-priority interrupt can itself be interrupted by a high-priority interrupt, but not by another low priority interrupt. A high-priority interrupt cannot be interrupted by any other interrupt source.

If two requests of different priority level are received simultaneously, the request of higher priority is serviced. If requests of the same priority are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence as shown in **table 9**.

Table 9
Interrupt Priority-Within-Level

Interrupt Source		Priority
External Interrupt 0	IE0	High
Timer 0 Interrupt	TF0	je
External Interrupt 1	IE1	je
Timer 1 Interrupt	TF1	je
Serial Channel	RI + TI	je
Timer 2 Interrupt	TF2 EXF2	Low

Power Saving Modes

Two power down modes are available, the Idle Mode and Power Down Mode.

The bits PDE and IDLE of the register PCON select the Power Down mode or the Idle mode, respectively. If the Power Down mode and the Idle mode are set at the same time, the Power Down mode takes precedence. **Table 10** gives a general overview of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering Instruction Example	Leaving by	Remarks
Idle mode	ORL PCON, #01H	- Enabled interrupt - Hardware Reset	CPU is gated off CPU status registers maintain their data. Peripherals are active
Power-down Mode	ORL PCON, #02H	Hardware Reset	Oscillator is stopped, contents of on-chip RAM and SFRs are maintained (leaving Power Down Mode means redefinition of SFR contents).

In the Power Down mode of operation, V_{CC} can be reduced to minimize power consumption. It must be ensured, however, that V_{CC} is not reduced before the Power Down Mode is invoked, and that V_{CC} is restored to its normal operating level, before the Power Down mode is terminated. The reset signal that terminates the Power Down Mode also restarts the oscillator. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize (similar to power-on reset).

Absolute Maximum Ratings

Ambient temperature under bias (T_A)	-40 to + 85 °C
Storage temperature (T_{ST})	-65 to + 150 °C
Voltage on V_{CC} pins with respect to ground (V_{SS})	-0.5 V to 6.5 V
Voltage on any pin with respect to ground (V_{SS})	-0.5 to $V_{CC} + 0.5$ V
Input current on any pin during overload condition	-10 mA to + 10 mA
Absolute sum of all input currents during overload condition	100 mA
Power dissipation	TBD

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During overload conditions ($V_{IN} > V_{CC}$ or $V_{IN} < V_{SS}$) the Voltage on V_{CC} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

DC Characteristics for GMS90C31/32, GMS90C51/52**GMS90C31B/32B, GMS90C51B/52B** $V_{CC} = 5\text{ V} \pm 10\%, -15\%$; $V_{SS} = 0\text{ V}$; $T_A = 0\text{ }^\circ\text{C to } 70\text{ }^\circ\text{C}$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except EA, RESET)	V_{IL}	-0.5	$0.2 V_{CC} - 0.1$	V	-
Input low voltage (EA)	V_{IL1}	-0.5	$0.2 V_{CC} - 0.3$	V	-
Input low voltage (RESET)	V_{IL2}	-0.5	$0.2 V_{CC} + 0.1$	V	-
Input high voltage (except XTAL1, EA, RESET)	V_{IH}	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	-
Input high voltage to XTAL1	V_{IH1}	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	-
Input high voltage to EA, RESET	V_{IH2}	$0.6 V_{CC}$	$V_{CC} + 0.5$	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	$I_{OL} = 1.6\text{mA}^{1)}$
Output high voltage (port 0, ALE, PSEN)	V_{OL1}	-	0.45	V	$I_{OL} = 3.2\text{mA}^{1)}$
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 $0.9 V_{CC}$	- -	V	$I_{OH} = -80\text{ }^\mu\text{A}$ $I_{OH} = -10\text{ }^\mu\text{A}$
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4 $0.9 V_{CC}$	- -	V	$I_{OH} = -800\text{ }^\mu\text{A}^{2)}$ $I_{OH} = -80\text{ }^\mu\text{A}^{2)}$
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	$^\mu\text{A}$	$V_{IN} = 0.45\text{V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	$^\mu\text{A}$	$V_{IN} = 2\text{V}$
Input leakage current (port 0, EA)	I_{LI}	-	± 1	$^\mu\text{A}$	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	$f_c = 1\text{MHz}$ $T_A = 25\text{ }^\circ\text{C}$
Power supply current:					
Active mode, 12MHz ⁶⁾	I_{CC}	-	21	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 12MHz ⁶⁾	I_{CC}	-	4.8	mA	$V_{CC} = 5\text{V}^{5)}$
Active mode, 24 MHz ⁶⁾	I_{CC}	-	36.2	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 24MHz ⁶⁾	I_{CC}	-	8.2	mA	$V_{CC} = 5\text{V}^{5)}$
Active mode, 33 MHz ⁶⁾	I_{CC}	-	45	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 33 MHz ⁶⁾	I_{CC}	-	10	mA	$V_{CC} = 5\text{V}^{5)}$
Active mode, 40 MHz ⁶⁾	I_{CC}	-	56.5	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 40 MHz ⁶⁾	I_{CC}	-	12.5	mA	$V_{CC} = 5\text{V}^{5)}$
Power Down Mode	I_{PD}	-	50	$^\mu\text{A}$	$V_{CC} = 5\text{V}^{3)}$

DC Characteristics for GMS90C54/56/58

 $V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$; $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except EA, RESET)	V_{IL}	-0.5	$0.2 V_{CC} - 0.1$	V	-
Input low voltage (EA)	V_{IL1}	-0.5	$0.2 V_{CC} - 0.3$	V	-
Input low voltage (RESET)	V_{IL2}	-0.5	$0.2 V_{CC} + 0.1$	V	-
Input high voltage (except XTAL1, EA, RESET)	V_{IH}	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	-
Input high voltage to XTAL1	V_{IH1}	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	-
Input high voltage to EA, RESET	V_{IH2}	$0.6 V_{CC}$	$V_{CC} + 0.5$	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	$I_{OL} = 1.6\text{mA}^{1)}$
Output high voltage (port 0, ALE, PSEN)	V_{OL1}	-	0.45	V	$I_{OL} = 3.2\text{mA}^{1)}$
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 $0.9 V_{CC}$	- -	V	$I_{OH} = -80\text{ }\mu\text{A}^{2)}$ $I_{OH} = -10\text{ }\mu\text{A}^{2)}$
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4 $0.9 V_{CC}$	- -	V	$I_{OH} = -800\text{ }\mu\text{A}^{2)}$ $I_{OH} = -80\text{ }\mu\text{A}^{2)}$
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	μA	$V_{IN} = 0.45\text{V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	μA	$V_{IN} = 2\text{V}$
Input leakage current (port 0, EA)	I_{LI}	-	± 1	μA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	$f_C = 1\text{MHz}$ $T_A = 25\text{ }^{\circ}\text{C}$
Power supply current:					
Active mode, 12MHz ⁶⁾	I_{CC}	-	TBD	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 12MHz ⁶⁾	I_{CC}	-	TBD	mA	$V_{CC} = 5\text{V}^{5)}$
Active mode, 24 MHz ⁶⁾	I_{CC}	-	TBD	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 24MHz ⁶⁾	I_{CC}	-	TBD	mA	$V_{CC} = 5\text{V}^{5)}$
Active mode, 33 MHz ⁶⁾	I_{CC}	-	TBD	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 33 MHz ⁶⁾	I_{CC}	-	TBD	mA	$V_{CC} = 5\text{V}^{5)}$
Power Down Mode	I_{PD}	-	50	μA	$V_{CC} = 5\text{V}^{3)}$

DC Characteristics for GMS97C51/52/54/56/58 $V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$; $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage (except EA, RESET)	V_{IL}	-0.5	$0.2 V_{CC} - 0.1$	V	-
Input low voltage (EA)	V_{IL1}	-0.5	$0.1 V_{CC} - 0.1$	V	-
Input low voltage (RESET)	V_{IL2}	-0.5	$0.2 V_{CC} + 0.1$	V	-
Input high voltage (except XTAL1, EA, RESET)	V_{IH}	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V	-
Input high voltage to XTAL1	V_{IH1}	$0.7 V_{CC}$	$V_{CC} + 0.5$	V	-
Input high voltage to EA, RESET	V_{IH2}	$0.6 V_{CC}$	$V_{CC} + 0.5$	V	-
Output low voltage (ports 1, 2, 3)	V_{OL}	-	0.45	V	$I_{OL} = 1.6\text{mA}^{1)}$
Output high voltage (port 0, ALE, PSEN)	V_{OL1}	-	0.45	V	$I_{OL} = 3.2\text{mA}^{1)}$
Output high voltage (ports 1, 2, 3)	V_{OH}	2.4 $0.9 V_{CC}$	- -	V	$I_{OH} = -80\text{ }\mu\text{A}^{2)}$ $I_{OH} = -10\text{ }\mu\text{A}^{2)}$
Output high voltage (port 0 in external bus mode, ALE, PSEN)	V_{OH1}	2.4 $0.9 V_{CC}$	- -	V	$I_{OH} = -800\text{ }\mu\text{A}^{2)}$ $I_{OH} = -80\text{ }\mu\text{A}^{2)}$
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-10	-50	μA	$V_{IN} = 0.45\text{V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-65	-650	μA	$V_{IN} = 2\text{V}$
Input leakage current (port 0, EA)	I_{LI}	-	± 1	μA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	$f_C = 1\text{MHz}$ $T_A = 25\text{ }^{\circ}\text{C}$
Power supply current:					
Active mode, 12 MHz ⁶⁾	I_{CC}	-	21	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 12 MHz ⁶⁾	I_{CC}	-	18	mA	$V_{CC} = 5\text{V}^{5)}$
Active mode, 24 MHz ⁶⁾	I_{CC}	-	36	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 24 MHz ⁶⁾	I_{CC}	-	20	mA	$V_{CC} = 5\text{V}^{5)}$
Active mode, 33 MHz ⁶⁾	I_{CC}	-	47	mA	$V_{CC} = 5\text{V}^{4)}$
Idle mode, 33 MHz ⁶⁾	I_{CC}	-	25	mA	$V_{CC} = 5\text{V}^{5)}$
Power down mode	I_{PD}	-	50	μA	$V_{CC} = 5\text{V}^{3)}$

DC Characteristics for GMS90L31/32, GMS90L51/52,**GMS90L31B/32B, GMS90L51B/52B (Low voltage version)** $V_{CC} = 3.3\text{ V} + 0.3\text{V}$, -0.6V ; $V_{SS} = 0\text{ V}$; $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage	V_{IL}	-0.5	0.8	V	-
Input high voltage	V_{IH}	2.0	$V_{CC} + 0.5$	V	-
Output low voltage Port 1,2,3	V_{OL1}	-	0.45	V	$I_{OL} = 1.6\text{mA}$ ¹⁾
Port 0,EA,RESET	V_{OL2}	-	0.45	V	$I_{OL} = 3.2\text{mA}$ ¹⁾
Port 1,2,3	V_{OL3}	-	0.3	V	$I_{OL} = 100\text{ }^{\mu}\text{A}$ ¹⁾
Port 0,EA,RESET	V_{OL4}	-	0.3	V	$I_{OL} = 200\text{ }^{\mu}\text{A}$ ¹⁾
Output high voltage Port 1,2,3	V_{OH1}	2.0	-	V	$I_{OH} = -20\text{ }^{\mu}\text{A}$
	V_{OH2}	$0.9V_{CC}$	-	V	$I_{OH} = -10\text{ }^{\mu}\text{A}$
Port 0 in external bus mode, ALE,PSEN	V_{OH3}	2.0	-	V	$I_{OH} = -800\text{ }^{\mu}\text{A}$ ²⁾
	V_{OH4}	$0.9V_{CC}$	-	V	$I_{OH} = -80\text{ }^{\mu}\text{A}$ ²⁾
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-1	-50	$\text{ }^{\mu}\text{A}$	$V_{IN} = 0.45\text{V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-25	-250	$\text{ }^{\mu}\text{A}$	$V_{IN} = 2.0\text{V}$
Input leakage current (port 0, EA)	I_{LI}	-	± 1	$\text{ }^{\mu}\text{A}$	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	$f_C = 1\text{MHz}$ $T_A = 25\text{ }^{\circ}\text{C}$
Power supply current: Active mode, 12 MHz	I_{CC}	-	11	mA	$V_{CC} = 3.6\text{V}$ ⁴⁾
Idle mode, 12 MHz	I_{CC}	-	5	mA	$V_{CC} = 3.6\text{V}$ ⁵⁾
Power Down Mode	I_{PD}	-	15	$\text{ }^{\mu}\text{A}$	$V_{CC} = 2 \dots 3.6\text{V}$ ³⁾

DC Characteristics for GMS90L54/56/58 (Low voltage version) $V_{CC} = 3.3\text{ V} + 0.3\text{V}, -0.6\text{V}; V_{SS} = 0\text{ V};$ $T_A = 0\text{ }^{\circ}\text{C to } 70\text{ }^{\circ}\text{C}$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage	V_{IL}	-0.5	0.8	V	-
Input high voltage	V_{IH}	2.0	$V_{CC} + 0.5$	V	-
Output low voltage Port 1,2,3	V_{OL1}	-	0.45	V	$I_{OL} = 1.6\text{mA}^{1)}$
Port 0,EA,RESET	V_{OL2}	-	0.45	V	$I_{OL} = 3.2\text{mA}^{1)}$
Port 1,2,3	V_{OL3}	-	0.3	V	$I_{OL} = 100\text{ }^{\mu}\text{A}^{1)}$
Port 0,EA,RESET	V_{OL4}	-	0.3	V	$I_{OL} = 200\text{ }^{\mu}\text{A}^{1)}$
Output high voltage Port 1,2,3	V_{OH1}	2.0	-	V	$I_{OH} = -20\text{ }^{\mu}\text{A}^{2)}$
	V_{OH2}	$0.9V_{CC}$	-	V	$I_{OH} = -10\text{ }^{\mu}\text{A}^{2)}$
Port 0 in external bus mode, ALE,PSEN	V_{OH3}	2.0	-	V	$I_{OH} = -800\text{ }^{\mu}\text{A}^{2)}$
	V_{OH4}	$0.9V_{CC}$	-	V	$I_{OH} = -80\text{ }^{\mu}\text{A}^{2)}$
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-1	-50	$\text{ }^{\mu}\text{A}$	$V_{IN} = 0.45\text{V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-25	-250	$\text{ }^{\mu}\text{A}$	$V_{IN} = 2.0\text{V}$
Input leakage current (port 0, EA)	I_{LI}	-	± 1	$\text{ }^{\mu}\text{A}$	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	$f_C = 1\text{MHz}$ $T_A = 25\text{ }^{\circ}\text{C}$
Power supply current: Active mode, 12 MHz	I_{CC}	-	TBD	mA	$V_{CC} = 3.6\text{V}^{4)}$
Idle mode, 12 MHz	I_{CC}	-	TBD	mA	$V_{CC} = 3.6\text{V}^{5)}$
Power Down Mode	I_{PD}	-	TBD	$\text{ }^{\mu}\text{A}$	$V_{CC} = 2 \dots 3.6\text{V}^{3)}$

DC Characteristics for GMS97L51/52/54/56/58 (Low voltage version) $V_{CC} = 3.3\text{ V} + 0.3\text{V}$, -0.6V ; $V_{SS} = 0\text{ V}$; $T_A = 0^\circ\text{C}$ to 70°C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input low voltage	V_{IL}	-0.5	0.8	V	-
Input high voltage	V_{IH}	2.0	$V_{CC} + 0.5$	V	-
Output low voltage					
Port 1,2,3	V_{OL1}	-	0.45	V	$I_{OL} = 1.6\text{mA}$ ¹⁾
Port 0,EA,RESET	V_{OL2}	-	0.45	V	$I_{OL} = 3.2\text{mA}$ ¹⁾
Port 1,2,3	V_{OL3}	-	0.3	V	$I_{OL} = 100\mu\text{A}$ ¹⁾
Port 0,EA,RESET	V_{OL4}	-	0.3	V	$I_{OL} = 200\mu\text{A}$ ¹⁾
Output high voltage					
Port 1,2,3	V_{OH1}	2.0	-	V	$I_{OH} = -20\mu\text{A}$
	V_{OH2}	$0.9V_{CC}$	-	V	$I_{OH} = -10\mu\text{A}$
Port 0 in external bus mode, ALE,PSEN	V_{OH3}	2.0	-	V	$I_{OH} = -800\mu\text{A}$ ²⁾
	V_{OH4}	$0.9V_{CC}$	-	V	$I_{OH} = -80\mu\text{A}$ ²⁾
Logic 0 input current (ports 1, 2, 3)	I_{IL}	-1	-50	μA	$V_{IN} = 0.45\text{V}$
Logical 1-to-0 transition current (ports 1, 2, 3)	I_{TL}	-25	-250	μA	$V_{IN} = 2.0\text{V}$
Input leakage current (port 0, EA)	I_{LI}	-	± 1	μA	$0.45 < V_{IN} < V_{CC}$
Pin capacitance	C_{IO}	-	10	pF	$f_C = 1\text{MHz}$ $T_A = 25^\circ\text{C}$
Power supply current:					
Active mode, 12 MHz	I_{CC}	-	11	mA	$V_{CC} = 3.6\text{V}$ ⁴⁾
Idle mode, 12 MHz	I_{CC}	-	5	mA	$V_{CC} = 3.6\text{V}$ ⁵⁾
Power Down Mode	I_{PD}	-	15	μA	$V_{CC} = 3.6\text{V}$ ³⁾

- 1) Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL} of ALE and port 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operation. In the worst case (capacitive loading: > 50pF at 3.3V, > 100pF at 5V), the noise pulse on ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a schmitt-trigger, or use an address latch with a schmitt-trigger strobe input.
- 2) Capacitive loading on ports 0 and 2 may cause the V_{OH} on ALE and PSEN to momentarily fall below the $0.9V_{CC}$ specification when the address lines are stabilizing.
- 3) I_{PD} (Power Down Mode) is measured under following conditions:
EA = Port0 = V_{CC} ; RESET = V_{SS} ; XTAL2 = N.C.; XTAL1 = V_{SS} ; all other pins are disconnected.
- 4) I_{CC} (active mode) is measured with:
XTAL1 driven with $t_{CLCH}, t_{CHCL} = 5ns$, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 = N.C.;
EA = Port0 = RESET = V_{CC} ; all other pins are disconnected. I_{CC} would be slightly higher if a crystal oscillator is used (appr. 1mA).
- 5) I_{CC} (Idle mode) is measured with all output pins disconnected and with all peripherals disabled;
XTAL1 driven with $t_{CLCH}, t_{CHCL} = 5ns$, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 = N.C.;
RESET = EA = V_{SS} ; Port0 = V_{CC} ; all other pins are disconnected;
- 6) $I_{CC\ max}$ at other frequencies is given by:
active mode: $I_{CC} = 1.27 \mu A + f_{OSC} + 5.73$
idle mode: $I_{CC} = 0.28 \mu A + f_{OSC} + 1.45$ (except OTP devices)
where f_{OSC} is the oscillator frequency in MHz. I_{CC} values are given in mA and measured at $V_{CC} = 5V$.

AC Characteristics for GMS90 series (12MHz version)

V_{CC} = 5 V : V_{CC} = 5 V + 10%, -15%; V_{SS} = 0 V; TA = 0°C to 70°C

(C_L for port 0. ALE and PSEN outputs = 100pF; C_L for all other outputs = 80 pF)

V_{CC} = 3.3 V : V_{CC} = 3.3 V + 0.3 V, -0.6 V; V_{SS} = 0 V; TA = 0°C to 70°C

(C_L for port 0. ALE and PSEN outputs = 50pF; C_L for all other outputs = 50 pF)

Variable clock : V_{CC} = 5V : 1/t_{CLCL} = 3.5 MHz to 12 MHz

V_{CC} = 3.3V : 1/t_{CLCL} = 1 MHz to 12 MHz

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock		
		min.	max.	min.	max.	
ALE pulse width	t _{LHLL}	127	-	2t _{CLCL} - 40	-	ns
Address setup to ALE	t _{AVLL}	43	-	t _{CLCL} - 40	-	ns
Address hold after ALE	t _{LLAX}	30	-	t _{CLCL} - 53	-	ns
ALE low to valid instr in	t _{LLIV}	-	233	-	4t _{CLCL} - 100	ns
ALE to PSEN	t _{LLPL}	58	-	t _{CLCL} - 25	-	ns
PSEN pulse width	t _{PLPH}	215	-	3t _{CLCL} - 35	-	ns
PSEN to valid instr in	t _{PLIV}	-	150	-	3t _{CLCL} - 100	ns
Input instruction hold after PSEN	t _{PXOX}	0	-	0	-	ns
Input instruction float after PSEN	t _{PXIZ} ^{*)}	-	63	-	t _{CLCL} - 20	ns
Address valid after PSEN	t _{PXAV} ^{*)}	75	-	t _{CLCL} - 8	-	ns
Address to valid instruction in	t _{AVIV}	-	302	-	5t _{CLCL} - 115	ns
Address float to PSEN	t _{AZPL}	0	-	0	-	ns

*) Interfacing the GMS90 series to devices with float times up to 75 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for GMS90 series (12MHz version)**External Data Memory Characteristics**

Parameter	Symbol	Limit Values				Unit
		12 MHz Clock		Variable Clock		
		min.	max.	min.	max.	
RD pulse width	t_{RLRH}	400	-	$6t_{CLCL} - 100$	-	ns
\overline{WR} pulse width	t_{WLWH}	400	-	$6t_{CLCL} - 100$	-	ns
Address hold after ALE	t_{LAX2}	53	-	$t_{CLCL} - 30$	-	ns
RD to valid data in	t_{RLDV}	-	252	-	$5t_{CLCL} - 165$	ns
Data hold after RD	t_{RHDX}	0	-	0	-	ns
Data float after RD	t_{RHDZ}	-	97	-	$2t_{CLCL} - 70$	ns
ALE to valid data in	t_{LLDV}	-	517	-	$8t_{CLCL} - 150$	ns
Address to valid data in	t_{AVDV}	-	585	-	$9t_{CLCL} - 165$	ns
ALE to \overline{WR} or RD	t_{LLWL}	200	300	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to \overline{WR} or RD	t_{AVWL}	203	-	$4t_{CLCL} - 130$	-	ns
\overline{WR} or RD high to ALE high	t_{WHLH}	43	123	$t_{CLCL} - 40$	$t_{CLCL} + 40$	ns
Data valid to \overline{WR} transition	t_{QVWX}	33	-	$t_{CLCL} - 50$	-	ns
Data setup before \overline{WR}	t_{QVWH}	433	-	$7t_{CLCL} - 150$	-	ns
Data hold after \overline{WR}	t_{WHQX}	33	-	$t_{CLCL} - 50$	-	ns
Address float after RD	t_{RLAZ}	-	0	-	0	ns

Advance Information (12MHz version)**External Clock Drive**

Parameter	Symbol	Limit Values		Unit
		Variable clock		
		min.	max.	
Oscillator period($V_{CC}=5V$)	t_{CLCL}	83.3	285.7	ns
Oscillator period($V_{CC}=3.3V$)	t_{CLCL}	83.3	1	us
High time	t_{CHCX}	20	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	20	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	20	ns
Fall time	t_{CHCL}	-	20	ns

AC Characteristics for GMS90 series (24MHz version)

$V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$; $T_A = 0^\circ\text{C}$ to 70°C

(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory characteristics

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5\text{ MHz to }24\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	43	-	$2t_{CLCL} - 40$	-	ns
Address setup to ALE	t_{AVLL}	17	-	$t_{CLCL} - 25$	-	ns
Address hold after ALE	t_{LLAX}	17	-	$t_{CLCL} - 25$	-	ns
ALE low to valid instr in	t_{LLIV}	-	80	-	$4t_{CLCL} - 87$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	22	-	$t_{CLCL} - 20$	-	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	95	-	$3t_{CLCL} - 30$	-	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	-	60	-	$3t_{CLCL} - 65$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{PXIZ}^*)$	-	32	-	$t_{CLCL} - 10$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{PXAV}^*)$	37	-	$t_{CLCL} - 5$	-	ns
Address to valid instruction in	t_{AVIV}	-	148	-	$5t_{CLCL} - 60$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	-	0	-	ns

*) Interfacing the GMS90 series to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC characteristics for GMS90 series (24MHz version)**External Data Memory Characteristics**

Parameter	Symbol	Limit Values				Unit
		24 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 24 \text{ MHz}$		
		min.	max.	min.	max.	
\overline{RD} pulse width	t_{RLRH}	180	-	$6t_{CLCL} - 70$	-	ns
\overline{WR} pulse width	t_{WLWH}	180	-	$6t_{CLCL} - 70$	-	ns
Address hold after ALE	t_{LAX2}	15	-	$t_{CLCL} - 27$	-	ns
\overline{RD} to valid data in	t_{RLDV}	-	118	-	$5t_{CLCL} - 90$	ns
Data hold after \overline{RD}	t_{RHDX}	0	-	0	-	ns
Data float after \overline{RD}	t_{RHDZ}	-	63	-	$2t_{CLCL} - 20$	ns
ALE to valid data in	t_{LLDV}	-	200	-	$8t_{CLCL} - 133$	ns
Address to valid data in	t_{AVDV}	-	220	-	$9t_{CLCL} - 155$	ns
ALE to \overline{WR} or \overline{RD}	t_{LLWL}	75	175	$3t_{CLCL} - 50$	$3t_{CLCL} + 50$	ns
Address valid to \overline{WR} or \overline{RD}	t_{AVWL}	67	-	$4t_{CLCL} - 97$	-	ns
\overline{WR} or \overline{RD} high to ALE high	t_{WHLH}	17	67	$t_{CLCL} - 25$	$t_{CLCL} + 25$	ns
Data valid to \overline{WR} transition	t_{QVWX}	5	-	$t_{CLCL} - 37$	-	ns
Data setup before \overline{WR}	t_{QVWH}	170	-	$7t_{CLCL} - 122$	-	ns
Data hold after \overline{WR}	t_{WHQX}	15	-	$t_{CLCL} - 27$	-	ns
Address float after \overline{RD}	t_{RLAZ}	-	0	-	0	ns

Advance Information (24MHz version)

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable clock Freq. = 3.5 MHz to 24 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	41.7	285.7	ns
High time	t_{CHCX}	12	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	12	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	12	ns
Fall time	t_{CHCL}	-	12	ns

AC Characteristics for GMS90 series (33MHz version)

$V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$; $T_A = 0\text{ }^{\circ}\text{C}$ to $70\text{ }^{\circ}\text{C}$

(C_L for port 0, ALE and PSEN outputs = 100pF; C_L for all other outputs = 80pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		33 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5\text{ MHz to }33\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	40	-	$2t_{CLCL} - 20$	-	ns
Address setup to ALE	t_{AVLL}	10	-	$t_{CLCL} - 20$	-	ns
Address hold after ALE	t_{LLAX}	10	-	$t_{CLCL} - 20$	-	ns
ALE low to valid instr in	t_{LLIV}	-	56	-	$4t_{CLCL} - 65$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	15	-	$t_{CLCL} - 15$	-	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	80	-	$3t_{CLCL} - 20$	-	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	-	35	-	$3t_{CLCL} - 55$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{PXIZ}^{*)}$	-	20	-	$t_{CLCL} - 10$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{PXAV}^{*)}$	25	-	$t_{CLCL} - 5$	-	ns
Address to valid instruction in	t_{AVIV}	-	91	-	$5t_{CLCL} - 60$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	0	-	0	-	ns

*) Interfacing the GMS90 series to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for GMS90series (33MHz version)**External Data Memory Characteristics**

Parameter	Symbol	Limit Values				Unit
		33 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 33 \text{ MHz}$		
		min.	max.	min.	max.	
\overline{RD} pulse width	t_{RLRH}	132	-	$6t_{CLCL} - 50$	-	ns
\overline{WR} pulse width	t_{WLWH}	132	-	$6t_{CLCL} - 50$	-	ns
Address hold after ALE	t_{LAX2}	10	-	$t_{CLCL} - 20$	-	ns
\overline{RD} to valid data in	t_{RLDV}	-	81	-	$5t_{CLCL} - 70$	ns
Data hold after \overline{RD}	t_{RHDX}	0	-	0	-	ns
Data float after \overline{RD}	t_{RHDZ}	-	46	-	$2t_{CLCL} - 15$	ns
ALE to valid data in	t_{LLDV}	-	153	-	$8t_{CLCL} - 90$	ns
Address to valid data in	t_{AVDV}	-	183	-	$9t_{CLCL} - 90$	ns
ALE to \overline{WR} or \overline{RD}	t_{LLWL}	71	111	$3t_{CLCL} - 20$	$3t_{CLCL} + 20$	ns
Address valid to \overline{WR} or \overline{RD}	t_{AVWL}	66	-	$4t_{CLCL} - 55$	-	ns
\overline{WR} or \overline{RD} high to ALE high	t_{WHLH}	10	40	$t_{CLCL} - 20$	$t_{CLCL} + 20$	ns
Data valid to \overline{WR} transition	t_{QVWX}	5	-	$t_{CLCL} - 25$	-	ns
Data setup before \overline{WR}	t_{QVWH}	142	-	$7t_{CLCL} - 70$	-	ns
Data hold after \overline{WR}	t_{WHQX}	10	-	$t_{CLCL} - 20$	-	ns
Address float after \overline{RD}	t_{RLAZ}	-	0	-	0	ns

Advance Information (33MHz version)**External Clock Drive**

Parameter	Symbol	Limit Values		Unit
		Variable clock Freq. = 3.5 MHz to 33 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	30.3	285.7	ns
High time	t_{CHCX}	11.5	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	11.5	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	5	ns
Fall time	t_{CHCL}	-	5	ns

AC Characteristics for GMS90 series (40MHz version)

$V_{CC} = 5\text{ V} + 10\%, -15\%$; $V_{SS} = 0\text{ V}$; $T_A = 0\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100pF; C_L for all other outputs = 80pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5\text{ MHz to }40\text{ MHz}$		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	-	$2t_{CLCL} - 15$	-	ns
Address setup to ALE	t_{AVLL}	10	-	$t_{CLCL} - 15$	-	ns
Address hold after ALE	t_{LLAX}	10	-	$t_{CLCL} - 15$	-	ns
ALE low to valid instr in	t_{LLIV}	-	55	-	$4t_{CLCL} - 45$	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	-	$t_{CLCL} - 15$	-	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	60	-	$3t_{CLCL} - 15$	-	ns
$\overline{\text{PSEN}}$ to valid instr in	t_{PLIV}	-	25	-	$3t_{CLCL} - 50$	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	-	0	-	ns
Input instruction float after $\overline{\text{PSEN}}$	$t_{PXIZ}^*)$	-	15	-	$t_{CLCL} - 10$	ns
Address valid after $\overline{\text{PSEN}}$	$t_{PXAV}^*)$	20	-	$t_{CLCL} - 5$	-	ns
Address to valid instruction in	t_{AVIV}	-	65	-	$5t_{CLCL} - 60$	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	-50	-	- 5	-	ns

*) Interfacing the GMS90 series to devices with float times up to 35 ns is permissible. This limited bus contention will not cause any damage to port 0 Drivers.

AC Characteristics for GMS90series (40MHz version)**External Data Memory Characteristics**

Parameter	Symbol	Limit Values				Unit
		40 MHz Clock		Variable Clock $1/t_{CLCL} = 3.5 \text{ MHz to } 40 \text{ MHz}$		
		min.	max.	min.	max.	
\overline{RD} pulse width	t_{RLRH}	120	-	$6t_{CLCL} - 30$	-	ns
\overline{WR} pulse width	t_{WLWH}	120	-	$6t_{CLCL} - 30$	-	ns
Address hold after ALE	t_{LAX2}	10	-	$t_{CLCL} - 15$	-	ns
\overline{RD} to valid data in	t_{RLDV}	-	75	-	$5t_{CLCL} - 50$	ns
Data hold after \overline{RD}	t_{RHDX}	0	-	0	-	ns
Data float after \overline{RD}	t_{RHDX}	-	38	-	$2t_{CLCL} - 12$	ns
ALE to valid data in	t_{LLDV}	-	150	-	$8t_{CLCL} - 50$	ns
Address to valid data in	t_{AVDV}	-	150	-	$9t_{CLCL} - 75$	ns
ALE to \overline{WR} or \overline{RD}	t_{LLWL}	60	90	$3t_{CLCL} - 15$	$3t_{CLCL} + 15$	ns
Address valid to \overline{WR} or \overline{RD}	t_{AVWL}	70	-	$4t_{CLCL} - 30$	-	ns
\overline{WR} or \overline{RD} high to ALE high	t_{WHLH}	10	40	$t_{CLCL} - 15$	$t_{CLCL} + 15$	ns
Data valid to \overline{WR} transition	t_{QVWX}	5	-	$t_{CLCL} - 20$	-	ns
Data setup before \overline{WR}	t_{QVWH}	125	-	$7t_{CLCL} - 50$	-	ns
Data hold after \overline{WR}	t_{WHQX}	5	-	$t_{CLCL} - 20$	-	ns
Address float after \overline{RD}	t_{RLAZ}	-	0	-	0	ns

Advance Information (40MHz version)

External Clock Drive

Parameter	Symbol	Limit Values		Unit
		Variable clock Freq. = 3.5 MHz to 40 MHz		
		min.	max.	
Oscillator period	t_{CLCL}	25	285.7	ns
High time	t_{CHCX}	10	$t_{CLCL} - t_{CLCX}$	ns
Low time	t_{CLCX}	10	$t_{CLCL} - t_{CHCX}$	ns
Rise time	t_{CLCH}	-	10	ns
Fall time	t_{CHCL}	-	10	ns

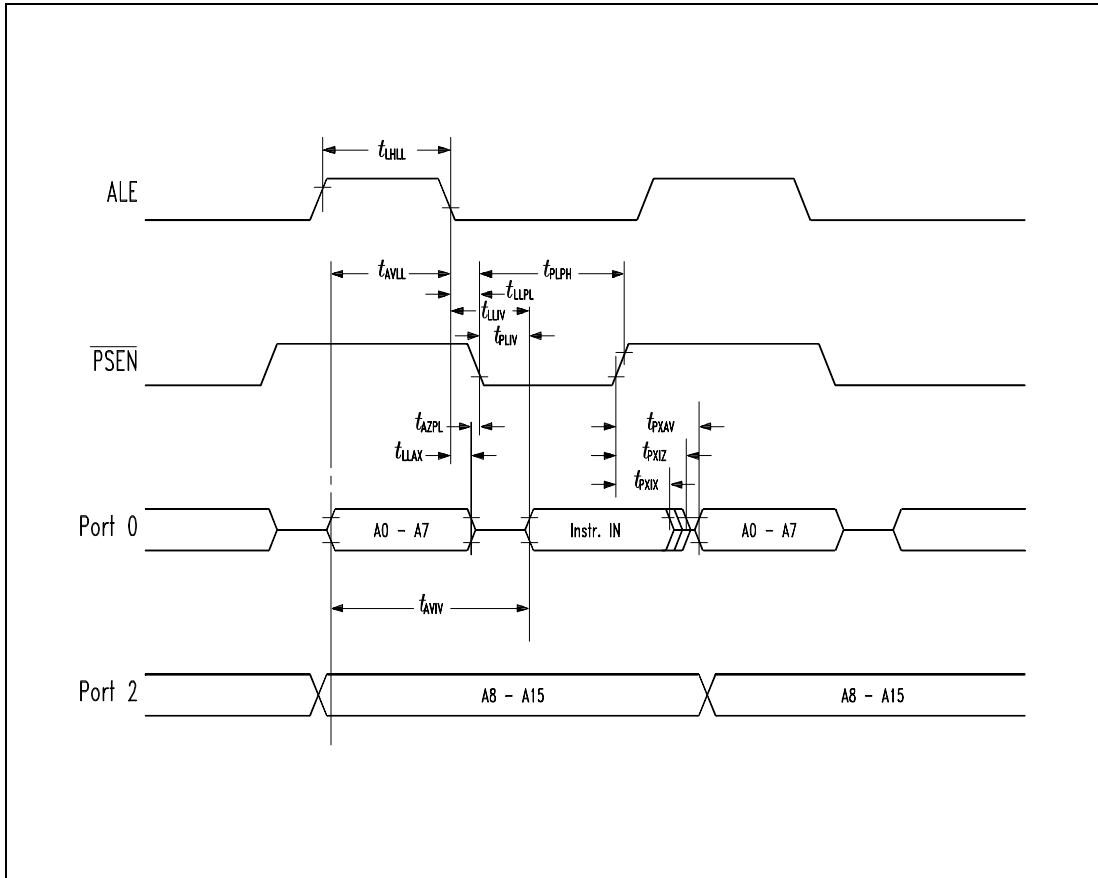


Figure 4
Program Memory Read Cycle

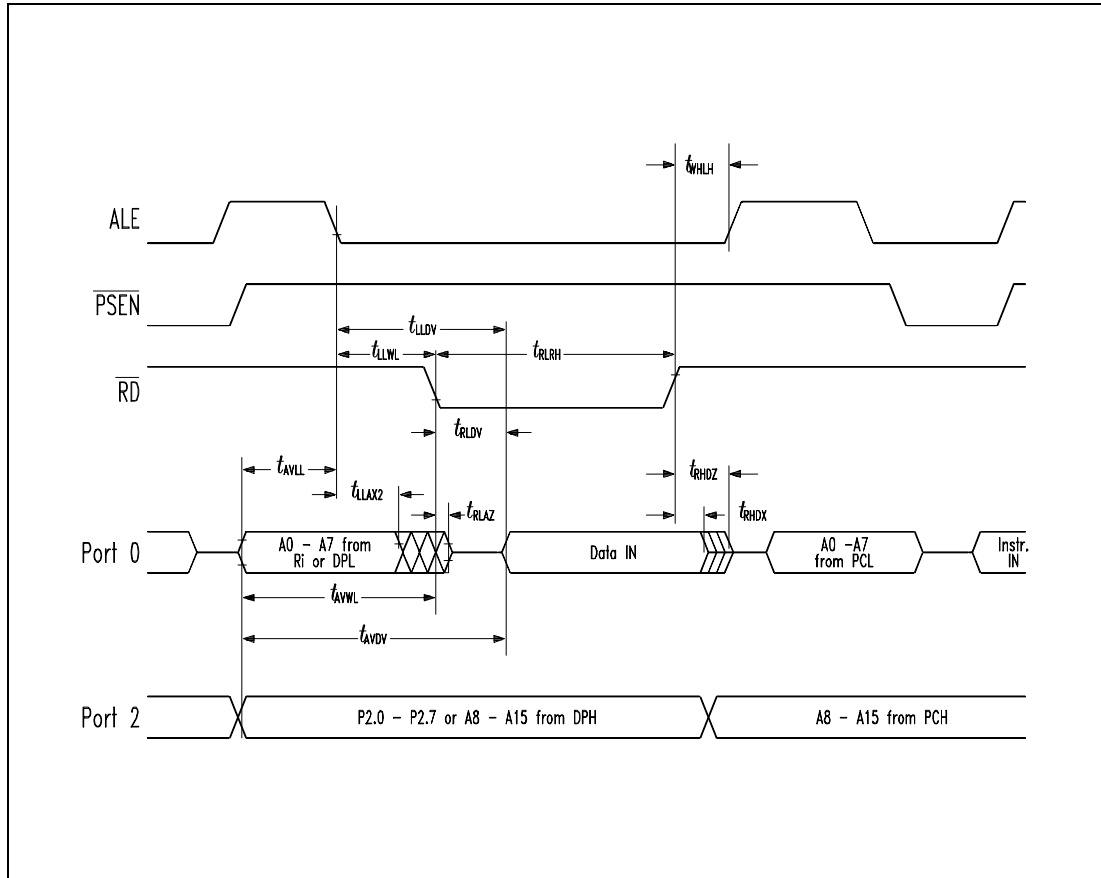


Figure 5
Data Memory Read Cycle

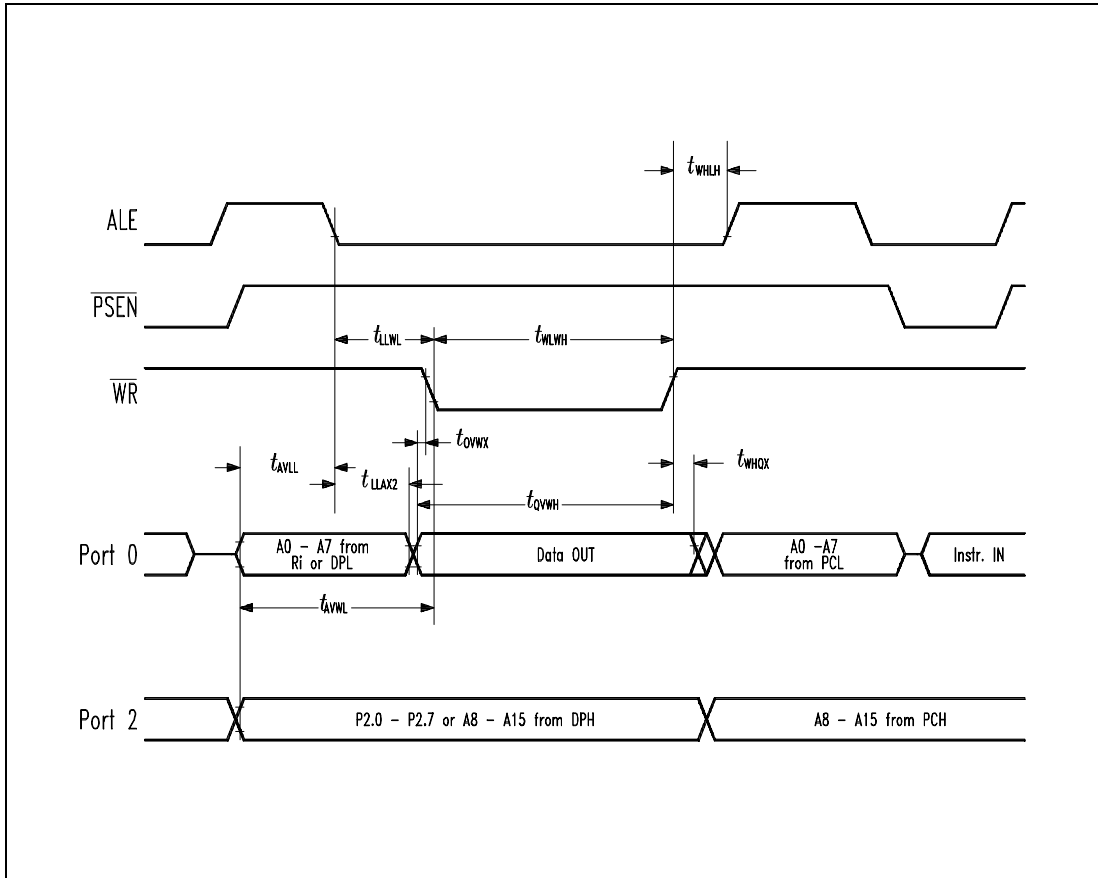


Figure 6
Data Memory Write Cycle

OTP ROM Verification Characteristics

ROM Verification Mode 1

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	-	$48t_{CLCL}$	ns
ENABLE to valid data	t_{ELQV}	-	$48t_{CLCL}$	ns
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	ns
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz

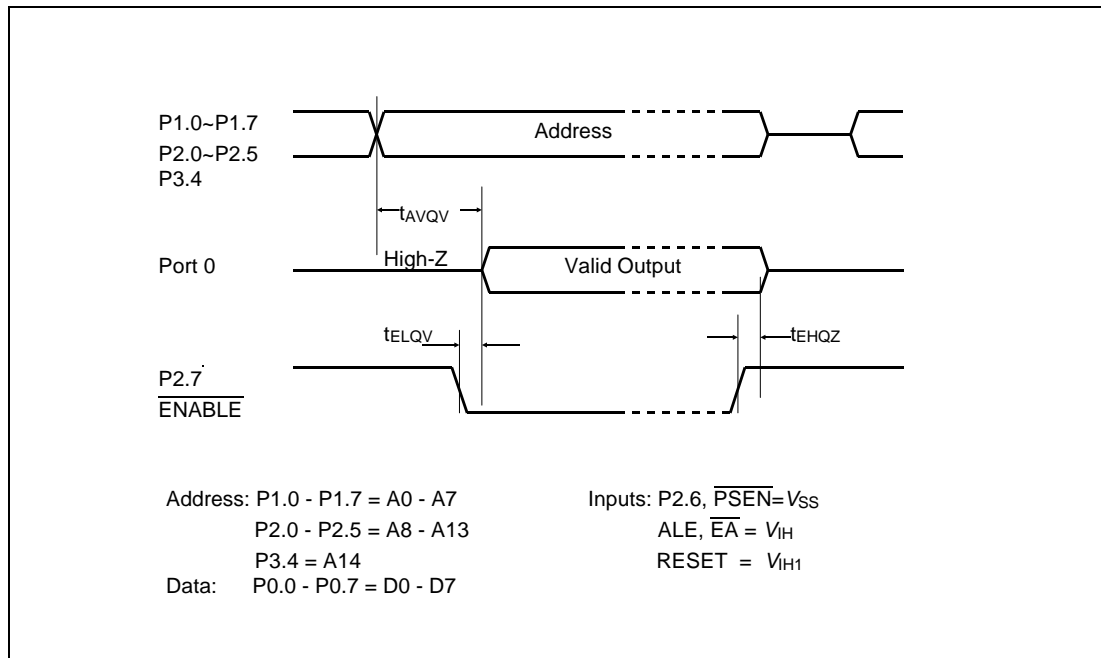


Figure 7
OTP ROM Verification Mode 1

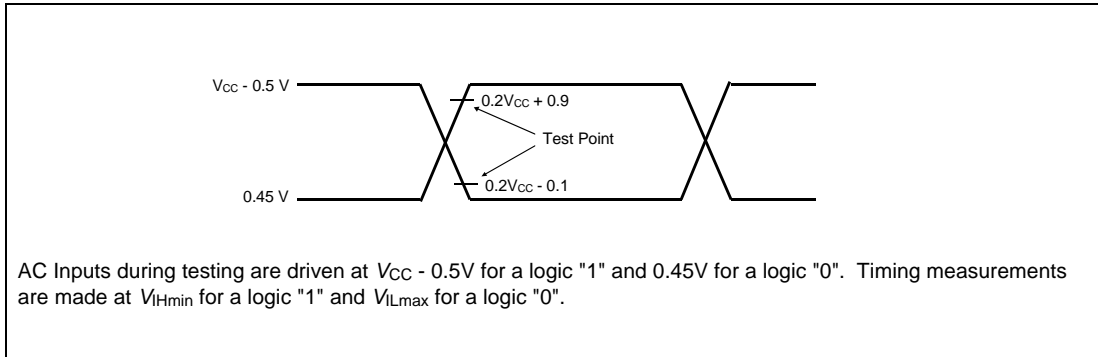


Figure 8
AC Testing : Input, Output Waveforms

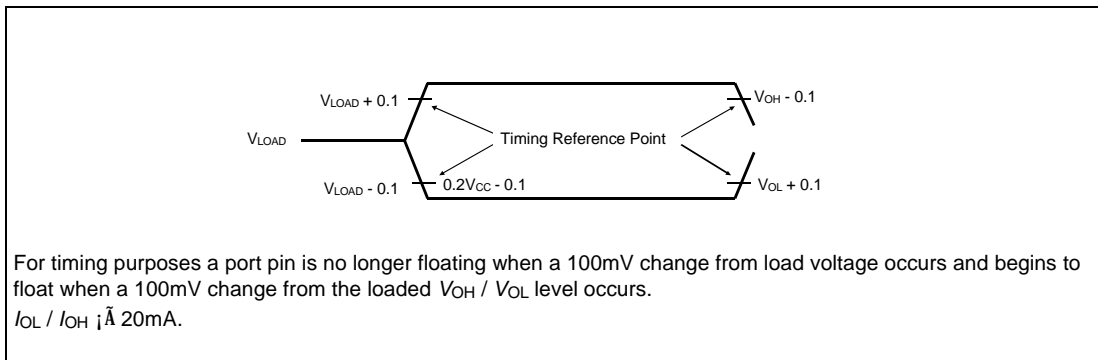


Figure 9
AC Testing : Float Waveforms

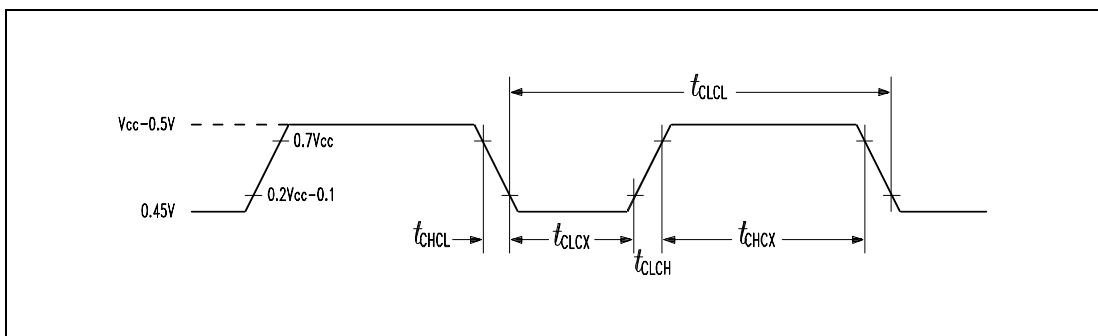


Figure 10
External Clock Cycle

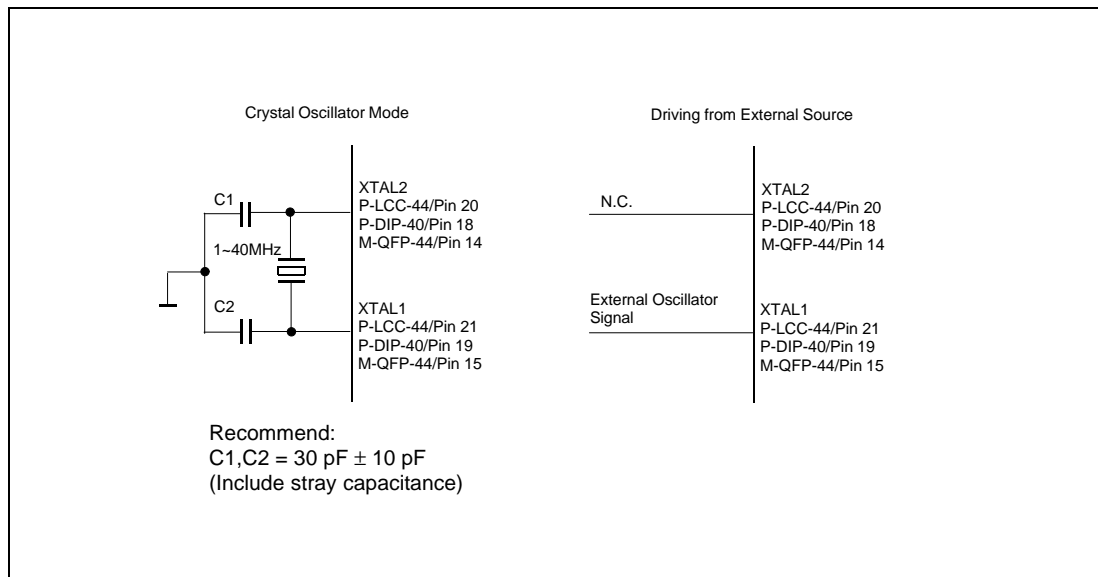


Figure 11
Recommended Oscillator Circuits

EPROM Characteristics

The GMS97C5x, 97L5x are programmed by using a modified Quick-Pulse Programming™ algorithm. It differs from older methods in the value used for V_{pp} (programming supply voltage) and in the width and number of the ALE/PROG pulses. The GMS97C5x, 97L5x contains two signature bytes that can be read and used by an EPROM programming system to identify the device. The signature bytes identify the device as manufactured by LGS. Table 11 shows the logic levels for reading the signature byte, and for programming the program memory, the encryption table, and the security bits. The circuit configuration and waveforms for quick-pulse programming are shown in Figures 12 and 13. Figure 14 shows the circuit configuration for normal program memory verification.

Quick-pulse programming

The setup for microcontroller quick-pulse programming is shown in Figure 13. Note that the GMS97C5x, 97L5x is running with a 4 to 6MHz oscillator. The reason the oscillator needs to be running is that the device is executing internal address and program data transfers. The address of the EPROM location to be programmed is applied to ports 1 and 2, as shown in Figure 12. The code byte to be programmed into that location is applied to port 0, RST, PSEN and pins of port 2 and 3 in Table 11 are held at the "Program Data" levels indicated in Table 11. The ALE/PROG is pulsed low 25 times as shown Figure 13. To program the encryption table, repeat the 25 pulses (10 pulses for 97x54/56/58) programming sequence for addresses 0 through 1FH(3FH for 97x54/56/58), using the "Pgm Encryption Table" levels. Do not forget that after the encryption table is programmed, verification cycles will produce only encrypted data. To program the security bits, repeat the 25 pulses (10 pulses for 97x54/56/58) programming sequence using the "Pgm Security Bit" levels after one security bit is programmed, further programming of the code memory and encryption table is disabled. However, the other security bit can still be programmed. Note that the EA/VPP pin must not be allowed to go above the maximum specified Vpp level for any amount of time. Even a narrow glitch above that voltage can cause permanent damage to the device. The VPP source should be well regulated and free glitches and overshoot.

Program Verification

If security bit 2 has not been programmed, the on-chip program memory can be read out for program verification. The address of the program memory location to be read is applied to ports 1 and 2 as shown in Figure 15. The other pins are held at the "Verify Code Data" levels indicated in Table 11. The contents of the address location will be emitted on port 0 for this operation. If the encryption table has been programmed, the data presented at port 0 will be the exclusive NOR of the program byte with one of the encryption bytes. The user will have to know the encryption table contents in order to correctly decode the verification data. The encryption table itself cannot be read out.

Program Memory Lock Bits

The two-level Program Lock system consists of 2 Lock bits and a 32-byte (64-byte for GMS97x54/56/58) Encryption Array which are used to protect the program memory against software piracy.

Encryption Array:

Within the EPROM array are 32 bytes (64 bytes for GMS97x54/56/58) of Encryption Array that are initially unprogrammed (all 1s). Every time that a byte is addressed during a verify, address lines are used to select a byte of the Encryption array. This byte is then exclusive-NORed (XNOR) with the code byte, creating an Encrypted Verify byte.

The algorithm, with the array in the unprogrammed state (all 1s), will return the code in its original, unmodified form, It is recommended that whenever the Encryption Array is used, at least one of the Lock Bits be programmed as well.

Lock Bit Protection Modes

Program Lock Bits			Protection Type
	LB1	LB2	
1	U	U	No program lock features
2	P	U	Further programming of the EPROM is disabled
3	P	P	Same as mode 2, also verify is disabled

U: unprogrammed, P: programmed

Reading the Signature Bytes :

The GMS97x51/52 signature bytes in locations 030_H and 031_H, the GMS97x54/56/58 signature bytes in locations 030_H and 060_H. To read these bytes follow the procedure for EPROM verify, except that P3.6 and P3.7 need to be pulled to a logic low. The values are:

Location	Device	Contents
30H	All	E0H
31H	GMS97C51/L51	73H
	GMS97C52/L52	71H
60H	GMS97C54/L54	54H
	GMS97C56/L56	56H
	GMS97C58/L58	58H

Program / Verify algorithms

Any algorithm in agreement with the conditions listed in Table 11, and which satisfies the timing specifications is suitable.

Table 11. EPROM programming modes

MODE	RST	PSEN	ALE/PROG	EA/V _{PP}	P2.7	P2.6	P3.7	P3.6
Read Signature	1	0	1	1	0	0	0	0
Program Code Data	1	0	0	V _{PP}	1	0	1	1
Verify Code Data	1	0	1	1	0	0	1	1
Program encryption table	1	0	0	V _{PP}	1	0	1	0
Program security bit 1	1	0	0	V _{PP}	1	1	1	1
Program security bit 2	1	0	0	V _{PP}	1	1	0	0

Notes :

- "0" = Valid low for that pin, "1" = valid high for that pin.
- V_{pp} = 12.75V ± 0.25V
- V_{cc} = 5V ± 10% during programming and verification.
- ALE/PROG receives 25 (10 for GMS97x54/56/58) programming pulses while V_{pp} is held at 12.75. Each programming pulse is low for 100us (± 10us) and high for a minimum of 10us.

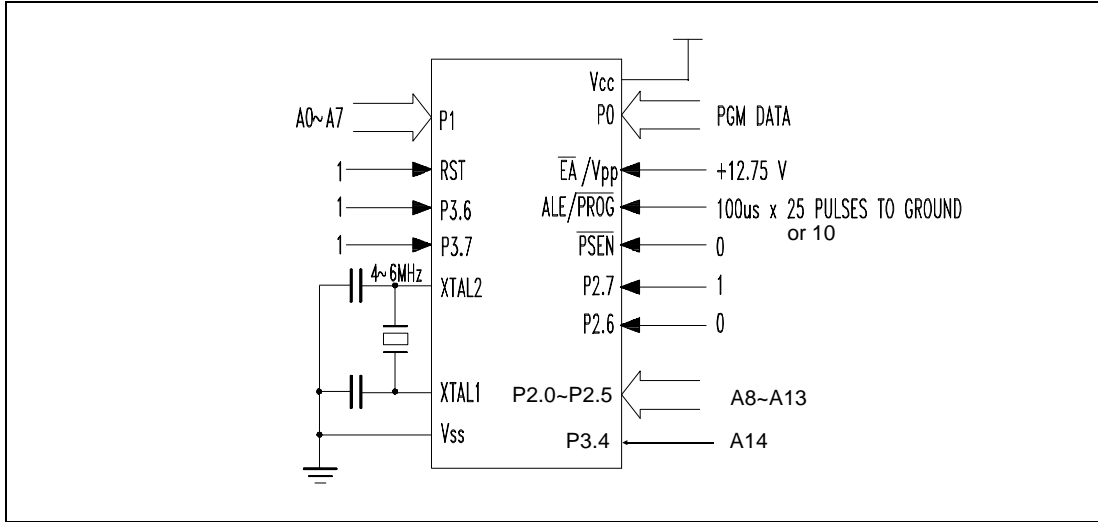


Figure 12
Programming Configuration

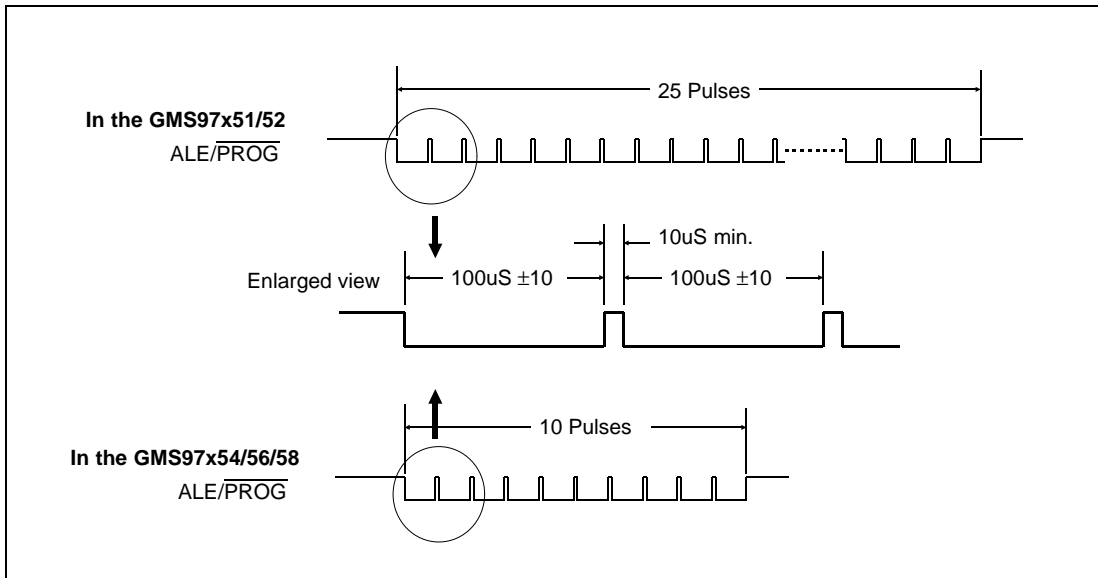


Figure 13
PROG Waveform

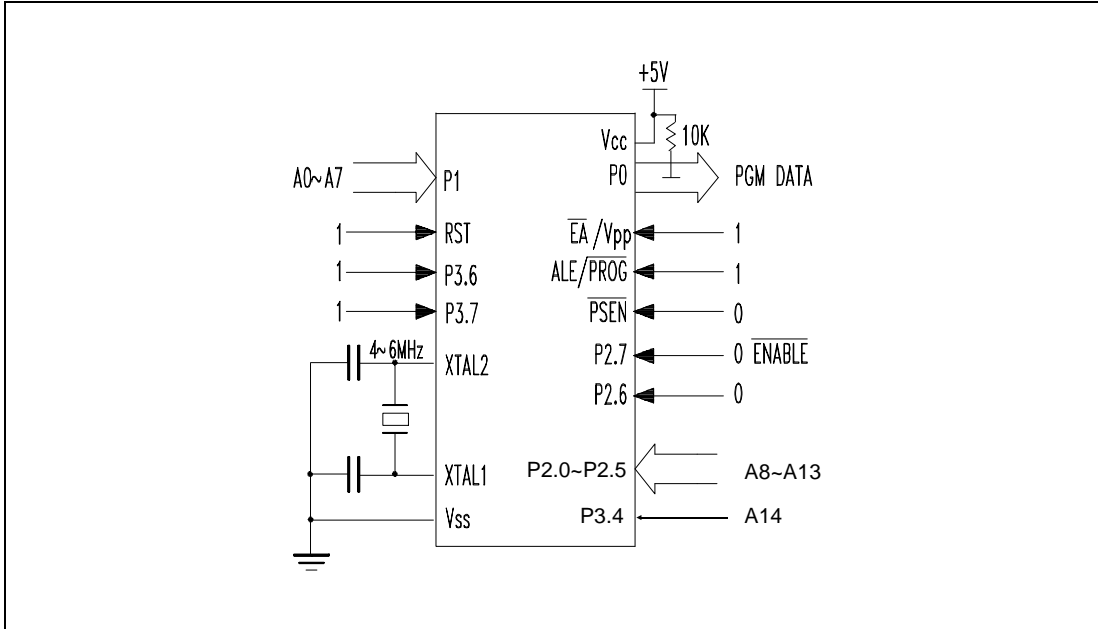


Figure 14
Program Verification

EPROM Programming and Verification Characteristics

$T_A = 21^\circ\text{C}$ to 27°C $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ (See Figure 15)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Programming supply voltage	V_{PP}	12.5	13.0	V
Programming supply current	I_{PP}	-	50	mA
Oscillator frequency	$1/t_{CLCL}$	4	6	MHz
Address setup to PROG low	t_{AVGL}	$48t_{CLCL}$	-	-
Address hold after PROG	t_{GHAX}	$48t_{CLCL}$	-	-
Data setup to PROG low	t_{DVGL}	$48t_{CLCL}$	-	-
Data setup after PROG	t_{GHDX}	$48t_{CLCL}$	-	-
P2.7 (ENABLE) high to V_{PP}	t_{EHS}	$48t_{CLCL}$	-	-
V_{PP} setup to PROG low	t_{SHGL}	10	-	us
V_{PP} hold after PROG	t_{GHSL}	10	-	us
PROG width	t_{GLGL}	90	110	us
Address to data valid	t_{AVQL}	-	$48t_{CLCL}$	-
ENABLE low to data valid	t_{ELQZ}	-	$48t_{CLCL}$	-
Data float after ENABLE	t_{EHQZ}	0	$48t_{CLCL}$	-
PROG high to PROG low	t_{GHGL}	10		us

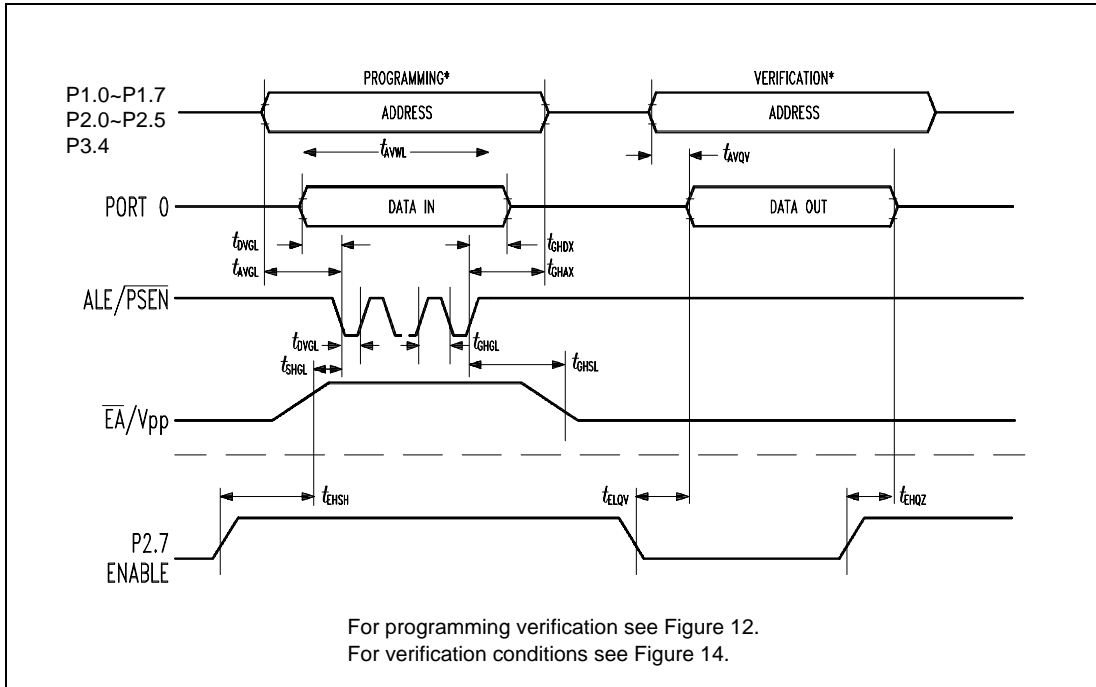
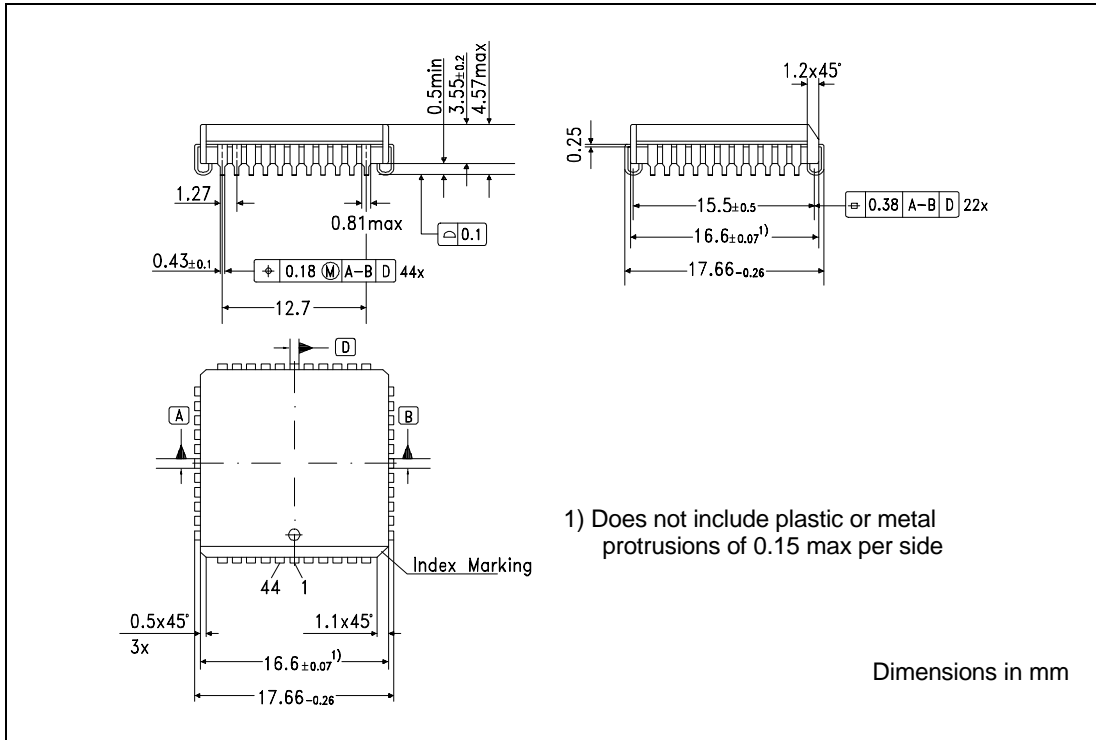


Figure 15
EPROM Programming and Verification

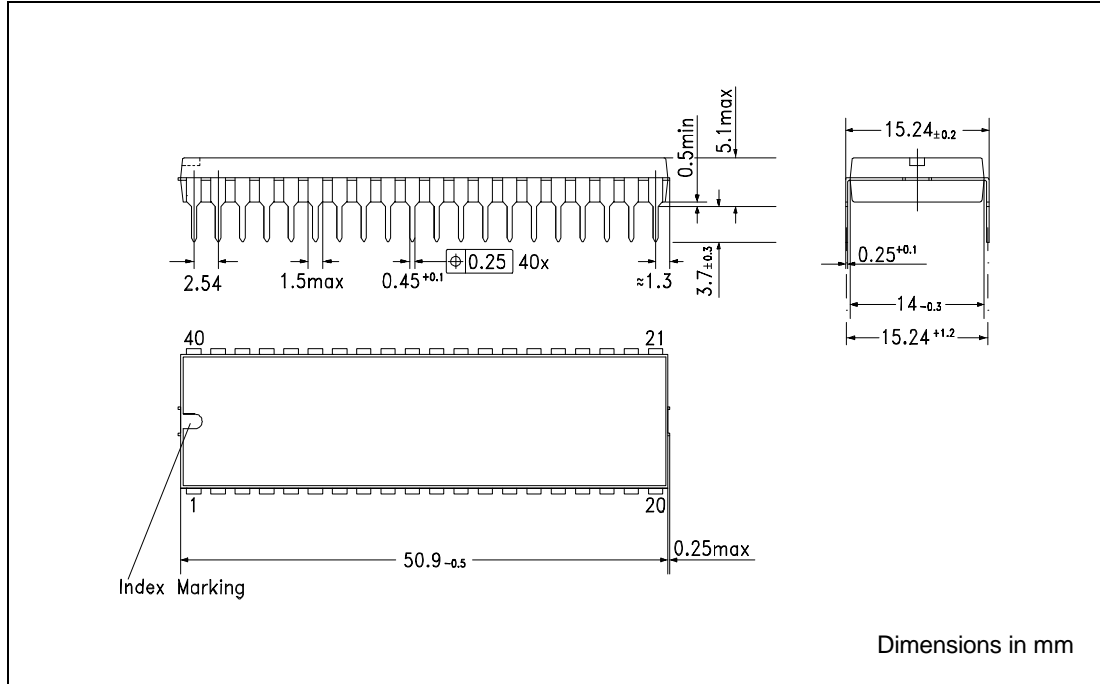
**Plastic Package, P-LCC-44-SMD
(Plastic Leaded Chip-Carrier)**



SMD = Surface Mounted Device

SMD = Surface Mounted Device

**Plastic Package, P-DIP-40
(Plastic Dual in-Line Package)**



**Plastic Package, P-MQFP-44(SMD)
(Plastic Metric Quad Flat Package)**

