ISO 9001 Registered

POWER MANAGEMENT

3.0V/3.3V Microprocessor Supervisors with Battery Backup Switch

The IMP690T/S/R, IMP802LT/S/R, IMP804T/S/R and IMP805T/S/R simplify power supply monitoring and control in 3V/3.3V microprocessor and battery powered systems. The circuits monitor and control the power supplied to memory, microcontrollers and microprocessors. Each circuit implements four functions: reset control, watchdog monitoring, battery-backup switching and power-failure monitoring. In addition to microprocessor reset under brownout, power-up and power-down conditions, these devices provide battery-backup switching to maintain control in power-loss situations.

The important features of these four functions are:

a) 200msec reset time

b) 1.6 second watchdog timer with disable function

c) Three threshold options: 3.075V (T devices), 2.925 (S devices) and 2.625V(R devices)

d) SPDT (single-pole, double-throw) 40Ω PMOS switch connects back-up power to RAM if V_{CC} fails

e) 1.25V threshold power-loss comparator for general purpose voltage monitoring

The auxiliary power-fail comparator with precision 1.25V reference acts as an undervoltage detector. All IMP802/804 devices have power-fail accuracy of ±2%. The IMP690/805 power fail threshold accuracy is ±4%.

The IMP690 reset is active LOW and the IMP80x reset is active HIGH. All parts are available in 8-pin DIP and SO packages. The IMP690T/S/R, IMP805T/S/R, IMP802T/S/R, and IMP804T/S/R (-1) devices have pinouts that match the Maxim MAX690T/S/R, MAX805T/S/R, MAX802T/S/R, and MAX804T/S/R supervisors. Backup battery switching and watchdog operation match IMP's 5V IMP690A/692A/805L/802L/M supervisors.
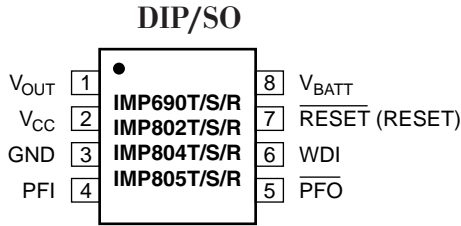
Key Features

◆ **Design Improvement over Maxim MAX690/802/804/805**

◆ **60µA Maximum supply current (3.6V)**

◆ **Three precision supply-voltage monitor options**
  — **3.075V (T devices)**
  — **2.925V (S devices)**
  — **2.625V (R devices)**

◆ **RESET and $\overline{RESET}$ outputs**
  — **200msec reset time**

◆ **Battery-backup power switch on-chip**
  — **Power CMOS RAM, CMOS µP or logic**

◆ **Watchdog timer: 1.6sec timeout**

◆ **Independent 1.25V Power Fail threshold detector**
  — **Power-fail warning, low battery detection**
  — **Monitor supplies other than 3.0V/3.3V**
  — **IMP690 and IMP805: ± 4 % PFI accuracy**
  — **IMP802 and IMP804: ± 2 % PFI accuracy**

◆ **Small 8-pin SO and DIP packages**

Applications

◆ Embedded control systems

◆ Battery-operated systems

◆ Intelligent instruments

◆ Wireless communication systems

◆ PDAs and handheld equipment

◆ µP/µC power supply monitoring

◆ CMOS memory backup

Selection Guide

IMP Part	Reset Threshold	Reset Polarity		Reset Accuracy	PFI Accuracy	Watchdog Timer	Backup-Battery Switch
		Low	High				
IMP690T	3.075V	●		±75mV	±4% (±50mV)	●	●
IMP805T			●				
IMP802T	3.075V	●		±60mV	±2% (±25mV)	●	●
IMP804T			●				
IMP690S	2.925V	●		±75mV	±4% (±50mV)	●	●
IMP805S			●				
IMP802S	2.925V	●		±60mV	±2% (±25mV)	●	●
IMP804S			●				
IMP690R	2.625V	●		±75mV	±4% (±50mV)	●	●
IMP805R			●				
IMP802R	2.625V	●		±60mV	±2% (±25mV)	●	●
IMP804R			●				

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Pin Configuration

DIP/SO

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         ┌───────────┐
VOUT  1 │•          8│ VBATT
VCC   2 │ IMP690T/S/R 7│ RESET (RESET)
         │ IMP802T/S/R │
GND   3 │ IMP804T/S/R 6│ WDI
         │ IMP805T/S/R │
PFI   4 │           5│ PFO
         └───────────┘
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( ) IMP804T/S/R and IMP805T/S/R only.

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Ordering Information

Part Number	Reset Threshold (V)	Temperature Range	Pins-Package
IMP690RCPA-1	2.625	0°C to 70°C	8-pin, DIP
IMP690RCSA-1	2.625	0°C to 70°C	8-pin, SO
IMP690REPA-1	2.625	−40°C to 85°C	8-pin, DIP
IMP690RESA-1	2.625	−40°C to 85°C	8-pin, SO
IMP690SCPA-1	2.925	0°C to 70°C	8-pin, DIP
IMP690SCSA-1	2.925	0°C to 70°C	8-pin, SO
IMP690SEPA-1	2.925	−40°C to 85°C	8-pin, DIP
IMP690SESA-1	2.925	−40°C to 85°C	8-pin, SO
IMP690TCPA-1	3.075	0°C to 70°C	8-pin, DIP
IMP690TCSA-1	3.075	0°C to 70°C	8-pin, SO
IMP690TEPA-1	3.075	−40°C to 85°C	8-pin, DIP
IMP690TESA-1	3.075	−40°C to 85°C	8-pin, SO
IMP802RCPA-1	2.625	0°C to 70°C	8-pin, DIP
IMP802RCSA-1	2.625	0°C to 70°C	8-pin, SO
IMP802REPA-1	2.625	−40°C to 85°C	8-pin, DIP
IMP802RESA-1	2.625	−40°C to 85°C	8-pin, SO
IMP802SCPA-1	2.925	0°C to 70°C	8-pin, DIP
IMP802SCSA-1	2.925	0°C to 70°C	8-pin, SO
IMP802SEPA-1	2.925	−40°C to 85°C	8-pin, DIP
IMP802SESA-1	2.925	−40°C to 85°C	8-pin, SO
IMP802TCPA-1	3.075	0°C to 70°C	8-pin, DIP
IMP802TCSA-1	3.075	0°C to 70°C	8-pin, SO
IMP802TEPA-1	3.075	−40°C to 85°C	8-pin, DIP
IMP802TESA-1	3.075	−40°C to 85°C	8-pin, SO
IMP804RCPA-1	2.625	0°C to 70°C	8-pin, DIP
IMP804RCSA-1	2.625	0°C to 70°C	8-pin, SO
IMP804REPA-1	2.625	−40°C to 85°C	8-pin, DIP
IMP804RESA-1	2.625	−40°C to 85°C	8-pin, SO
IMP804SCPA-1	2.925	0°C to 70°C	8-pin, DIP
IMP804SCSA-1	2.925	0°C to 70°C	8-pin, SO
IMP804SEPA-1	2.925	−40°C to 85°C	8-pin, DIP
IMP804SESA-1	2.925	−40°C to 85°C	8-pin, SO
IMP804TCPA-1	3.075	0°C to 70°C	8-pin, DIP
IMP804TCSA-1	3.075	0°C to 70°C	8-pin, SO
IMP804TEPA-1	3.075	−40°C to 85°C	8-pin, DIP
IMP804TESA-1	3.075	−40°C to 85°C	8-pin, SO
IMP805RCPA-1	2.625	0°C to 70°C	8-pin, DIP
IMP805RCSA-1	2.625	0°C to 70°C	8-pin, SO
IMP805REPA-1	2.625	−40°C to 85°C	8-pin, DIP
IMP805RESA-1	2.625	−40°C to 85°C	8-pin, SO
IMP805SCPA-1	2.925	0°C to 70°C	8-pin, DIP
IMP805SCSA-1	2.925	0°C to 70°C	8-pin, SO
IMP805SEPA-1	2.925	−40°C to 85°C	8-pin, DIP
IMP805SESA-1	2.925	−40°C to 85°C	8-pin, SO
IMP805TCPA-1	3.075	0°C to 70°C	8-pin, DIP
IMP805TCSA-1	3.075	0°C to 70°C	8-pin, SO
IMP805TEPA-1	3.075	−40°C to 85°C	8-pin, DIP
IMP805TESA-1	3.075	−40°C to 85°C	8-pin, SO

Pin Number		Name	Function
IMP690 IMP802	IMP804 IMP805		
1	1	V$_{OUT}$	Voltage supply for RAM or other circuitry. When V$_{CC}$ is above the reset threshold, V$_{OUT}$ connects to V$_{CC}$ through a P-channel MOS device. If V$_{CC}$ falls below the reset threshold, V$_{OUT}$ is connected to the higher of V$_{BATT}$ or V$_{CC}$. Connect to V$_{CC}$ if no battery is used.
2	2	V$_{CC}$	Main power supply input.
3	3	GND	Ground.
4	4	PFI	Power failure monitor input. PFI is connected to the internal power fail comparator that is referenced to 1.25V. When PFI is less than the power-fail-input threshold, V$_{PFT}$, $\overline{PFO}$ goes LOW; otherwise, $\overline{PFO}$ remains HIGH. If this feature is unused, the PFI pin should be connected to GND or V$_{OUT}$.
5	5	$\overline{PFO}$	Power-fail output. $\overline{PFO}$ is active LOW whenever the PFI pin is less than 1.25V. Leave open if unused.
6	6	WDI	Watchdog input. If WDI remains HIGH or LOW for 1.6 seconds, the internal watchdog timer triggers a reset. The watchdog timer clears when reset is asserted or WDI sees a rising or falling edge. If WDI is held HIGH or LOW for longer than the watchdog timeout period, typically 1.6 seconds, reset becomes active for the reset pulse width time, t$_{RS}$, of 140ms minimum. If WDI is left floating or connected to a high impedance three-state buffer the watchdog function is disabled.
7	——	$\overline{RESET}$	Active-LOW $\overline{RESET}$ output. Pulses LOW for 200ms when the watchdog timer runs out. It remains LOW whenever V$_{CC}$ is below the reset threshold. It remains LOW for 200msec after either V$_{CC}$ rises above the reset threshold or the watchdog triggers a reset.
——	7	RESET	Active-HIGH RESET output. The inverse of $\overline{RESET}$.
8	8	V$_{BATT}$	Auxiliary power or backup-battery input. This input has hysteresis to prevent rapid toggling between V$_{CC}$ and V$_{BATT}$. When V$_{CC}$ rises above the reset threshold, V$_{OUT}$ reconnects to V$_{CC}$. V$_{BATT}$ should be connected to V$_{CC}$ if the function is not used. V$_{BATT}$ may not exceed V$_{CC}$ by more than 0.6V.

Pin Terminal Voltage with Respect to Ground
    V$_{CC}$ . . . . −0.3V to 6.0V
    V$_{BATT}$ . . . . −0.3V to 6.0V
    All Other Inputs* . . . . −0.3V to (V$_{CC}$ + 0.3V)
Input Current at V$_{CC}$ 200mA
Input Current at V$_{BATT}$ 50mA
Input Current at GND 20mA
Output Current:
    V$_{OUT}$ . . . . Short circuit protected for up to 10 sec
    All Other Inputs 20mA
    Rate of Rise: V$_{BATT}$ and V$_{CC}$ 100V/µs

Continuous Power Dissipation
    Plastic DIP (derate 9mW/°C above 70°C) . . . 800mW
    SO (derate 5.9mW/°C above 70°C) 500mW

Storage Temperature Range . . . . −65°C to 160°C
Lead Temperature Soldering, (10 sec) . . . . 300°C

The input voltage limits on PFI and WDI may be exceeded if the current is limited to less than 10mA

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.

Electrical Characteristics

Unless otherwise noted, V_{CC} = 3.17V to 5.5V for the IMP690T/802T/804T/805T, V_{CC} = 3.02V to 5.5V for the IMP690S/802S/804S/805S, V_{CC} = 2.72V to 5.5V for the IMP690R/802R/804R/805R, V_{BATT} = 3.6V; and T_A= T_{MIN} to T_{MAX}. Typical values at T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating Temperature Range		IMP690_C_ _ IMP802_C_ _, IMP804_C_ _, IMP805_C_ _	0		+70	°C
		IMP690_E_ _ IMP802_E_ _, IMP804_E_ _, IMP805_E_ _	−40		+85	
Operating Voltage Range, V_{CC}, V_{BATT}		Note 1	1.1		5.5	V
V_{OUT}		I_{OUT} = 5mA	V_{CC} − 0.025	V_{CC} − 0.015		V
		I_{OUT} = 50mA	V_{CC} − 0.25	V_{CC} − 0.15		
		I_{OUT} = 250µA, V_{CC} > 2.5V, V_{BATT} < V_{CC} − 0.2V		V_{CC} − 0.002		
V_{OUT} in Battery- Backup Mode		I_{OUT} = 250µA, V_{BATT} > 2.3V, V_{CC} < V_{BATT} − 0.2V	V_{BATT} − 0.1	V_{BATT} − 0.01		V
		I_{OUT} = 1mA, V_{BATT} > 2.3V, V_{CC} < V_{BATT} − 0.2V		V_{BATT} − 0.02		
Supply Current Excluding I_{OUT}	I_S	V_{CC} < 3.6V		25	60	µA
		V_{CC} < 5.5V		35	80	
Supply Current in Battery Backup Mode	I_S	Note 2			10	µA
Battery Leakage Current		5.5V > V_{CC} > V_{BATT} + 0.2V. Note 3 & 4, T_A = 25°C	−20		20	nA
Reset Threshold Note 5	V_{RST}	IMP690T, IMP805T, V_{CC} falling	3.00	3.075	3.15	V
		IMP690T, IMP805T, V_{CC} rising	3.00	3.085	3.17	
		IMP690S, IMP805S, V_{CC} falling	2.85	2.925	3.00	
		IMP690S, IMP805S, V_{CC} rising	2.85	2.935	3.02	
		IMP690R, IMP805R, V_{CC} falling	2.55	2.625	2.70	
		IMP690R, IMP805R, V_{CC} rising	2.55	2.635	2.72	
		IMP802T, IMP804T, V_{CC} falling	3.00	3.075	3.12	
		IMP802T, IMP804T, V_{CC} rising	3.00	3.085	3.14	
		IMP802S, IMP804S, V_{CC} falling	2.88	2.925	3.00	
		IMP802S, IMP804S, V_{CC} rising	2.88	2.935	3.02	
		IMP802R, IMP804R, V_{CC} falling	2.59	2.625	2.70	
		IMP802R, IMP804R, V_{CC} rising	2.59	2.635	2.72	
Reset Pulse Width	t_{RS}		140	200	280	ms
$\overline{RESET}$ Output Voltage	V_{OH}	I_{SOURCE} = 800µA, 4.5V < V_{CC} < 5.5V	V_{CC} − 1.5V			V
	V_{OL}	I_{SINK} = 3.2mA, 4.5V < V_{CC} < 5.5V			0.4	
	V_{OH}	I_{SOURCE} = 500µA, $V_{RST\ (MAX)}$ < V_{CC} < 3.6V	0.8V_{CC}			
	V_{OL}	I_{SINK} = 1.2mA, $V_{RST\ (MAX)}$ < V_{CC} < 3.6V			0.3	
	V_{OL}	I_{SINK} = 50µA, V_{CC} = 1.1V			0.3	
	V_{OL}	I_{SINK} = 100µA, V_{CC} = 1.2V			0.3	

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Electrical Characteristics

Unless otherwise noted, V_{CC} = 3.17V to 5.5V for the IMP690T/802T/804T/805T, V_{CC} = 3.02V to 5.5V for the IMP690S/802S/804S/805S, V_{CC} = 2.72V to 5.5V for the IMP690R/802R/804R/805R, V_{BATT} = 3.6V; and T_A = T_{MIN} to T_{MAX}. Typical values at T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RESET Output Voltage	V_{OH}	I_{SOURCE} = 800µA, 4.5V < V_{CC} < 5.5V	V_{CC} − 1.5V			V
	V_{OL}	I_{SINK} = 3.2mA, 4.5V < V_{CC} < 5.5V			0.4	
	V_{OH}	I_{SOURCE} = 500µA, $V_{RST (MAX)}$ < V_{CC} < 3.6V	$0.8V_{CC}$			
	V_{OL}	I_{SINK} = 1.2mA, $V_{RST (MAX)}$ < V_{CC} < 3.6V			0.3	
Watchdog Timeout	t_{WD}	V_{CC} < 3.6V	1.12	1.60	2.24	s
WDI Pulse Width	t_{WP}		100	20		ns
WDI Input Current		WDI = V_{CC}			150	µA
		WDI = 0V	−150			
WDI Input Threshold	V_{IH}	Logic HIGH	$0.7V_{CC}$			V
	V_{IL}	Logic LOW			$0.3V_{CC}$	
PFI Input Threshold	V_{PFT}	V_{CC} = 3.6V, IMP690, IMP805	1.187	1.25	1.287	V
		V_{CC} = 3.6V, IMP802, IMP804	1.212	1.25	1.262	
PFI Input Current			−25	0.01	25	nA
$\overline{PFO}$ Output Current	V_{OH}	I_{SOURCE} = 800µA, 4.5V < V_{CC} < 5.5V	V_{CC} − 1.5V			V
	V_{OL}	I_{SINK} = 3.2mA, 4.5V < V_{CC} < 5.5V			0.4	
	V_{OH}	I_{SOURCE} = 500µA, $V_{RST (MAX)}$ < V_{CC} < 4.5V	$0.8V_{CC}$			
	V_{OL}	I_{SINK} = 1.2mA, $V_{RST (MAX)}$ < V_{CC} < 4.5V			0.3	

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Notes: 1. The following are tested at V_{BATT} = 3.6V and V_{CC} = 5.5V: V_{CC} supply current, watchdog functionality, logic input leakage, PFI functionality, and the $\overline{RESET}$ and RESET states. The state of $\overline{RESET}$ or RESET and $\overline{PFO}$ is tested at V_{CC} = $V_{CC (MIN)}$.

2. Tested at V_{BATT} = 2.8V, V_{CC} = 2.3V and 0V

3. Leakage current into the battery is tested under the following worst-case conditions: V_{CC} = 5.5V, V_{BATT} = 1.8V, and at V_{CC} = 1.5V, V_{BATT} = 1.0V.

4. "-" equals the battery-charging current and "+" equals the battery-discharging current.

5. The reset threshold tolerance is wider for V_{CC} rising than for V_{CC} falling to accommodate the 30mV typical hysteresis, which prevents internal oscillation.

Application Information

The IMP690T/S/R, IMP802T/S/R, IMP804T/S/R and IMP805T/S/R monitor system power supplies, generate power failure signals and issue reset signals to the system controller. Four key functions are provided:

1. A battery backup switch for CMOS processors, logic or memory.

2. A reset signal if the watchdog timer is not reset by the system processor.

3. A Reset signal during power-up, power-down and brownout conditions.

4. An independent 1.25V threshold comparator for power-fail warning, low battery detection, or for monitoring voltages other than 3.0/3.3V.

Reset Output

It is important to initialize a microprocessor to a known state. The IMP690T/S/R, IMP802T/S/R, IMP804T/S/R and IMP805T/S/R devices assert a reset during power-up, power-down and brownout conditions. The reset output of these supervisory circuits send a reset pulse to the microprocessor in response to power-up, power-down/power-loss or a watchdog time-out. The reset pulse width, t_{RS}, is typically around 200msec. The reset signal is active LOW for the IMP690/IMP802 and active HIGH for the IMP804/IMP805. The watchdog timer can also generate a reset signal.
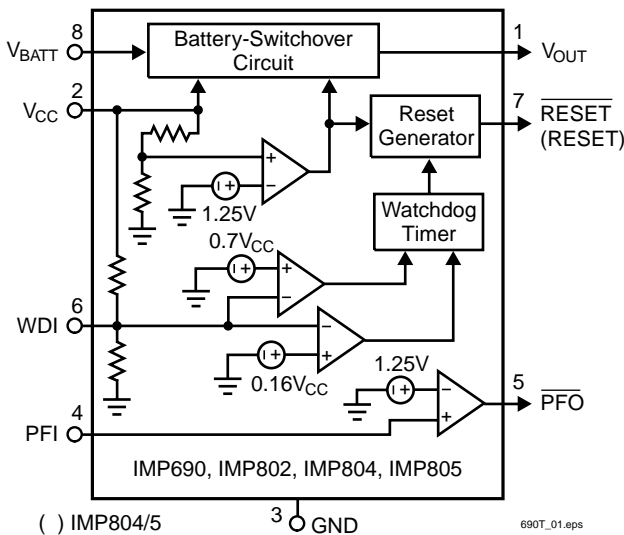
$\overline{\text{RESET}}$ guaranteed to be a logic LOW for 0V< V_{CC} < V_{RST} if V_{BATT} is greater than 1.1V. $\overline{\text{RESET}}$ is valid for V_{CC} >1.1V if no backup battery is used.

Once V_{CC} is above the reset threshold, $\overline{\text{RESET}}$ remains LOW for the reset timeout period, typically 200msec, and then returns HIGH. Timing is shown in *Figure 2*.

Power-up reset occurs when a rising V_{CC} reaches the reset threshold, forcing a reset condition in which the reset output is asserted for the duration of t_{RS}.

Power-loss or "brown-out" reset occurs when V_{CC} dips below the reset threshold resulting in a reset assertion for the duration of t_{RS}. The reset signal remains asserted as long as V_{CC} is between V_{RT} and 1.1V, the lowest V_{CC} for which these devices can provide a guaranteed logic-low output.

A watchdog timeout reset occurs when a logic "1" or logic "0" is continuously applied to the WDI pin for a period that exceeds the watchdog timeout period (typically 1.6 seconds). After the duration of the reset interval, the watchdog timer starts a new 1.6-second timing interval.

The system microprocessor must reset the internal watchdog timer by changing states at the WDI input. If the WDI pin is held either HIGH or LOW, a reset pulse will be triggered every 1.8 seconds (the 1.6-second timing interval plus the 200msec reset pulse width, t_{RS}).
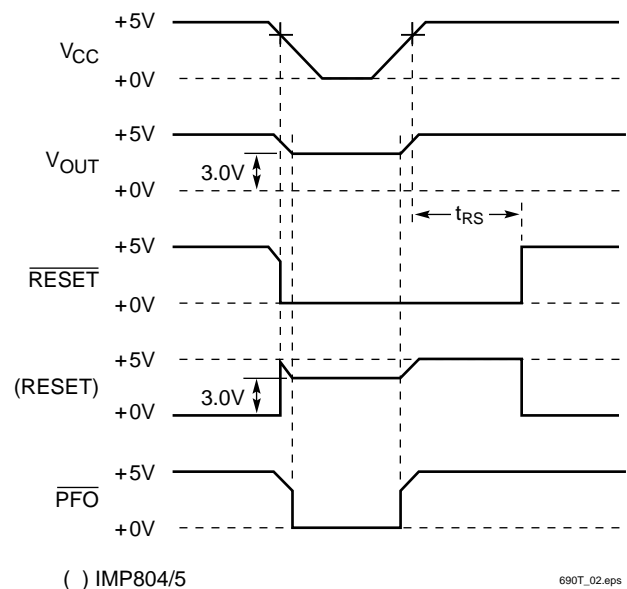

Figure 1. Block Diagram

Figure 2. Timing Diagram

Watchdog Input

The watchdog circuit monitors microprocessor activity. It can be used to insure that the microprocessor is in a continually responsive state by requiring that the WDI pin be toggled every 1.6 seconds typically. If the WDI pin is not toggled within the 1.6 second, a reset pulse will be asserted.

If WDI is tied HIGH or LOW, a reset pulse is triggered every 1.8 seconds ($t_{WD} + t_{RS}$).

The IMP690/802/804/805 watchdog function can be disabled by open circuiting the WDI pin and allowing it to float.
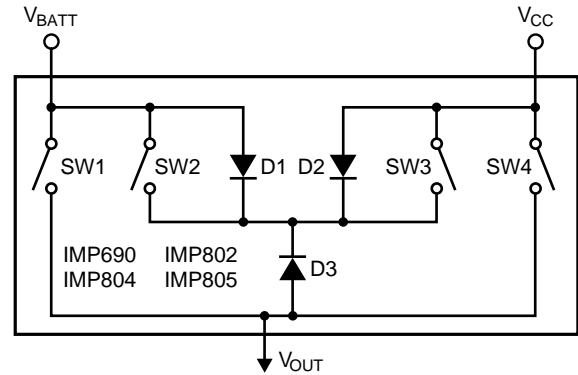
Backup-Battery Switchover

A power loss can be made less severe if the system RAM contents are preserved or other critical low power logic is powered. This is achieved in the IMP690/802/804/805 by switching from the failed V_{CC} to an alternate power source connected at V_{BATT} when V_{CC} is less than the reset threshold voltage ($V_{CC} < V_{RST}$), and V_{CC} is less than V_{BATT}.

Switchover Reference	Conditions for $V_{OUT} = V_{BATT}$
RESET Threshold	$V_{BATT} > V_{CC}$ AND $V_{CC} < V_{RST}$

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For IMP devices, whenever $V_{CC} > V_{RST}$, V_{OUT} is switched back to V_{CC}. There is hysteresis in the switchover circuit.

The V_{OUT} pin is normally connected to V_{CC} through a 3Ω PMOS switch but a brownout or loss of V_{CC} will cause a switchover to V_{BATT} by means of a 40Ω PMOS switch. Although both conditions ($V_{CC} < V_{RST}$ and $V_{CC} < V_{BATT}$) must occur for the switchover to V_{BATT} to occur, V_{OUT} will be switched back to V_{CC} when V_{CC} exceeds V_{RST} irrespective of the voltage at V_{BATT}. It should be noted that an internal device diode (D1 in *Figure 3*) would be forward biased if V_{BATT} exceeds V_{CC} by more than a diode drop when V_{CC} is switched to V_{OUT}. Because of this, it is recommended that V_{BATT} be no greater than $V_{RST} + 0.6V$ (see *Table 2*).

CONDITION	SW1/SW2	SW3/SW4
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and $V_{CC} > V_{BATT}$	Open	Closed
V_{CC} < Reset Threshold and $V_{CC} < V_{BATT}$	Closed	Open

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Figure 3. Internal device configuration of battery switch-over function

Backup Power Sources

Battery voltage selection is important to insure that the battery does not discharge through the parasitic device diode D1 (see *Figure 3*) when V_{CC} is less than V_{BATT} and $V_{CC} > V_{RST}$.

Table 2: Maximum Battery Voltages

| Part No.	Maximum Battery Voltage
IMP690/802/804/805T	$V_{RST\ (MAX)}$ + 0.6V (3.75V)
IMP690/802/804/805S	$V_{RST\ (MAX)}$ + 0.6V (3.525V)
IMP690/802/804/805R	$V_{RST\ (MAX)}$ + 0.6V (3.225V)

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Power-Fail Comparator

The Power Fail feature is an independent voltage monitoring function that can be used for any number of monitoring activities. For example, the PFI function can provide an early sensing of power supply failure by sensing the unregulated DC voltage ahead of the regulated supply sensing seen by the backup-battery switchover circuitry.

The PFI pin is compared to a 1.25V internal reference. If the voltage at the PFI pin is less the power fail threshold, V_{PFT}, the $\overline{PFO}$ goes LOW. The PFI input voltage is often set by a voltage divider from the monitored supply.
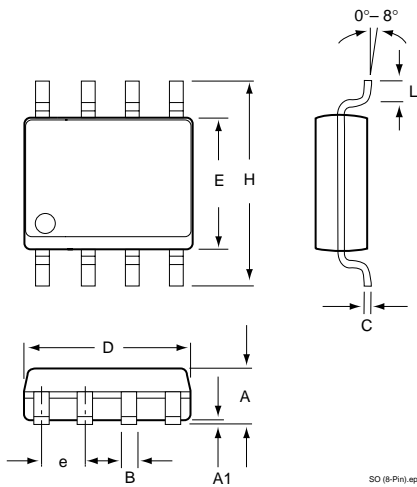
The PFI comparator operates without hysteresis.

Package Dimensions

Plastic DIP (8-Pin)

Plastic DIP (8-Pin)a.eps

SO (8-Pin)

SO (8-Pin).eps
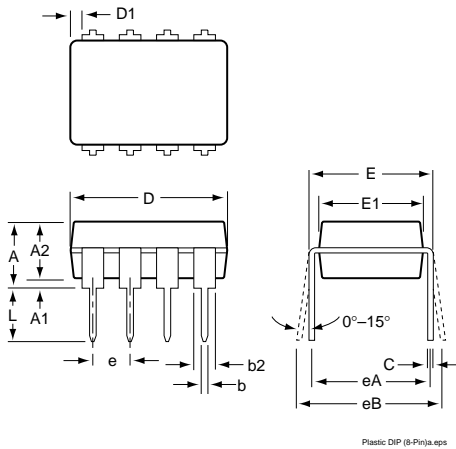
	Inches		Millimeters	
	Min	**Max**	**Min**	**Max**
Plastic DIP (8-Pin)*				
A	——	0.210	——	5.33
A1	0.015	——	0.38	——
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.36	0.56
b2	0.045	0.070	1.14	1.78
b3	0.030	0.045	0.80	1.14
D	0.355	0.400	9.02	10.16
D1	0.005	——	0.13	——
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	——	2.54	
eA	0.300	——	7.62	
eB	——	0.430	——	10.92
eC	——	0.060		
L	0.115	0.150	2.92	3.81
SO (8-Pin)**				
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
D	0.189	0.197	4.80	5.00

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JEDEC Drawing MS-001BA
**JEDEC Drawing MS-012AA*

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