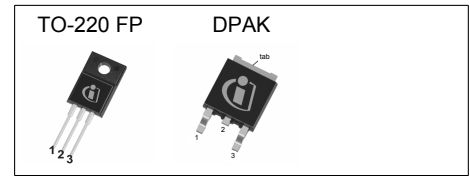


MOSFET

600V CoolMOS™ CE Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ CE is a price-performance optimized platform enabling to target cost sensitive applications in Consumer and Lighting markets by still meeting highest efficiency standards. The new series provides all benefits of a fast switching Superjunction MOSFET while not sacrificing ease of use and offering the best cost down performance ratio available on the market.



Features

- Extremely low losses due to very low FOM $R_{DS(on)} \cdot Q_g$ and E_{oss}
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for standard grade applications

Applications

PFC stages, hard switching PWM stages and resonant switching stages for e.g. PC Silverbox, Adapter, LCD & PDP TV and indoor lighting.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.



Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|----------------------|-------|------|
| $V_{DS} @ T_{j,max}$ | 650 | V |
| $R_{DS(on),max}$ | 650 | mΩ |
| I_d | 9.9 | A |
| $Q_{g,typ}$ | 20.5 | nC |
| $I_{D,pulse}$ | 19 | A |
| $E_{oss@400V}$ | 1.9 | μJ |

| Type / Ordering Code | Package | Marking | Related Links |
|----------------------|-------------------|----------|----------------|
| IPA60R650CE | PG-TO 220 FullPAK | 60S650CE | see Appendix A |
| IPD60R650CE | PG-TO 252 | | |

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|---------------|--------|------|------------|------------------|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 9.9 6.2 | A | $T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$ |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | - | - | 19 | A | $T_C=25^\circ\text{C}$ |
| Avalanche energy, single pulse | E_{AS} | - | - | 133 | mJ | $I_D=1.3\text{A}$; $V_{DD}=50\text{V}$; see table 11 |
| Avalanche energy, repetitive | E_{AR} | - | - | 0.20 | mJ | $I_D=1.3\text{A}$; $V_{DD}=50\text{V}$; see table 11 |
| Avalanche current, repetitive | I_{AR} | - | - | 1.3 | A | - |
| MOSFET dv/dt ruggedness | dv/dt | - | - | 50 | V/ns | $V_{DS}=0\dots480\text{V}$ |
| Gate source voltage (static) | V_{GS} | -20 | - | 20 | V | static; |
| Gate source voltage (dynamic) | V_{GS} | -30 | - | 30 | V | AC ($f>1\text{ Hz}$) |
| Power dissipation (Non FullPAK) TO-251 | P_{tot} | - | - | 82 | W | $T_C=25^\circ\text{C}$ |
| Storage temperature | T_{stg} | -40 | - | 150 | $^\circ\text{C}$ | - |
| Operating junction temperature | T_j | -40 | - | 150 | $^\circ\text{C}$ | - |
| Continuous diode forward current | I_S | - | - | 7 | A | $T_C=25^\circ\text{C}$ |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | - | - | 19 | A | $T_C=25^\circ\text{C}$ |
| Reverse diode dv/dt ³⁾ | dv/dt | - | - | 15 | V/ns | $V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 9 |
| Maximum diode commutation speed | di/dt | - | - | 500 | A/ μs | $V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 9 |
| Power dissipation (FullPAK) TO-220FP | P_{tot} | - | - | 28 | W | $T_C=25^\circ\text{C}$ |
| Mounting torque (FullPAK) TO-220FP | - | - | - | 50 | Ncm | M2.5 screws |
| Insulation withstand voltage for TO-220FP | V_{ISO} | - | - | 2500 | V | V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$ |

2 Thermal characteristics

Table 3 Thermal characteristics (FullPAK) TO-220FP

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------|--------|------|------|--------------------|-------------------------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 4.5 | $^\circ\text{C/W}$ | - |
| Thermal resistance, junction - ambient | R_{thJA} | - | - | 80 | $^\circ\text{C/W}$ | leaded |
| Soldering temperature, wavesoldering only allowed at leads | T_{sold} | - | - | 260 | $^\circ\text{C}$ | 1.6mm (0.063 in.) from case for 10s |

¹⁾ Limited by $T_{j,max}$. TO252 equivalent, Maximum duty cycle $D=0.50$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch with identical R_θ

Table 4 Thermal characteristics TO-252

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | 1.52 | °C/W | - |
| Thermal resistance, junction - ambient | R_{thJA} | - | - | 62 | °C/W | device on PCB, minimal footprint |
| Thermal resistance, junction - ambient for SMD version | R_{thJA} | - | 35 | 45 | °C/W | Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling. |
| Soldering temperature, wave & reflow soldering allowed | T_{sold} | - | - | 260 | °C | reflow MSL1 |

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 5 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|--------------|------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 600 | - | - | V | $V_{GS}=0V, I_D=0.25mA$ |
| Gate threshold voltage | $V_{(GS)th}$ | 2.5 | 3.0 | 3.5 | V | $V_{DS}=V_{GS}, I_D=0.2mA$ |
| Zero gate voltage drain current | I_{DSS} | - | - | 1 | μA | $V_{DS}=600, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=600, V_{GS}=0V, T_j=150^\circ\text{C}$ |
| Gate-source leakage current | I_{GSS} | - | - | 100 | nA | $V_{GS}=20V, V_{DS}=0V$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.54 1.40 | 0.65 | Ω | $V_{GS}=10V, I_D=2.4A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=2.4A, T_j=150^\circ\text{C}$ |
| Gate resistance | R_G | - | 10 | - | Ω | $f=1\text{MHz}$, open drain |

Table 6 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance | C_{iss} | - | 440 | - | pF | $V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$ |
| Output capacitance | C_{oss} | - | 30 | - | pF | $V_{GS}=0V, V_{DS}=100V, f=1\text{MHz}$ |
| Effective output capacitance, energy related ¹⁾ | $C_{o(er)}$ | - | 21 | - | pF | $V_{GS}=0V, V_{DS}=0\dots480V$ |
| Effective output capacitance, time related ²⁾ | $C_{o(tr)}$ | - | 88 | - | pF | $I_D=\text{constant}, V_{GS}=0V, V_{DS}=0\dots480V$ |
| Turn-on delay time | $t_{d(on)}$ | - | 10 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=3A,$ $R_G=6.8\Omega$; see table 10 |
| Rise time | t_r | - | 8 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=3A,$ $R_G=6.8\Omega$; see table 10 |
| Turn-off delay time | $t_{d(off)}$ | - | 58 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=3A,$ $R_G=6.8\Omega$; see table 10 |
| Fall time | t_f | - | 11 | - | ns | $V_{DD}=400V, V_{GS}=13V, I_D=3A,$ $R_G=6.8\Omega$; see table 10 |

Table 7 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-----------------------|---------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 2.5 | - | nC | $V_{DD}=480V, I_D=3A, V_{GS}=0$ to 10V |
| Gate to drain charge | Q_{gd} | - | 10.5 | - | nC | $V_{DD}=480V, I_D=3A, V_{GS}=0$ to 10V |
| Gate charge total | Q_g | - | 20.5 | - | nC | $V_{DD}=480V, I_D=3A, V_{GS}=0$ to 10V |
| Gate plateau voltage | $V_{plateau}$ | - | 5.4 | - | V | $V_{DD}=480V, I_D=3A, V_{GS}=0$ to 10V |

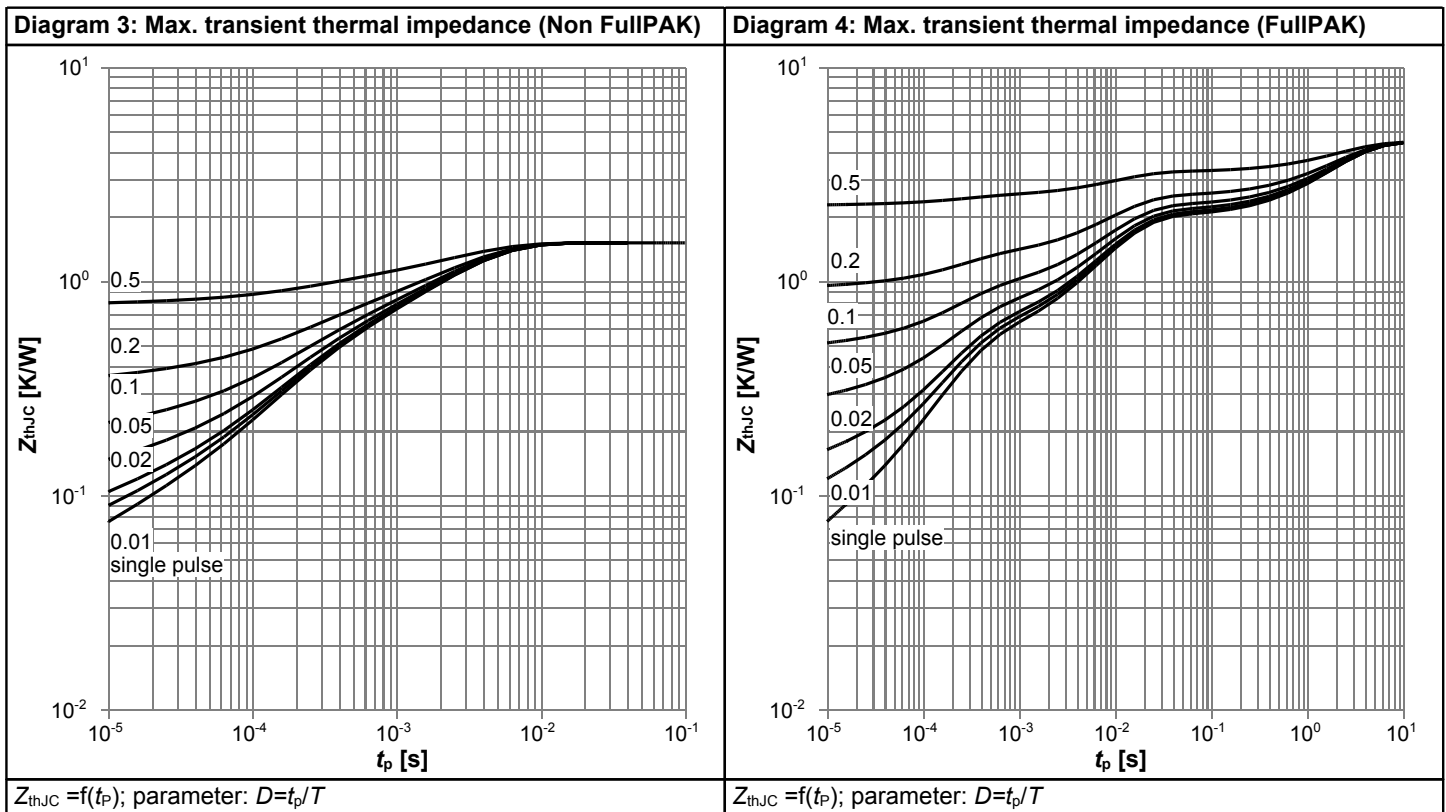
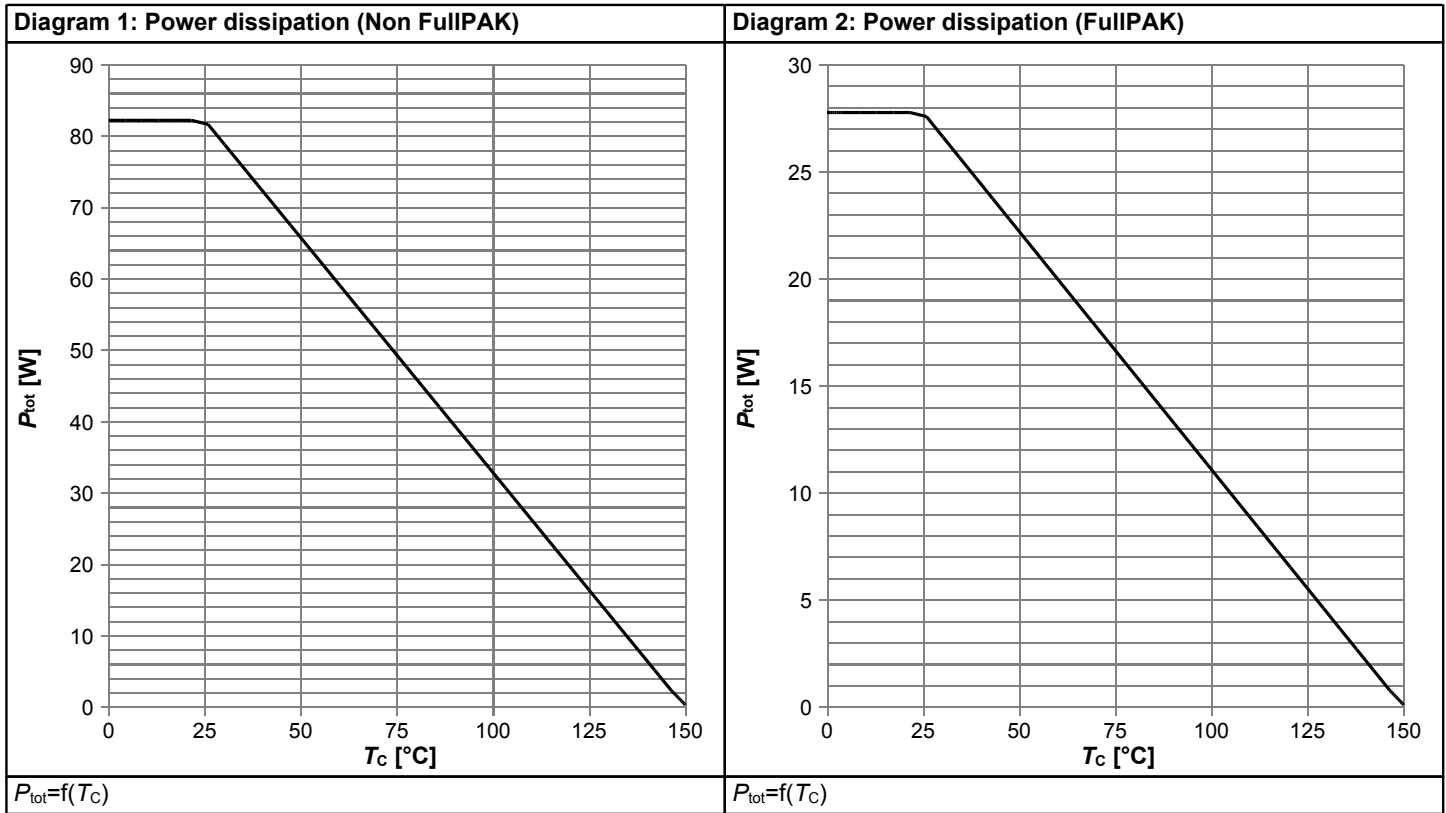
¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 8 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|-----------|--------|------|------|---------|---|
| | | Min. | Typ. | Max. | | |
| Diode forward voltage | V_{SD} | - | 0.9 | - | V | $V_{GS}=0V, I_F=3A, T_j=25^\circ C$ |
| Reverse recovery time | t_{rr} | - | 250 | - | ns | $V_R=400V, I_F=3A, di_F/dt=100A/\mu s$; see table 9 |
| Reverse recovery charge | Q_{rr} | - | 2.1 | - | μC | $V_R=400V, I_F=3A, di_F/dt=100A/\mu s$; see table 9 |
| Peak reverse recovery current | I_{rrm} | - | 16 | - | A | $V_R=400V, I_F=3A, di_F/dt=100A/\mu s$; see table 9 |

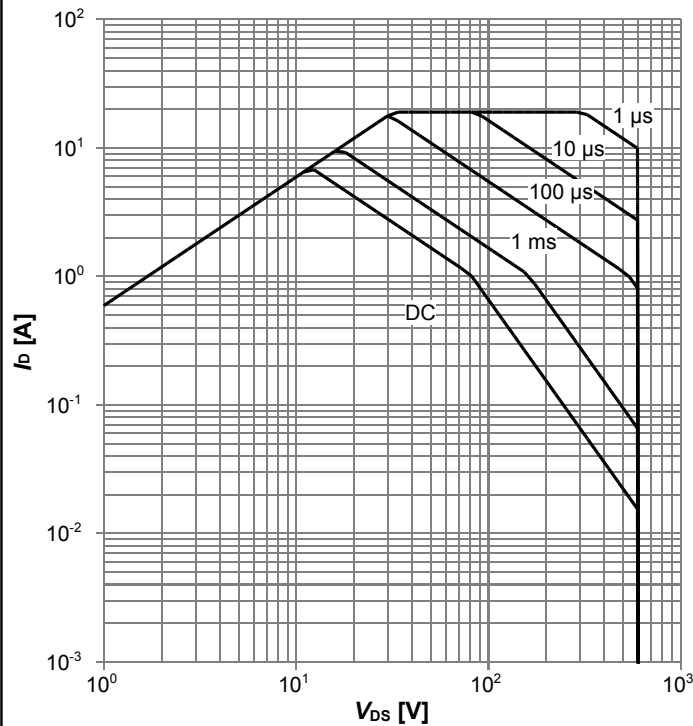
4 Electrical characteristics diagrams



600V CoolMOS™ CE Power Transistor

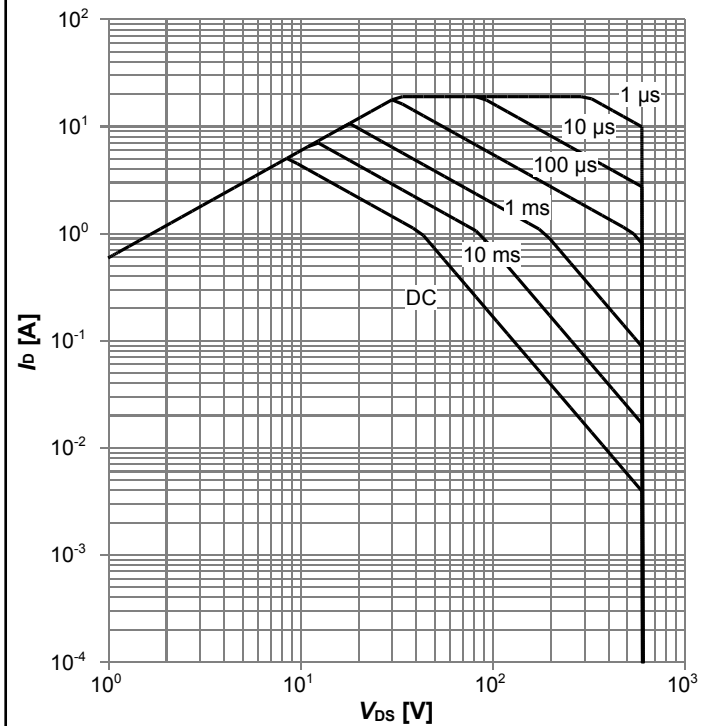
IPA60R650CE, IPD60R650CE

Diagram 5: Safe operating area (Non FullIPAK)



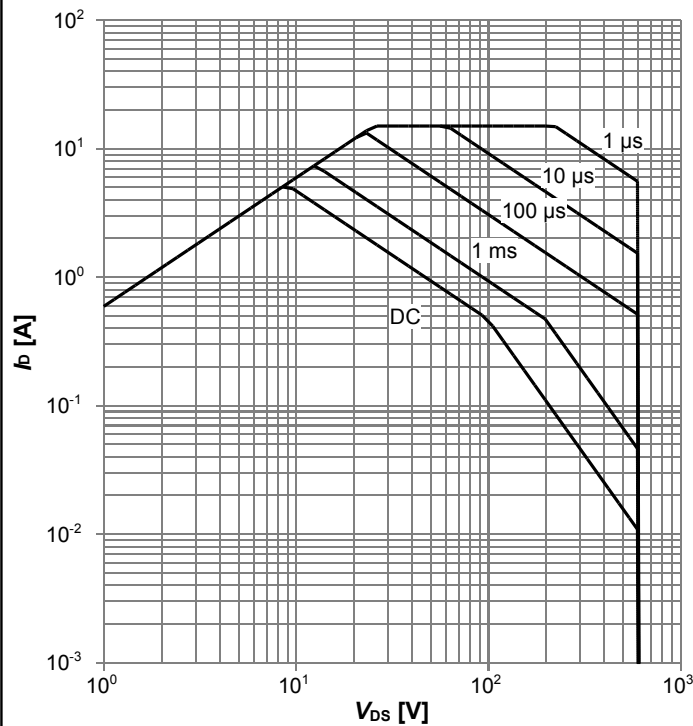
$I_b=f(V_{Ds}); T_C=25\text{ }^\circ\text{C}; D=0; \text{parameter: } t_p$

Diagram 6: Safe operating area (FullIPAK)



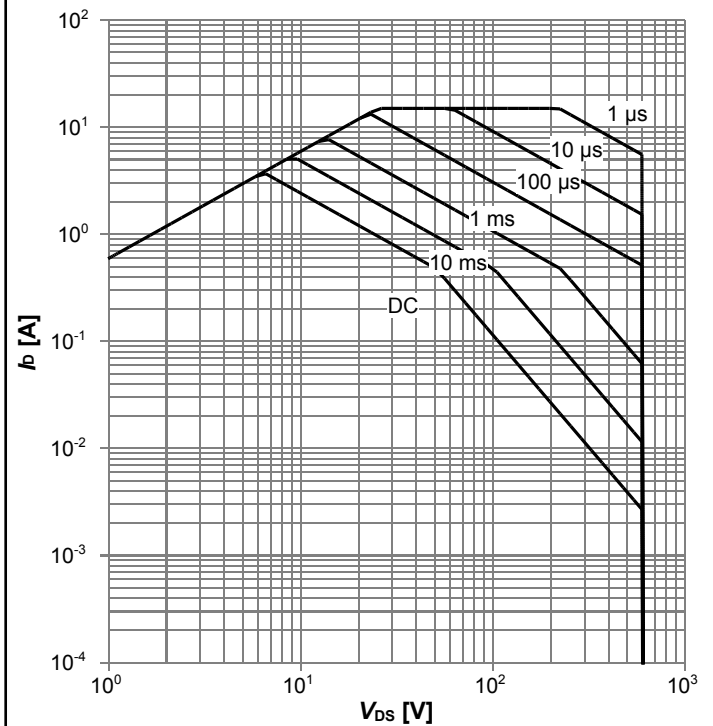
$I_b=f(V_{Ds}); T_C=25\text{ }^\circ\text{C}; D=0; \text{parameter: } t_p$

Diagram 7: Safe operating area (Non FullIPAK)



$I_b=f(V_{Ds}); T_C=80\text{ }^\circ\text{C}; D=0; \text{parameter: } t_p$

Diagram 8: Safe operating area (FullIPAK)

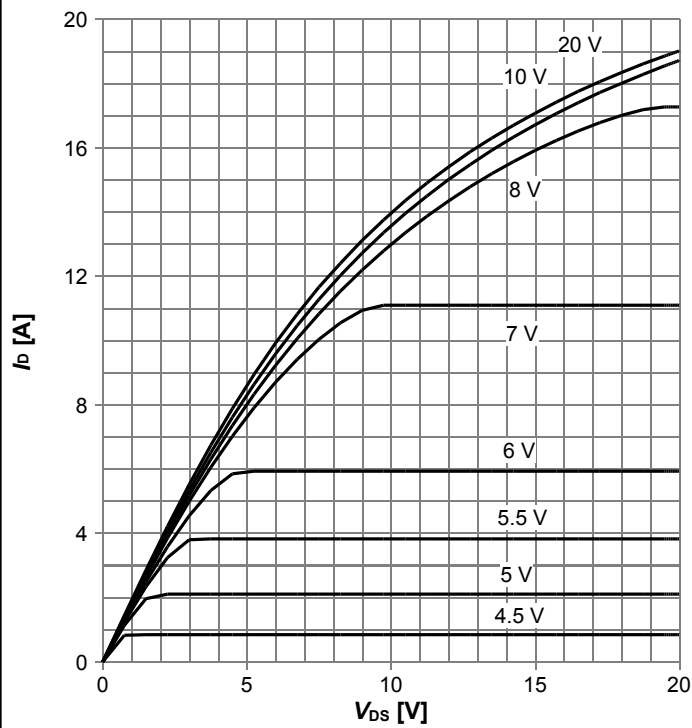


$I_b=f(V_{Ds}); T_C=80\text{ }^\circ\text{C}; D=0; \text{parameter: } t_p$

600V CoolMOS™ CE Power Transistor

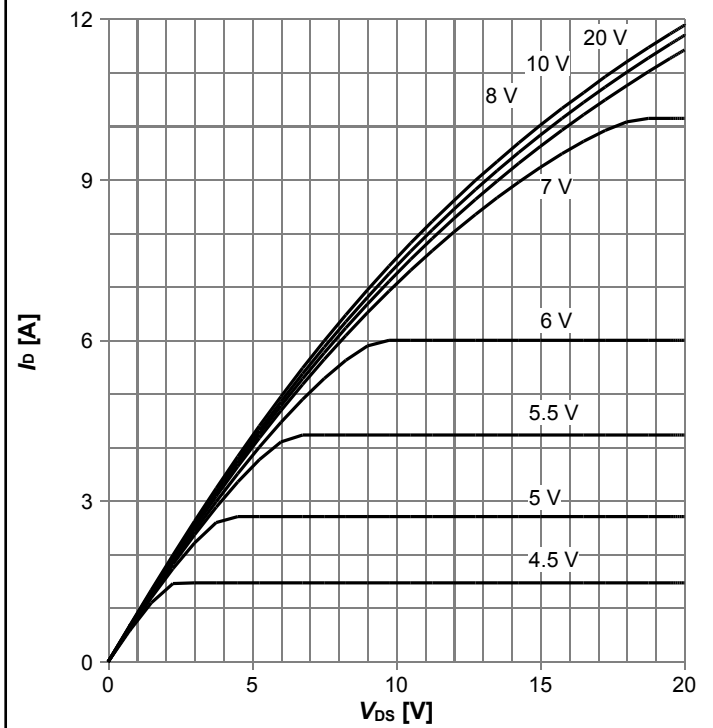
IPA60R650CE, IPD60R650CE

Diagram 9: Typ. output characteristics



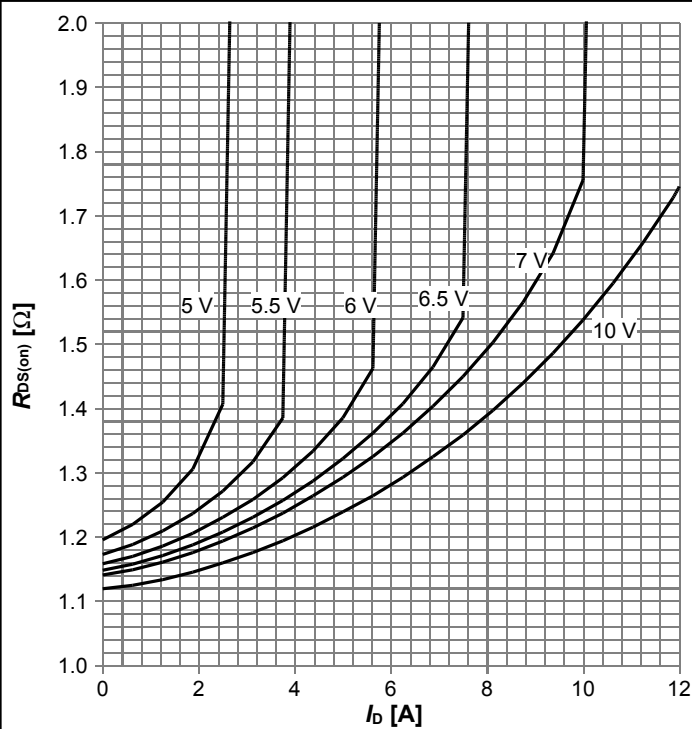
$I_D=f(V_{DS})$; $T_j=25\text{ °C}$; parameter: V_{GS}

Diagram 10: Typ. output characteristics



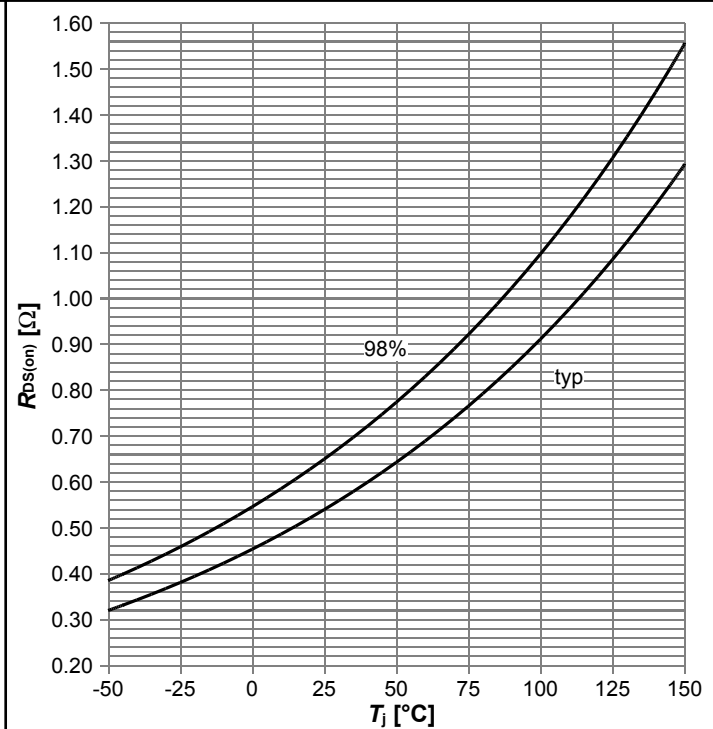
$I_D=f(V_{DS})$; $T_j=125\text{ °C}$; parameter: V_{GS}

Diagram 11: Typ. drain-source on-state resistance



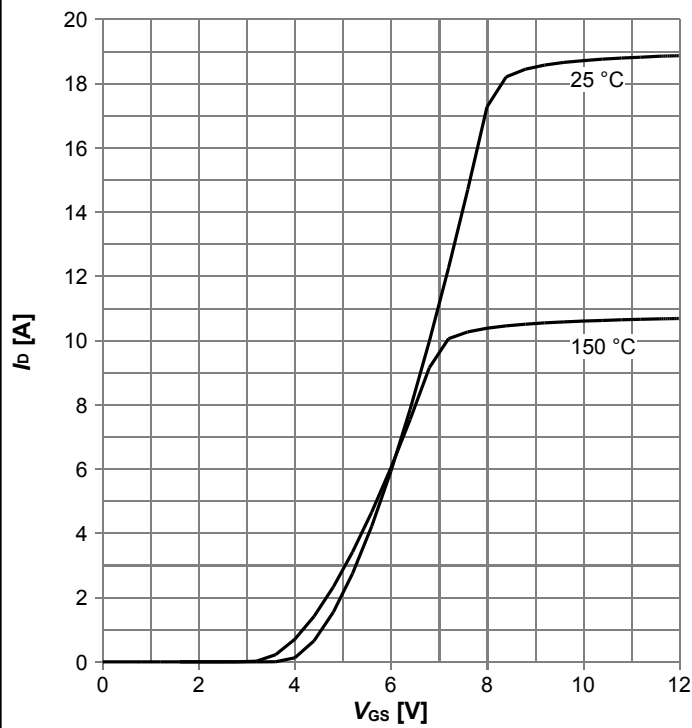
$R_{DS(on)}=f(I_D)$; $T_j=125\text{ °C}$; parameter: V_{GS}

Diagram 12: Drain-source on-state resistance



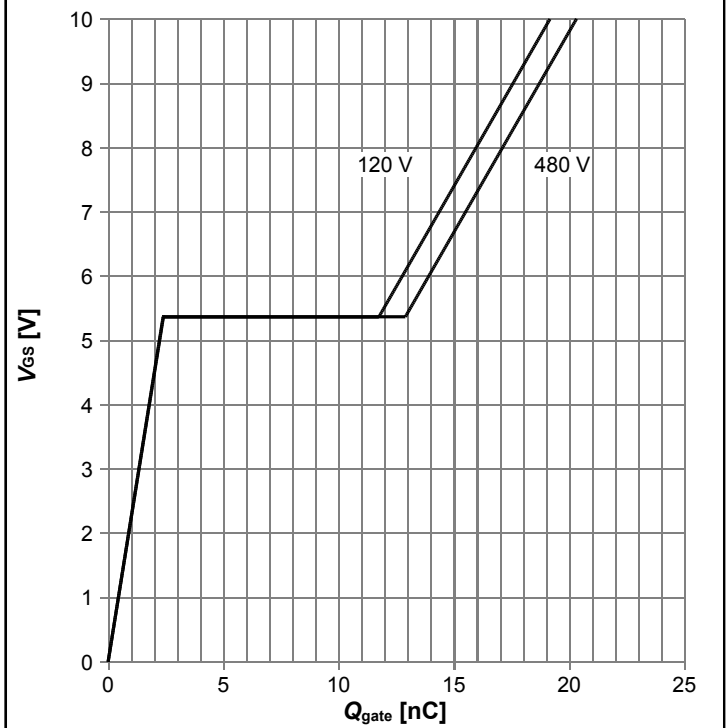
$R_{DS(on)}=f(T_j)$; $I_D=2.4\text{ A}$; $V_{GS}=10\text{ V}$

Diagram 13: Typ. transfer characteristics



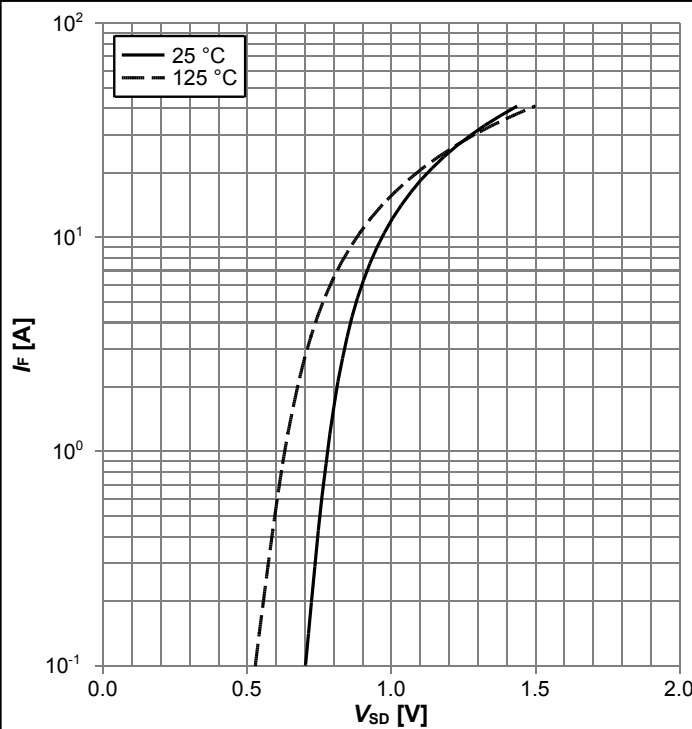
$I_D=f(V_{GS}); V_{DS}=20V$; parameter: T_j

Diagram 14: Typ. gate charge



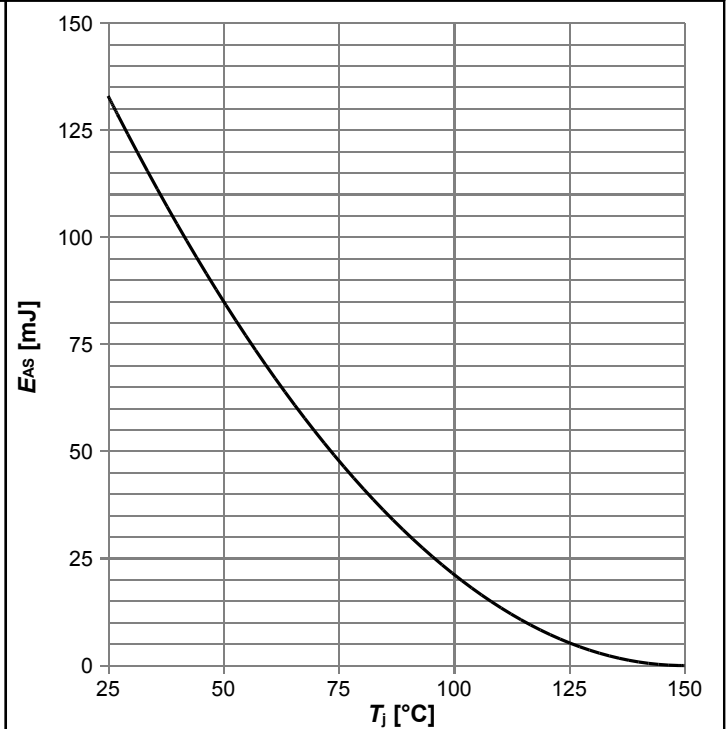
$V_{GS}=f(Q_{gate}); I_D=3.0\text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Forward characteristics of reverse diode



$I_F=f(V_{SD})$; parameter: T_j

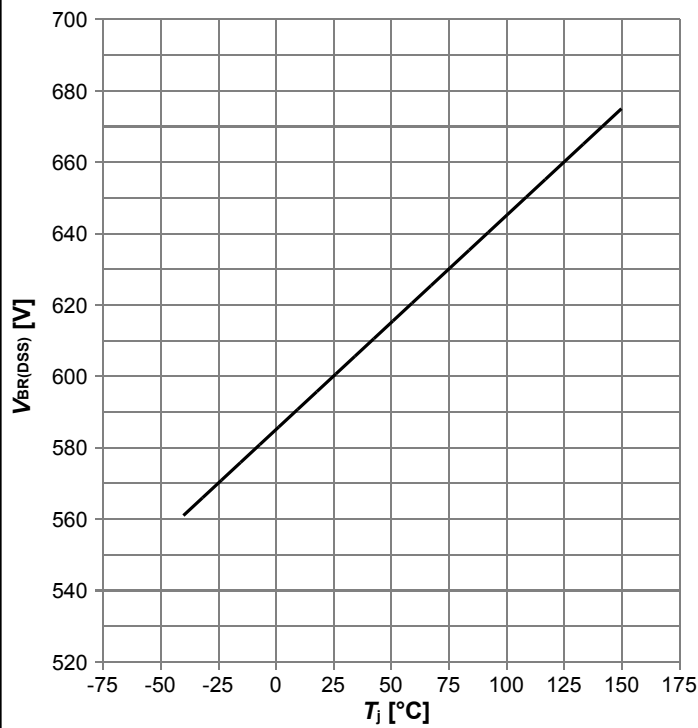
Diagram 16: Avalanche energy



$E_{AS}=f(T_j); I_D=1.3\text{ A}; V_{DD}=50\text{ V}$

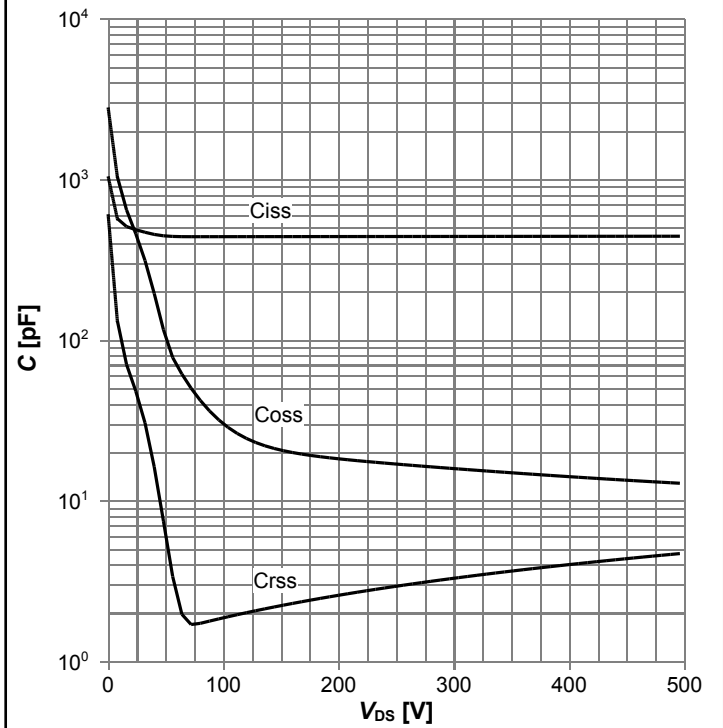
600V CoolMOS™ CE Power Transistor
IPA60R650CE, IPD60R650CE

Diagram 17: Drain-source breakdown voltage



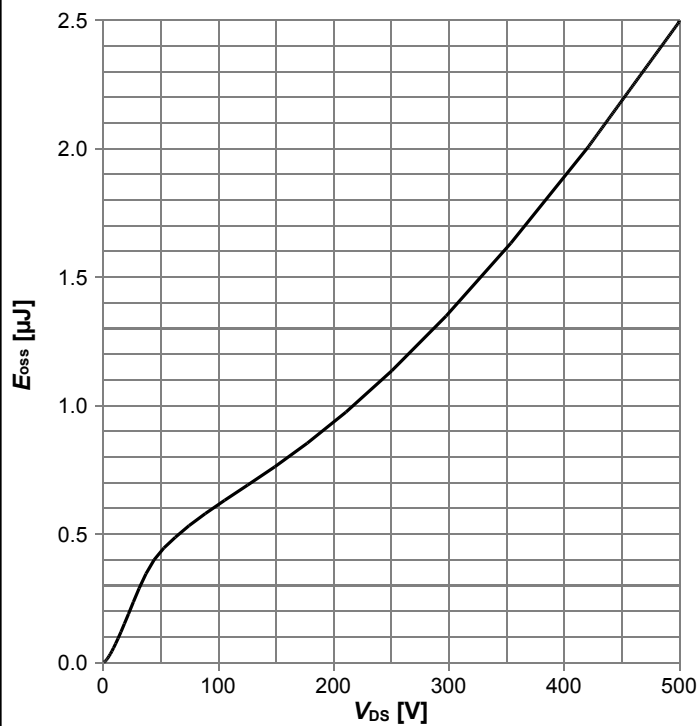
$V_{BR(DSS)}=f(T_j); I_D=0.25\text{ mA}$

Diagram 18: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 19: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 9 Diode characteristics

| Test circuit for diode characteristics | Diode recovery waveform |
|--|---|
| <p>$R_{g1} = R_{g2}$</p> | <p>$t_{rr} = t_F + t_S$ $Q_{rr} = Q_F + Q_S$</p> |

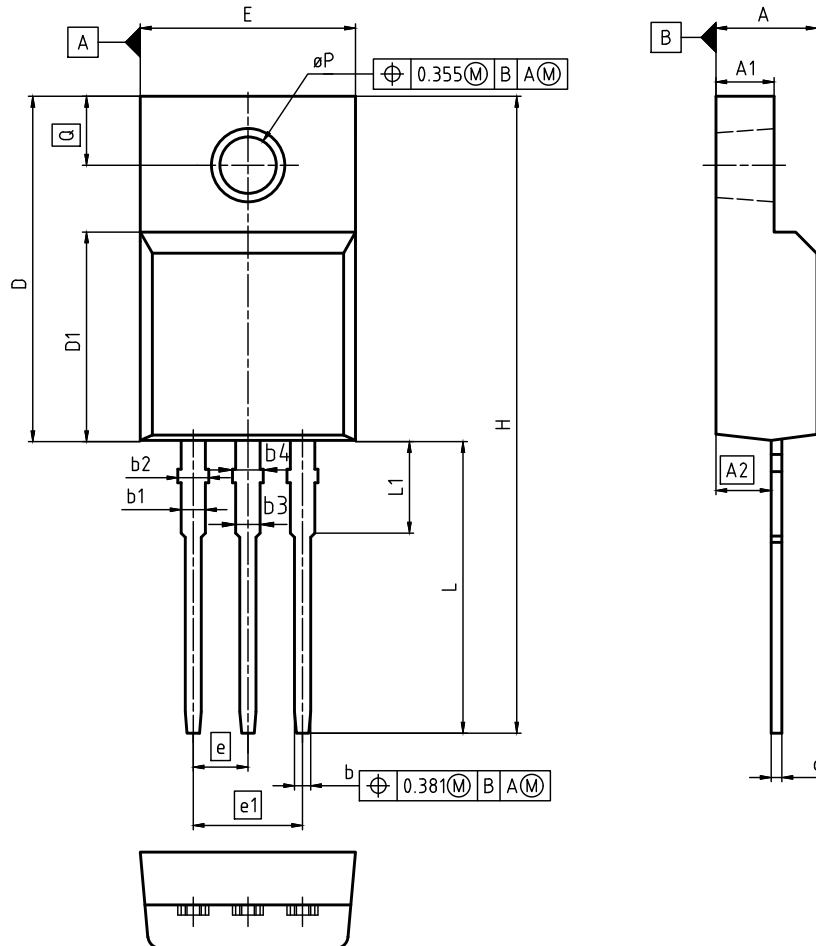
Table 10 Switching times

| Switching times test circuit for inductive load | Switching times waveform |
|---|--------------------------|
| | |

Table 11 Unclamped inductive load

| Unclamped inductive load test circuit | Unclamped inductive waveform |
|---------------------------------------|------------------------------|
| | |

6 Package Outlines



| DIM | MILLIMETERS | | INCHES | |
|-----------------|-------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.50 | 4.90 | 0.177 | 0.193 |
| A1 | 2.34 | 2.85 | 0.092 | 0.112 |
| A2 | 2.42 | 2.86 | 0.095 | 0.113 |
| b | 0.65 | 0.90 | 0.026 | 0.035 |
| b1 | 0.95 | 1.38 | 0.037 | 0.054 |
| b2 | 0.95 | 1.51 | 0.037 | 0.059 |
| b3 | 0.65 | 1.38 | 0.026 | 0.054 |
| b4 | 0.65 | 1.51 | 0.026 | 0.059 |
| c | 0.40 | 0.63 | 0.016 | 0.025 |
| D | 15.67 | 16.15 | 0.617 | 0.636 |
| D1 | 8.97 | 9.83 | 0.353 | 0.387 |
| E | 10.00 | 10.65 | 0.394 | 0.419 |
| e | 2.54 (BSC) | | 0.100 (BSC) | |
| e1 | 5.08 | | 0.200 | |
| N | 3 | | 3 | |
| H | 28.70 | 29.75 | 1.130 | 1.171 |
| L | 12.78 | 13.75 | 0.503 | 0.541 |
| L1 | 2.83 | 3.45 | 0.111 | 0.136 |
| $\varnothing P$ | 2.95 | 3.38 | 0.116 | 0.133 |
| Q | 3.15 | 3.50 | 0.124 | 0.138 |

Dimensions do not include mold flash, protrusions or gate burrs

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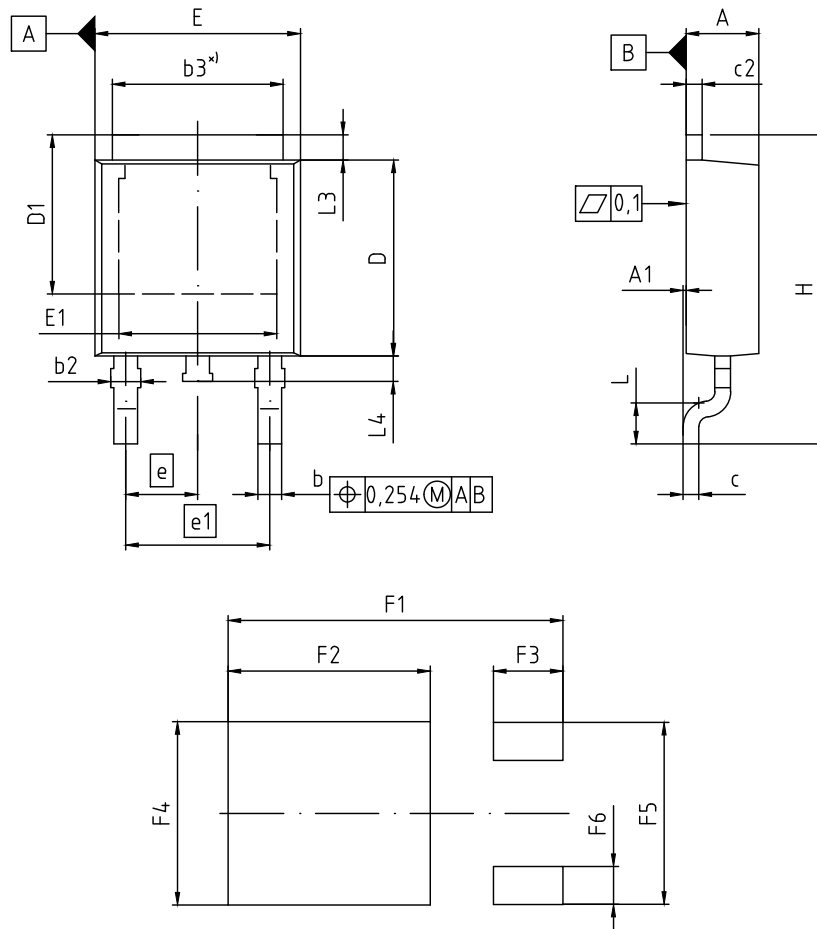
SCALE

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ISSUE DATE
05-05-2014

REVISION
04

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches



*) mold flash not included

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 2.16 | 2.41 | 0.085 | 0.095 |
| A1 | 0.00 | 0.15 | 0.000 | 0.006 |
| b | 0.64 | 0.89 | 0.025 | 0.035 |
| b2 | 0.65 | 1.15 | 0.026 | 0.045 |
| b3 | 5.00 | 5.50 | 0.197 | 0.217 |
| c | 0.46 | 0.60 | 0.018 | 0.024 |
| c2 | 0.46 | 0.98 | 0.018 | 0.039 |
| D | 5.97 | 6.22 | 0.235 | 0.245 |
| D1 | 5.02 | 5.84 | 0.198 | 0.230 |
| E | 6.40 | 6.73 | 0.252 | 0.265 |
| E1 | 4.70 | 5.60 | 0.185 | 0.220 |
| e | 2.29 (BSC) | | 0.090 (BSC) | |
| e1 | 4.57 (BSC) | | 0.180 (BSC) | |
| N | 3 | | 3 | |
| H | 9.40 | 10.48 | 0.370 | 0.413 |
| L | 1.18 | 1.70 | 0.046 | 0.067 |
| L3 | 0.90 | 1.25 | 0.035 | 0.049 |
| L4 | 0.51 | 1.00 | 0.020 | 0.039 |
| F1 | 10.60 | | 0.417 | |
| F2 | 6.40 | | 0.252 | |
| F3 | 2.20 | | 0.087 | |
| F4 | 5.80 | | 0.228 | |
| F5 | 5.76 | | 0.227 | |
| F6 | 1.20 | | 0.047 | |

DOCUMENT NO.
Z8B00003328

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05

Figure 2 Outline PG-TO 252, dimensions in mm/inches

7 Appendix A

Table 12 Related Links

- IFX CoolMOS™ CE Webpage: www.infineon.com
- IFX CoolMOS™ CE application note: www.infineon.com
- IFX CoolMOS™ CE simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPA60R650CE, IPD60R650CE

Revision: 2016-03-31

Previous Revision

| Date | Subjects (major changes since last revision) |
|------------|---|
| 2014-09-25 | Release of final version |
| 2016-03-31 | Modified Id, Rthjc. Modified SOA and Zthjc curves |

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