Quad (SD/HD) SDI Receiver with Adaptive Equalizer, VC-2 Decoder and Audio CODEC

TW6874

The TW6874 is a quad (SD/HD) SDI receiver. It has four independent channels, each consisting of an adaptive equalizer, clock data recovery, audio decoder and VC-2 decompression engine. Each channel receives high speed serial data over extended coaxial cable lengths and deserialize the data into video/audio streams for the back-end device.

The video streams are output as: 8-bit BT.656 for SD; BT.1120 in 8/16 bit mode for HD. The audio streams are output through an I2S audio digital interface in a multichannel interleaving format. In addition to the extraction of embedded SDI audio, the TW6874 incorporates a 5-channel audio ADC decoder to decode analog audio inputs and output them through the same I2S interface.

A visually lossless VC-2 (Dirac) compression/decompression engine is implemented in the TW6872/TW6874 SDI Tx/Rx pair to extend the reach of HD-SDI to that of SD-SDI. An interrupt pin can be used to signal the host processor of ancillary data packet detection. Finally, integrated audio test patterns and PRBS checker ease system design and implementation.

Applications

- SD/HD DVR

Features

- Quad (SD/HD) SDI receiver for standard (SD) and high (HD) definition 10-bit component video
- Automatic SDI detection of SMPTE 259M Level C (SD-SDI), SMPTE ST 292 (1.5G SDI) signals
- Each SDI input standard supported with ITU-R BT.656 (SD) or ITU-R BT.1120 (1.5G) interface
- Converts 10-bit serial digital component video input to 8-bit parallel video output
- Adaptive equalizer/clock data recovery/VC-2 decompression engine for each channel
- 4 separate video output ports with BT.656/BT.1120 output format
- 5-channel audio ADC (Analog-to-Digital Converter)
- Single multiplexed audio output DAC (Digital-to-Analog Converter)
- Supports I2S master/slave interface for record output and playback input with cascade
- I^2C and SPI interface
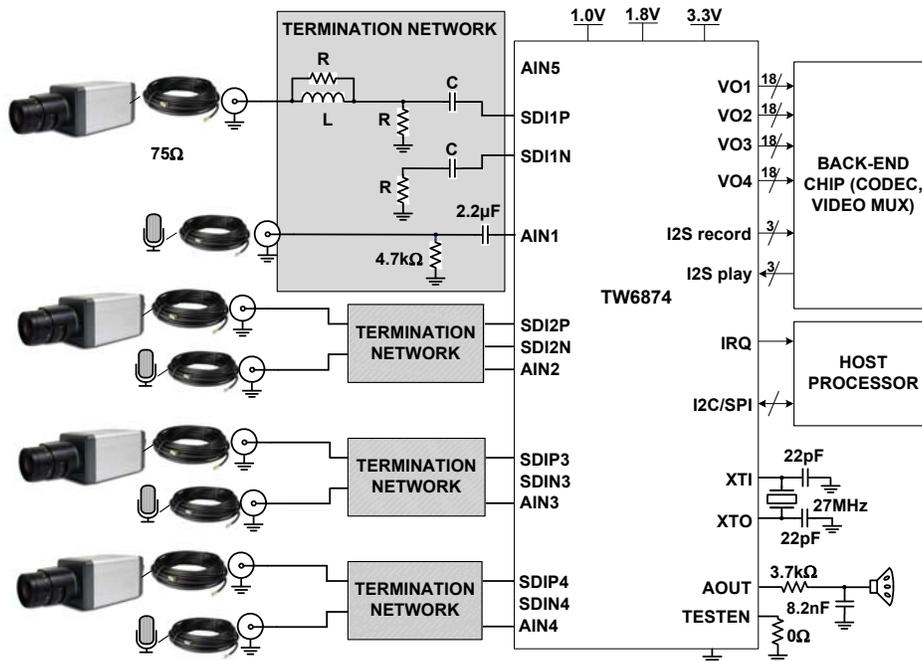- Pb-free (RoHS compliant) 256 ball LFBGA

FIGURE 1. TW6874 TYPICAL APPLICATION

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