# *3.0V Core Async/Page PSRAM*

## Overview

The IS66WVE4M16BLL is an integrated memory device containing 64Mbit Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 4M words by 16 bits. The device includes several power saving modes : Partial Array Refresh mode where data is retained in a portion of the array and Deep Power Down mode. Both these modes reduce standby current drain. The die has separate power rails, VDDQ and VSSQ for the I/O to be run from a separate power supply from the device core.

## Features

- Asynchronous and page mode interface
- Dual voltage rails for optional performance
  - VDD 2.7V~3.6V, VDDQ 2.7V~3.6V
- Page mode read access
  - Interpage Read access : 70ns
  - Intrapage Read access : 20ns
- Low Power Consumption
  - Asynchronous Operation < 30 mA
  - Intrapage Read < 18mA
  - Standby < 180 uA (max.)
  - Deep power-down (DPD) < 3uA (Typ)
- Low Power Feature
  - Temperature Controlled Refresh
  - Partial Array Refresh
  - Deep power-down (DPD) mode
- Operating temperature Range
  Industrial -40°C~85°C
- Packages:
  48-ball TFBGA, 48-pin TSOP-I

**Notes:**

1. The 48-pin TSOP-I package option is not yet available. Please contact SRAM Marketing at sram@issi.com for additional information.

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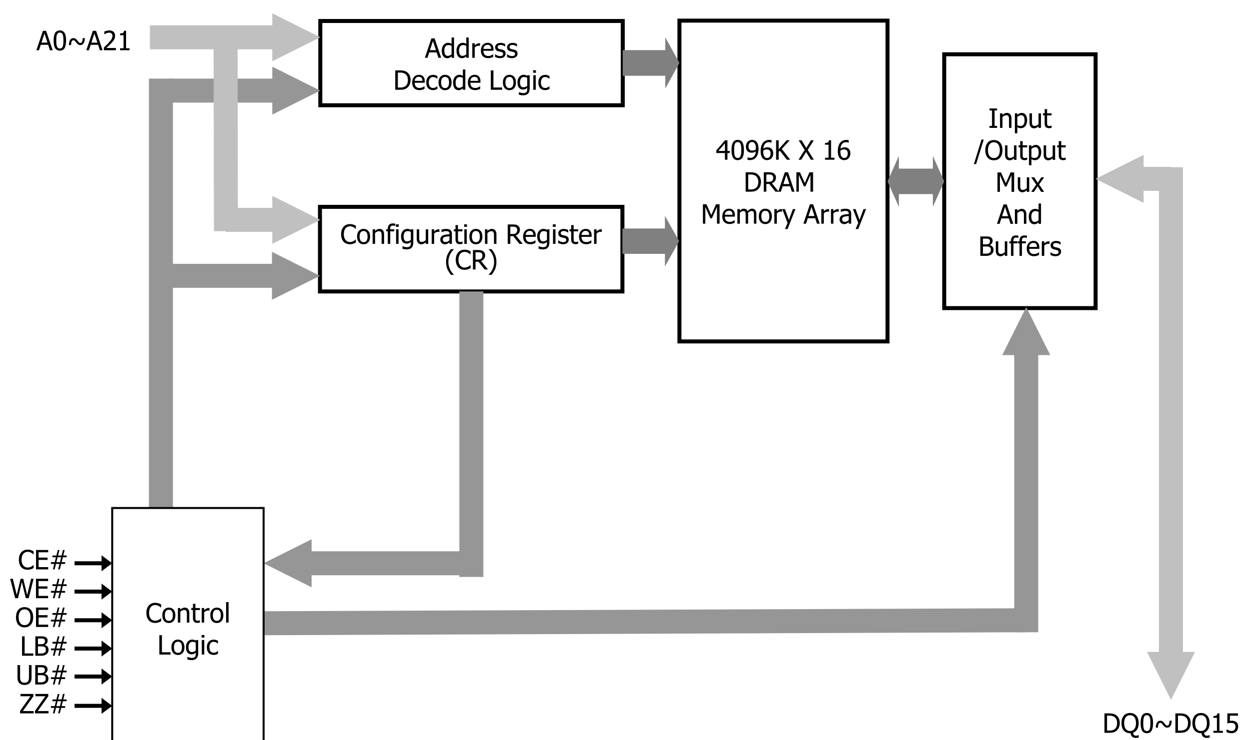
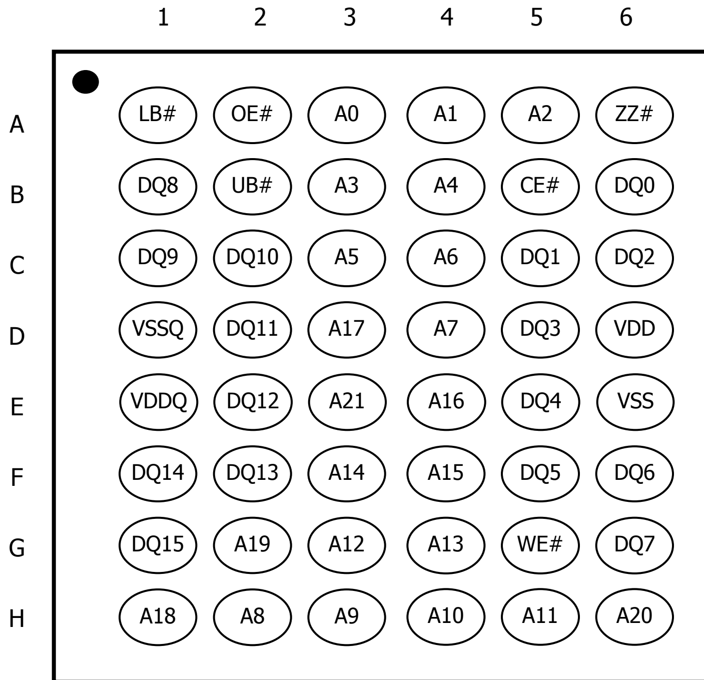
## General Description

PSRAM products are high-speed, CMOS pseudo-static random access memory developed for low-power, portable applications. The 64Mb DRAM core device is organized as 4 Meg x 16 bits. These devices include the industry-standard, asynchronous memory interface found on other low-power SRAM or pseudo-SRAM (PSRAM) offerings.
For seamless operation on an asynchronous memory bus, PSRAM products incorporated a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.
A user-accessible configuration registers (CR) defines how the PSRAM device performs on-chip refresh and whether page mode read accesses are permitted. This register is automatically loaded with a default setting during power-up and can be updated at any time during normal operation.
Special attention has been focused on current consumption during self-refresh. This product includes two system-accessible mechanisms to minimize refresh current. Setting sleep enable (ZZ#) to LOW enables one of two low-power modes: partial-array refresh (PAR) or deep power-down (DPD). PAR limits refresh to only that part of the DRAM array that contains essential data. DPD halts refresh operation altogether and is used when no vital information is stored in the device. The system-configurable refresh mechanisms are accessed through the CR.




[ Functional Block Diagram]

## 48Ball TFBGA Ball Assignment




**[Top View]**
**(Ball Down)**

**48-pin TSOP-I (Top View)**

**Notes:**

1. The 48-pin TSOP-I package option is not yet available. Please contact SRAM Marketing at sram@issi.com for additional information.

## Signal Descriptions

All signals for the device are listed below in Table 1.

**Table 1. Signal Descriptions**

| Symbol | Type | Description |
|---|---|---|
| VDD | Power Supply | Core Power supply (2.7V~3.6V) |
| VDDQ | Power Supply | I/O Power supply (2.7V~3.6V) |
| VSS | Power Supply | All VSS supply pins must be connected to Ground |
| VSSQ | Power Supply | All VSSQ supply pins must be connected to Ground |
| DQ0~DQ15 | Input / Output | Data Inputs/Outputs (DQ0~DQ15) |
| A0~A21 | Input | Address Input(A0~A21) |
| LB# | Input | Lower Byte select |
| UB# | Input | Upper Byte select |
| CE# | Input | Chip Enable/Select |
| OE# | Input | Output Enable |
| WE# | Input | Write Enable |
| ZZ# | Input | Sleep enable : When ZZ# is LOW, the CR can be loaded, or the device can enter one of two low-power modes ( DPD or PAR). |

## Functional Description

All functions for the device are listed below in Table 2.

### Table 2. Functional Descriptions

| Mode | Power | CE# | WE# | OE# | UB#/LB# | ZZ# | DQ [15:0][4] | Note |
|---|---|---|---|---|---|---|---|---|
| Standby | Standby | H | X | X | X | H | High-Z | 2,5 |
| Read | Active | L | H | L | L | H | Data-Out | 1,4 |
| Write | Active | L | L | X | L | H | Data-In | 1,3,4 |
| No operation | Idle | L | X | X | X | H | X | 4,5 |
| PAR | PAR | H | X | X | X | L | High-Z | 6 |
| DPD | DPD | H | X | X | X | L | High-Z | 6 |
| Load Configuration register | Active | L | L | X | X | L | High-Z | |

Notes

1. When UB# and LB# are in select mode (LOW), DQ0~DQ15 are affected as shown. When only LB# is in select mode, DQ0~DQ7 are affected as shown. When only UB# is in select mode, DQ8~DQ15 are affected as shown.
2. When the device is in standby mode, control inputs (WE#, OE#), address inputs, and data inputs/outputs are internally isolated from any external influence.
3. When WE# is active, the OE# input is internally disabled and has no effect on the I/Os.
4. The device will consume active power in this mode whenever addresses are changed.
5. Vin=VDDQ or 0V, all device pins be static (unswitched) in order to achieve standby current.
6. DPD is enabled when configuration register bit CR[4] is "0"; otherwise, PAR is enabled.

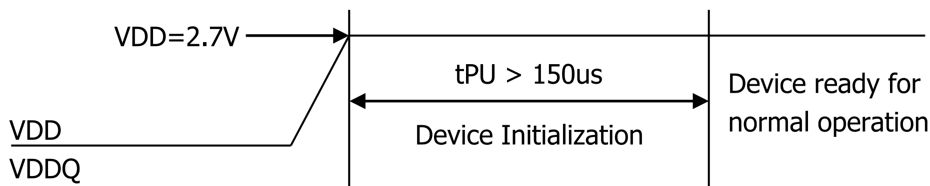
## Functional Description

In general, this device is high-density alternatives to SRAM and Pseudo SRAM products popular in low-power, portable applications.
The 64Mb device contains a 67,108,864-bit DRAM core organized as 4,194,304 addresses by 16 bits. This device include the industry-standard, asynchronous memory interface found on other low-power SRAM or PSRAM offerings
Page mode access is also supported as a bandwidth-enhancing extension to the asynchronous read protocol.

## Power-Up Initialization

PSRAM products include an on-chip voltage sensor that is used to launch the power-up initialization process. Initialization will load the CR with its default settings (see Table 3). VDD and VDDQ must be applied simultaneously. When they reach a stable level above 2.7V, the device will require 150µs to complete its self-initialization process ( see Figure 1). During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

**Figure 1: Power-Up Initialization Timing**



## Bus Operating Modes

PSRAM products incorporates the industry-standard, asynchronous interface. This bus interface supports asynchronous Read and WRITE operations as well as page mode READ operation for enhanced bandwidth. The supported interface is defined by the value loaded into the CR.

## Asynchronous Mode Operation

PSRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control interface (CE#, OE#, WE#, and LB#/UB#).
READ operations are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH (see Figure 2). Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations occur when CE#,WE#, and LB#/UB# are driven LOW (see Figure 3). During WRITE operations, the level of OE# is a "Don't Care"; WE# overrides OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB#, whichever occurs first. WE# LOW time must be limited to tCEM.

**Figure 2. Asynchronous Read Operation**

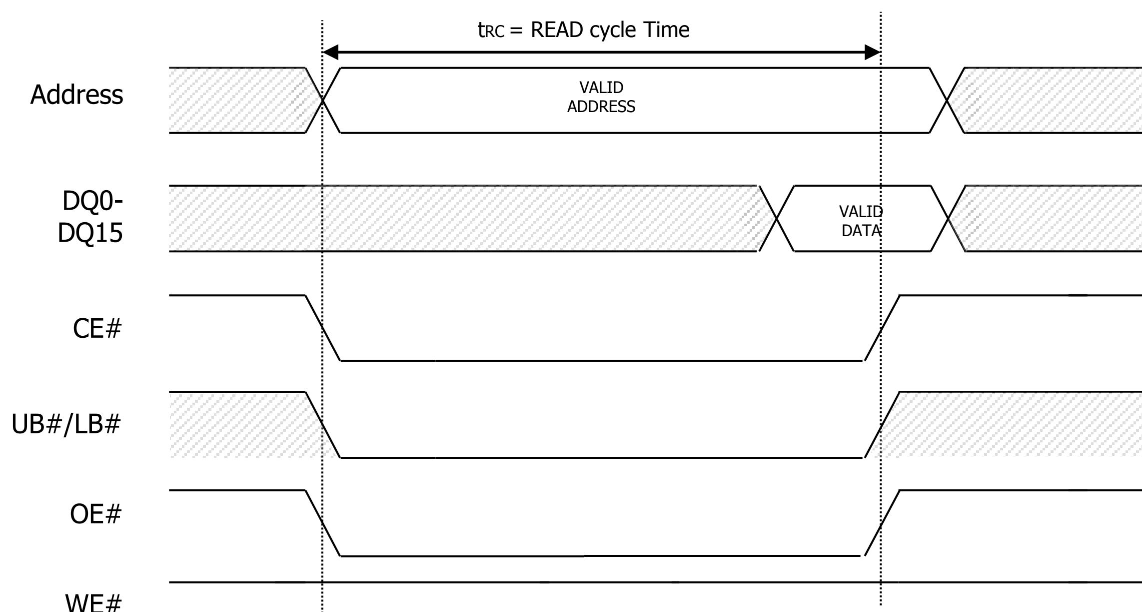
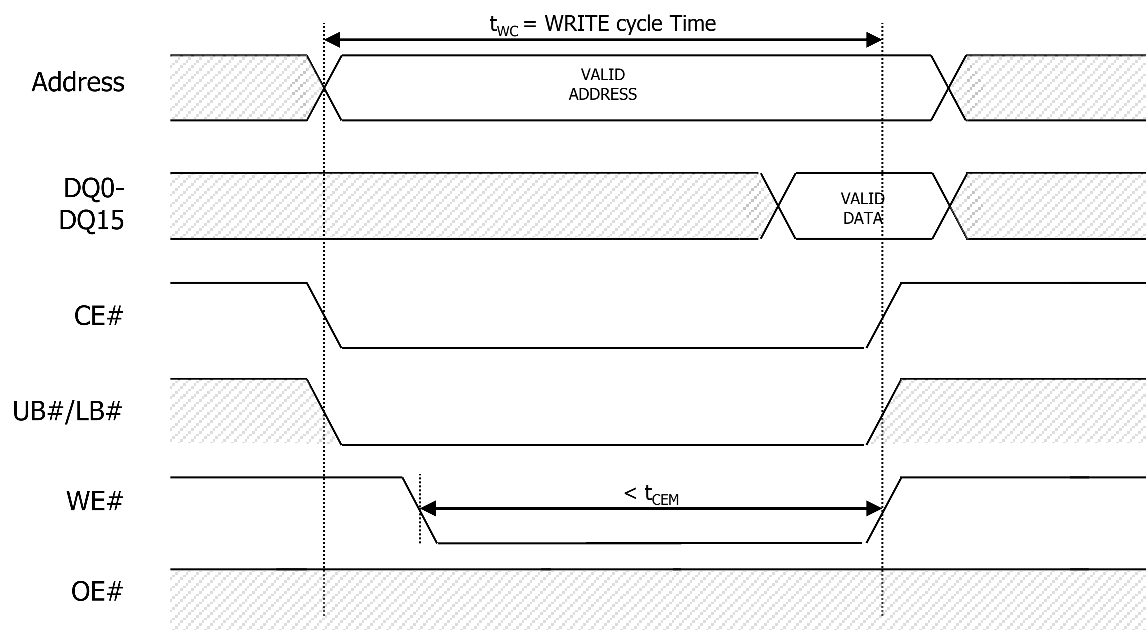


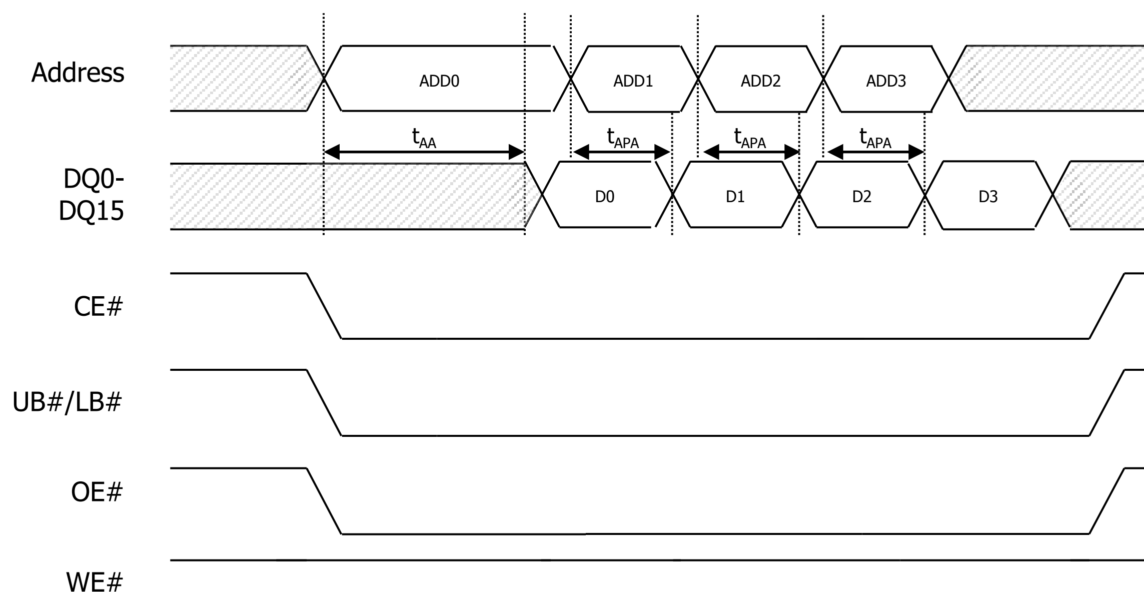
**Figure 3. Asynchronous WRITE operation**



## Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is preformed, then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address PSRAM page. Any change in addresses A[4] or higher will initiate a new tAA access time. Figure 4 shows the timing for a page mode access.
Page mode takes advantage of the fact that adjacent addresses can be read faster than random addresses. WRITE operations do not include comparable page mode functionality. The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than tCEM.

**Figure 4. Page Mode READ Operation**




## UB#/LB# Operation

The UB#/LB# enable signals accommodate byte-wide data transfers. During READ operations, enabled bytes are driven onto the DQ. The DQ signals associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, disabled bytes are not transferred to the memory array. and the internal value remains unchanged. During a WRITE cycle the data to be written is latched on the rising edge of CE#, WE#, LB# or UB#, whichever occurs first.
When both the UB#/LB# are disabled (HIGH) during an operation, the device prevents the data bus from receiving or transmitting data. Although the device may appear to be deselected, it remains in active mode as long as CE# remains LOW.

## Low-Power Feature

### Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# and ZZ# are HIGH. The device will enter a reduced power state upon completion of a READ or WRITE operations when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

### Temperature Compensated Refresh

Temperature compensated refresh (TCR) is used to adjust the refresh rate depending on the device operating temperature. DRAM technology requires more frequent refresh operations to maintain data integrity as temperatures increase. More frequent refresh is required due to the increased leakage of the DRAM's capacitive storage elements as temperatures rise. A decreased refresh rate at lower temperatures will result in a savings in standby current.

TCR allows for adequate refresh at four different temperature thresholds: +15°C, +45°C, +70°C, and +85°C. The setting selected must be for a temperature higher than the case temperature of the device. If the case temperature is +50°C, the system can minimize self refresh current consumption by selecting the +70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

### Partial-Array Refresh

Partial-array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array that is absolutely necessary. The refresh options are full array, and none of the array. Data stored in addresses not receiving refresh will become corrupted. Read and WRITE operations are ignored during PAR operation.
The device only enters PAR mode if the sleep bit in the CR has been set HIGH (CR[4] = 1). PAR can be initiated by taking the ZZ# ball to the LOW state for longer than 10us. Returning ZZ# to HIGH will cause an exit from PAR, and the entire array will be immediately available for READ and WRITE operations.
Alternatively, PAR can be initiated using the CR software-access sequence (see "Software Access to the Configuration Register"). Using this method, PAR is enabled immediately upon setting CR[4] to "1" However, using software access to write to the CR alters the function of ZZ# so that ZZ# LOW no longer initiates PAR, even though ZZ# continues to enable WRITEs to the CR. This functional change persists until the next time the device is powered up.

### Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the PSRAM device. Any stored data will become corrupted upon entering DPD. When refresh activity has been re-enabled, the PSRAM device will require 150µs to perform an initialization procedure before normal operations can resume. READ and WRITE operations are ignored during DPD operation.
The device can only enter DPD if the sleep bit in the CR has been set LOW (CR[4] =0). DPD is initiated by bringing ZZ# to the LOW state for longer than 10us. Returning ZZ# to HIGH will cause the device to exit DPD and begin a 150us initialization process. During this time, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.
Driving ZZ# LOW puts the device in PAR mode if the SLEEP bit in the CR has been set HIGH (CR[4] = 1).
The device should not be put into DPD using the CR software-access sequence.

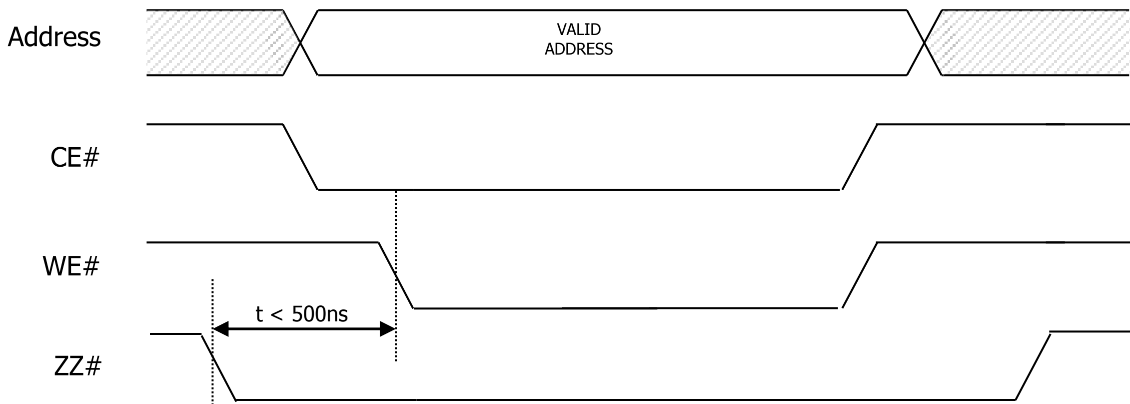
## Configuration Registers Operation

The configuration register (CR) defines how the PSRAM device performs a transparent self refresh. Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode controls is embedded in the CR. This register can be updated any time the device is operating in a standby state. The control bits used in the CR are shown in Table 3. At power-up, the CR is set to 0070h.

## Access Using ZZ#

The CR can be loaded using a WRITE operation immediately after ZZ# makes a HIGH-to-LOW transition (see Figure 5). The values placed on addresses A[21:0] are latched into the CR on the rising edge of CE# or WE#, whichever occurs first. LB#/UB# are "Don't Care." Access using ZZ# is WRITE only.

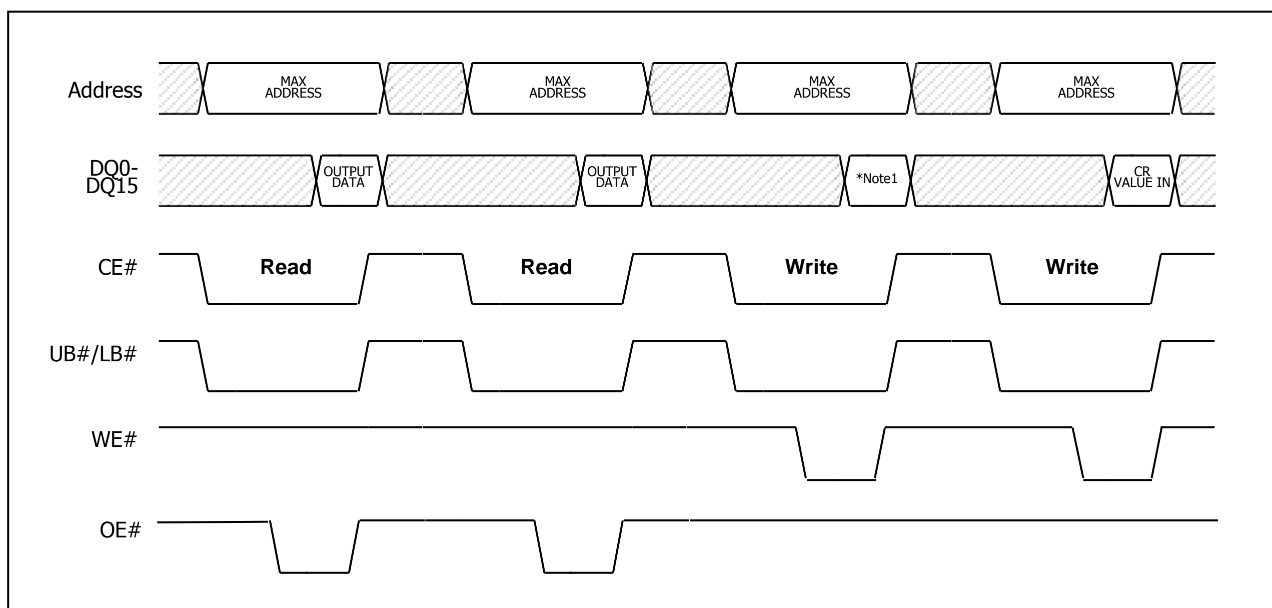
**Figure 5: Load Configuration Register Operation Using ZZ#**



## Software Access Sequence

The contents of the CR can be read or modified using a software access sequence. The nature of this access mechanism can potentially eliminate the need for the ZZ# ball.
If the software-access mechanism is used, ZZ# can simply be tied to VDDQ; the port line typically used for ZZ# control purposes will no longer be required. However, ZZ# should not be tied to VDDQ if the system will use DPD; DPD cannot be enabled or disabled using the software-access sequence.
The CR is loaded using a four-step sequence consisting of two READ operations followed by two WRITE operations (see Figure 6). The READ sequence is virtually identical except that an asynchronous READ is performed during the fourth operation (see Figure 7).
The address used during all READ and WRITE operations is the highest address of the PSRAM device being accessed (3FFFFFh); the content of this address is not changed by using the software-access sequence. The data bus is used to transfer data into or out of bit[15:0] of the CR.
Writing to the CR using the software-access sequence modifies the function of the ZZ# ball. After the software sequence loads the CR, the level of the ZZ# ball no longer enables PAR operation. PAR operation is updated whenever the software-access sequence loads a new value into the CR. This ZZ# functionality will remain active until the next time the device is powered up. The operation of the ZZ# ball is not affected if the software-access sequence is only used to read the contents of the CR. Use of the software-access sequence does not affect the performance of standard (ZZ#-controlled) CR loading.

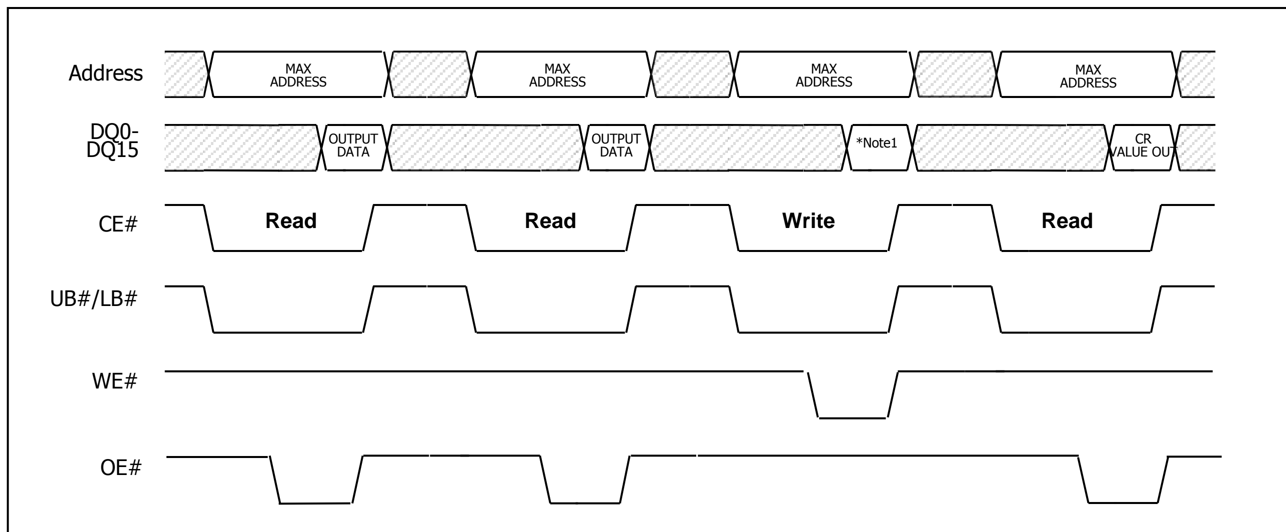
### Figure 6 : Configuration Register Write




Notes :

1. CR : 0000h

## Figure 7 : Configuration Register Read




Notes :

1. CR : 0000h

**Table 3. Configuration Register**

| Bit Number | Definition | Remark |
|---|---|---|
| 21 – 8 | Reserved | All Must be set to "0" |
| 7 | Page | 0 = Page mode disabled (default)<br>1 = Page mode enabled |
| 6 – 5 | TCR | 1 1 = +85°C (default)<br>0 0 = +70°C<br>0 1 = +45°C<br>1 0 = +15°C |
| 4 | Sleep | 0 = DPD enabled<br>1 = PAR enabled (default) |
| 3 | Reserved | Must be set to "0" |
| 2 – 0 | PAR[1] | 000 = Full array (default)<br>100 = None of array |

Notes :

1. Use of other setting will result in full-array refresh coverage.

**Partial-Array Refresh (CR[2:0]) Default = Full-Array Refresh**

The PAR bits restrict REFRESH operation to a portion of the total memory array. The refresh options are "full array" and " none of the array."

**Sleep Mode (CR[4]) Default = PAR Enabled, DPD Disabled**

The sleep mode bit defines the low-power mode to be entered when ZZ# is driven LOW. If CR[4] = 1, PAR operation is enabled. If CR[4] = 0, DPD operation is enabled. PAR can also be enabled directly by writing to the CR using the software-access sequence. Note that this disables ZZ# initiation of PAR. DPD cannot properly be enabled or disabled using the software-access sequence; DPD should only be enabled or disabled using ZZ# to access the CR.
DPD operation disables all refresh-related activity. This mode is used when the system does not require the storage provided by the PSRAM device. When DPD is enabled, any stored data will become corrupted. When refresh activity has been re-enabled. The PSRAM device will require 150us to perform an initialization procedure before normal operation can resume. DPD should not be enabled using CR software access.

**Temperature Compensated Refresh (CR[6:5]) Default = +85°C Operation**

Temperature compensated refresh register bits can be programmed using the CR [5, 6] configuration registers and has four different temperature levels: +15°C, +45°C, +70°C, and +85°C. The temperature selected must be equal to or higher than the case temperature of the device. Setting a lower temperature level would cause data to be corrupted due to insufficient refresh rate.

**Page Mode READ Operation (CR[7]) Default = Disabled**

The page mode operation bit determines whether page mode READ operations are enabled In the power-up default state, page mode is disabled.

## Electrical Characteristics

### Table 4. Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| Voltage to Any Ball Except VDD, VDDQ Relative to VSS | -0.5V to 4.0V or VDDQ + 0.3V |
| Voltage on VDD Supply Relative to VSS | -0.2V to + 4.0V |
| Voltage on VDDQ Supply Relative to VSS | -0.2V to + 4.0V |
| Storage Temperature (plastic) | -55°Cto + 150°C |
| Operating Temperature | -40°C to + 85°C |
| Soldering Temperature and Time<br>10s (solder ball only) | + 260°C |

Notes:

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Table 5. Electrical Characteristics and Operating Conditions

Industrial Temperature (–40ºC < TC < +85ºC)

| Description | Conditions | Symbol | | MIN | MAX | Unit | Note |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | VDD | | 2.7 | 3.6 | V | |
| I/O Supply Voltage | | VDDQ | | 2.7 | 3.6 | V | |
| Input High Voltage | | VIH | | VDDQ-0.4 | VDDQ+0.2 | V | 1 |
| Input Low Voltage | | VIL | | -0.20 | 0.4 | V | 2 |
| Output High Voltage | IOH = -0.2mA | VOH | | 0.80 VDDQ | | V | |
| Output Low Voltage | IOL = +0.2mA | VOL | | | 0.20 VDDQ | V | |
| Input Leakage Current | VIN = 0 to VDDQ | ILI | | | 1 | uA | |
| Output Leakage Current | OE#=VIH or<br>Chip Disabled | ILO | | | 1 | uA | |
| **Operating Current** | **Conditions** | **Symbol** | | **Typ** | **MAX** | **Unit** | **Note** |
| Asynchronous Random READ/WRITE | VIN = VDDQ or 0V<br>Chip enabled,<br>IOUT = 0 | IDD1 | -70 | | 30 | mA | 3 |
| Asynchronous PAGE READ | | IDD1P | -70 | | 18 | mA | 3 |
| Standby Current | VIN=VDDQ or 0V<br>CE# = VDDQ | ISB | | | 180 | uA | 4 |

Notes:

1. Input signals may overshoot to VDDQ + 1.0V for periods less than 2ns during transitions.
2. Input signals may undershoot to Vss – 1.0V for periods less than 2ns during transitions.
3. This parameter is specified with the outputs disabled to avoid external loading effects. User must add required current to drive output capacitance expected in the actual system.
4. ISB (MAX) values measured with PAR set to FULL ARRAY at +85°C. In order to achieve low standby current, all inputs must be driven to either VDDQ or VSS. ISB might be set slightly higher for up to 500ms after power-up, or when entering standby mode.

### Table 6. Deep Power-Down Specifications

| Description | Conditions | Symbol | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Deep Power-Down | VIN=VDDQ or 0V; +25°C ZZ# = 0V, CR[4] = 0 | Izz | 3 | 10 | uA |

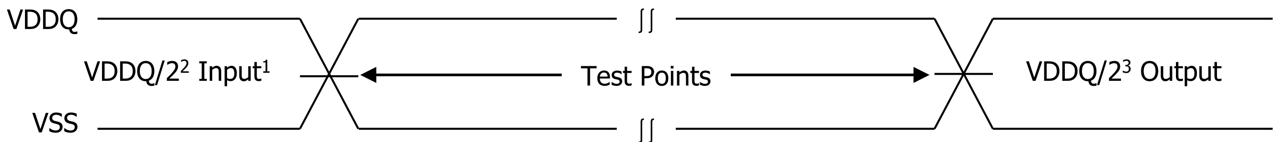
### Table 7. Capacitance

| Description | Conditions | Symbol | MIN | MAX | Unit | Note |
|---|---|---|---|---|---|---|
| Input Capacitance | Tc=+25°C; f=1Mhz; VIN=0V | $C_{IN}$ | 2.0 | 6.5 | pF | 1 |
| Input/Output Capacitance (DQ) | | $C_{IO}$ | 3.5 | 6.5 | pF | 1 |

Notes:

1. These parameters are verified in device characterization and are not 100% tested.

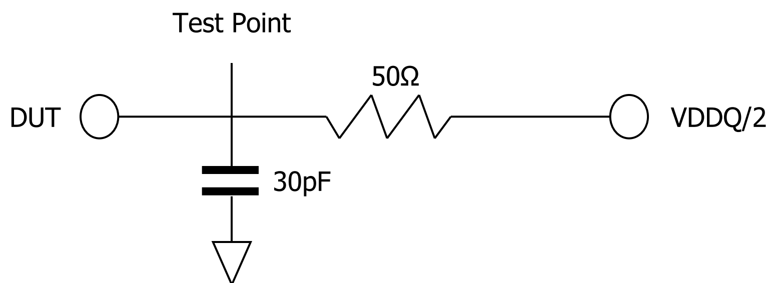
### Figure 8. AC Input/Output Reference Waveform




Notes:

1. AC test inputs are driven at VDDQ for a logic 1 and VSS for a logic 0. Input rise and fall times (10% to 90%) < 1.6ns.
2. Input timing begins at VDDQ/2.
3. Output timing ends at VDDQ/2.

### Figure 9. Output Load Circuit



## AC Characteristics

### Table 8 . Asynchronous READ Cycle Timing Requirements

| Symbol | Parameter | -70 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{AA}$ | Address Acess Time | | 70 | ns | |
| $t_{APA}$ | Page access Time | | 20 | ns | |
| $t_{BA}$ | LB# /UB# access Time | | 70 | ns | |
| $t_{BHZ}$ | LB#/UB# disable to High-Z output | | 8 | ns | 1 |
| $t_{BLZ}$ | LB#/UB# enable to Low-Z output | 10 | | ns | 2 |
| $t_{CEM}$ | Maximum CE# pulse width | | 8 | us | |
| $t_{CO}$ | Chip select access time | | 70 | ns | |
| $t_{HZ}$ | Chip disable to High-Z output | | 8 | ns | 1 |
| $t_{LZ}$ | Chip enable to Low-Z output | 10 | | ns | 2 |
| $t_{OE}$ | Output enable to valid output | | 20 | ns | |
| $t_{OH}$ | Output hold from address change | 5 | | ns | |
| $t_{OHZ}$ | Output disable to High-Z output | | 8 | ns | 1 |
| $t_{OLZ}$ | Output enable to Low-Z output | 3 | | ns | 2 |
| $t_{PC}$ | Page cycle time | 20 | | ns | |
| $t_{RC}$ | Read cycle time | 70 | | ns | |
| $t_{CPH}$ | CE# HIGH time Read | 5 | | ns | |

Notes:

1. Low-Z to High-Z timings are tested with the circuit shown in Figure 9. The High-Z timings measure a 100mV transition from either VOH or VOL toward VDDQ/2.
2. High-Z to Low-Z timings are tested with the circuit shown in Figure 9. The Low-Z timings measure a 100mV transition away from the High-Z (VDDQ/2) level toward either VOH or VOL.

**Table 9 . Asynchronous WRITE Cycle Timing Requirements**

| Symbol | Parameter | -70 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{AS}$ | Address setup Time | 0 | | ns | |
| $t_{AW}$ | Address valid to end of write | 70 | | ns | |
| $t_{BW}$ | Byte select to end of write | 70 | | ns | |
| $t_{CPH}$ | CE# HIGH time during write | 5 | | ns | |
| $t_{CW}$ | Chip enable to end of Write | 70 | | ns | |
| $t_{DH}$ | Data hold from write time | 0 | | ns | |
| $t_{DW}$ | Data write setup time | 23 | | ns | |
| $t_{LZ}$ | Chip enable to Low-Z output | 10 | | ns | 1 |
| $t_{OW}$ | End write to Low-Z output | 5 | | ns | 1 |
| $t_{WC}$ | Write cycle time | 70 | | ns | |
| $t_{WHZ}$ | Write to High-Z output | | 8 | ns | 2 |
| $t_{WP}$ | Write pulse width | 46 | | ns | 3 |
| $t_{WPH}$ | Write pulse width HIGH | 10 | | ns | |
| $t_{WR}$ | Write recovery time | 0 | | ns | |

Notes:

1. Low-Z to High-Z timings are tested with the circuit shown in Figure 9. The High-Z timings measure a 100mV transition from either VOH or VOL toward VDDQ/2.
2. High-Z to Low-Z timings are tested with the circuit shown in Figure 9. The Low-Z timings measure a 100mV transition away from the High-Z (VDDQ/2) level toward either VOH or VOL.
3. WE# LOW must be limited to $t_{CEM}$ (8us)

**Table10 . Load Configuration Register Timing Requirements**

| Symbol | Parameter | -70 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{AS}$ | Address setup time | 0 | | ns | |
| $t_{AW}$ | Address valid to end of write | 70 | | ns | |
| $t_{CDZZ}$ | Chip deselect to ZZ# LOW | 5 | | ns | |
| $t_{CW}$ | Chip enable to end of write | 70 | | ns | |
| $t_{WC}$ | Write cycle time | 70 | | ns | |
| $t_{WP}$ | Write pulse width | 46 | | ns | |
| $t_{WR}$ | Write recovery time | 0 | | ns | |
| $t_{ZZWE}$ | ZZ# LOW to WE# LOW | 10 | 500 | ns | |

**Table11 . DPD Timing Requirements**

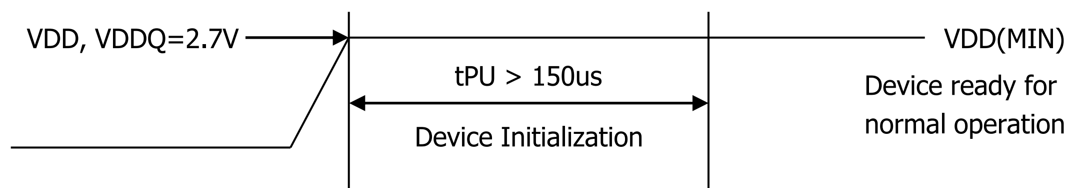
| Symbol | Parameter | -70 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{CDZZ}$ | Chip deselect to ZZ# LOW | 5 | | ns | |
| $t_R$ | Deep Power-down recovery | 150 | | us | |
| $t_{ZZ}$( MIN) | Minimum ZZ# pulse width | 10 | | us | |

**Table12 . Initialization Timing Requirements**

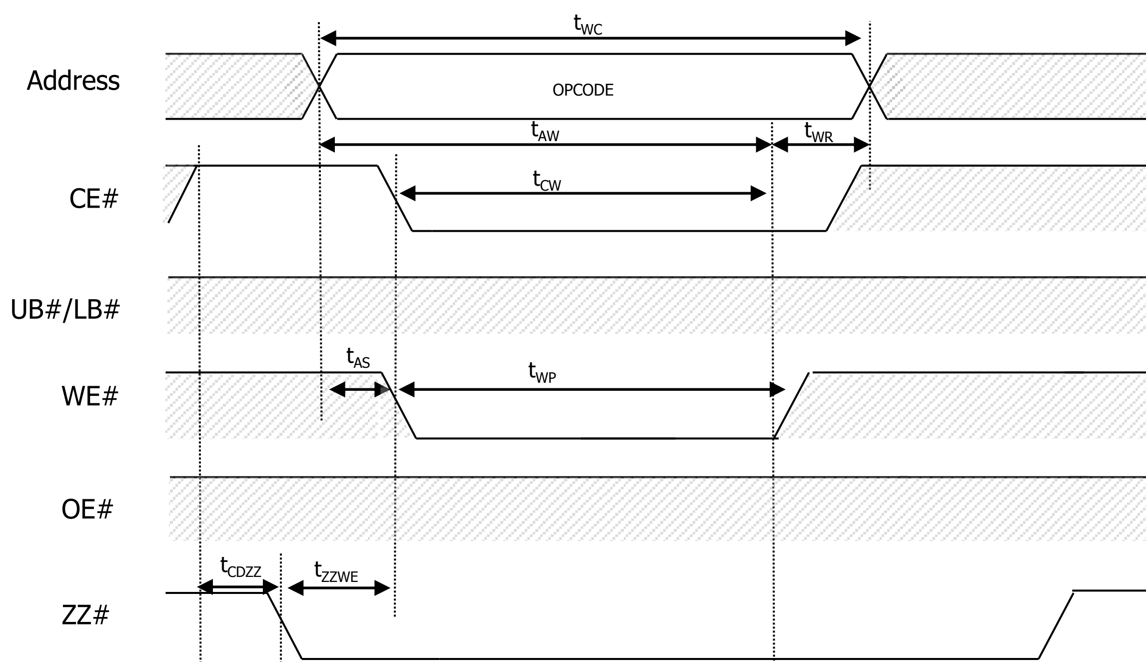
| Symbol | Parameter | -70 | | Unit | Notes |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $t_{PU}$ | Initialization Period (required before normal operations) | | 150 | us | |

# Timing Diagrams

### Figure 10: Power-Up Initialization Timing




### Figure 11: Load Configuration Register




### Figure 12: DPD Entry and Exit Timing

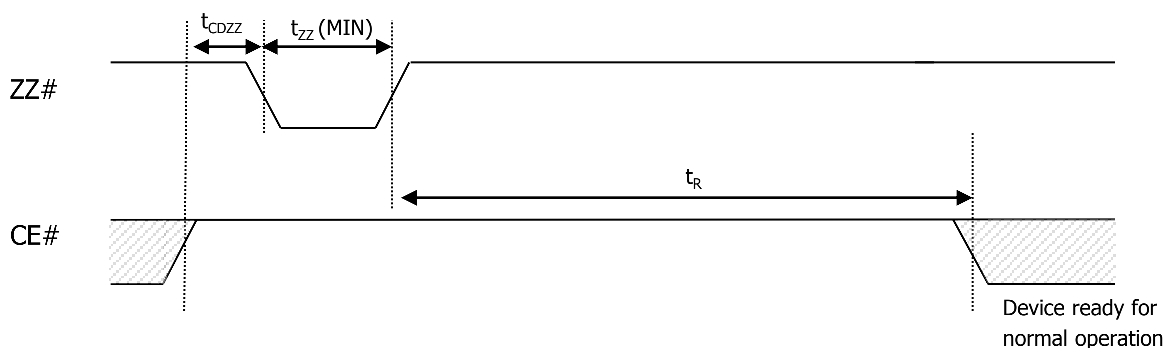


**Figure 13: Single Read Operation**

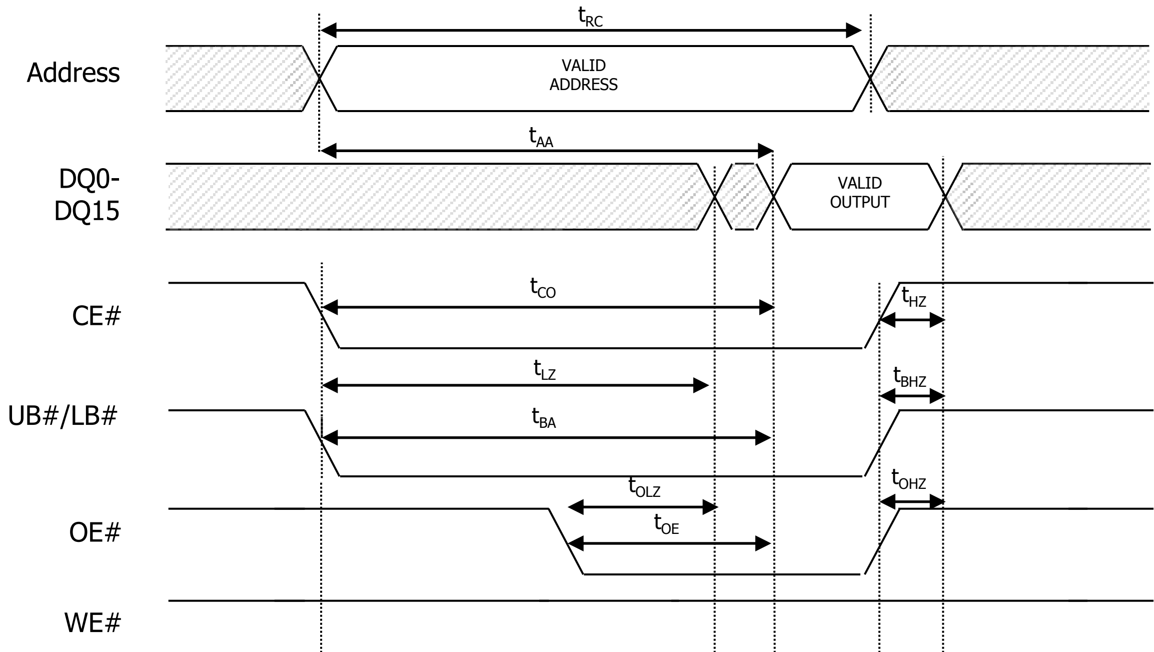



**Figure 14: PAGE MODE READ**

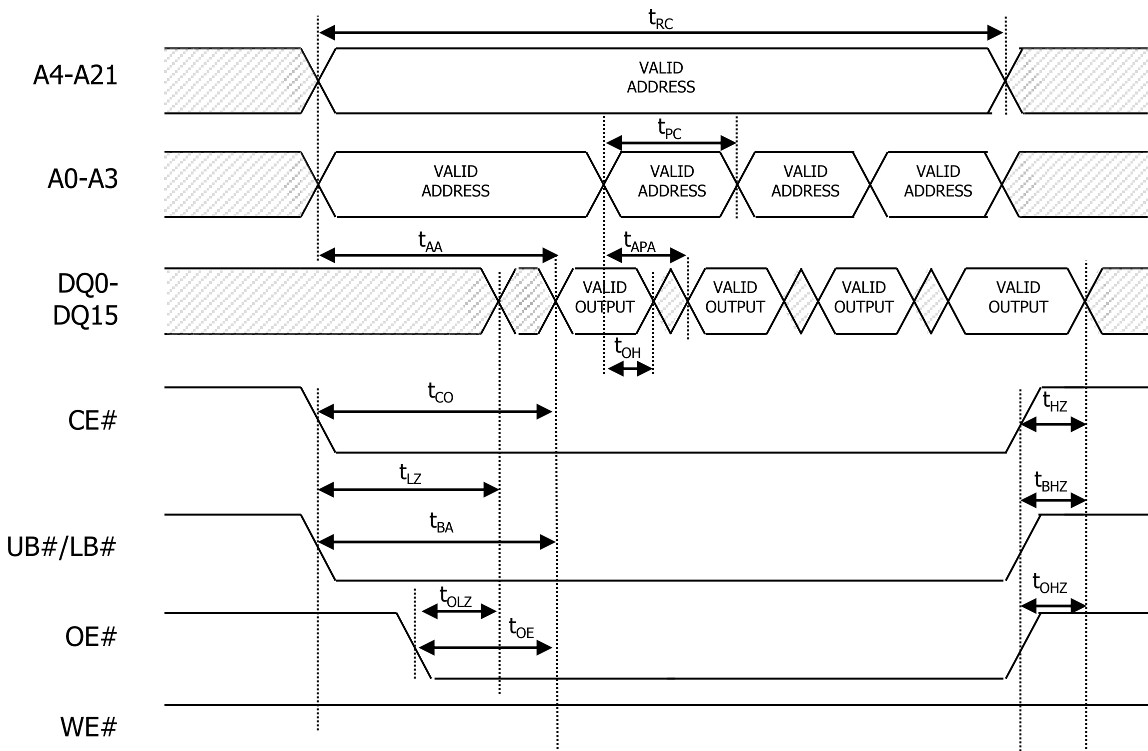


**Figure 15: CE#-Controlled Asynchronous WRITE**

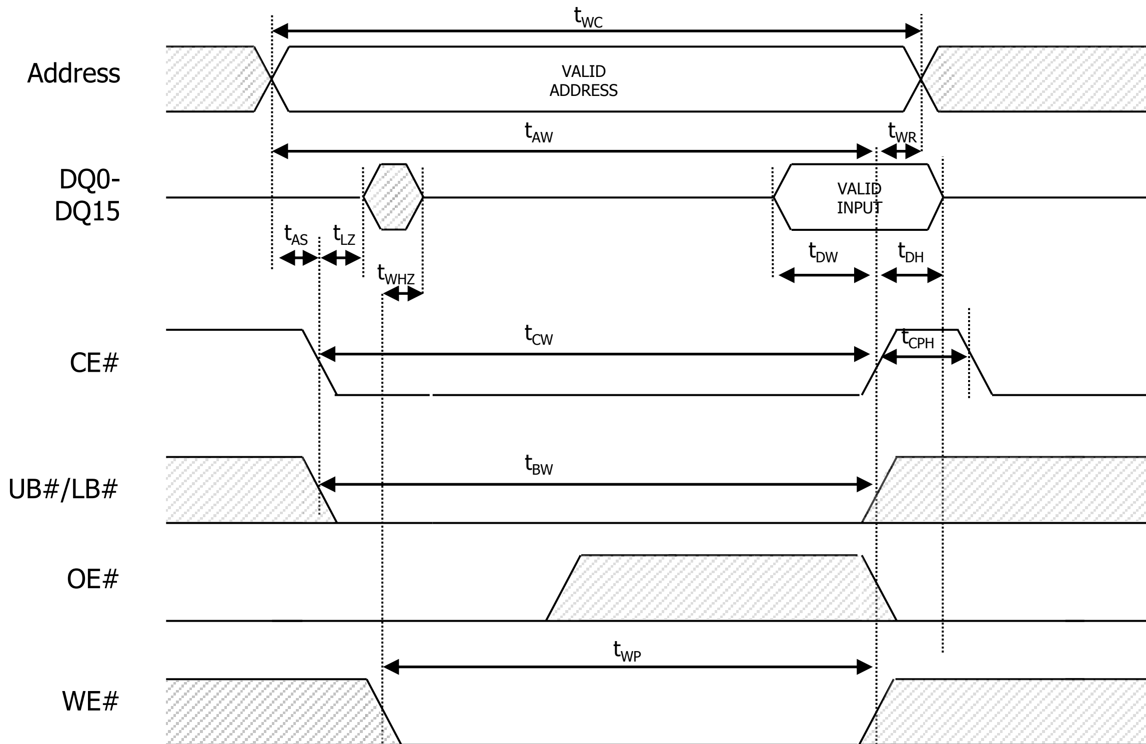


**Figure 16: LB#/UB#-Controlled Asynchronous WRITE**

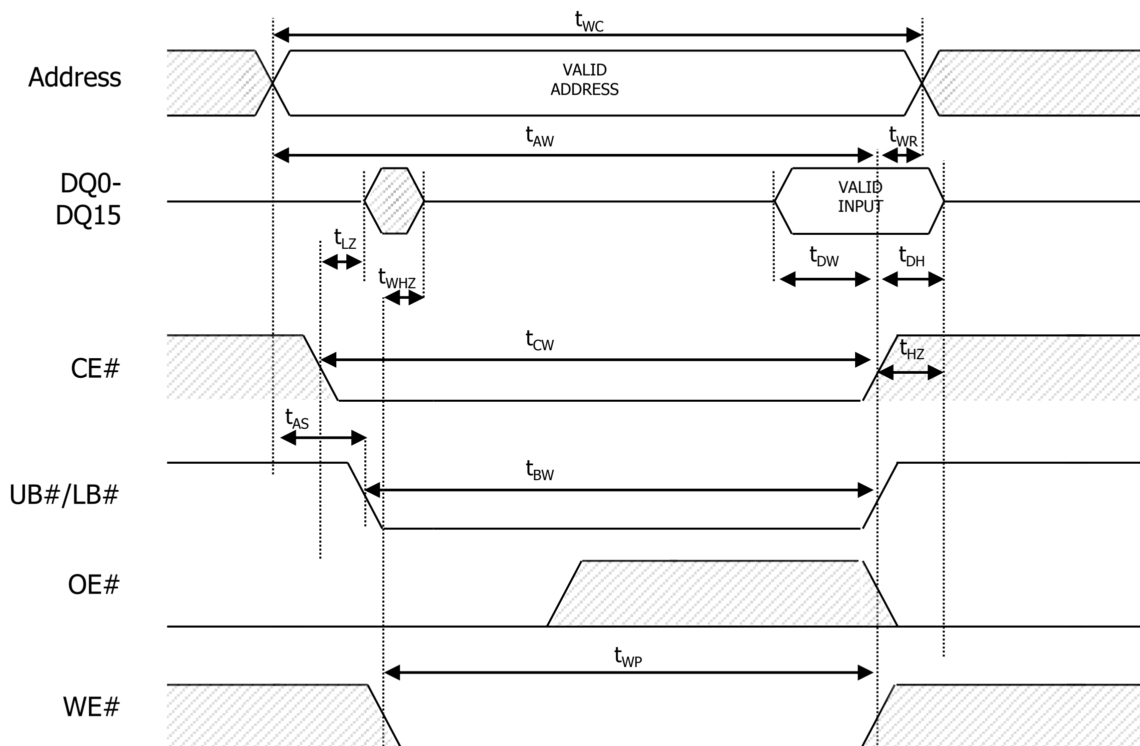
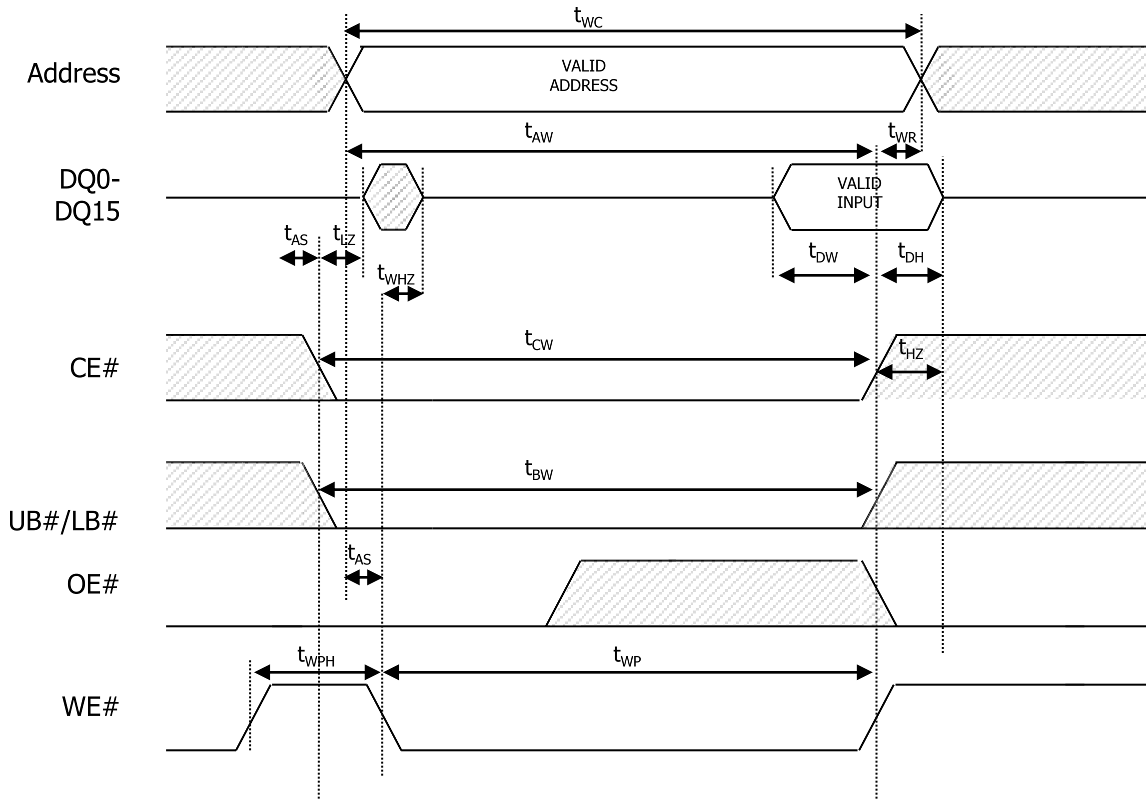


**Figure 17: WE#-Controlled Asynchronous WRITE**



## Ordering Information – VDD = 3.0V

### Industrial Temperature Range: (-40°C to +85°C)

| Config. | Speed (ns) | Order Part No. | Package |
|---|---|---|---|
| 4Mx16 | 70 | IS66WVE4M16BLL-70BLI | 48-ball TFBGA, Lead-free |

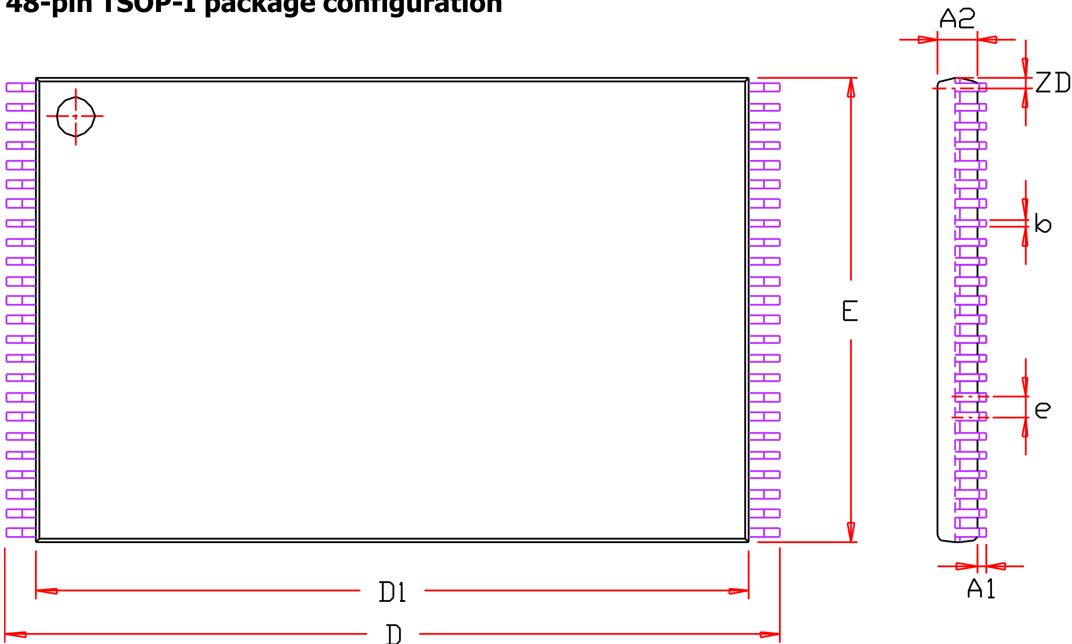
### Automotive Temperature Range: (-40°C to +85°C)

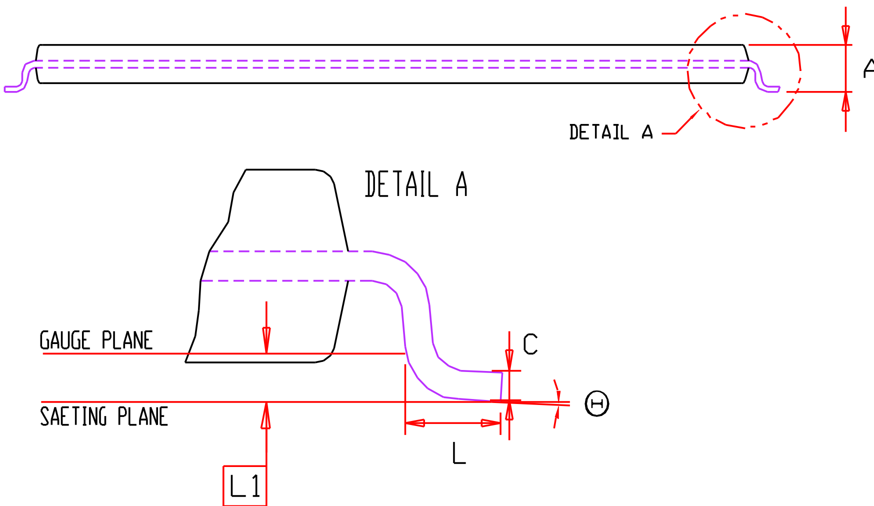
| Config. | Speed (ns) | Order Part No. | Package |
|---|---|---|---|
| 4Mx16 | 70 | IS67WVE4M16BLL-70BLA1 | 48-ball TFBGA, Lead-free |

**Notes:**

1. The 48-pin TSOP-I package option is not yet available. Please contact SRAM Marketing at sram@issi.com for additional information.

## 48-pin TSOP-I package configuration

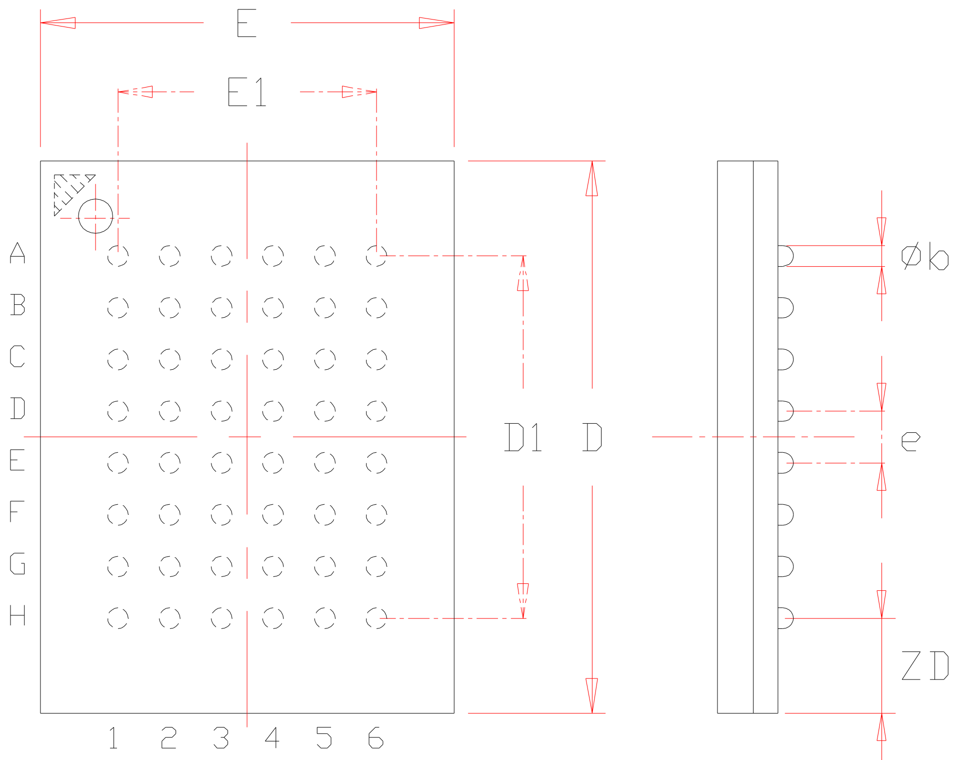


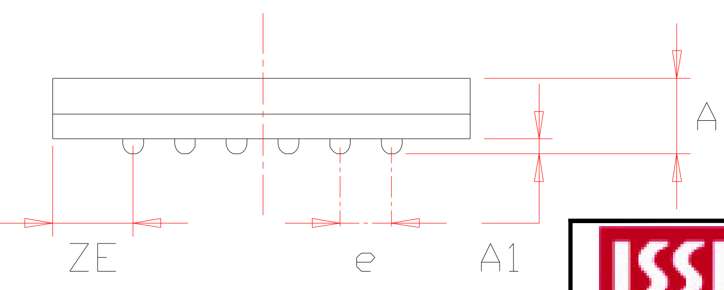




| SYMBOL | DIMENSION IN MM | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | | | 1.20 |
| A1 | 0.05 | | 0.15 |
| b | 0.17 | 0.22 | 0.27 |
| C | 0.10 | | 0.21 |
| D | 19.80 | 20.00 | 20.20 |
| D1 | 18.20 | 18.40 | 18.60 |
| E | 11.80 | 12.00 | 12.20 |
| e | 0.50 BSC. | | |
| L | 0.50 | 0.60 | 0.70 |
| L1 | 0.25 BSC. | | |
| ZD | 0.25 REF. | | |
| Θ | 0 | 3° | 5° |

**NOTE :**

1. Controlling dimension : mm
2. Dimension D1 and E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.




| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.20 | | 0.30 | 0.008 | | 0.012 |
| Øb | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D1 | 5.25 BSC | | | 0.207 BSC | | |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E1 | 3.75 BSC | | | 0.148 BSC | | |
| e | 0.75 BSC. | | | 0.030 BSC. | | |
| ZD | 1.375 REF. | | | 0.054 REF. | | |
| ZE | 1.125 REF. | | | 0.044 REF. | | |

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207

| TITLE | 48L 6x8mm TF-BGA Package Outline | REV. | C | DATE | 08/12/2008 |
|---|---|---|---|---|---|