80V, 500mA, 3-Phase MOSFET Driver

HIP4086, HIP4086A

The HIP4086 and HIP4086A (referred to as the HIP4086/A) are three phase N-Channel MOSFET drivers. Both parts are specifically targeted for PWM motor control. These drivers have flexible input protocol for driving every possible switch combination. The user can even override the shoot-through protection for switched reluctance applications.

The HIP4086/A have a wide range of programmable dead times (0.5ms to 4.5ms) which makes them very suitable for the low frequencies (up to 100kHz) typically used for motor drives.

The only difference between the HIP4086 and the HIP4086A is that the HIP4086A has the built-in charge pumps disabled. This is useful in applications that require very quiet EMI performance (the charge pumps operate at 10MHz). The advantage of the HIP4086 is that the built-in charge pumps allow indefinitely long on times for the high-side drivers.

To insure that the high-side driver boot capacitors are fully charged prior to turning on, a programmable bootstrap refresh pulse is activated when VDD is first applied. When active, the refresh pulse turns on all three of the low-side bridge FETs while holding off the three high-side bridge FETs to charge the high-side boot capacitors. After the refresh pulse clears, normal operation begins.

Another useful feature of the HIP4086/A is the programmable undervoltage set point. The set point range varies from 6.6V to 8.5V.

Features

- Independently drives 6 N-Channel MOSFETs in three phase bridge configuration
- Bootstrap supply max voltage up to 95VDC with bias supply from 7V to 15V
- 1.25A peak turn-off current
- User programmable dead time (0.5µs to 4.5µs)
- Bootstrap and optional charge pump maintain the high-side driver bias voltage.
- Programmable bootstrap refresh time
- Drives 1000pF load with typical rise time of 20ns and Fall Time of 10ns
- Programmable undervoltage set point

Applications

- Brushless Motors (BLDC)
- 3-phase AC motors
- Switched reluctance motor drives
- Battery powered vehicles
- Battery powered tools

Related Literature

AN9642 “HIP4086 3-Phase Bridge Driver Configurations and Applications”

”HIP4086EVAL Evaluation Board Application Note” (Coming Soon)

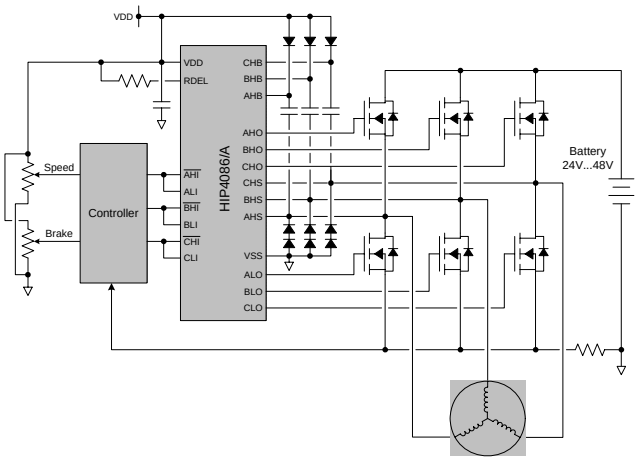


FIGURE 1. TYPICAL APPLICATION

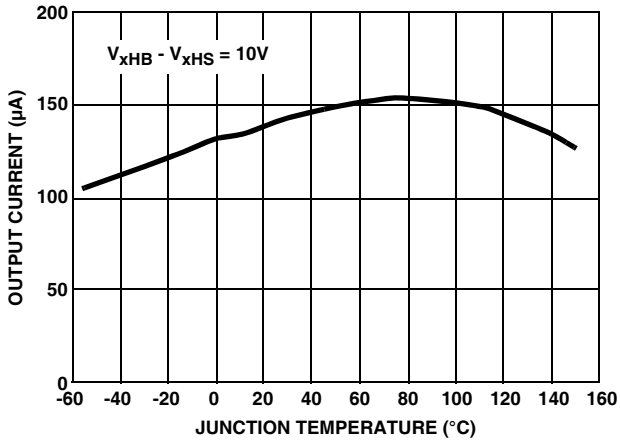
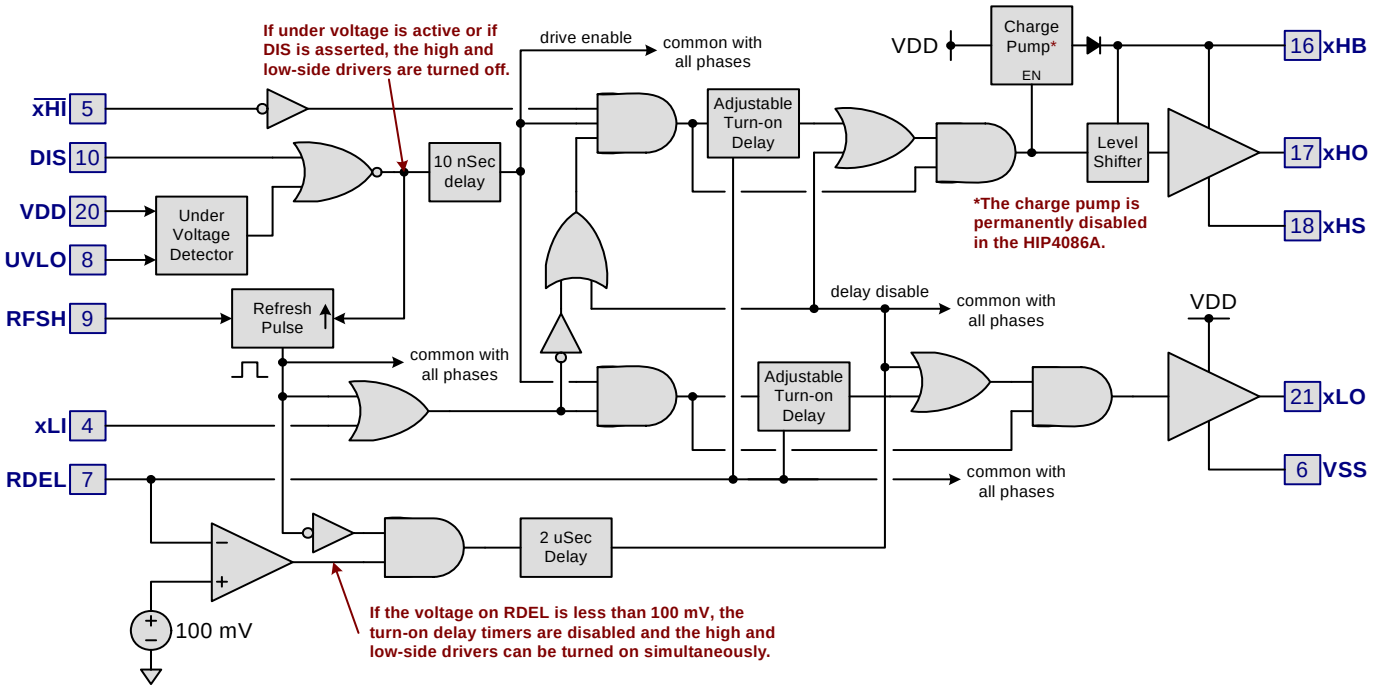


FIGURE 2. CHARGE PUMP OUTPUT CURRENT

Block Diagram (for clarity, only one phase is shown)



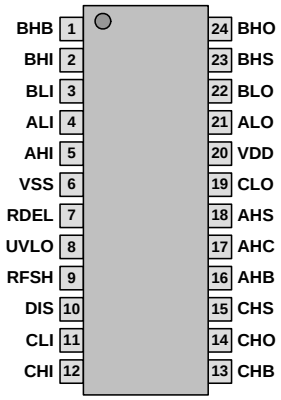
Truth Table

INPUT					OUTPUT	
ALI, BLI, CLI	$\overline{AHI}$, $\overline{BHI}$, $\overline{CHI}$	UV	DIS	RDEL	ALO, BLO, CLO	AHO, BHO, CHO
X	X	X	1	X	0	0
X	X	1	X	X	0	0
1	X	0	0	>100mV	1	0
0	0	0	0	X	0	1
0	1	0	0	X	0	0
1	0	0	0	<100mV	1	1

NOTE: X signifies that input can be either a “1” or “0”.

Pin Configuration

HIP4086, HIP4086A
(PDIP, SOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
16 1 13	AHB BHB CHB (xHB)	High-Side Bias Connections. One external bootstrap diode and one capacitor are required for each. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to each xHB pin.
15 23 15	AHS BHS CHS (xHS)	High-Side Source Connections. Connect the sources of the High-Side power MOSFETs to these pins. The negative side of the bootstrap capacitors are also connected to these pins.
5 2 12	$\overline{\text{AHI}}$ $\overline{\text{BHI}}$ $\overline{\text{CHI}}$ ($\overline{\text{xHI}}$)	High-Side Logic Level Inputs. Logic at these three pins controls the three high side output drivers, AHO (Pin 17), BHO (Pin 24) and CHO (Pin 14). When $\overline{\text{xHI}}$ is low, xHO is high. When $\overline{\text{xHI}}$ is high, xHO is low. Unless the dead time is disabled by connecting RDEL (Pin 7) to ground, the low side input of each phase will override the corresponding high side input on that phase - see “Truth Table” on page 2. If RDEL is tied to ground, dead time is disabled and the outputs follow the inputs with no shoot-thru protection. DIS (Pin 10) also overrides the high side inputs. $\overline{\text{xHI}}$ can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
4 3 11	ALI BLI CLI (xLI)	Low-Side Logic Level Inputs. Logic at these three pins controls the three low-side output drivers ALO (Pin 21), BLO (Pin 22) and CLO (Pin 19). If the upper inputs are grounded then the lower inputs control both xLO and xHO drivers, with the dead time set by the resistor at RDEL (Pin 7). DIS (Pin 10) high level input overrides xLI, forcing all outputs low. xLI can be driven by signal levels of 0V to 15V (no greater than V_{DD}).
6	V_{SS}	Ground. Connect the sources of the Low-Side power MOSFETs to this pin.
7	RDEL	Delay Time Set point. Connect a resistor from this pin to V_{DD} to set timing current that defines the dead time between drivers - see Figure 17. All drivers turn-off with minimal delay, RDEL resistor prevents shoot-through by delaying the turn-on of all drivers. When RDEL is tied to V_{SS}, both upper and lowers can be commanded on simultaneously. While not necessary in most applications, a decoupling capacitor of 0.1µF or smaller may be connected between RDEL and V_{SS}.
8	UVLO	Under voltage Set point. A resistor can be connected between this pin and V_{SS} to program the under voltage set point, see Figure 18. With this pin not connected, the under voltage disable is typically 6.6V. When this pin is tied to V_{DD}, the under voltage disable is typically 6.2V.
9	RFSH	Refresh Pulse Setting. An external capacitor can be connected from this pin to V_{SS} to increase the length of the start up refresh pulse - see Figure 16. If this pin is not connected, the refresh pulse is typically 1.5µs.
10	DIS	Disable Input. Logic level input that when taken high sets all six outputs low. DIS high overrides all other inputs. With DIS low, the outputs are controlled by the other inputs. DIS can be driven by signal levels of 0V to 15V (no greater than V_{DD}).

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
17 24 14	AHO BHO CHO (xHO)	High-Side Outputs. Connect to the gates of the High-Side power MOSFETs in each phase.
20	V_{DD}	Positive Supply. Decouple this pin to V_{SS} (Pin 6).
21 22 19	ALO BLO CLO (xLO)	Low-Side Outputs. Connect the gates of the Low-Side power MOSFETs to these pins.

NOTE: x = A, B or C.

Ordering Information

PART NUMBER (Notes 1, 3)	PART MARKING	TEMP RANGE (°C)	CHARGE PUMP	PACKAGE	PKG. DWG. #
HIP4086AB	HIP4086AB	-40 to +125	Yes	24 Ld SOIC	M24.3
HIP4086ABZ (Note 2)	HIP4086ABZ	-40 to +125	Yes	24 Ld SOIC (Pb-free)	M24.3
HIP4086APZ (Note 2)	HIP4086APZ	-40 to +125	Yes	24 Ld PDIP (Pb-free)	E24.3
HIP4086AABZ (Note 2)	HIP4086AABZ	-40 to +125	No	24 Ld SOIC (Pb-free)	M24.3
HIP4086EVAL	Evaluation Board				

NOTES:

1. Add "-T*", suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for HIP4086, HIP4086A. For more information on MSL, please see Technical Brief TB363.

Absolute Maximum Ratings

(Note 7)

Supply Voltage, V_{DD} Relative to GND . . . . . -0.3V to 16V
Logic Inputs (xLI, $\overline{xHI}$) . . . . . GND - 0.3v to V_{DD} + 0.3V
Voltage on xHS . . . . . -6V (Transient) to 85V (-40°C to +150°C)
Voltage on xHB . . . . . V_{xHS} - 0.3V to V_{xHS} +VDD
Voltage on xLO . . . . . V_{SS} - 0.3V to V_{DD} +0.3V
Voltage on xHO . . . . . V_{xHS} - 0.3V to V_{xHB} +0.3V
Phase slew rate (on xHS) 20V/ns

Maximum Recommended Operating Conditions

Supply Voltage, V_{DD} Relative to GND . . . . . 7V to 15V
Logic Inputs (xLI, $\overline{xHI}$) . . . . . 0V to VDD
Voltage on xHB . . . . . VxHS + VDD
Voltage on xHS . . . . . 0V to 80V
Ambient Temperature Range . . . . . -40°C to +125°C
Junction Temperature Range . . . . . -40°C to +150°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Notes 4, 6)	75	22
SOIC Package HIP4086AABZ (Notes 5, 6)	51	22
PDIP* Package (Notes 4, 6)	70	29

Storage Temperature Range . . . . . -65°C to +150°C
Operating Junction Temp Range . . . . . -40°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.
7. Replace x with A, B, or C.

DC Electrical Specifications

$V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $R_{DEL} = 20k$, $R_{UV} = \infty$, Gate Capacitance (C_{GATE}) = 1000pF, unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +150°C.**

PARAMETER	TEST CONDITIONS	T_J = +25°C			T_J = -40°C TO +150°C		UNITS
		MIN (Note 9)	TYP	MAX (Note 9)	MIN (Note 9)	MAX (Note 9)	
SUPPLY CURRENTS							
V_{DD} Quiescent Current	$\overline{xHI}$ = 5V, xLI = 5V (HIP4086)	2.7	3.4	4.2	**2.1**	**4.3**	mA
	$\overline{xHI}$ = 5V, xLI = 5V (HIP4086A)	2.3	2.4	2.6	**2.1**	**2.7**	mA
V_{DD} Operating Current	f = 20kHz, 50% Duty Cycle (HIP4086)	6.3	8.25	10.5	**5**	**11**	mA
	f = 20kHz, 50% Duty Cycle (HIP4086A)	3.1	3.6	4.1	**2.8**	**4.4**	mA
xHB On Quiescent Current	$\overline{xHI}$ = 0V (HIP4086)	-	40	80	-	**100**	µA
	$\overline{xHI}$ = 0V (HIP4086A)		80	100		**200**	µA
xHB Off Quiescent Current	$\overline{xHI}$ = V_{DD} (HIP4086)	0.6	0.8	1.3	**0.5**	**1.4**	mA
	$\overline{xHI}$ = V_{DD} (HIP4086A)	0.8	0.9	1	**0.7**	**1.2**	mA
xHB Operating Current	f = 20kHz, 50% Duty Cycle (HIP4086)	0.7	0.9	1.3	-	**2.0**	mA
	f = 20kHz, 50% Duty Cycle (HIP4086A)	0.8	0.9	1	-	**1.2**	mA
xHB, xHS Leakage Current	V_{xHS} = 80V, V_{xHB} = 93V	7	24	45	-	**50**	µA
Charge Pump, HIP4086 only, (Note 8)							
Q_{PUMP} Output Voltage	No Load	11.5	12.5	14	**10.5**	**14.5**	V
Q_{PUMP} Output Current	V_{xHS} = 12V, V_{xHB} = 22V	50	100	130	-	**140**	µA
UNDERVOLTAGE PROTECTION							
V_{DD} Rising Undervoltage Threshold	R_{UV} open	6.2	7.1	8.0	**6.1**	**8.1**	V
V_{DD} Falling Undervoltage Threshold	R_{UV} open	5.75	6.6	7.5	**5.6**	**7.6**	V
Minimum Undervoltage Threshold	R_{UV} = V_{DD}	5	6.2	6.8	**4.9**	**6.9**	V

DC Electrical Specifications

$V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $R_{DEL} = 20k$, $R_{UV} = \infty$, Gate Capacitance (C_{GATE}) = 1000pF, unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +150°C. (Continued)**

PARAMETER	TEST CONDITIONS	T_J = +25°C			T_J = -40°C TO +150°C		UNITS
		MIN (Note 9)	TYP	MAX (Note 9)	MIN (Note 9)	MAX (Note 9)	
INPUT PINS: ALI, BLI, CLI, $\overline{AHI}$, $\overline{BHI}$, $\overline{CHI}$, AND DIS							
Low Level Input Voltage		-	-	1.0	-	**0.8**	V
High Level Input Voltage		2.5	-	-	**2.7**	-	V
Input Voltage Hysteresis		-	35	-	-	-	mV
Low Level Input Current	V_{IN} = 0V	-60	-100	-135	**-55**	**-140**	µA
High Level Input Current	V_{IN} = 5V	-1	-	+1	**-10**	**+10**	µA
GATE DRIVER OUTPUT PINS: ALO, BLO, CLO, AHO, BHO, AND CHO							
Low Level Output Voltage (V_{OUT} - V_{SS})	$I_{SINKING}$ = 30mA	-	100	-	-	**200**	mV
Peak Turn-On Current	V_{OUT} = 0V	0.3	0.5	0.7	-	**1.0**	A

NOTES:

8. the specified charge pump current is the total amount available to drive external loads across xHO and xHS.
9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications

$V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $C_{GATE} = 1000pF$, $R_{DEL} = 10k$, unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +150°C.**

PARAMETER	TEST CONDITIONS	T_J = +25°C			T_J = -40°C TO +150°C		UNITS
		MIN (Note 9)	TYP	MAX (Note 9)	MIN (Note 9)	MAX (Note 9)	
TURN-ON DELAY AND PROPAGATION DELAY							
Dead Time (Figure 3)	R_{DEL} = 100k	3.8	4.5	6	**3**	**7**	µs
	R_{DEL} = 10k	0.38	0.5	0.65	**0.3**	**0.7**	µs
Dead Time Channel Matching	R_{DEL} = 10k	-	7	15	-	**20**	%
Lower Turn-Off Propagation Delay (xLI to xLO turn-off) (Figure 3 or 4)	No Load	-	30	45	-	**65**	ns
Upper Turn-Off Propagation Delay ($\overline{xHI}$ to xHO turn-off) (Figure 3 or 4)	No Load	-	75	90	-	**100**	ns
Lower Turn-On Propagation Delay (xLI to xLO turn-on) (Figure 3 or 4)	No Load	-	45	75	-	**90**	ns
Upper Turn-On Propagation Delay ($\overline{xHI}$ to xHO turn-on) (Figure 3 or 4)	No Load	-	65	90	-	**100**	ns
Rise Time	C_{GATE} = 1000pF	-	20	40	-	**50**	ns
Fall Time	C_{GATE} = 1000pF	-	10	20	-	**25**	ns
Disable Turn-Off Propagation Delay (DIS to xLO turn-off) (Figure 5)		-	55	80	-	**90**	ns
Disable Turn-Off Propagation Delay (DIS to xHO turn-off) (Figure 5)		-	80	90	-	**100**	ns
$\overline{Disable}$ to Lower Turn-On Propagation Delay ($\overline{DIS}$ to xLO turn-on) (Figure 5)		-	55	80	-	**100**	ns
$\overline{Disable}$ to Upper Enable ($\overline{DIS}$ to xHO turn-on) (Figure 5)	R_{DEL} = 10k, C_{RFSH} Open	-	2.0	-	-	-	µs

Test Waveforms and Timing Diagrams

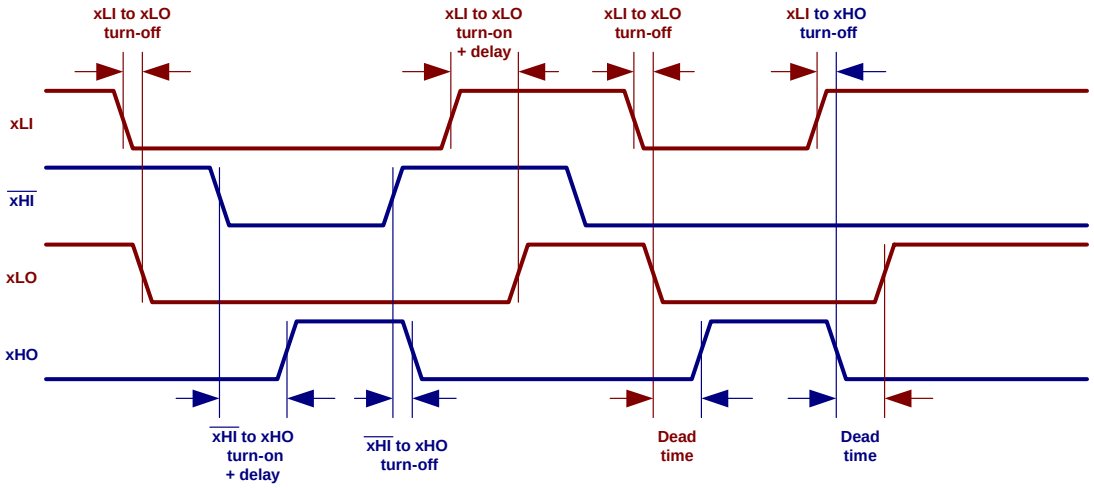


FIGURE 3. PROP DELAYS WITH PROGRAMMED TURN-ON DELAYS (RDEL CONNECTED TO VDD WITH A RESISTOR)

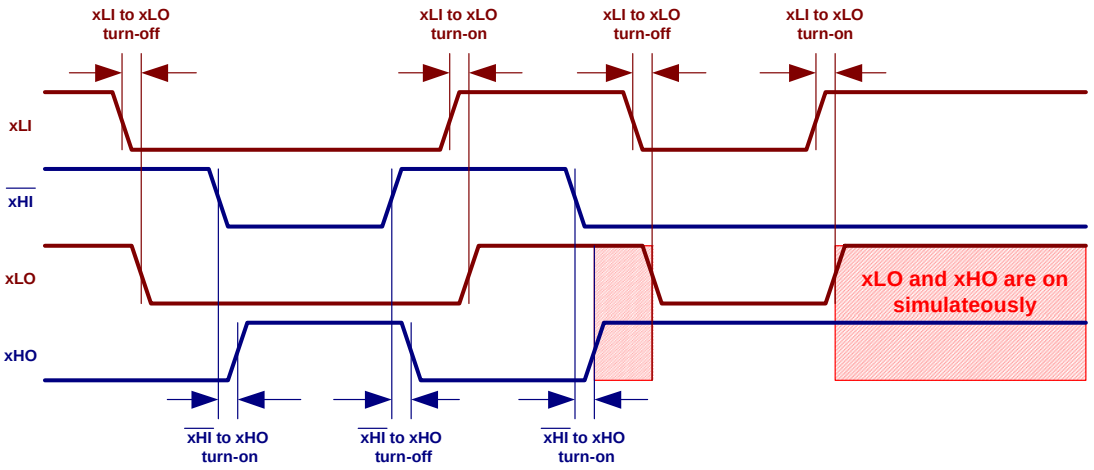


FIGURE 4. PROP DELAYS WITH NO PROGRAMMED TURN-ON DELAYS (RDEL CONNECTED TO VSS)

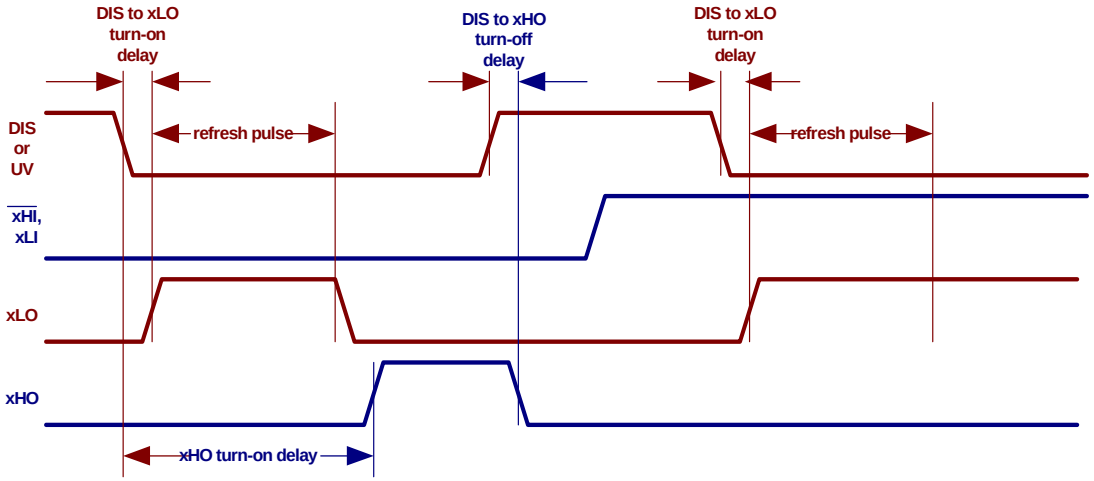


FIGURE 5. DISABLE FUNCTION

Typical Performance Curves

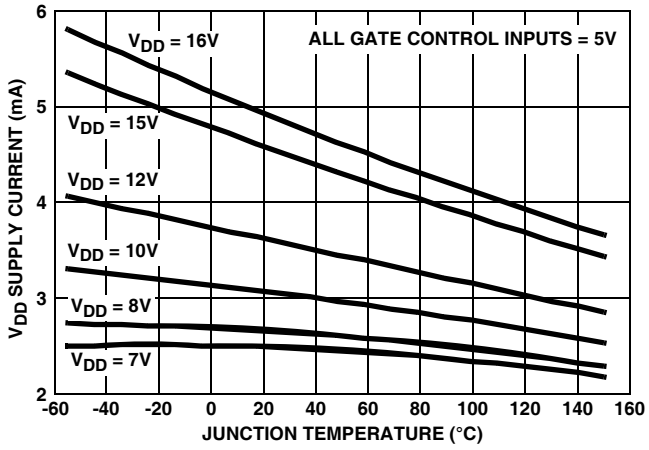


FIGURE 6. V_{DD} SUPPLY CURRENT vs V_{DD} SUPPLY VOLTAGE

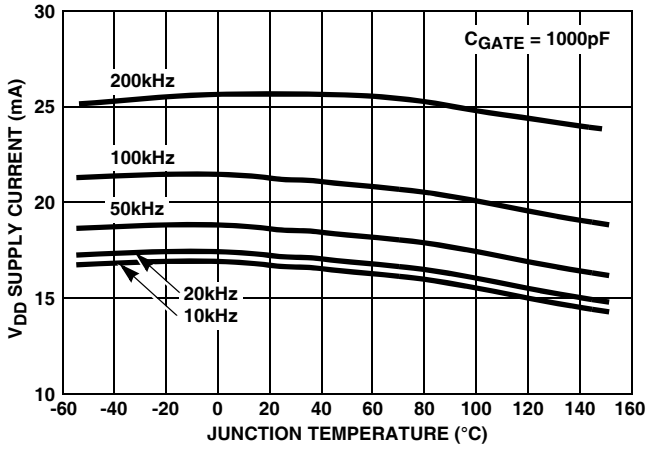


FIGURE 7. V_{DD} SUPPLY CURRENT vs SWITCHING FREQUENCY

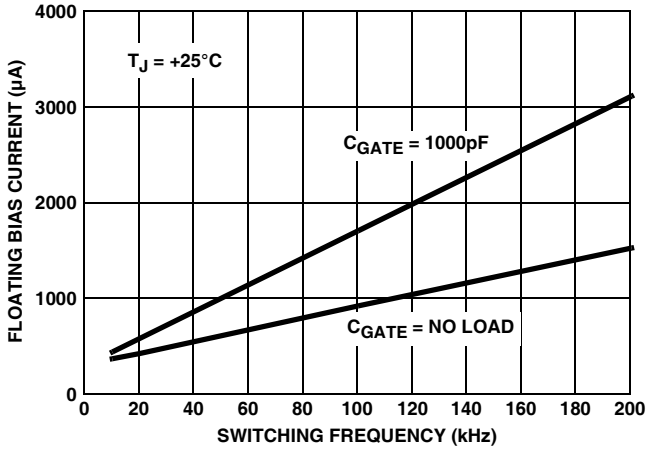


FIGURE 8. FLOATING I_{XHB} BIAS CURRENT

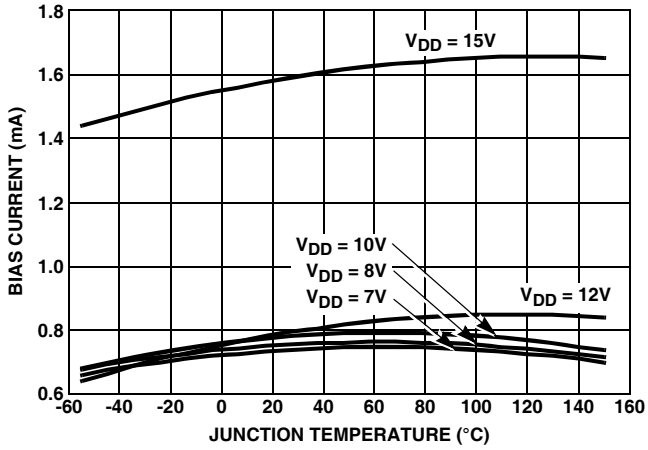


FIGURE 9. OFF-STATE I_{XHB} BIAS CURRENT

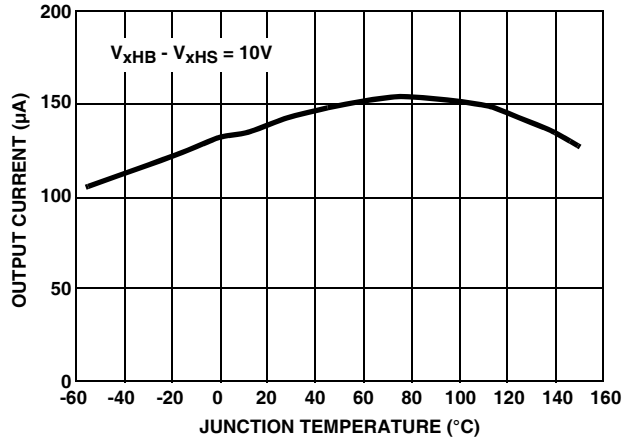


FIGURE 10. CHARGE PUMP OUTPUT CURRENT (HIP4086 only)

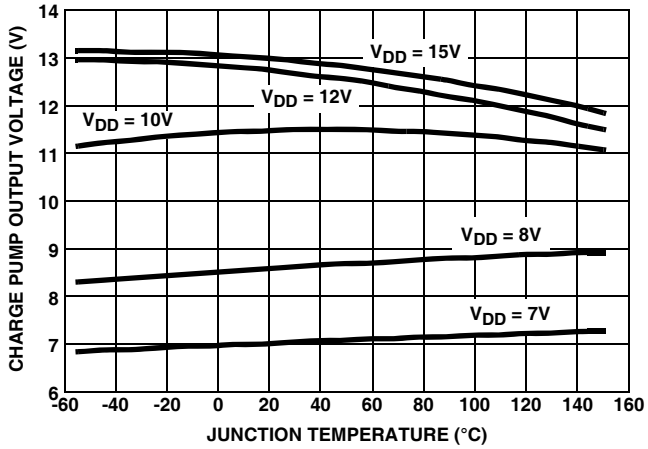


FIGURE 11. CHARGE PUMP OUTPUT VOLTAGE(HIP4086 only)(

Typical Performance Curves (Continued)

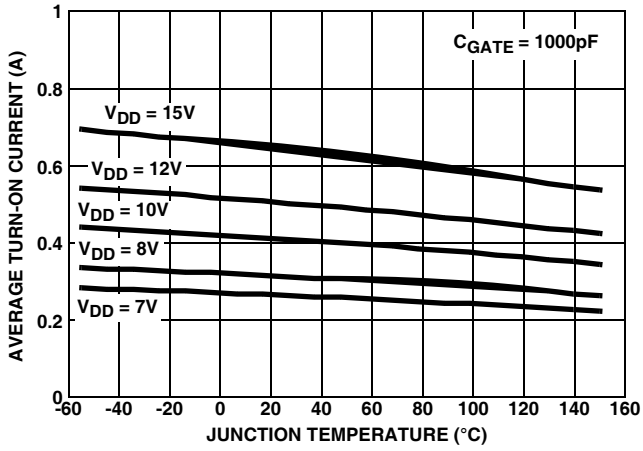


FIGURE 12. AVERAGE TURN-ON CURRENT (0 TO 5V)

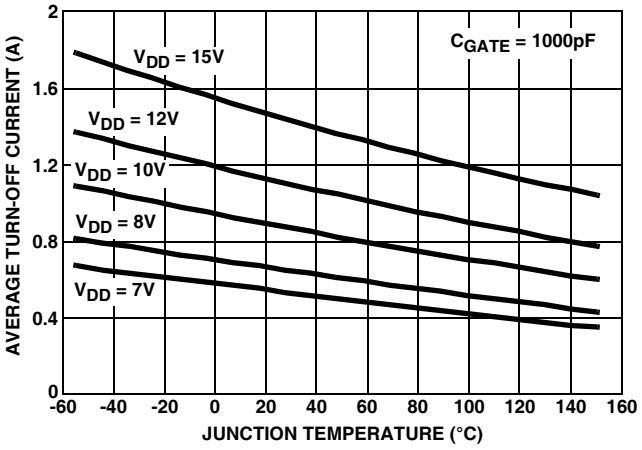


FIGURE 13. AVERAGE TURN-OFF CURRENT (V_{DD} TO 4V)

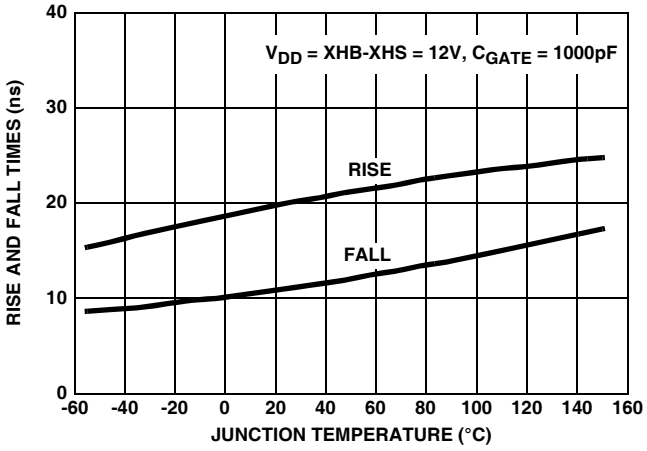


FIGURE 14. RISE AND FALL TIMES (10 to 90%)

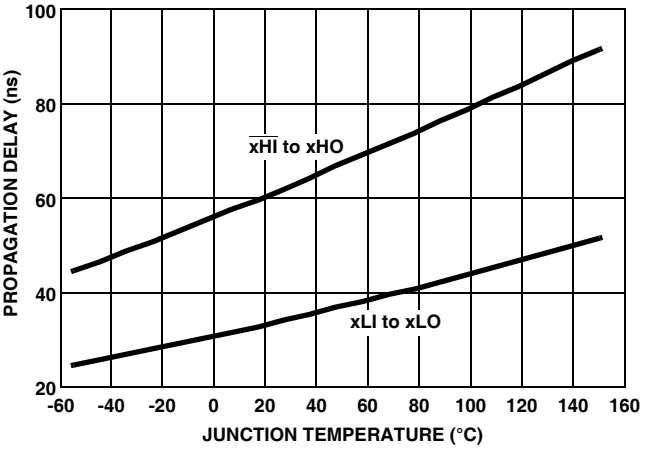


FIGURE 15. PROPAGATION DELAY

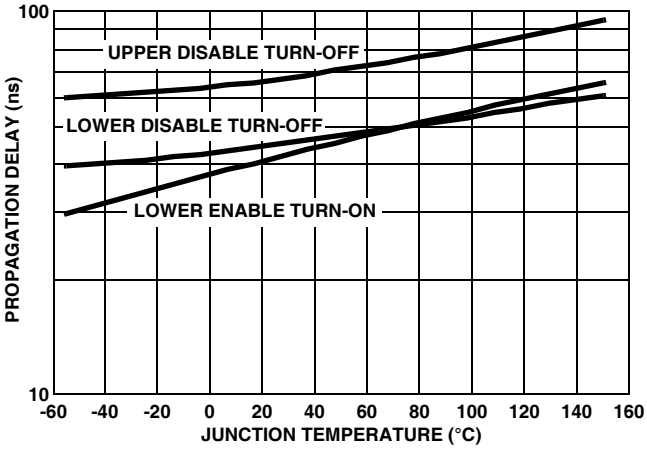


FIGURE 16. DISABLE PIN PROPAGATION DELAY

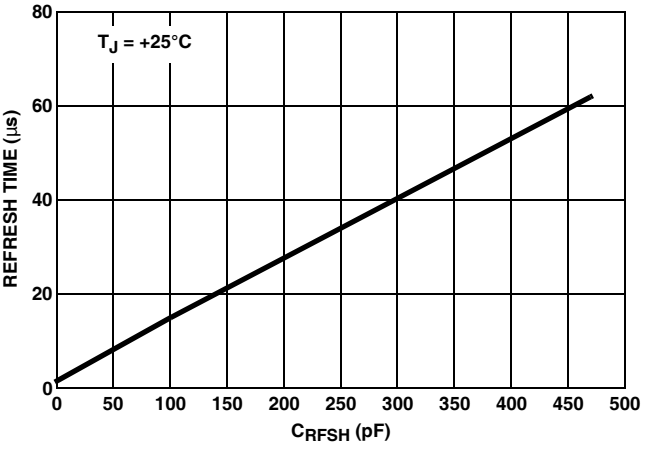


FIGURE 17. REFRESH TIME

Typical Performance Curves (Continued)

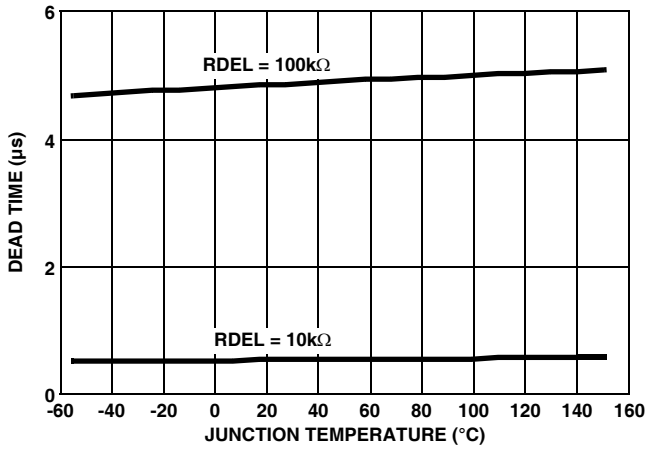


FIGURE 18. DEAD TIME

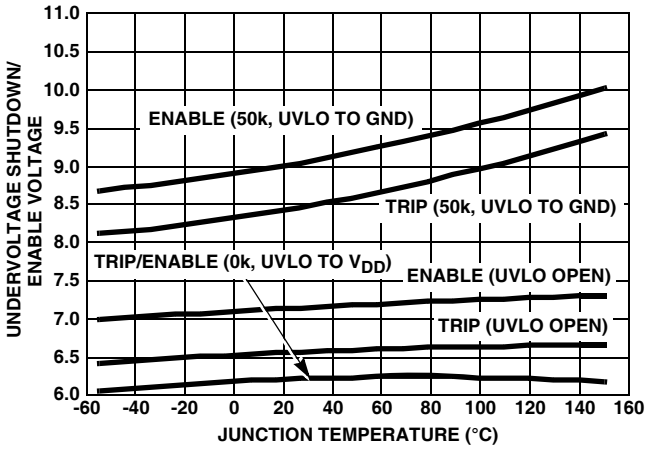


FIGURE 19. UNDERVOLTAGE THRESHOLD

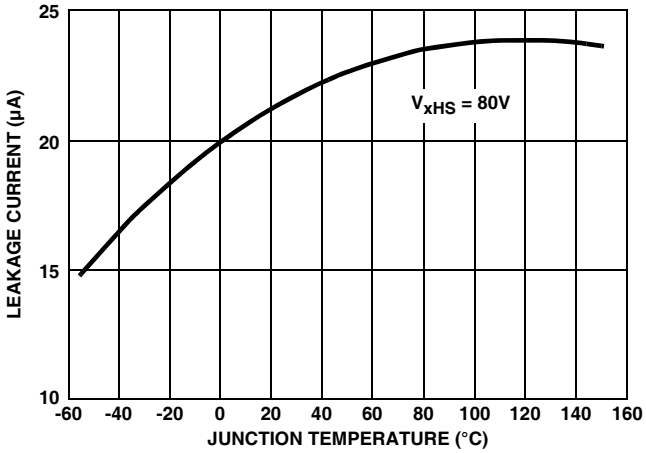


FIGURE 20. I_{xHS} LEAKAGE CURRENT

Functional Description

Input Logic

NOTE: When appropriate for brevity, input and output pins will be prefixed with an "x" as a substitute for A, B, or C. For example, xHS refers to pins AHS, BHS, and CHS.

The HIP4086/A is a three phase bridge driver designed specifically for motor drive applications. Three identical half bridge sections, A, B, and C, can be controlled individually by their input pins, ALI, $\overline{AHI}$, BLI, $\overline{BHI}$, and CLI, $\overline{CHI}$ (xLI, $\overline{xHI}$) or the 2 corresponding input pins for each section can be tied together to form a PWM input (xLI connected to xHI = xPWM). When controlling individual inputs, the programmable dead time is optional but shoot-thru protection must then be incorporated in the timing of the input signals. If the PWM mode is chosen, then the internal programmable dead time must be used.

Shoot-Thru Protection

Dead time, to prevent shoot-thru, is implemented by delaying the turn-on of the high-side and low-side drivers. The delay timers are enabled if the voltage on the RDEL pin is greater than 100mV. The voltage on RDEL will be greater than 100mV for any value of programming resistor in the specified range. If the voltage on RDEL is less than 100mV, the delay timers are disabled and no shoot-thru protection is provided by the internal logic of the HIP4086/A. When the dead time is to be disabled, RDEL should be shorted to VSS.

Refresh Pulse

To insure that the boot capacitors are charged prior to turning on the high-side drivers, a refresh pulse is triggered when DIS is low or when the UV comparator transitions low (VDD is greater than the programmed undervoltage threshold). Please refer to the "Block Diagram (for clarity, only one phase is shown)" on page 2. When triggered, the refresh pulse turns on all of the low-side drivers (xLO = 1) and turns off all of the high-side drivers (xHO = 0) for a duration set by a resistor tied between RDEL and VSS. When xLO = 1, the low-side bridge FETs charge the boot caps from VDD through the boot diodes.

Charge Pump

The internal charge pump of the HIP4086/A is used to maintain the bias on the boot cap for 100% duty cycle. There is no limit for the duration of this period. The user must understand that this charge pump is only intended to provide the static bias current of the high-side drivers and the gate leakage current of the high-side bridge FETs. It cannot provide in a reasonable time, the majority of the charge on the boot cap that is consumed, when the xHO drivers source the gate charge to turn on the high-side bridge FETs. The boot caps should be sized so that they do not discharge excessively when sourcing the gate charge. See "Application Information" on page 11 for methods to size the boot caps.

The charge pump has sufficient capacity to source a worst-case minimum of 50µA to the external load. The gate leakage current of most power MOSFETs is about 100nA so there is more than sufficient current to maintain the charge on the boot caps. Because the charge pump current is small, a gate-source resistor on the high-side bridge FETs is not recommended. When calculating the leakage load on the outputs of xHS, also include the leakage current of the boot capacitor. This is rarely a problem but it could be an issue with electrolytic capacitors at high temperatures.

Application Information

Selecting the Boot Capacitor Value

The boot capacitor value is chosen not only to supply the internal bias current of the high-side driver but also, and more significantly, to provide the gate charge of the driven FET without causing the boot voltage to sag excessively. In practice, the boot capacitor should have a total charge that is about 20 times the gate charge of the driven power FET for approximately a 5% drop in voltage after charge has been transferred from the boot capacitor to the gate capacitance.

The following parameters shown in Table 1, are required to calculate the value of the boot capacitor for a specific amount of voltage droop when using the HIP4086/A (no charge pump). In Table 1, the values used are arbitrary. They should be changed to comply with the actual application.

TABLE 1.

V_{DD} = 10V	V_{DD} can be any value between 7 and 15VDC
$V_{HB} = V_{DD}$ - 0.6V = V_{HO}	High side driver bias voltage (V_{DD} - boot diode voltage) referenced to V_{HS}
Period = 1ms	This is the longest expected switching period
I_{HB}= 100µA	Worst case high side driver current when xHO = high (this value is specified for VDD = 12V but the error is not significant)
R_{GS} = 100kΩ	Gate-source resistor (usually not needed)
Ripple = 5%	Desired ripple voltage on the boot cap (larger ripple is not recommended)
I_{gate_leak} = 100nA	From the FET vendor's datasheet
Qgate80V = 64nC	From Figure L

Equation 1 calculates the total charge required for the Period duration. This equation assumes that all of the parameters are constant during the Period duration. The error is insignificant if Ripple is small.

$$Q_C = Q_{gate80V} + Period \times (I_{HB} + V_{HO}/R_{GS} + I_{gate\_leak})$$

$$C_{boot} = Q_C/(Ripple*VDD)$$

$$C_{boot} = 0.52\mu F \quad \text{(EQ. 1)}$$

If the gate to source resistor is removed (R_{GS} is usually not needed or recommended), then:

C_{boot} = 0.33µF

These values of C_{boot} will sustain the high side driver bias during Period with only a small amount of Ripple. But in the case of the HIP4086, the charge pump reduces the value of C_{boot} even more. The specified charge pump current is a minimum of 50µA which is more than sufficient to source I_{gate_leak}. Also, because the specified charge pump current is in excess of what is needed for I_{HB}, the total charge required to be sourced by the boot capacitor is just

$$Q_C = Q_{gate80V} \text{ or } C_{boot} = 0.13\mu F \quad \text{(EQ. 2)}$$

Not only is the required boot cap smaller in value, there is no restriction on the duration of Period.

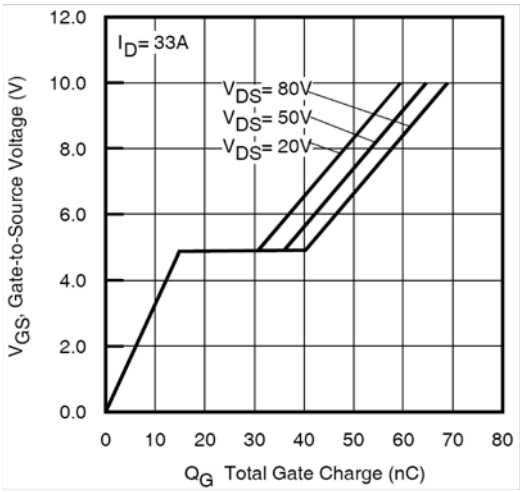


FIGURE 21. TYPICAL GATE VOLTAGE vs GATE CHARGE

Typical Application Circuit

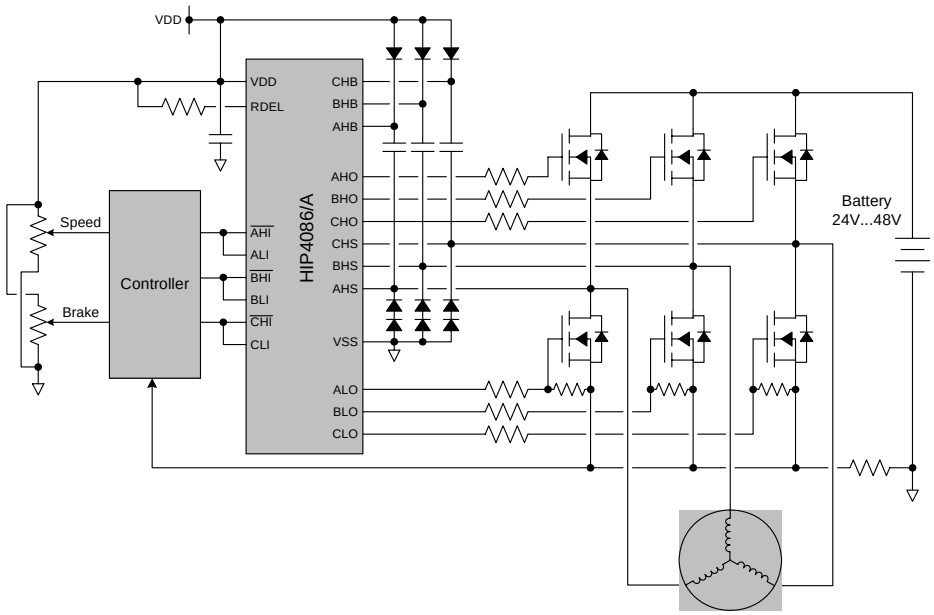


FIGURE 22. TYPICAL APPLICATION CIRCUIT

Figure 22 is an example of how the HIP4086 and HIP4086A 3-phase drivers can be applied to drive a 3-phase motor.

Depending on the application, the switching speed of the bridge FETs can be reduced by adding series connected resistors between the xHO outputs and the FET gates. Gate-Source resistors are recommended on the low-side FETs to prevent unexpected turn-on of the bridge should the bridge voltage be applied before VDD. Gate-source resistors on the high-side FETs are not usually required if low-side gate-source resistors are used. If relatively small gate-source resistors are used on the high-side FETs, be aware that they will load the charge pump of the HIP4086 negating the ability of the charge pump to keep the high-side driver biased during very long periods.

An important operating condition that is frequently overlooked by designers is the negative transient on the xHS pins that occurs when the high-side bridge FET turns off. The Absolute Maximum transient allowed on the xHS pin is -6V but it is wise to minimize the amplitude to lower levels. This transient is the result of the parasitic inductance of the low-side drain-source conductor on the PCB. Even the parasitic inductance of the low-side FET contributes to this transient.

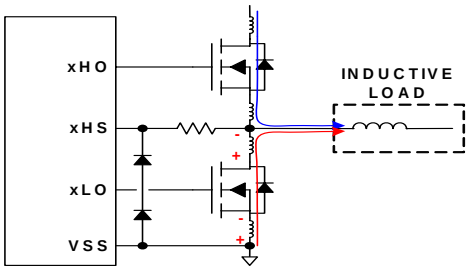


FIGURE 23. BRIDGE WITH PARASITIC INDUCTANCES

When the high-side bridge FET turns off, because of the inductive characteristics of a motor load, the current that was flowing in the high-side FET (blue) must rapidly commutate to flow through the low-side FET (red). The amplitude of the negative transient impressed on the xHS node is (di/dt x L) where L is the total parasitic inductance of the low-side FET drain-source path and di/ddt is the rate at which the high-side FET is turned off. With the increasing power levels of new generation motor drives, clamping this transient becomes more and more significant for the proper operation of the HIP4086/A.

There are several ways of reducing the amplitude of this transient. If the bridge FETs are turned off more slowly to reduce di/dt, the amplitude will be reduced but at the expense of more switching losses in the FETs. Careful PCB design will also reduce the value of the parasitic inductance. However, these two solutions by themselves may not be sufficient. Figure 23 illustrates a simple method for clamping the negative transient. Two series connected, fast PN junction, 1A diodes are connected between xHS and VSS as shown. It is important that the components be placed as close as possible to the xHS and VSS pins to minimize the parasitic inductance of this current path. Two series connected diodes are required because they are in parallel with the body diode of the low-side FET. If only one diode is used for the clamp, it will conduct some of the negative load current that is flowing in the low-side FET. In severe cases, a small value resistor in series with the xHS pin as shown, will further reduce the amplitude of the negative transient.

Please note that a similar transient with a positive polarity occurs when the low-side FET turns off. This is less frequently a problem because xHS node is floating up toward the bridge bias voltage. The Absolute Max voltage rating for the xHS node does need to be observed when the positive transient occurs.

General PCB Layout Guidelines

The AC performance of the HIP4086/A depends significantly on the design of the PC board. The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FETs.
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET will induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they are usually more effective than parallel traces.
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt will induce currents and consequently, noise voltages in the low level signal lines.
- When practical, minimize impedances in low level signal circuits. The noise, magnetically induced on a 10k resistor, is 10x larger than the noise on a 1k resistor.
- Be aware of magnetic fields emanating from motors, transformers and inductors. Gaps in these magnetic structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling.
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductance in the VDD and GND leads. To be effective, these caps must also have the shortest possible conduction paths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits especially on xHO and xLO. If an external gate resistor is unacceptable, then the layout must be improved to minimize lead inductance.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the HIP4086/A.
- Avoid having a signal ground plane under a high amplitude dv/dt circuit. This will inject di/dt currents into the signal ground paths.
- Do power dissipation and voltage drop calculations of the power traces. Many PCB/CAD programs have built in tools for calculation of trace resistance.
- Large power components (Power FETs, Electrolytic caps, power resistors, etc.) will have internal parasitic inductance which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components especially parasitic lead inductance.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
5/10/11	FN4220.7	Added alternate parameters for HIP4086A in DC Electrical Spec Table Supply Currents on page 5. Added to Charge Pump Figures 10 and 11 in Typical Performance Curves "HIP4086 Only"
3/18/11		-Converted to new Intersil Template per PL request. -Changed Title from "80V, 500mA, 3-Phase Driver" to "80V, 500mA, 3-Phase MOSFET Driver" -Rewrote description on page 1 by adding HIP4086A and stating the differences between parts. -Updated ordering information by adding part number HIP4086AABZ and EVAL Board. Added MSL note and numbered all notes to meet new standard, Removed obsolete part HIP4086AP -Updated Application Block Diagram on page 1 -Added Charge Pump Current Curve on page 1 -Updated Features and Applications Section -Added Related Literature -Updated Functional Block Diagram by adding color and notes -Updated Thermal Information and notes on page 5 -Added Boldface limits note to Electrical Spec Table conditions, added note to MIN and MAX columns to reference new standard compliance note. -Updated all timing diagrams for better clarification on page 7 -Added Functional Description, Applications Information and General PCB Layout Guidelines sections beginning on page 10 -Updated POD M24.3 by removing table listing dimensions and putting dimensions on drawing. Added Land Pattern. Added Revision History and Products Information.
7/26/04	FN4220.6	Pb-Free Parts added
2/18/03	FN4220.5	Updated Datasheet
6/21/02	FN4220.4	Initial Release.

Products

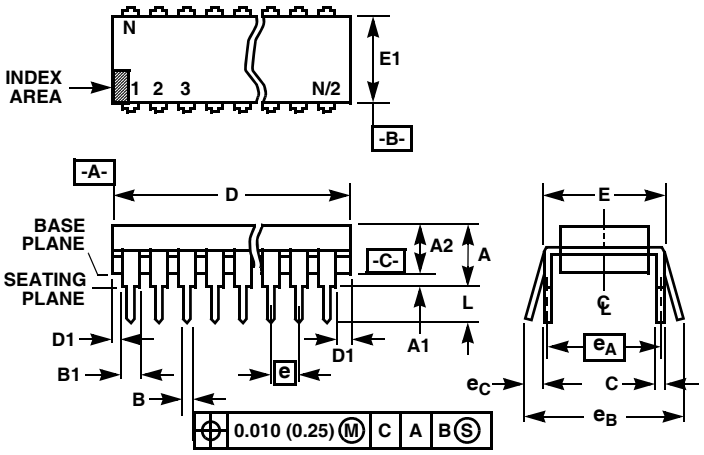
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: HIP4086, HIP4086A

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E24.3 (JEDEC MS-001-AF ISSUE D)
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	1.230	1.280	31.24	32.51	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	24		24		9

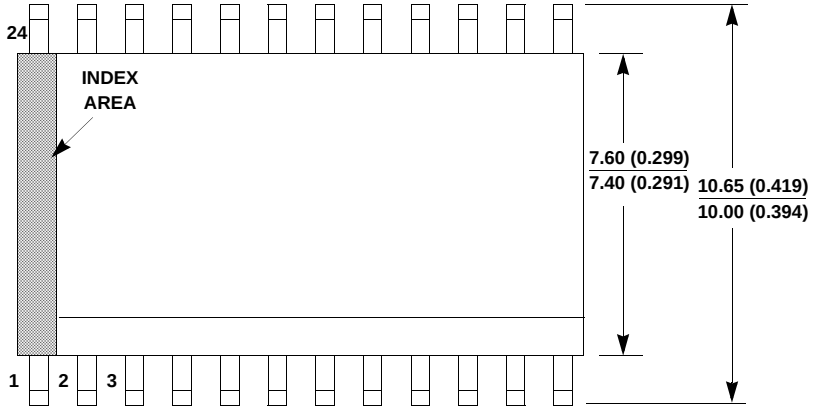
Rev. 0 12/93

Package Outline Drawing

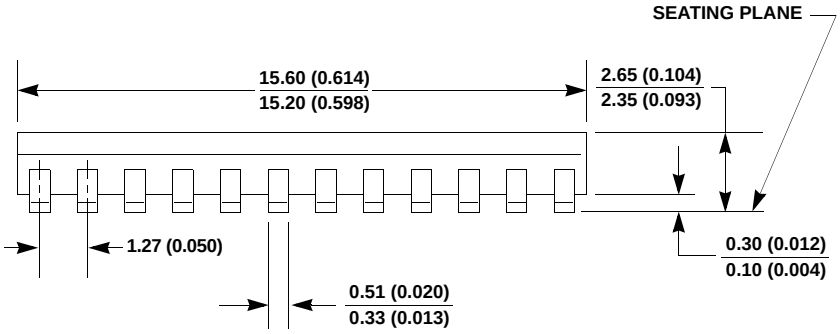
M24.3

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE (SOIC)

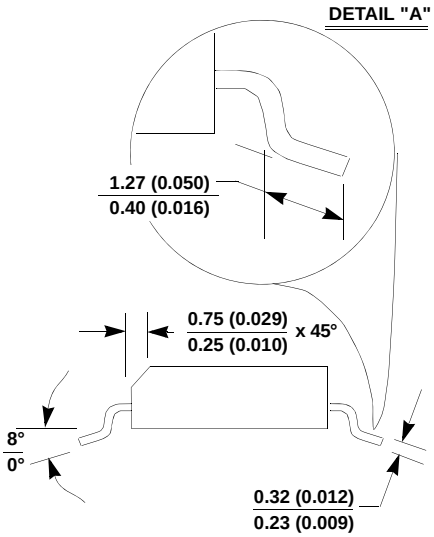
Rev 2, 3/11



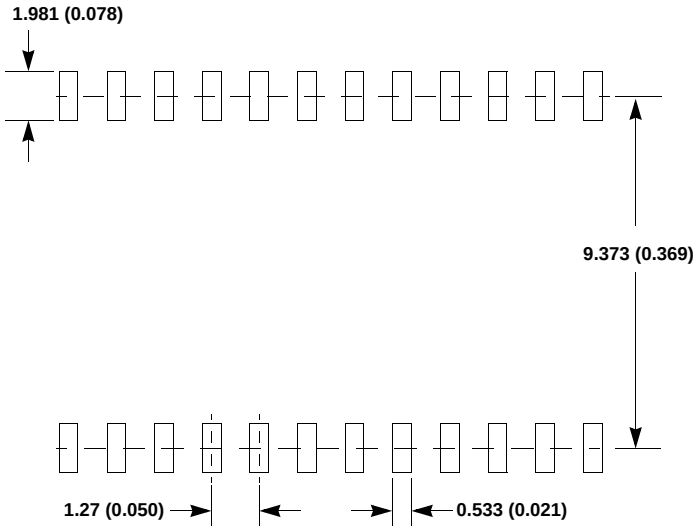
TOP VIEW



SIDE VIEW “A”



SIDE VIEW “B”



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions in ( ) are not necessarily exact.
8. This outline conforms to JEDEC publication MS-013-AD ISSUE C.