

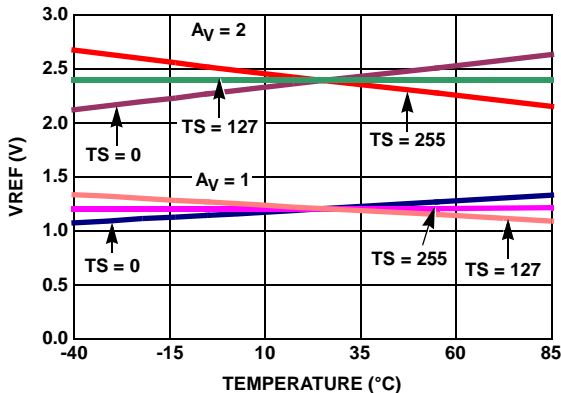
### Programmable Temperature Slope Voltage Reference

The ISL21400 features a precision voltage reference combined with a temperature sensor whose output voltage varies linearly with temperature. The precision 1.20V reference has a very low temperature coefficient (tempco), and its output voltage is scaled by an internal DAC ( $V_{REF}$ ) to produce a temperature stable output voltage that is programmable from 0V to 1.20V. The output voltage from the temperature sensor ( $V_{TS}$ ) is summed with  $V_{REF}$  to produce a temperature dependent output voltage.

The slope of the  $V_{TS}$  portion of the output voltage can be programmed to be positive or negative in the range -2.1mV/°C to +2.1mV/°C. A programmable gain amplifier (PGA) sums the  $V_{TS}$  and the  $V_{REF}$  voltages and provides gains of 1x, 2x, and 4x to scale the output up to 4.8V and the slope to  $\pm 8.4$ mV/°C.

The  $V_{REF}$  and  $V_{TS}$  terms are programmable with 8 bits of resolution via an I<sup>2</sup>C bus and the values are stored in non-volatile registers. The PGA gain is also set via the I<sup>2</sup>C bus and the value is stored in a non-volatile register. Non-volatile memory storage assures the programmed settings are retained on power-down, eliminating the need for software initialization at device power-up.

### Temperature Characteristics Curve



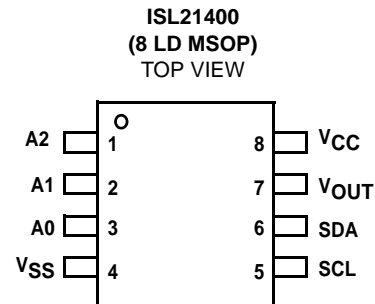
### Features

- Programmable reference voltage
- Programmable temperature slope
- Programmable Gain Amplifier
- Non-volatile storage of programming registers
- I<sup>2</sup>C serial interface
- 2% total accuracy over temperature and  $V_{CC}$  range
- 200µA typical active supply current
- Operating temperature range = -40°C to +85°C
- 8 Ld MSOP package
- Pb-free plus anneal available (RoHS compliant)

### Applications

- RF power amplifier bias compensation
- LCD bias compensation
- Laser diode bias compensation
- Sensor bias and linearization
- Data acquisition systems
- Variable DAC reference
- Amplifier biasing

### Pinout



### Ordering Information

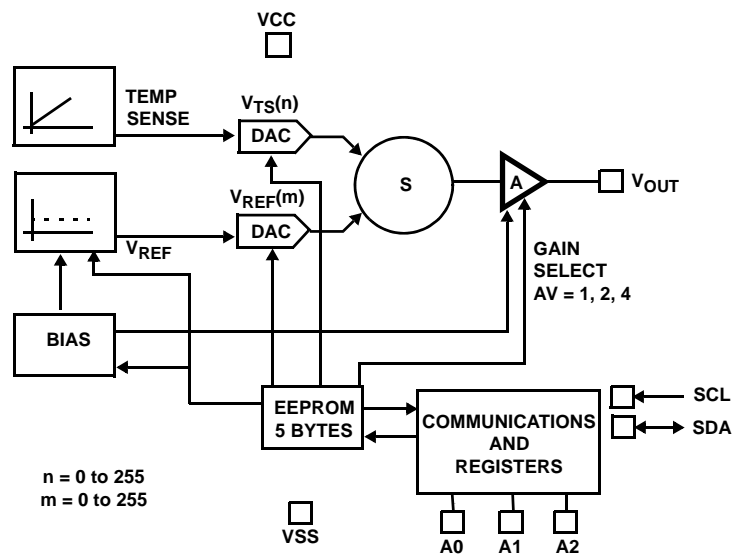
PART NUMBER (Note)	PART MARKING	V <sub>DD</sub> RANGE (V)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL21400IU8Z	DEW	2.7 to 5.5	-40 to +85	8 Ld MSOP (3.0mm), green mtl	M8.118
ISL21400IU8Z-TK	DEW	2.7 to 5.5	-40 to +85	8 Ld MSOP (3.0mm), green mtl	M8.118

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Pin Description**

MSOP	SYMBOL	DESCRIPTION
1	A2	Hardwire slave address pin for I <sup>2</sup> C serial bus
2	A1	Hardwire slave address pin for I <sup>2</sup> C serial bus
3	A0	Hardwire slave address pin for I <sup>2</sup> C serial bus
4	V <sub>SS</sub>	Ground pin
5	SCL	Serial bus clock input
6	SDA	Serial bus data input/output
7	V <sub>OUT</sub>	Output voltage
8	V <sub>CC</sub>	Device power supply

**Block Diagram**



**Absolute Maximum Ratings**

Supply Voltage Range	-1V to 6.5V
Storage Temperature Range	-65°C to +150°C
Voltage on V <sub>OUT</sub> Pin	.0V to V <sub>CC</sub>
Voltage on All Other Pins	-0.3V to V <sub>CC</sub> +0.3V
Lead Temperature (Soldering, 10s)	+300°C
ESD Rating	
Human Body Model	.2kV
Machine Model	200V

**Thermal Information**

Thermal Resistance (Typical)	$\theta_{JA}$ (°C/W)
8 Ld MSOP Package	130
Moisture Sensitivity for MSOP Package (See Technical Brief TB363)	Level 2
Maximum Junction Temperature (Plastic Package)	+150°C
Pb-free reflow profile	see link below
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

**Recommended Operating Conditions**

Temperature	-40°C to +85°C
Supply Voltage	2.7V to 5.5V

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**Analog Specifications**    V<sub>CC</sub> = 5.5V, T<sub>A</sub> = +25°C to +85°C, Unless Otherwise Noted

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
<b>POWER SUPPLY</b>						
V <sub>CC</sub>	Supply Voltage Range		2.7	3.0	5.5	V
I <sub>Q</sub>	Supply	V <sub>CC</sub> = 2.7V Standby, SDA = SCL = V <sub>CC</sub>		200	400	μA
		V <sub>CC</sub> = 5.5V Standby, SDA = SCL = V <sub>CC</sub>		235	500	μA
I <sub>Q(NV)</sub>	Non-Volatile Supply	V <sub>CC</sub> = 2.7V Nonvolatile write		500	750	μA
		V <sub>CC</sub> = 5.5V Nonvolatile write		1.3	1.6	mA
V <sub>por</sub>	Power-on Recall Voltage Minimum V <sub>CC</sub> at which memory recall occurs		2.0		2.6	V
V <sub>CC Ramp</sub>	V <sub>CC</sub> Ramp Rate		0.2			V/ms
t <sub>D</sub>	Power-Up Delay V <sub>CC</sub> above V <sub>por</sub> , time delay to Register recall, and I <sup>2</sup> C Interface in standby state				3	ms
<b>OUTPUT VOLTAGE PERFORMANCE SPECIFICATIONS</b>						
GE <sub>1</sub>	Gain Error	A <sub>V</sub> = 2 (Notes 1, 3, 12)	-1		+1	%
GE <sub>2</sub>	Gain Error	A <sub>V</sub> = 4 (Notes 1, 3, 12)	-1		+1	%
K	Temperature Sensor Coefficient	(Notes 1, 8)	-2.2	-2.1	-2.0	mV/°C
	Absolute Output Voltage (Swing) Range	Unloaded, T <sub>A</sub> = +25°C (Note 3)	V <sub>CC</sub> - 0.100		GND + 0.100	V
	Absolute Output Voltage (Swing) Range	Loaded, I <sub>OUT</sub> = ±500μA (Note 3)	V <sub>CC</sub> - 0.250		GND + 0.250	V
TS <sub>1</sub>	Temperature Sensor Slope	A <sub>V</sub> = 1, n = 255, m = 255 (Notes 1, 6)		-2.1		mV/°C
TS <sub>2</sub>	Temperature Sensor Slope	A <sub>V</sub> = 2, n = 255, m = 255 (Notes 1, 6)		-4.2		mV/°C
TS <sub>3</sub>	Temperature Sensor Slope	A <sub>V</sub> = 4, n = 255, m = 255 (Notes 1, 6)		-8.4		mV/°C
TS <sub>4</sub>	Incremental Temperature Sensor Slope	A <sub>V</sub> = 1, n = 255, m = 0 to 255 (Notes 1, 10)		8.2		μV/°C per Code
TSNL	Temperature Slope Non-Linearity	n = 255, m = 0 to 255, T = -40°C to +85°C (Notes 1, 11)		±0.5	±1.0	%
DNL	DAC Relative Linearity (V <sub>CC</sub> = 2.7 to 5.5V)	V <sub>REF</sub> and Temp Sense; A <sub>V</sub> = 1 (Note 13)	-1.0		+1.0	LSB

# ISL21400

## Analog Specifications $V_{CC} = 5.5V$ , $T_A = +25^\circ C$ to $+85^\circ C$ , Unless Otherwise Noted

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
INL	DAC Absolute Linearity ( $V_{CC} = 2.7$ to $5.5V$ )	$V_{REF}$ and Temp Sense; $A_V = 1$ (Note 13)	-3.0		+3.0	LSB
$V_{OUT(TE)}$	Total Error for $V_{OUT}$	(Notes 1, 8, 9)		$\pm 1$	$\pm 2$	%
$V_{OUT1}$	Output Voltage $V_{REF}$ , Gain = 1	$A_V = 1$ , $n = 255$ , $m = 128$ , $T_A = +25^\circ C$ , $V_{CC} = 5.5V$	1.189	1.2	1.211	V
$V_{OUT2}$	Output Voltage $V_{REF}$ , Gain = 2	$A_V = 2$ , $n = 255$ , $m = 128$ , $T_A = +25^\circ C$ , $V_{CC} = 5.5V$	2.378	2.40	2.422	V
$V_{OUT3}$	Output Voltage $V_{REF}$ , Gain = 4	$A_V = 4$ , $n = 255$ , $m = 128$ , $T_A = +25^\circ C$ , $V_{CC} = 5.5V$	4.756	4.80	4.844	V
$V_{OUT4}$	Output Voltage $V_{REF} + TS$	$A_V = 1$ , $n = 255$ , $m = 0$ , $T_A = +85^\circ C$ (Note 3)	1.315	1.326	1.337	V
$V_{OUT5}$	Output Voltage $V_{REF} + TS$	$A_V = 1$ , $n = 255$ , $m = 128$ , $T_A = +85^\circ C$ (Note 3)	1.188	1.199	1.210	V
$V_{OUT6}$	Output Voltage $V_{REF} + TS$	$A_V = 1$ , $n = 255$ , $m = 255$ , $T_A = +85^\circ C$ (Note 3)	1.063	1.074	1.085	V
$V_{OUT7}$	Output Voltage $V_{REF} + TS$	$A_V = 1$ , $n = 255$ , $m = 0$ , $T_A = -40^\circ C$ , (Note 3)	1.052	1.063	1.074	V
$V_{OUT8}$	Output Voltage $V_{REF} + TS$	$A_V = 1$ , $n = 255$ , $m = 128$ , $T_A = -40^\circ C$ , (Note 3)	1.189	1.200	1.211	V
$V_{OUT9}$	Output Voltage $V_{REF} + TS$	$A_V = 1$ , $n = 255$ , $m = 255$ , $T_A = -40^\circ C$ , (Note 3)	1.336	1.325	1.347	V

### OUTPUT VOLTAGE DC SPECIFICATIONS

PSRR	Power Supply Rejection Ratio	$A_V = 1$ , $n = 255$ , $m = 128$ , (Note 7)	50	60		dB
$R_{OUT}$	Output Impedance (load regulation)	Given by $R_{OUT} = (\Delta V_{OUT} / \Delta I_{OUT})$ , $T_A = +25^\circ C$ , $I_{OUT} = \pm 500\mu A$		2	5	$\Omega$
$I_{SC}$	Short Circuit, Sourcing	$V_{CC} = 5.5V$ , $V_{OUT} = 0V$		5	9	mA
	Short Circuit, Sinking	$V_{CC} = 5.5V$ , $V_{OUT} = 5.5V$		6	9	mA
$C_L$	Load Capacitance	Reference output stable for all $C_L$ up to specifications		5		nF

### OUTPUT VOLTAGE AC SPECIFICATIONS

$V_N$	Output Voltage Noise	0.1Hz to 10Hz, $A_V = 1$		90		$\mu V_{P-P}$
		10Hz to 10kHz, $C_L = 0$ , $A_V = 1$		TBD		mV <sub>RMS</sub>
	Power On Response	1% Settling		500		$\mu s$
	Line Ripple Rejection	$V_{CC} = 5V \pm 100mV$ , $f = 120Hz$		60		dB

### Serial Interface Specification (for SCL, SDA, A0, A1, A2 unless specified otherwise)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
$I_{LI}$	Input Leakage	$V_{IN} = GND$ to $V_{CC}$			1	V
$V_{IL}$	Input LOW Voltage		-0.3		$0.3 \times V_{CC}$	V
$V_{IH}$	Input HIGH Voltage		$0.7 \times V_{CC}$		$V_{CC} + 0.3$	V
Hysteresis	SDA and SCL Input Buffer Hysteresis		$0.05 \times V_{CC}$			V
$V_{OL}$	SDA Output Buffer LOW Voltage	$I_{OL} = 3mA$	0		0.4	V
$C_{pin}$	Pin Capacitance	(Note 3)		10		pF

**Serial Interface Specification** (for SCL, SDA, A0, A1, A2 unless specified otherwise) (Continued)

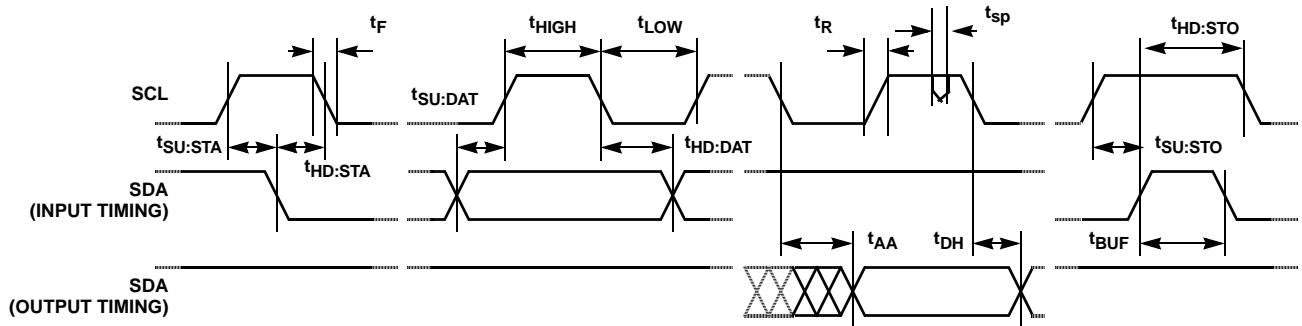
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
f <sub>SCL</sub>	SCL Frequency	(Note 3)			400	kHz
t <sub>sp</sub>	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed (Note 3)			50	ns
t <sub>AA</sub>	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V <sub>CC</sub> , until SDA exits the 30% to 70% of V <sub>CC</sub> window (Note 3)			900	ns
t <sub>BUF</sub>	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V <sub>CC</sub> during a STOP condition, to SDA crossing 70% of V <sub>CC</sub> during the following START condition (Note 3)	1300			ns
t <sub>LOW</sub>	Clock LOW Time	Measured at the 30% of V <sub>CC</sub> crossing (Note 3)	1300			ns
t <sub>HIGH</sub>	Clock HIGH Time	Measured at the 70% of V <sub>CC</sub> crossing (Note 3)	600			ns
t <sub>SU:STA</sub>	START Condition Setup Time	SCL rising edge to SDA falling edge; both crossing 70% of V <sub>CC</sub> (Note 3)	600			ns
t <sub>HD:STA</sub>	START Condition Hold Time	From SDA falling edge crossing 30% of V <sub>CC</sub> to SCL falling edge crossing 70% of V <sub>CC</sub> (Note 3)	600			ns
t <sub>SU:DAT</sub>	Input Data Setup Time	From SDA exiting the 30% to 70% of V <sub>CC</sub> window, to SCL rising edge crossing 30% of V <sub>CC</sub> (Note 3)	100			ns
t <sub>HD:DAT</sub>	Input Data Hold Time	From SCL rising edge crossing 70% of V <sub>CC</sub> to SDA entering the 30% to 70% of V <sub>CC</sub> window (Note 3)	0			ns
t <sub>SU:STO</sub>	STOP Condition Setup Time	From SCL rising edge crossing 70% of V <sub>CC</sub> , to SDA rising edge crossing 30% of V <sub>CC</sub> (Note 3)	600			ns
t <sub>HD:STO</sub>	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge; both crossing 70% of V <sub>CC</sub> (Note 3)	1300			ns
t <sub>DH</sub>	Output Data Hold Time	From SCL falling edge crossing 30% of V <sub>CC</sub> , until SDA enters the 30% to 70% of V <sub>CC</sub> window (Note 3)	0			ns
t <sub>R</sub>	SDA and SCL Rise Time	From 30% to 70% of V <sub>CC</sub> (Note 3)	20 + 0.1 x Cb		250	ns
t <sub>F</sub>	SDA and SCL Fall Time	From 70% to 30% of V <sub>CC</sub> (Note 3)	20 + 0.1 x Cb		250	ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip (Note 4)	10		400	pF

**Serial Interface Specification** (for SCL, SDA, A0, A1, A2 unless specified otherwise) (Continued)

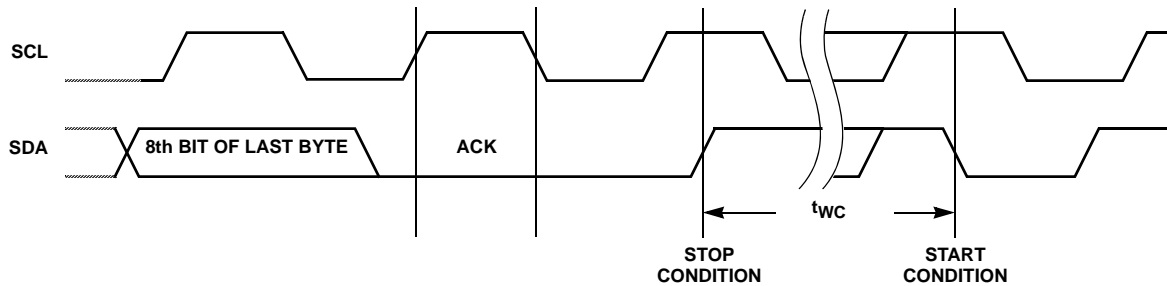
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
R <sub>pu</sub>	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t <sub>R</sub> and t <sub>F</sub> For C <sub>b</sub> = 400pF, max is about 2~2.5kΩ For C <sub>b</sub> = 40pF, max is about 15~20kΩ	1			kΩ
I <sub>LO</sub>	Output Leakage Current (SDA only)	V <sub>OUT</sub> = GND to V <sub>CC</sub>			1	μA
V <sub>IL</sub>	A1, A0, $\overline{\text{SHDN}}$ , SDA, and SCL Input Buffer LOW Voltage		-0.3		V <sub>CC</sub> x 0.3	V
V <sub>IH</sub>	A1, A0, $\overline{\text{SHDN}}$ , SDA, and SCL Input Buffer HIGH Voltage		V <sub>CC</sub> x 0.7		V <sub>CC</sub>	V
V <sub>OL</sub>	SDA Output Buffer LOW Voltage	I <sub>OL</sub> = 100μA (Note 3), at 3mA sink	0		0.4	V
C <sub>L</sub>	Capacitive Loading of SDA or SCL	Total on-chip and off-chip (Note 3)	10		400	pF
	EEPROM Endurance		1,000,000			Cycles
	EEPROM Retention	Temperature T ≤ +55°C	50			Years
t <sub>WC</sub> (Note 14)	Non-Volatile Write Cycle Time			12	20	ms

**Timing Diagrams**

**Bus Timing**



**Write Cycle Timing**



NOTES:

1. Equation 1 governs the output voltage and is stated as follows:

$$V_{OUT} = A_V \cdot \left\{ V_{REF} \cdot \frac{n}{255} + K(T - T_0) \frac{(2 \cdot m) - 255}{255} \right\}, n = 0 \text{ to } 255, m = 0 \text{ to } 255, K = -2.1\text{mV/C(} \text{typ)}, T_0 = +25^\circ\text{C}$$

2. Typical values are for T<sub>A</sub> = +25°C and V<sub>CC</sub> = 5.5V.

3. This parameter is not 100% tested.
4.  $C_b$  = total capacitance of one bus line in pF.
5.  $t_{WC}$  is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user.
6. Over the specified temperature range. Temperature slope (TS) is measured by the box method whereby the change in  $V_{OUT}$  is divided by the temperature range; in this case,  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  =  $+125^{\circ}\text{C}$ .  $TS_1, TS_2, TS_3 =$

$$TS = \frac{V_{OUT}(T_{min}) - V_{OUT}(T_{max})}{T_{min} - T_{max}}$$

7. Given by  $PSRR \text{ (dB)} = 20 * \log_{10} (\Delta V_{out}/\Delta V_{CC})$  at DC.
8. Test  $+25^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$  only.
9. Total error of Equation 1 @  $A_V = 1, K = -2.1\text{mV}/^{\circ}\text{C}, V_{REF} = 1.20\text{V}, m = 255, n = 255 \text{ to } 0, V_{CC} = 3.0\text{V}$ .

$$V_{OUT}(TE) = \frac{V_{OUT}(\text{measured}) - V_{OUT}(\text{Equation 1})}{V_{OUT}(\text{Equation 1})} \times 100\%$$

10. Over the specified temperature range. Temperature slope (TS) is measured by the box method whereby the change in  $V_{OUT}$  is divided by the temperature range. Incremental TS is the temperature slope at  $m = 255$  minus the temperature slope at  $m = 0$  divided by 255 with  $A_V = 1, n = 255$

$$TS4 = \left[ \left( \frac{V_{OUT}(T_{min}) - V_{OUT}(T_{max})}{(T_{min} - T_{max})} \right) \Big|_{m=255} - \left( \frac{V_{OUT}(T_{min}) - V_{OUT}(T_{max})}{(T_{min} - T_{max})} \right) \Big|_{m=0} \right] \div 255$$

11. Temperature Slope Non-linearity is measured over the specified temperature range. The actual change in output voltage is subtracted from the expected change in output voltage, and then divided by the expected change to normalize before converting to percent.

$$TSNL = \frac{(TS_y(\Delta T)) - \Delta V_{OUT}}{TS_y \times \Delta T} \times 100\%; y = 1, 2, 3$$

12. For codes  $n = 8$  to 255
13. Guaranteed monotonic
14.  $t_{WC}$  is the time from a valid STOP condition at the end of a Write sequence of  $I^2C$  serial interface, to the end of the self-timed internal nonvolatile write cycle.
15.  $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

### Typical Performance Curves

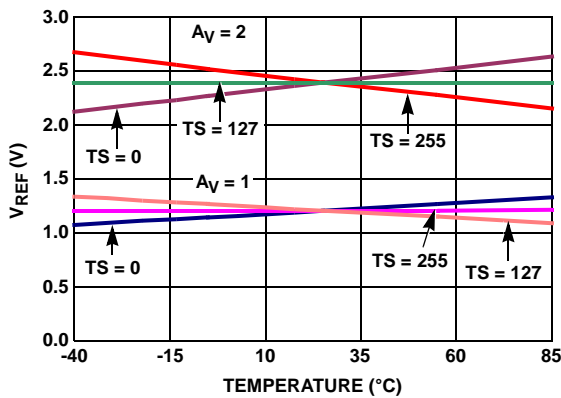


FIGURE 1.  $V_{OUT}$  vs TEMPERATURE ( $A_V = 1, 2$ )

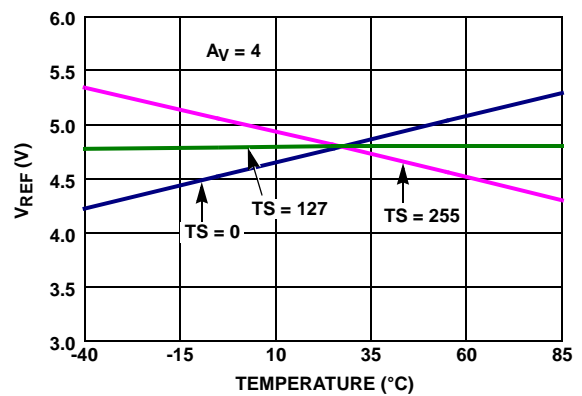


FIGURE 2.  $V_{OUT}$  vs TEMPERATURE ( $A_V = 4$ )

Typical Performance Curves (Continued)

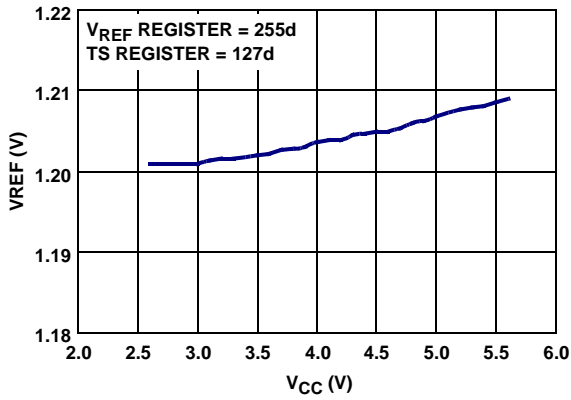


FIGURE 3.  $V_{OUT}$  vs  $V_{CC}$  ( $V_{CC} = +2.7V$  to  $+5.5V$ )

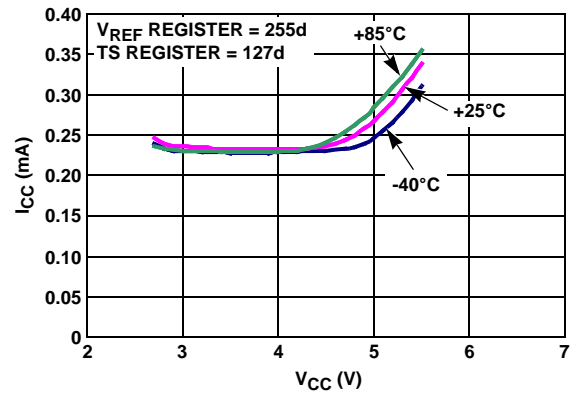


FIGURE 4. SUPPLY VOLTAGE vs SUPPLY CURRENT

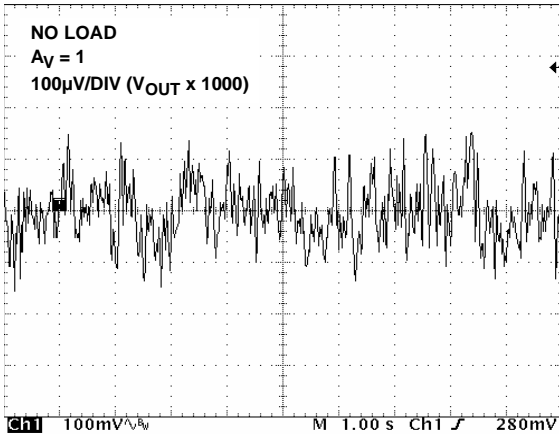


FIGURE 5.  $V_{OUT}$  VOLTAGE NOISE ( $A_V = 1$ , NO LOAD)

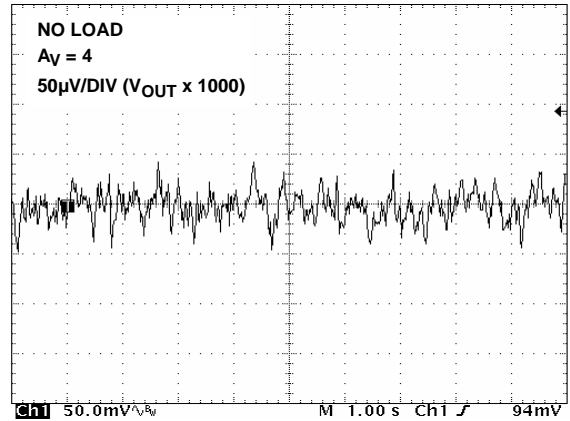


FIGURE 6.  $V_{OUT}$  VOLTAGE NOISE ( $A_V = 4$ , NO LOAD)

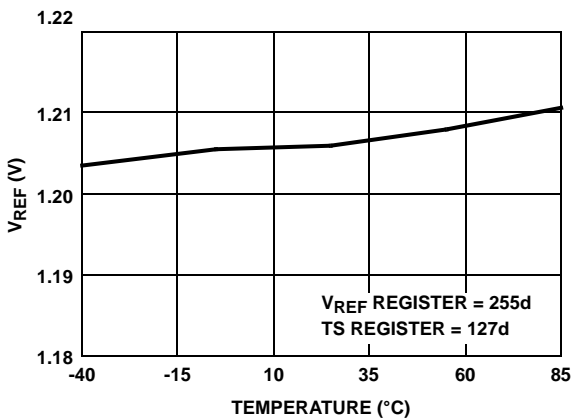


FIGURE 7. ACCURACY vs TEMPERATURE ( $-40^{\circ}C$  TO  $+85^{\circ}C$ )

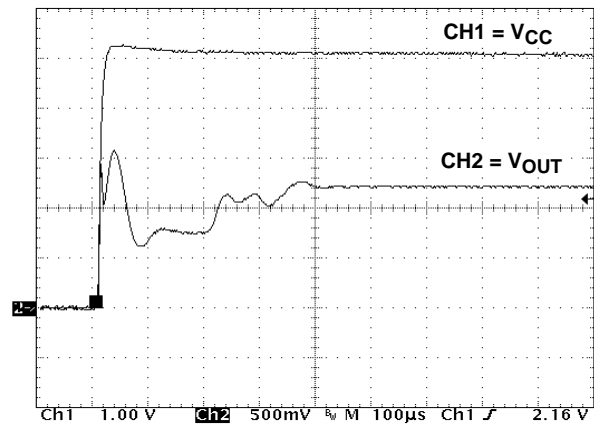


FIGURE 8. POWER ON



Typical Performance Curves (Continued)

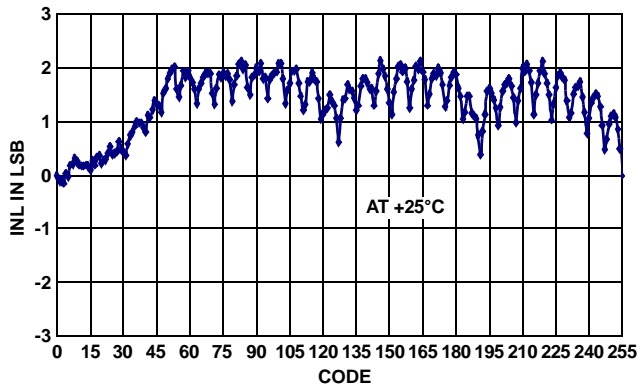


FIGURE 9. INL,  $V_{REF}$  AND TEMP SLOPE DAC

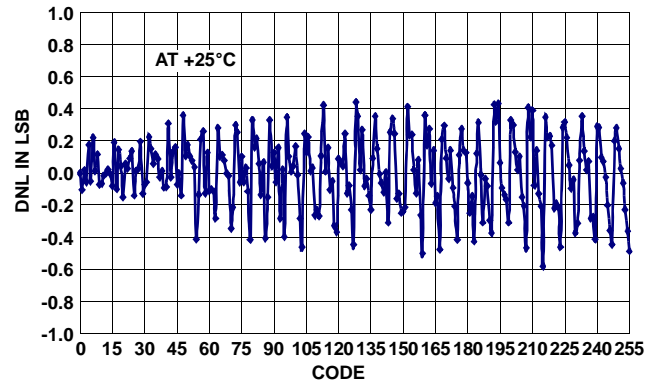


FIGURE 10. DNL,  $V_{REF}$  AND TEMP SLOPE DAC

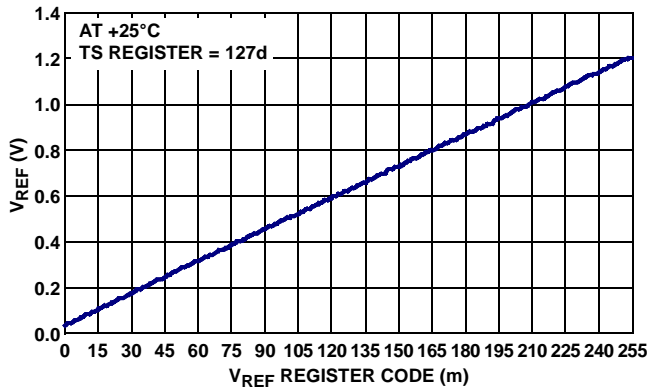


FIGURE 11.  $V_{OUT}$  vs  $V_{REF}$  CODE (m)

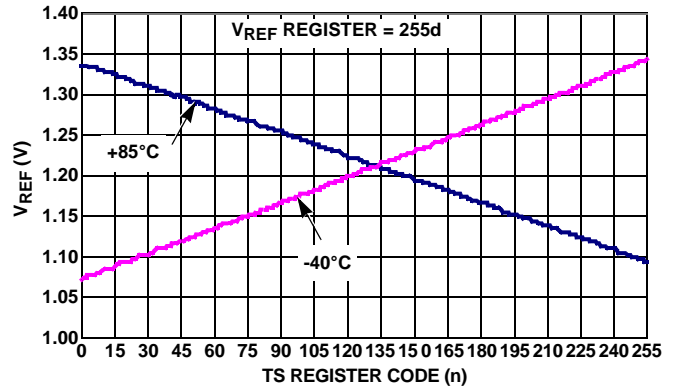


FIGURE 12.  $V_{OUT}$  vs TEMP SENSE CODE (n),  $T_A = -40^\circ\text{C}$  AND  $+85^\circ\text{C}$

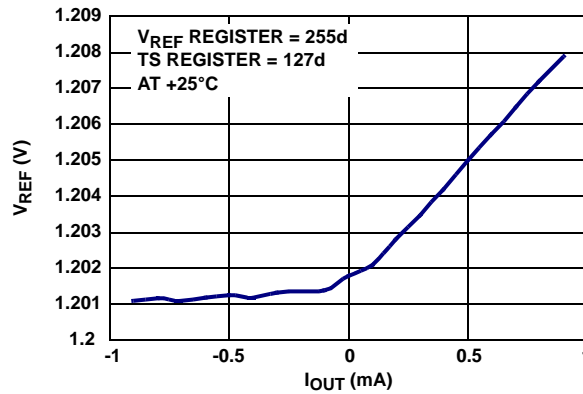


FIGURE 13.  $V_{OUT}$  vs  $I_{OUT}$  ( $\pm 1\text{mA}$ )

## Pin Descriptions

### $V_{OUT}$

Programmable voltage output pin. Absolute voltage is determined by device temperature and Equation 1. Drive capability is limited to  $\pm 500\mu\text{A}$  output current and 5000pF output capacitance.

### A2, A1, A0

Hardware slave address pins that can be used to provide several ISL21400 with a unique physical address to allow for multiple devices off one I<sup>2</sup>C bus.

### GND

This is the circuit ground pin. It is common for the  $V_{OUT}$  and control signal inputs.

### SDA

Serial Data Input/Output. Bidirectional pin used for serial data transfer. As an output, it is open drain and may be wire-ored with any number of open drain or open collector outputs. A pullup resistor is required and the value is dependent on the speed of the serial data bus and the number of outputs tied together.

### SCL

Serial Clock Input. Accepts a clock signal for clocking serial data into and out of the device. The SCL line requires a pull-up resistor whose value is dependent on the speed of the serial clock bus and the number of inputs tied together.

### $V_{CC}$

Positive Power Supply. Connect to a voltage supply in the range of  $2.7\text{V} < V_{CC} < 5.5\text{V}$ , with minimum noise and ripple. For best performance, bypass with a  $0.1\mu\text{F}$  capacitor to ground. If the  $A_V$  gain is set to 4 and  $V_{OUT}$  approaches 5.0V, then  $V_{CC}$  must be set to  $> 5.2\text{V}$  for best output performance.

## Functional Description

### Functional Overview

Refer to the Functional Block Diagram on page 2. The ISL21400 provides a programmable output voltage which combines both a temperature independent term and a temperature dependent term. The temperature independent term uses a bandgap voltage reference, and the temperature dependent term uses a Proportional To Absolute Temperature (PTAT) reference, or Temperature Sensor. Each voltage source is scalable using two DACs via the I<sup>2</sup>C serial bus. The resulting output voltage can vary from 0V to over 5V and has a variable, programmable Temperature Slope (TS).

## Reference Sections

Referring to the Block Diagram on page 2, the  $V_{REF}$  and Temperature Sense ( $V_{TS}$ ) outputs are summed together ( $\Sigma$ ) and then passed through the output gain stage (A). The voltage output is programmable and is determined by the Equation 1:

$$V_{OUT} = A_V \cdot \left\{ V_{REF} \cdot \frac{n}{255} + V_{TS} \frac{(2 \cdot m) - 255}{255} \right\} \quad (\text{EQ. 1})$$

where

- $A_V = 1, 2, 4$
- $V_{REF} = 1.200$  (not temperature dependent)
- $0 \leq n \leq 255$  (setting contained in Register 0,  $V_{REF}$ )
- $V_{TS} = K(T - T_0)$
- $K = dV_{TS}/dT = -2.1\text{mV}/\text{C}$
- $T =$  device temperature
- $T_0 = +25^\circ\text{C}$
- $0 \leq m \leq 255$  (setting contained in Register 1, TS)

See “Applications Information” on page 14 for ways to use Equation 1 and methods for output voltage calculations.

### DACs Section

The ISL21400 contains two 8-bit DACs whose registers can be programmed via the I<sup>2</sup>C serial bus. The DAC registers are non-volatile such that the values are restored during the  $V_{CC}$  power-up cycle of the device. One DAC ( $V_{REF}$ ) is dedicated to scale the bandgap voltage reference (Temperature invariant) and the other DAC ( $V_{TS}$ ) is dedicated to scale the Temperature Sensor. Both of these DACs can determine the output voltage as defined by Equation 1 (See “Register Descriptions” on page 11.).

### Output Gain Amplifier Section

The ISL21400 contains an output gain amplifier (A) that is programmed via the I<sup>2</sup>C serial bus. The gain amplifier is the last stage before the output and therefore controls the overall gain for the device. The gain can be programmed for 1x, 2x, or 4x amplification. This gain factor is used to program the output voltage as determined by Equation 1 (See “Register Descriptions” on page 11.).

There are 5 registers in the ISL21400 device, all nonvolatile (see Table 2). All registers are accessible for reading or writing through the I<sup>2</sup>C serial bus.

## Register Descriptions

TABLE 1. ISL21400 REGISTER BIT MAP

Addr	D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
0	V <sub>REF</sub> 7	V <sub>REF</sub> 6	V <sub>REF</sub> 5	V <sub>REF</sub> 4	V <sub>REF</sub> 3	V <sub>REF</sub> 2	V <sub>REF</sub> 1	V <sub>REF</sub> 0
1	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0
2	D7	D6	D5	D4	D3	D2	GAIN1	GAIN0
3	D7	D6	D5	D4	D3	D2	D1	D0
4	D7	D6	D5	D4	D3	D2	D1	D0

TABLE 2. REGISTER DESCRIPTIONS

REG	NONVOLATILE	DESCRIPTION
0	Y	Reference setting
1	Y	Temperature Sensor setting
2	Y	Gain and storage
3	Y	Storage
4	Y	Storage

**Register 0: Bandgap Reference Gain (Nonvolatile)**

Register 0 sets the output voltage of the bandgap reference (V<sub>REF</sub>). Referring to Equation 1, the number “n” is the setting from Register 0 as follows:

$$V_{REF} \cdot \frac{n}{255}, \text{ for } n = 0 \text{ to } 255$$

This term of Equation 1 can vary from 0V to 1.20V.

**Register 1: Temperature Slope Gain (Nonvolatile)**

Register 1 sets the Temperature Slope (TS) of the temperature sensor. Referring to Equation 1, the number “m” is the setting from Register 1 as follows:

$$V_{TS} \frac{(2 \cdot m) - 255}{255}$$

V<sub>TS</sub> is the temperature dependent term and varies from +136mV at -40°C to -126mV at +85°C. The other term varies from -1 to +1 and scales the temperature term before adding to the V<sub>REF</sub> portion.

**Register 2: Device Gain and Storage (nonvolatile)**TABLE 3. REGISTER 2 OUTPUT GAIN (NONVOLATILE):  
OUTPUT GAIN

GAIN1	GAIN0	OUTPUT GAIN, A <sub>V</sub>
0	0	x 1
0	1	x 2
1	0	x 2
1	1	x 4

Register 2 contains 2 bits (2 LSB's) which control the output gain of the device. Table 3 shows the state of these two bits

and the resulting output gain. Note that two states produce the same gain (Gain 1:0 set to 01b and 10b) of x2.

The other 6-bits in the register can be used for general purpose memory (nonvolatile) or left alone.

**Registers 3 and 4: general purpose data (nonvolatile)**

These two registers are one byte each and can be used for general purpose nonvolatile memory.

**I<sup>2</sup>C Serial Interface**

The ISL21400 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL21400 operates as a slave device in all applications.

All communication over the I<sup>2</sup>C interface is conducted by sending the MSB of each byte of data first.

**Protocol Conventions**

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 10). On power-up of the ISL21400 the SDA pin is in the input mode.

All I<sup>2</sup>C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL21400 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 10). A START condition is ignored during the power-up sequence and during non-volatile write cycles for the device.

All I<sup>2</sup>C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 10) A STOP condition at the end of a read operation, or at the end of a write operation places the device in its standby mode. A STOP condition at the end of a write operation to a non-volatile byte initiates an internal

non-volatile write cycle. The device enters its standby state when the internal, non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 11).

The ISL21400 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL21400 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0101 A2 A1 A0 as the seven MSBs. The A2 A1 A0 bits must correspond to the logic levels at those pins of the ISL21400 device. The LSB in the Read/Write bit. Its value is "1" for a Read operation, and "0" for a Write operation (See Table 4).

### Write Operation

TABLE 4. IDENTIFICATION BYTE FORMAT

0	1	0	1	A2	A1	A0	R/W
(MSB)				(LSB)			

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL21400 responds with an ACK. The master will then send a STOP and at this time the device begins its internal non-volatile write cycle. During this time, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the ISL21400 enters its standby state (see Figure 12).

STOP conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the ISL21400 resets itself without performing the write. The contents of the array are not affected.

### Data Protection

A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection for the registers. A STOP condition also acts as a protection for non-volatile memory. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. The presence of the STOP condition after the rest of the bits are received then triggers the non-volatile write.

### Read Operation

A Current Address Read operation is shown in Figure 13. It consists of a minimum 2 bytes: a START followed by the ID byte from the master with the R/W bit set to 1, then an ACK followed by the data byte or bytes sent by the slave. The master terminates the Read operation by not responding with an ACK and then issuing a STOP condition. This operation is useful if the master knows the current address and desires to read one or more data bytes.

A Random Address Read operation consists of a three byte "dummy write" instruction followed by a Current Address Read operation (See Figure 14). The master initiates the operation issuing the following sequence: a START, the identification byte with the R/W bit set to "0", an Address Byte, a second START, and a second Identification byte with the R/W bit set to "1". After each of the three bytes, the ISL21400 responds with an ACK. The ISL21400 then transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the Read operation (issuing a STOP condition) following the last bit of the last Data Byte (See Figure 13).

The Data Bytes are from the registers indicated by an internal pointer. This pointer initial's value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. Address 04h is the last valid data byte, higher addresses are not available. Data from addresses higher than memory location 04h will be invalid.

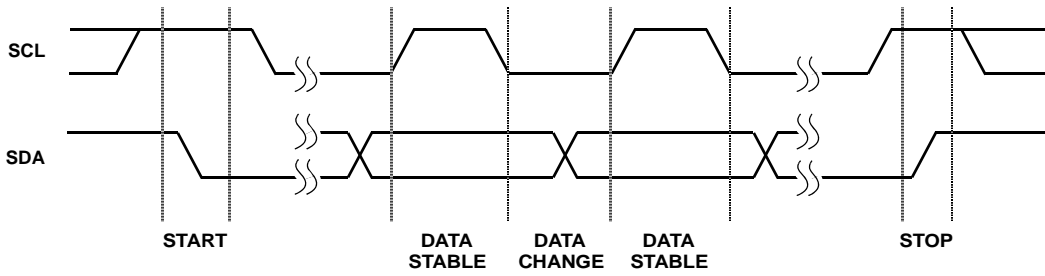


FIGURE 14. VALID DATA CHANGES, START AND STOP CONDITIONS

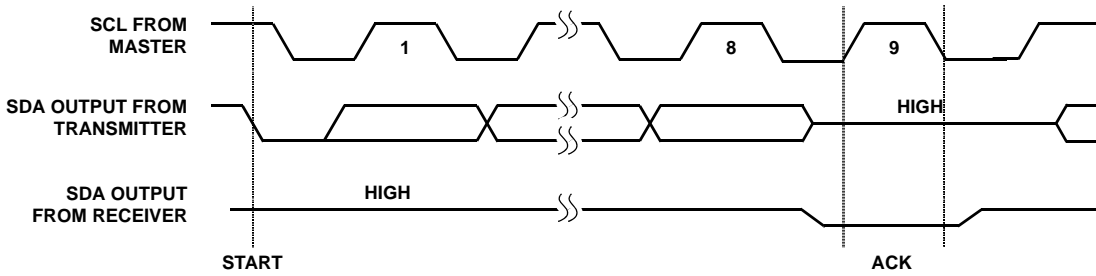


FIGURE 15. ACKNOWLEDGE RESPONSE FROM RECEIVER

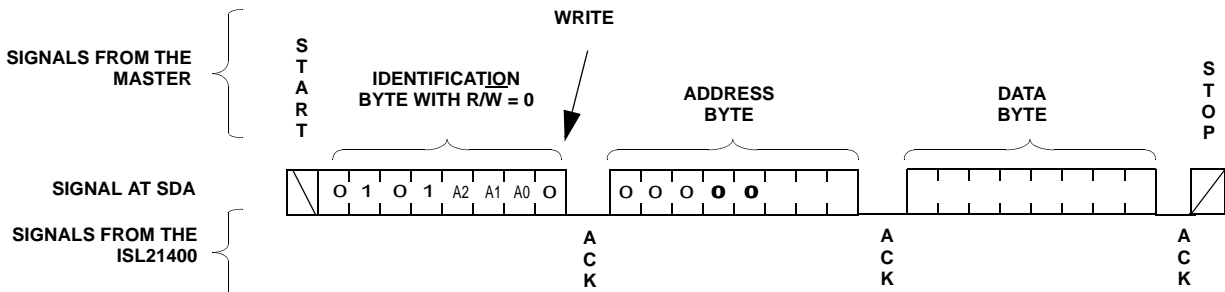


FIGURE 16. BYTE WRITE SEQUENCE

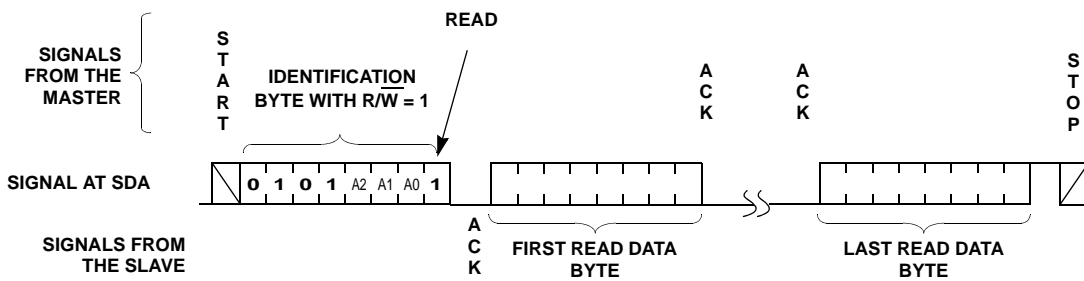


FIGURE 17. ADDRESS READ SEQUENCE

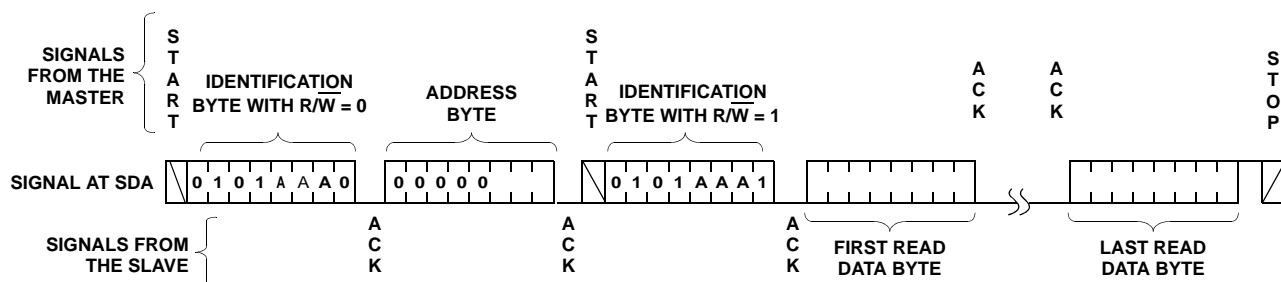


FIGURE 18. RANDOM ADDRESS READ SEQUENCE

## Applications Information

### Power-Up Considerations

The ISL21400 has on-chip EEPROM memory storage for the DAC and gain settings of the device. These settings must be recalled correctly on power-up for proper operation. Normally there are no issues with recall, although it is always best to provide a smooth, glitch-free power-up waveform on  $V_{CC}$ . Adding a small  $0.1\mu\text{F}$  capacitor at the device  $V_{CC}$  will help with power-up as well as  $V_{OUT}$  load changes.

### Noise Performance

The output noise voltage in a 0.1Hz to 10Hz bandwidth is typically  $90\mu\text{V}_{\text{P-P}}$ . The noise measurement is made with a bandpass filter made of a 1 pole high-pass filter with a corner frequency at 0.1Hz and a 2-pole low-pass filter with a corner frequency at 12.6Hz to create a filter with a 9.9Hz bandwidth. Load capacitance up to  $5000\text{pF}$  can be added but will result in only marginal improvements in output noise and transient response. The output stage of the ISL21400 is not designed to drive heavily capacitive loads. For high impedance loads, an R-C network can be added to filter high frequency noise and preserve DC control.

### Output Voltage Programming Considerations

Setting and controlling the output voltage of the ISL21400 can be done easily by breaking down the components into temperature variant and invariant, and setting them separately. Let's use Equation 1 to derive separate Reference Output and Output Temp Slope equations:

$$V_{\text{OUT}} = \left\{ A_V \cdot V_{\text{REF}} \cdot \frac{n}{255} \right\} + \left\{ A_V \cdot V_{\text{TS}} \cdot \left( \frac{(2 \cdot m) - 255}{255} \right) \right\}$$

$$= \{ A_V \cdot V_{\text{REF}} \cdot A_{\text{REF}} \} + \{ A_V \cdot V_{\text{TS}} \cdot A_{\text{TS}} \}$$

Reference Term + Temp Slope Term

The first term controls the output DC value, and the second term controls the Temp slope, where

$$A_{\text{REF}} = \frac{n}{255} \quad (\text{ranges from } 0 \text{ to } 1)$$

$$A_{\text{TS}} = \left( \frac{(2 \cdot m) - 255}{255} \right) \quad (\text{ranges from } -1 \text{ to } +1)$$

### DC OUTPUT CONTROL DISCUSSION

The reference term yields Equation 2 for Reference Output:

$$V_{\text{OUT(DC)}} = A_V \cdot V_{\text{REF}} \cdot A_{\text{REF}} \quad (\text{EQ. 2})$$

Note that the DC term is dependent on the 1.20V reference voltage, which is constant, the overall gain,  $A_V$ , and the Reference gain,  $A_{\text{REF}}$ . Since the product  $A_V \cdot A_{\text{REF}}$  ranges from 0 to 4, the total reference DC output can range from 0.0V to 4.8V. In order to get the 4.8V output,  $V_{CC}$  must be greater than 4.8V by the output dropout plus any overhead for output loading (the specification for  $V_{\text{OUT}} = 5.0\text{V}$  is listed with  $V_{CC} = 5.5\text{V}$ ). The Resolution of  $V_{\text{OUT(DC)}}$  control changes with  $A_V$ , so that with a 4.80V full scale output ( $A_V = 4$ ), the resolution is  $4.80/255$  or  $18.8\text{mV/bit}$ . With  $A_V = 1$ , the resolution is  $4.7\text{mV/bit}$ .

### TEMP SENSE CONTROL DISCUSSION

Equation 2 yields this expression, Equation 3, for Temp Slope:

$$V_{\text{OUT(TS)}} = A_V \cdot V_{\text{TS}} \cdot A_{\text{TS}} \quad (\text{EQ. 3})$$

Since  $V_{\text{TS}} = K(T - T_0)$ , the slope term is dependent on the base temp slope of the device,  $K$  ( $-2.1\text{mV}/^\circ\text{C}$ ), and the gain terms  $A_V$  and  $A_{\text{TS}}$ . This gives a formula (Equation 4) for the portion of  $V_{\text{OUT}}$  at a specific temperature:

$$V_{\text{OUT(TS)}} = A_V \cdot K \cdot A_{\text{TS}} \cdot (T - T_0) \quad (\text{EQ. 4})$$

The product  $A_V \cdot A_{\text{TS}}$  ranges from -4 to 4, so the Temperature Slope can range from  $-8.4$  to  $+8.4\text{mV}/^\circ\text{C}$ , which is independent of the output DC voltage. The resolution of Slope control is determined by this range ( $\pm 8.4\text{mV}/^\circ\text{C}$ ) and the gain terms, and will vary from  $65.8\mu\text{V}/^\circ\text{C/bit}$  ( $A_V = 4$ ) down to  $16.2\mu\text{V}/^\circ\text{C/bit}$  ( $A_V = 1$ ).

At  $T = T_0 = +25^\circ\text{C}$ ,  $V_{\text{OUT(TS)}} = 0$ , no changes in  $A_{\text{TS}}$  will cause a change in  $V_{\text{OUT}}$ , and  $V_{\text{OUT}}$  will only vary with the  $V_{\text{OUT(DC)}}$  control. As temperature increases or decreases, from  $T = +25^\circ\text{C}$ ,  $V_{\text{OUT}}$  will then change according to the programmed Temp Slope.

In many cases a form of Equation 4 is needed which yields a  $V_{OUT}$  change with respect to temperature. By rearranging, we get:

$$V_{OUT}(T) = \frac{V_{OUT}(T_S)}{(T - T_0)} = A_V \cdot K \cdot A_{TS} \text{ , (in mV/°C)} \quad (\text{EQ. 5})$$

### EXAMPLE 1: PROGRAMMED TEMPERATURE COMPENSATION EXAMPLE

The ISL21400 can easily compensate for known temperature drift by programming the device for the initial  $V_{OUT}$  setting and Tempco using standard equations and some simple steps. The accuracy of the final programmed output will be limited to the data sheet specs (typically 1% accuracy for  $V_{OUT}$  and Slope).

In this example, an N-Channel MOSFET gate has a  $-2.8\text{mV/°C}$  Tempco from  $-10\text{°C}$  to  $+85\text{°C}$ . A constant bias drain current is desired, with a target  $V_{GS}$  range derived from the data sheet of  $2.5\text{V}$  to  $3.5\text{V}$  at  $+25\text{°C}$ .

**Offset Setting:** Using Equation 2 and targeting

$$V_{OUT} = 3.0\text{VDC};,$$

$$\begin{aligned} V_{OUT}(\text{DC}) &= (A_V \cdot V_{REF} \cdot A_{REF}) = 3.00\text{V} \\ V_{REF} &= 1.20\text{V} \\ A_V \cdot A_{REF} &= 2.50 \end{aligned}$$

Note that  $A_{REF}$  varies from 0 to 1, so to get 2.40,  $A_V = 4$ .

$$A(\text{REF}) = \frac{2.50}{4} = 0.625 = \frac{n}{255}$$

$$\begin{aligned} n &= 159 \text{ decimal} \\ &= 9\text{F hex} \end{aligned}$$

**Temperature Slope Setting:** Using Equation 5, which can solve for Slope directly:

$$V_{OUT}(T) = A_V \cdot K \cdot A_{TS} = -2.8\text{mV/°C}$$

$$A_{TS} = \frac{-2.8}{4 \cdot -2.1}$$

$$A_{TS} = 0.333 = \frac{(2 \cdot m) - 255}{255}$$

$$\begin{aligned} m &= 170 \text{ decimal} \\ &= \text{A9 hex} \end{aligned}$$

The ISL21400 device can be programmed with these calculated parameters and perform temperature compensation or direct control in the target circuit. If parameters change for some reason, then the device can be reprogrammed with new values and the circuit retested.

### EXAMPLE 2. CALCULATING THE $V_{OUT}$ TEMPERATURE SLOPE

In some applications, it may be desirable to calculate what the output voltage and temp slope are, given the programmed register settings. Such an application could be a closed loop system with internal calibration procedure. By reading the registers of the ISL21400, then calculating the

$V_{OUT}$  parameters, the system characteristics can be recorded.

For the example below, let's determine the voltage output,  $V_{OUT}(\text{DC})$  at  $+25\text{°C}$ , and also the change due to temperature variation (ppm) from  $+25\text{°C}$  to  $+85\text{°C}$ .

Equations 2 and 5 will be used to calculate the answers.

Given, the contents of the registers:

$$A_V = 1$$

$$n = 178 \text{ decimal}$$

$$m = 74 \text{ decimal}$$

**Using Equation 2:**

$$\begin{aligned} V_{OUT}(\text{DC}) &= (A_V \cdot V_{REF} \cdot A_{REF}) \\ &= \left( 1 \cdot 1.20 \cdot \frac{178}{255} \right) \\ &= 0.8376\text{V} \end{aligned}$$

**Using Equation 5:**

$$\begin{aligned} V_{OUT}(T) &= (A_V \cdot K \cdot A_{TS}) \text{ mV/°C} \\ &= 1 \cdot -2.1 \cdot \left[ \frac{(2 \cdot 74) - 255}{255} \right] \\ &= 0.8812\text{mV/°C} \end{aligned}$$

Also, to solve for overall temp slope of the output:

$$\frac{0.8812\text{mV/°C}}{872.5\text{mV}} \cdot 10^6 = 1010\text{ppm/°C}$$

Note that Equation 1 can be used directly to solve for output voltage at a given temperature, in this case  $+85\text{°C}$ :

$$\begin{aligned} V_{OUT} &= A_V \cdot \left\{ V_{REF} \cdot \frac{n}{255} + K(T - T_0) \frac{(2 \cdot m) - 255}{255} \right\} \\ V_{OUT}(+85\text{°C}) &= 1 \cdot \left\{ 1.20 \cdot \frac{178}{255} + (-0.0021)(85 - 25) \frac{(2 \cdot 74) - 255}{255} \right\} \\ &= 0.8905\text{V} \end{aligned}$$

### Typical Applications Circuits

**LDMOS RF Power Amplifier (RFPA).** The ISL21400 is used to set the gate bias for the LDMOS transistor in a single stage of an RFPA. Normally this is done with a DAC or digital potentiometer with some discrete temperature compensation circuitry. The ISL21400 simplifies this control and allows a full range of DC bias and tempco control.

A typical circuit can be calibrated for correct bias at room temperature ( $+25\text{°C}$ ) on power-up using a microcontroller or direct  $I^2C$  control. The temperature of the unit can then be increased to the highest operating range, and the Temperature Slope setting can then be adjusted to bring the amplifier back to correct bias. Since the Temp Slope setting has a negligible effect on the room temperature setting, the amplifier will be biased correctly over the operating temperature of the unit.

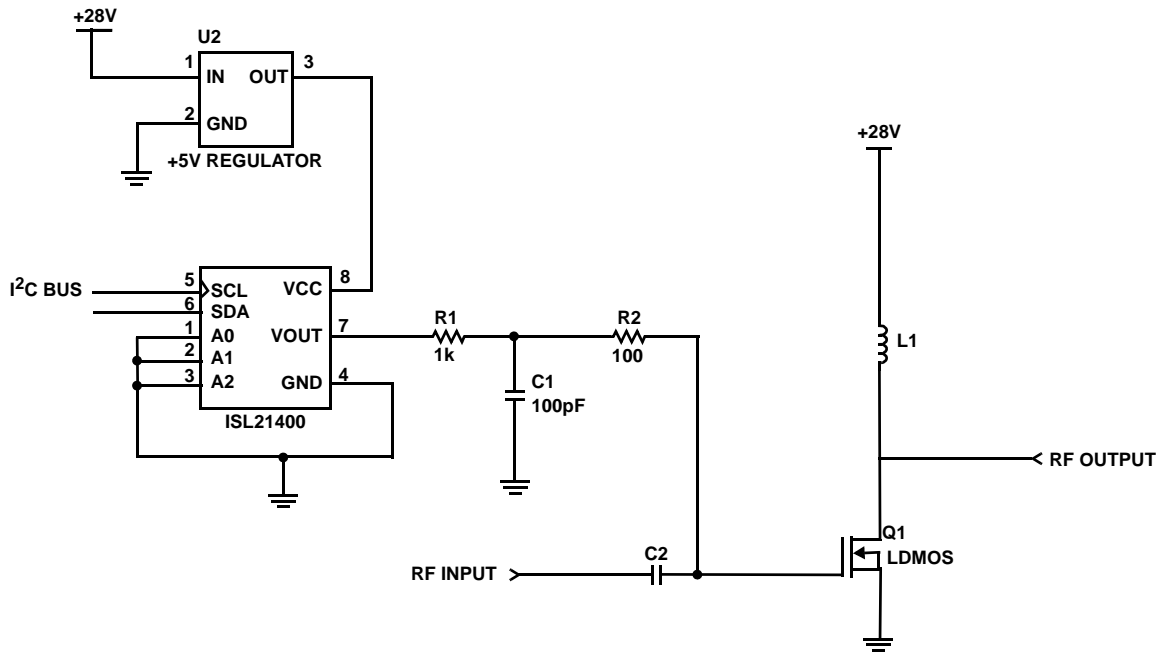
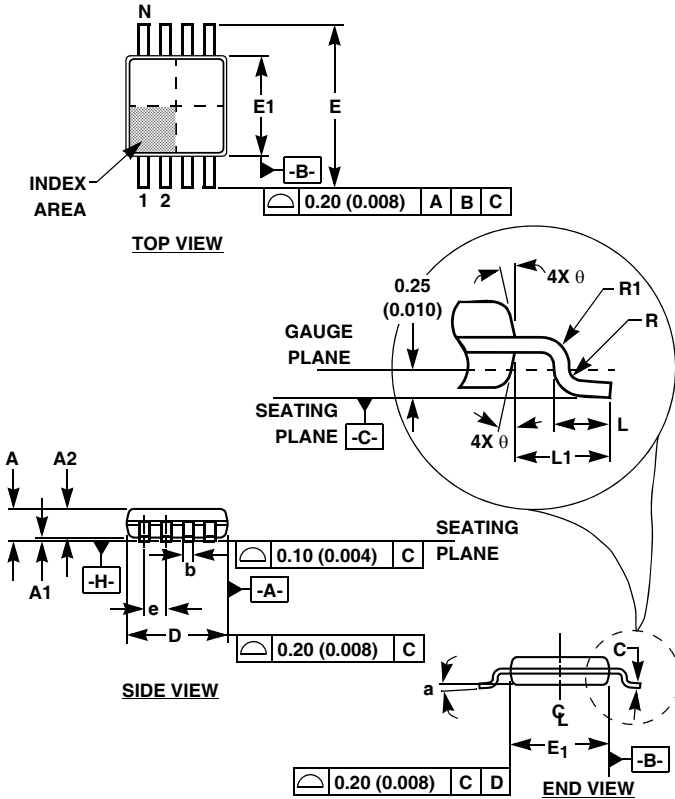


FIGURE 19. LD MOS RFPA BIAS CONTROL



Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)  
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5°	15°	5°	15°	-
α	0°	6°	0°	6°	-

Rev. 2 01/03

NOTES:

- These package dimensions are within allowable dimensions of JEDEC MO-187BA.
- Dimensioning and tolerancing per ANSI Y14.5M-1994.
- Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
- Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. [-H-] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
- Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
- "L" is the length of terminal for soldering to a substrate.
- "N" is the number of terminal positions.
- Terminal numbers are shown for reference only.
- Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
- Datums [-A-] and [-B-] to be determined at Datum plane [-H-].
- Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

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