

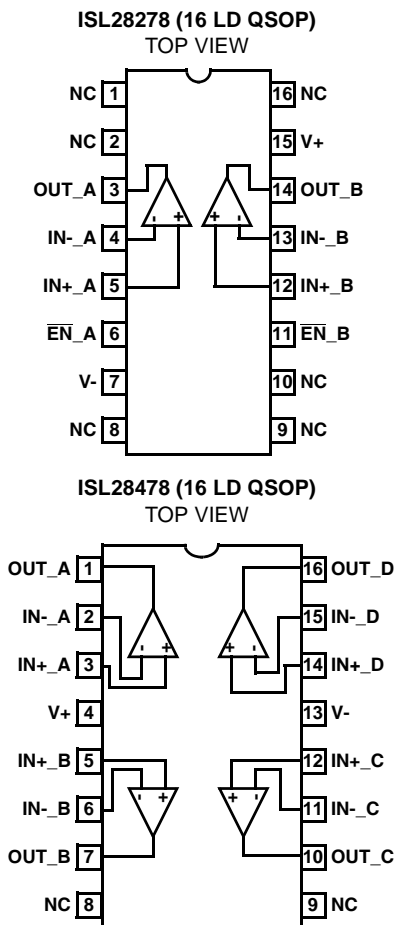
## Dual and Quad Micropower Single Supply Rail-to-Rail Input and Output (RRIO) Op Amp

The ISL28278 and ISL28478 are dual and quad channel micropower operational amplifiers optimized for single supply operation over the 2.4V to 5.5V range. They can be operated from one lithium cell or two Ni-Cd batteries. For equivalent performance in a single channel op amp reference EL8178.

These devices feature an Input Range Enhancement Circuit (IREC) which enables them to maintain CMRR performance for input voltages 10% above the positive supply rail and to 100mV below the negative supply. The output operation is rail-to-rail.

The ISL28278 and ISL28478 draw minimal supply current while meeting excellent DC-accuracy, AC-performance, noise and output drive specifications. The ISL28278 contains a power down enable pin that reduces the power supply current to typically 4 $\mu$ A in the disabled state.

### Pinouts



### Features

- Low power 120 $\mu$ A typical supply current (ISL28278)
- 225 $\mu$ V max offset voltage
- 30pA max input bias current
- 300kHz typical gain-bandwidth product
- 105dB typical PSRR
- 100dB typical CMRR
- Single supply operation down to 2.4V
- Input is capable of swinging above V+ and below V- (ground sensing)
- Rail-to-rail input and output (RRIO)
- Enable Pin (ISL28278 only)
- Pb-free (RoHS compliant)

### Applications

- Battery- or solar-powered systems
- 4mA to 25mA current loops
- Handheld consumer products
- Medical devices
- Thermocouple amplifiers
- Photodiode pre-amps
- pH probe amplifiers

### Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28278FAZ*	28278 FAZ	16 Ld QSOP	MDP0040
ISL28478FAZ*	28478 FAZ	16 Ld QSOP	MDP0040

\*Add "-T7" suffix is for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

# ISL28278, ISL28478

## Absolute Maximum Ratings (T<sub>A</sub> = +25°C)

Supply Voltage, V <sub>-</sub> to V <sub>+</sub>	5.75V
Supply Turn On Voltage Slew Rate	1V/μs
Differential Input Current	5mA
Differential Input Voltage	0.5V
Input Voltage	V <sub>-</sub> - 0.5V to V <sub>+</sub> + 0.5V
ESD Tolerance	
Human Body Model	.3kV
Machine Model	.300V
Charged Device Model	1200V

## Thermal Information

Thermal Resistance (Typical, Note 1)	θ <sub>JA</sub> (°C/W)
16 Ld QSOP Package	112
Output Short-Circuit Duration	Indefinite
Ambient Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature	+125°C
Pb-free reflow profile	see link below
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

### NOTE:

1. θ<sub>JA</sub> is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T<sub>J</sub> = T<sub>C</sub> = T<sub>A</sub>

## Electrical Specifications V<sub>+</sub> = 5V, V<sub>-</sub> = 0V, V<sub>CM</sub> = 2.5V, R<sub>L</sub> = Open, T<sub>A</sub> = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C, temperature data established by characterization.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
<b>DC SPECIFICATIONS</b>						
V <sub>OS</sub>	Input Offset Voltage		-225 <b>-450</b>	±0.20	225 <b>450</b>	μV
$\frac{\Delta V_{OS}}{\Delta T}$	Input Offset Voltage vs Temperature			1.0		μV/°C
I <sub>OS</sub>	Input Offset Current	-40°C to +85°C	-30 <b>-80</b>	±5	30 <b>80</b>	pA
I <sub>B</sub>	Input Bias Current	-40°C to +85°C	-30 <b>-80</b>	±10	30 <b>80</b>	pA
CMIR	Common-Mode Voltage Range	Guaranteed by CMRR	<b>0</b>		<b>5</b>	V
CMRR	Common-Mode Rejection Ratio	V <sub>CM</sub> = 0V to 5V	80 <b>75</b>	100		dB
PSRR	Power Supply Rejection Ratio	V <sub>+</sub> = 2.4V to 5.5V	85 <b>80</b>	105		dB
A <sub>VOL</sub>	Large Signal Voltage Gain	V <sub>O</sub> = 0.5V to 4.5V, R <sub>L</sub> = 100kΩ	200 <b>190</b>	300		V/mV
		V <sub>O</sub> = 0.5V to 4.5V, R <sub>L</sub> = 1kΩ		60		V/mV
V <sub>OUT</sub>	Maximum Output Voltage Swing	Output low, R <sub>L</sub> = 100kΩ		3	6 <b>30</b>	mV
		Output low, R <sub>L</sub> = 1kΩ		130	175 <b>225</b>	mV
		Output high, R <sub>L</sub> = 100kΩ	4.990 <b>4.97</b>	4.996		V
		Output high, R <sub>L</sub> = 1kΩ	4.800 <b>4.750</b>	4.880		V
I <sub>S,ON</sub>	Quiescent Supply Current, Enabled	ISL28278, All channels enabled.		120	156 <b>175</b>	μA
		ISL28478, All channels enabled.		240	315 <b>350</b>	μA

## ISL28278, ISL28478

**Electrical Specifications**  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ ,  $T_A = +25^\circ\text{C}$ . **Boldface limits apply over the operating temperature range,  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ , temperature data established by characterization. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 2)	TYP	MAX (Note 2)	UNIT
$I_{S,OFF}$	Quiescent Supply Current, Disabled	All channels disabled. ISL28278		4	<b>7 9</b>	$\mu\text{A}$
$I_{O+}$	Short Circuit Sourcing Capability	$R_L = 10\Omega$	<b>24 20</b>	31		mA
$I_{O-}$	Short Circuit Sinking Capability	$R_L = 10\Omega$		-26	<b>-24 -20</b>	mA
$V_{SUPPLY}$	Supply Operating Range	$V_-$ to $V_+$	<b>2.4</b>		<b>5.5</b>	V
$\overline{V}_{ENH}$	$\overline{EN}$ Pin High Level	ISL28278	<b>2</b>			V
$\overline{V}_{ENL}$	$\overline{EN}$ Pin Low Level	ISL28278			<b>0.8</b>	V
$\overline{I}_{ENH}$	$\overline{EN}$ Pin Input High Current	$\overline{V}_{EN} = V_+$ ISL28278		0.8	<b>1 1.5</b>	$\mu\text{A}$
$\overline{I}_{ENL}$	$\overline{EN}$ Pin Input Low Current	$\overline{V}_{EN} = V_-$ ISL28278		0	<b>0.1</b>	$\mu\text{A}$
<b>AC SPECIFICATIONS</b>						
GBW	Gain Bandwidth Product	$A_V = 100$ , $R_F = 100k\Omega$ , $R_G = 1k\Omega$ , $R_L = 10k\Omega$ to $V_{CM}$		300		kHz
$e_n$	Input Noise Voltage Peak-to-Peak	$f = 0.1\text{Hz}$ to $10\text{Hz}$		3		$\mu\text{V}_{P-P}$
	Input Noise Voltage Density	$f_O = 1\text{kHz}$		48		$\text{nV}/\sqrt{\text{Hz}}$
$i_n$	Input Noise Current Density	$f_O = 1\text{kHz}$		9		$\text{fA}/\sqrt{\text{Hz}}$
CMRR @ 60Hz	Input Common Mode Rejection Ratio	$V_{CM} = 1V_{P-P}$ , $R_L = 10k\Omega$ to $V_{CM}$		-70		dB
PSRR+ @ 120Hz	Power Supply Rejection Ratio, +V	$V_+, V_- = \pm 1.2V$ and $\pm 2.5V$ , $V_{SOURCE} = 1V_{P-P}$ , $R_L = 10k\Omega$ to $V_{CM}$		-80		dB
PSRR- @ 120Hz	Power Supply Rejection Ratio, -V	$V_+, V_- = \pm 1.2V$ and $\pm 2.5V$ $V_{SOURCE} = 1V_{P-P}$ , $R_L = 10k\Omega$ to $V_{CM}$		-60		dB
<b>TRANSIENT RESPONSE</b>						
SR	Slew Rate		$\pm 0.12$ <b><math>\pm 0.09</math></b>	$\pm 0.14$	$\pm 0.16$ <b><math>\pm 0.21</math></b>	$\text{V}/\mu\text{s}$
$t_{\overline{EN}}$	Enable to Output Turn-on Delay Time, 10% $\overline{EN}$ to 10% $V_{out}$	$\overline{V}_{EN} = 5V$ to $0V$ , $A_V = -1$ , $R_G = R_F = R_L = 1k$ to $V_{CM}$ , ISL28278		2		$\mu\text{s}$
	Enable to Output Turn-off Delay Time, 10% $\overline{EN}$ to 10% $V_{out}$	$\overline{V}_{EN} = 0V$ to $5V$ , $A_V = -1$ , $R_G = R_F = R_L = 1k$ to $V_{CM}$ , ISL28278		0.1		$\mu\text{s}$

NOTE:

- Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.

**Typical Performance Curves**  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ , unless otherwise specified.

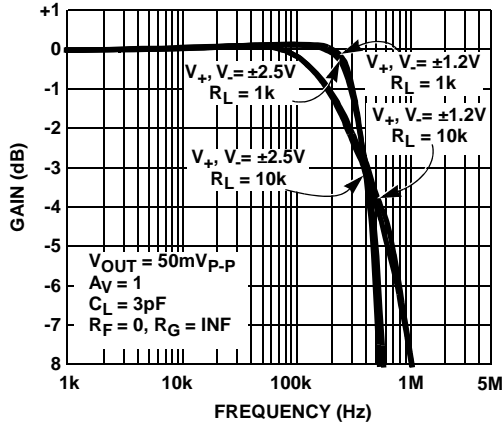


FIGURE 1. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

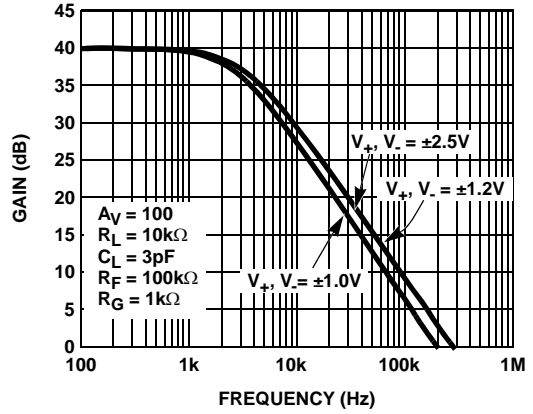


FIGURE 2. FREQUENCY RESPONSE vs SUPPLY VOLTAGE

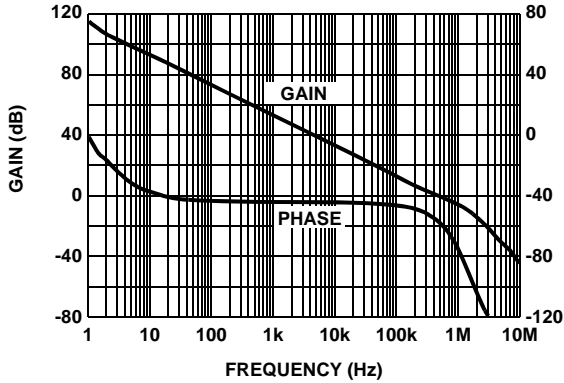


FIGURE 3.  $A_{VOL}$  vs FREQUENCY @  $100k\Omega$  LOAD

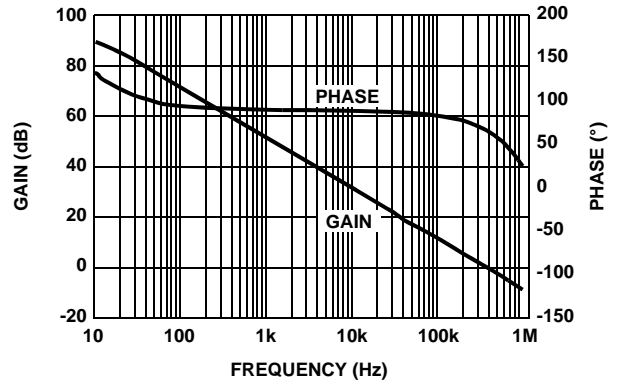


FIGURE 4.  $A_{VOL}$  vs FREQUENCY @  $1k\Omega$  LOAD

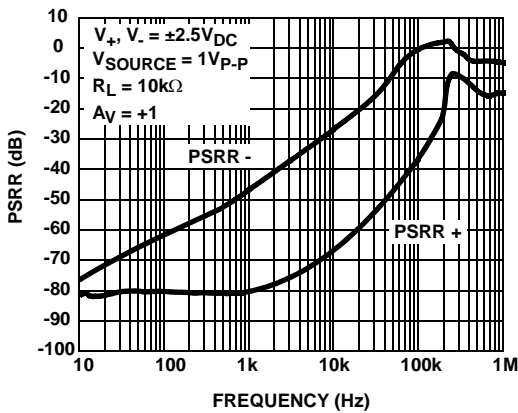


FIGURE 5. PSRR vs FREQUENCY

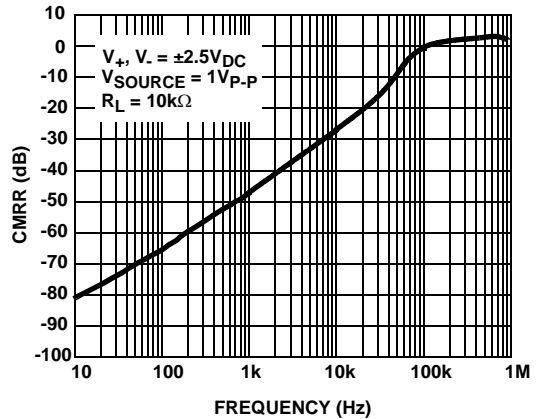


FIGURE 6. CMRR vs FREQUENCY

**Typical Performance Curves**  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

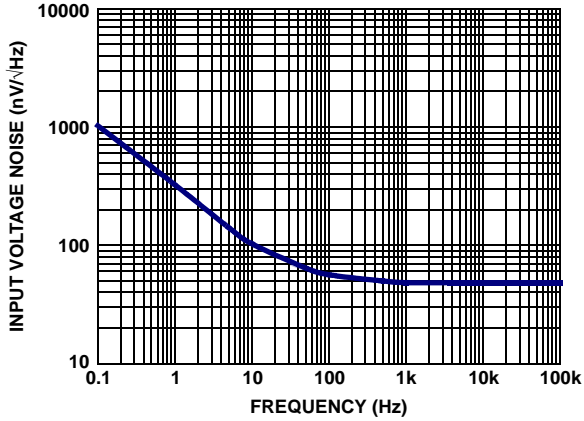


FIGURE 7. VOLTAGE NOISE vs FREQUENCY

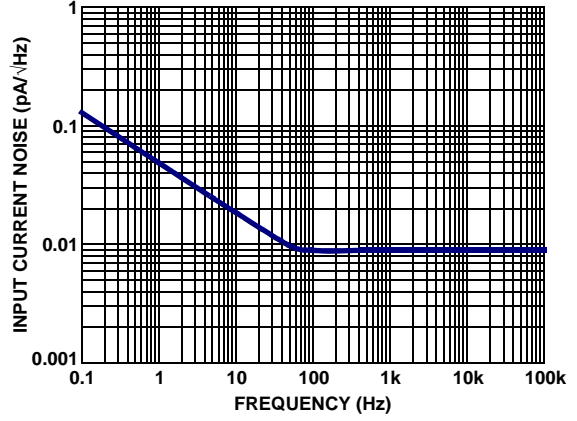


FIGURE 8. CURRENT NOISE vs FREQUENCY

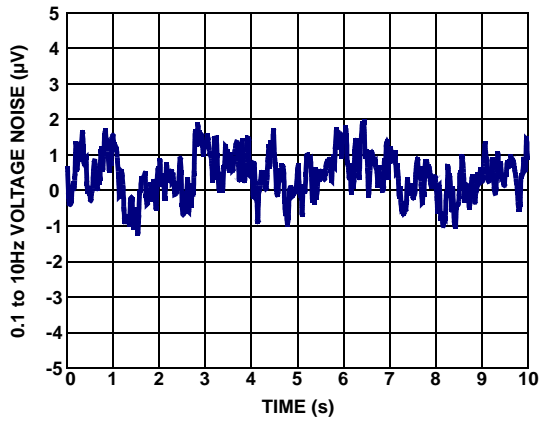


FIGURE 9. 0.1Hz TO 10Hz INPUT VOLTAGE NOISE

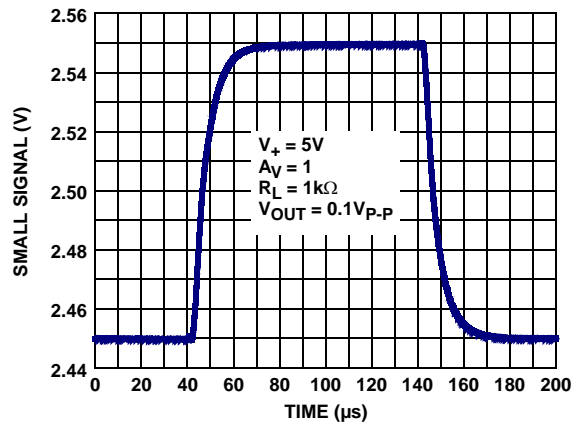


FIGURE 10. SMALL SIGNAL TRANSIENT RESPONSE

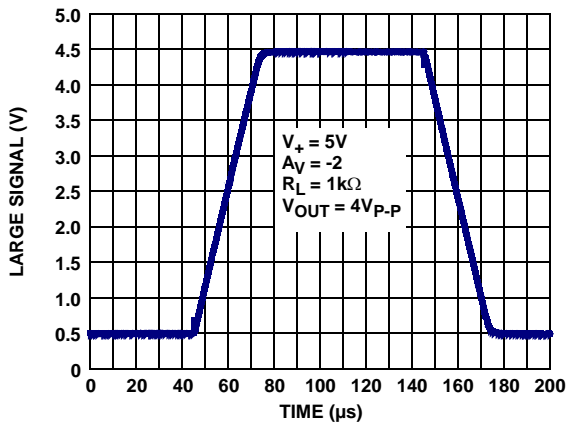


FIGURE 11. LARGE SIGNAL TRANSIENT RESPONSE

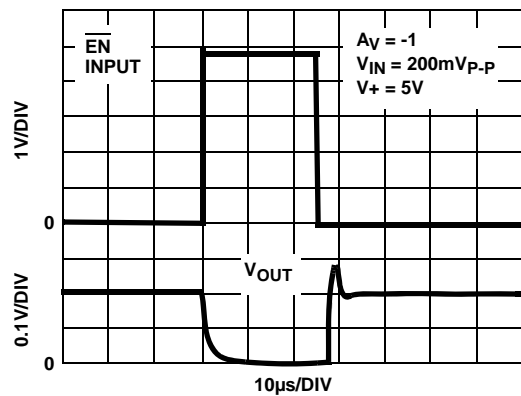


FIGURE 12. ISL28278 ENABLE TO OUTPUT DELAY TIME

**Typical Performance Curves**  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

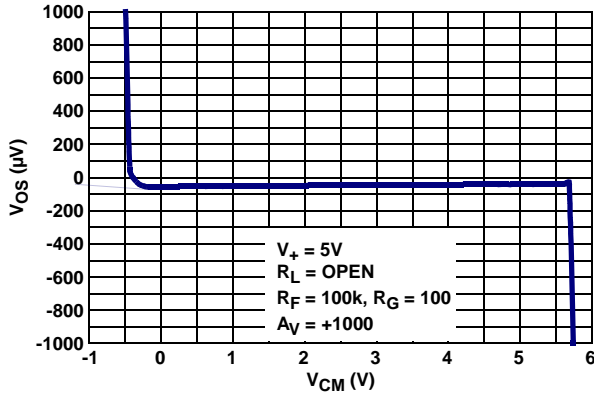


FIGURE 13. INPUT OFFSET VOLTAGE vs COMMON MODE INPUT VOLTAGE

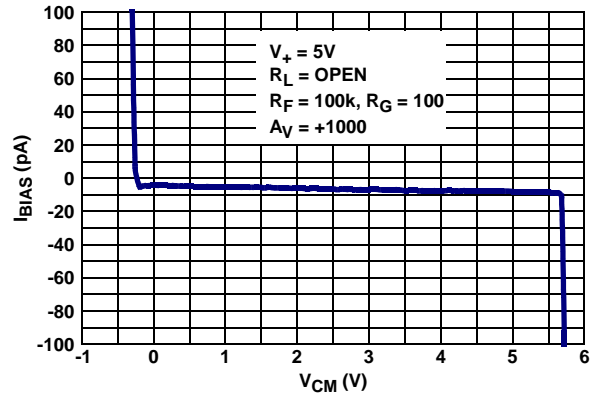


FIGURE 14. INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

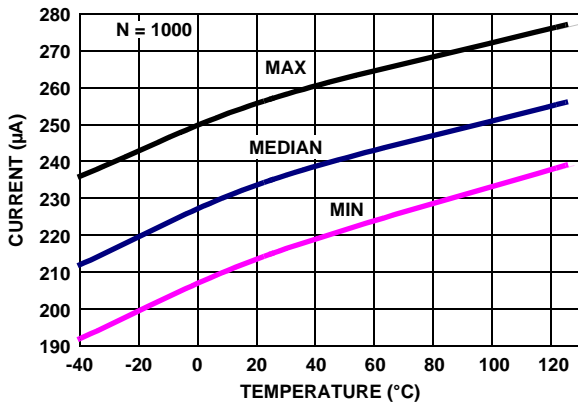


FIGURE 15. ISL28478 SUPPLY CURRENT vs TEMPERATURE,  $V_+$ ,  $V_- = \pm 2.5V$ ,  $R_L = \text{INF}$

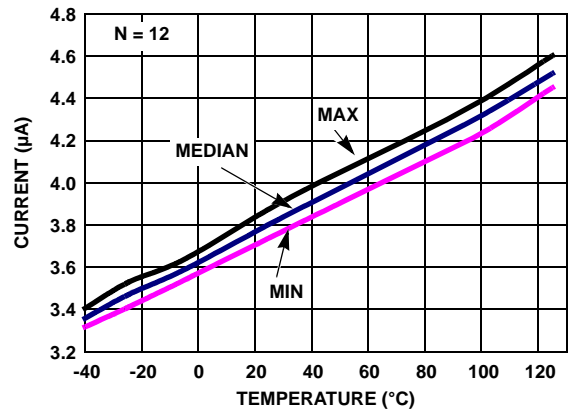


FIGURE 16. ISL28278 DISABLED SUPPLY CURRENT vs TEMPERATURE,  $V_+$ ,  $V_- = \pm 2.5V$ ,  $R_L = \text{INF}$

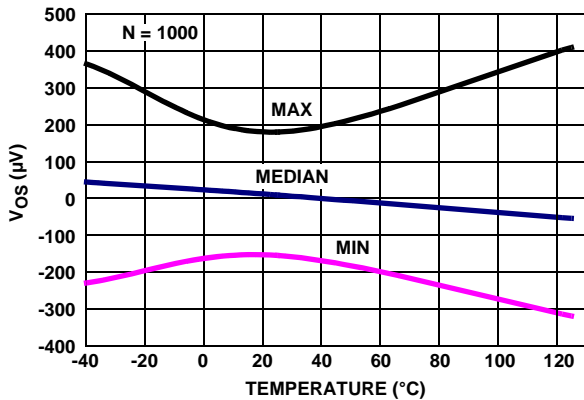


FIGURE 17.  $V_{OS}$  vs TEMPERATURE,  $V_{IN} = 0V$ ,  $V_+$ ,  $V_- = \pm 2.5V$

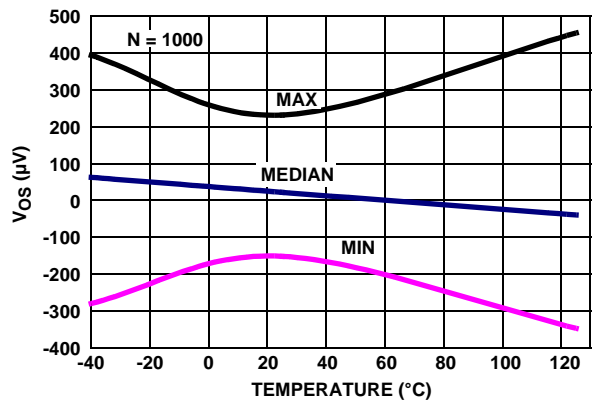


FIGURE 18.  $V_{OS}$  vs TEMPERATURE,  $V_{IN} = 0V$ ,  $V_+$ ,  $V_- = \pm 1.2V$

**Typical Performance Curves**  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

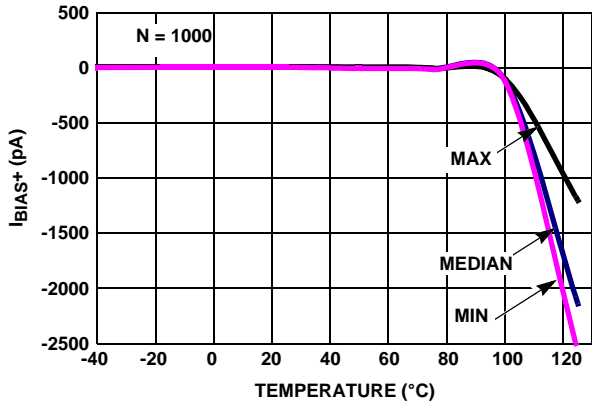


FIGURE 19.  $I_{BIAS+}$  vs TEMPERATURE,  $V_+, V_- = \pm 2.5V$

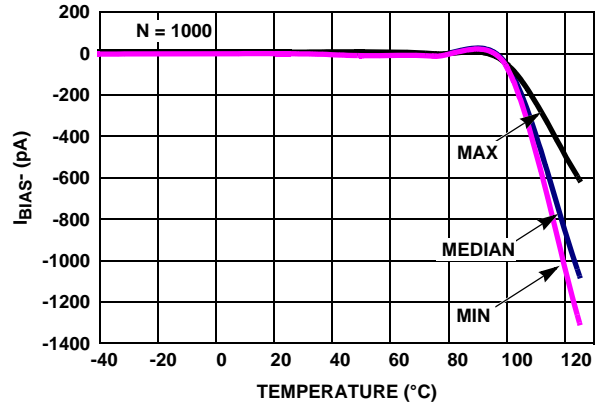


FIGURE 20.  $I_{BIAS-}$  vs TEMPERATURE,  $V_+, V_- = \pm 2.5V$

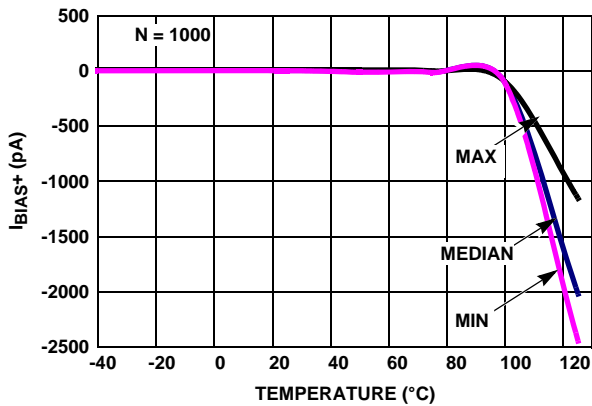


FIGURE 21.  $I_{BIAS+}$  vs TEMPERATURE,  $V_+, V_- = \pm 1.2V$

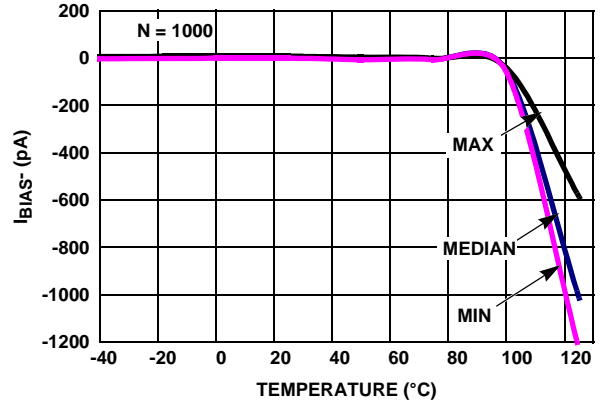


FIGURE 22.  $I_{BIAS-}$  vs TEMPERATURE,  $V_+, V_- = \pm 1.2V$

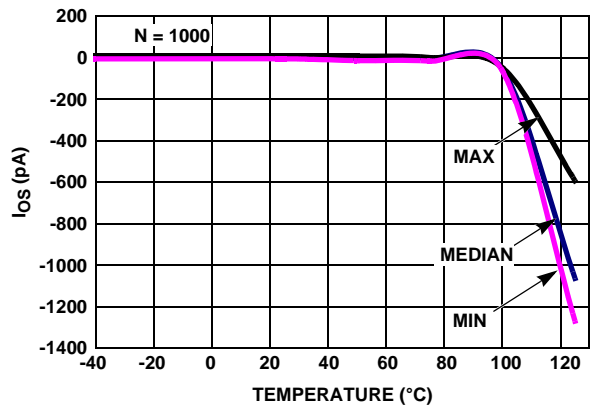


FIGURE 23.  $I_{OS}$  vs TEMPERATURE,  $V_+, V_- = \pm 2.5V$

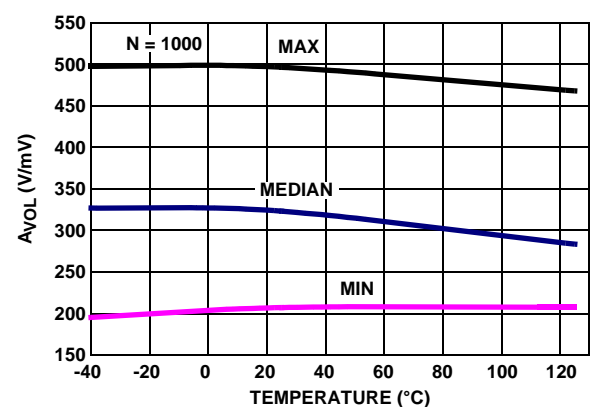


FIGURE 24.  $A_{VOL}$  vs TEMPERATURE,  $V_+, V_- = \pm 2.5V$ ,  $R_L = 100k$

**Typical Performance Curves**  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

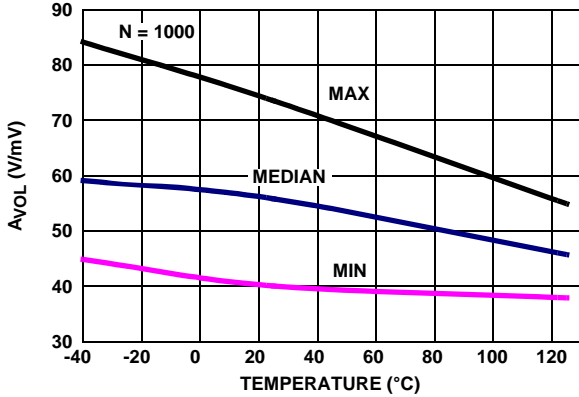


FIGURE 25.  $A_{VOL}$  vs TEMPERATURE,  $V_+$ ,  $V_- = \pm 2.5V$ ,  $R_L = 1k$

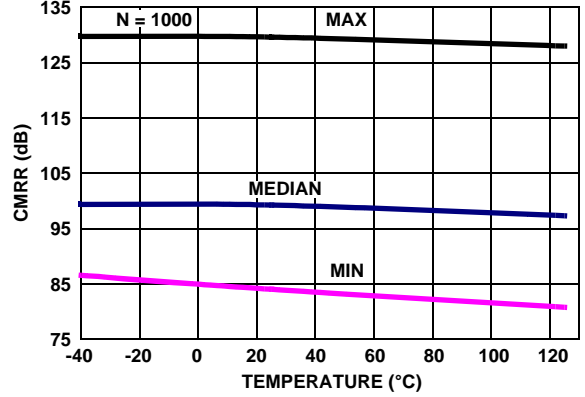


FIGURE 26.  $CMRR$  vs TEMPERATURE,  $V_{CM} = +2.5V$  TO  $-2.5V$ ,  $V_+$ ,  $V_- = \pm 2.5V$

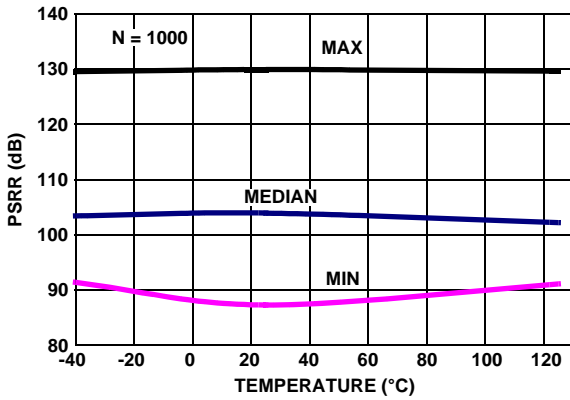


FIGURE 27.  $PSRR$  vs TEMPERATURE,  $V_+$ ,  $V_- = \pm 1.2V$  TO  $\pm 2.5V$

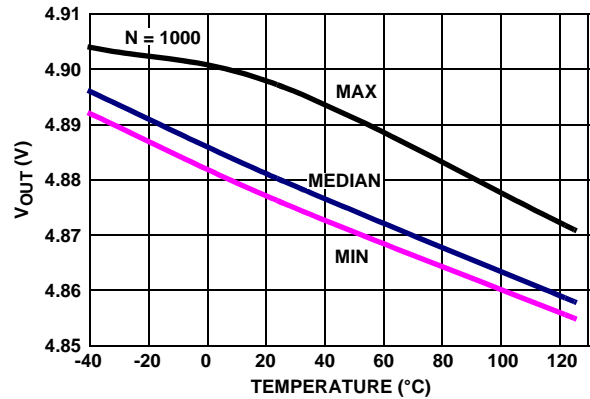


FIGURE 28.  $V_{OUT}$  HIGH vs TEMPERATURE,  $V_+$ ,  $V_- = \pm 2.5V$ ,  $R_L = 1k$

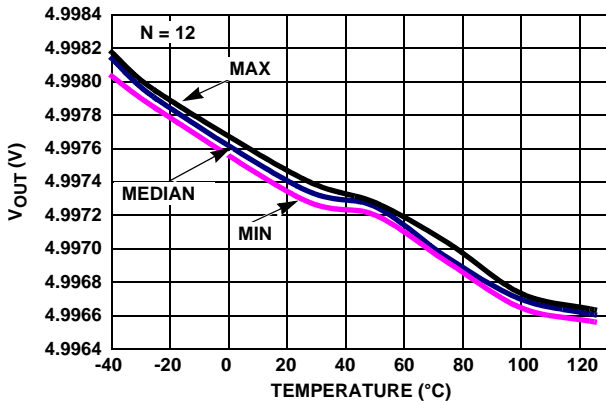


FIGURE 29.  $V_{OUT}$  HIGH vs TEMPERATURE,  $V_+$ ,  $V_- = \pm 2.5V$ ,  $R_L = 100k$

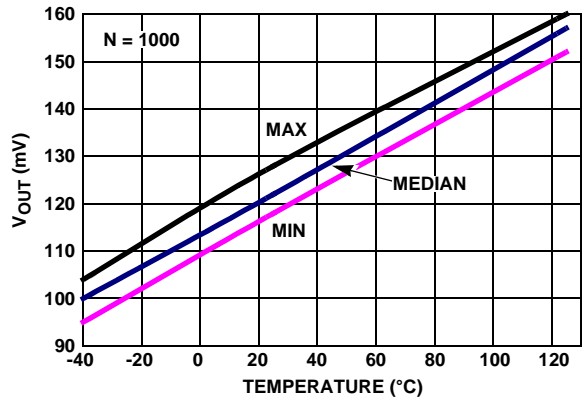


FIGURE 30.  $V_{OUT}$  LOW vs TEMPERATURE,  $V_+$ ,  $V_- = \pm 2.5V$ ,  $R_L = 1k$



**Typical Performance Curves**  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

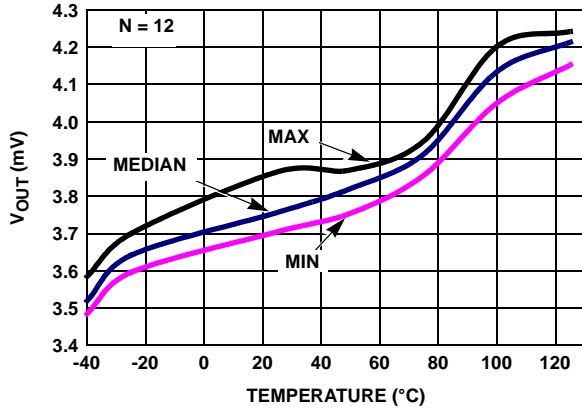


FIGURE 31.  $V_{OUT\ LOW}$  vs TEMPERATURE,  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

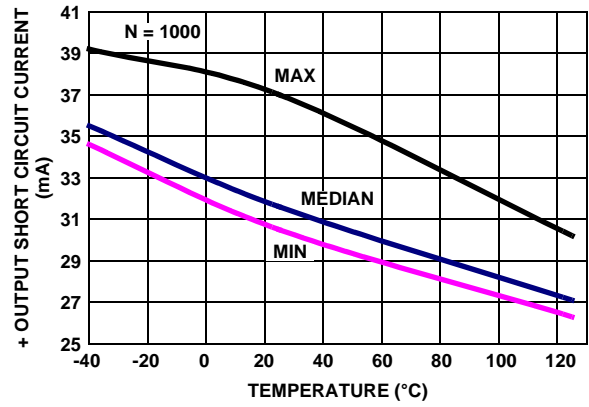


FIGURE 32. +OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE,  $V_{IN} = -2.55V$ ,  $R_L = 10\Omega$ ,  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

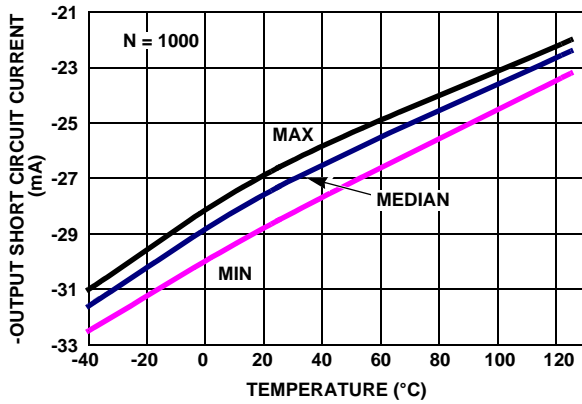


FIGURE 33. -OUTPUT SHORT CIRCUIT CURRENT vs TEMPERATURE,  $V_{IN} = +2.55V$ ,  $R_L = 10\Omega$ ,  $V_+ = 5V$ ,  $V_- = 0V$ ,  $V_{CM} = 2.5V$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

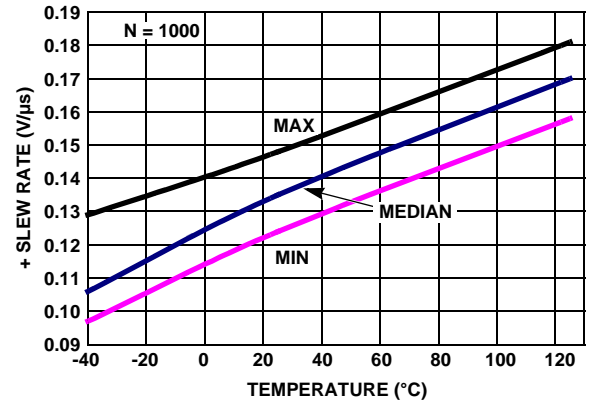


FIGURE 34. +SLEW RATE vs TEMPERATURE,  $V_{OUT} = \pm 1.5V$ ,  $A_V = +2$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

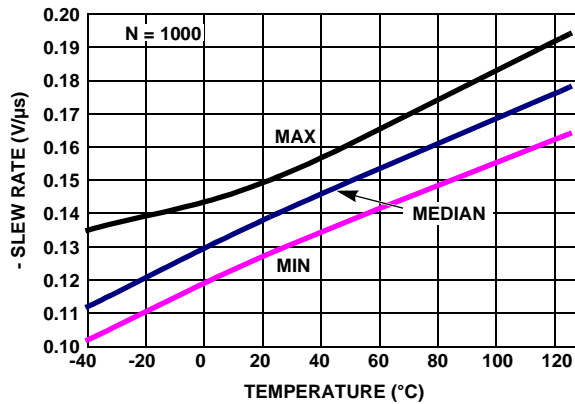
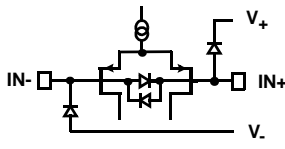


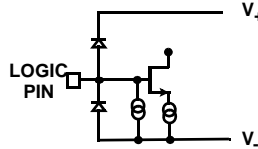
FIGURE 35. -SLEW RATE vs TEMPERATURE,  $V_{OUT} = \pm 1.5V$ ,  $A_V = +2$ ,  $R_L = \text{Open}$ , unless otherwise specified. (Continued)

**Pin Descriptions**

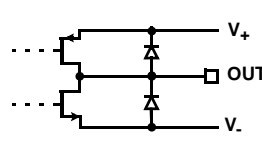
ISL28278 (16 LD QSOP)	ISL28478 (16 LD QSOP)	PIN NAME	EQUIVALENT CIRCUIT	DESCRIPTION
3	1	OUT_A	Circuit 3	Amplifier A output
4	2	IN-_A	Circuit 1	Amplifier A inverting input
5	3	IN+_A	Circuit 1	Amplifier A non-inverting input
15	4	V+	Circuit 4	Positive power supply
12	5	IN+_B	Circuit 1	Amplifier B non-inverting input
13	6	IN-_B	Circuit 1	Amplifier B inverting input
14	7	OUT_B	Circuit 3	Amplifier B output
1, 2, 8, 9, 10, 16	8, 9	NC		No internal connection
	10	OUT_C	Circuit 3	Amplifier C output
	11	IN-_C	Circuit 1	Amplifier C inverting input
	12	IN+_C	Circuit 1	Amplifier B non-inverting input
7	13	V-	Circuit 4	Negative power supply
	14	IN+_D	Circuit 1	Amplifier D non-inverting input
	15	IN-_D	Circuit 1	Amplifier D inverting input
	16	OUT_D	Circuit 3	Amplifier D output
6		$\overline{\text{EN}}_A$	Circuit 2	Amplifier A enable pin internal pull-down; Logic "1" selects the disabled state; Logic "0" selects the enabled state.
11		$\overline{\text{EN}}_B$	Circuit 2	Amplifier B enable pin with internal pull-down; Logic "1" selects the disabled state; Logic "0" selects the enabled state.



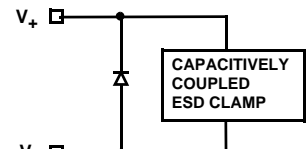
CIRCUIT 1



CIRCUIT 2



CIRCUIT 3



CIRCUIT 4

**Applications Information**

**Introduction**

The ISL28278 and ISL28478 are dual and quad CMOS rail-to-rail input, output (RRIO) micropower operational amplifiers. These devices are designed to operate from a single supply (2.4V to 5.5V) or dual supplies ( $\pm 1.2V$  to  $\pm 2.75V$ ) while drawing only 120 $\mu A$  (ISL28278) of supply current. This combination of low power and precision performance makes these devices suitable for solar and battery power applications.

**Rail-to-Rail Input**

Many rail-to-rail input stages use two differential input pairs; a long-tail PNP (or PFET) and an NPN (or NFET). Severe penalties have to be paid for this circuit topology. As the input signal moves from one supply rail to another, the operational amplifier switches from one input pair to the other causing drastic changes in input offset voltage and an

undesired change in magnitude and polarity of input offset current.

The ISL28278 achieves input rail-to-rail without sacrificing important precision specifications and degrading distortion performance. The devices' input offset voltage exhibits a smooth behavior throughout the entire common-mode input range. The input bias current versus the common-mode voltage range gives us an undistorted behavior from typically 100mV below the negative rail and 10% higher than the  $V_+$  rail (0.5V higher than  $V_+$  when  $V_+$  equals 5V).

**Input Protection**

All input terminals have internal ESD protection diodes to the positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. There is an additional pair of back-to-back diodes across the input terminals. For applications where the input differential voltage is expected to exceed 0.5V, external series resistors must be used to ensure the input currents never exceed 5mA.

**Rail-to-Rail Output**

A pair of complementary MOSFET devices are used to achieve the rail-to-rail output swing. The NMOS sinks current to swing the output in the negative direction. The PMOS sources current to swing the output in the positive direction. Both parts, with a 100kΩ load, will typically swing to within 4mV of the positive supply rail and within 3mV of the negative supply rail.

**Enable/Disable Feature**

The ISL28278 offers two  $\overline{EN}$  pins ( $\overline{EN}_A$  and  $\overline{EN}_B$ ) which disable the op amp when pulled up to at least 2.0V. In the disabled state (output in a high impedance state), the part consumes typically 4μA. By disabling the part, multiple parts can be connected together as a MUX. The outputs are tied together in parallel and a channel can be selected by the  $\overline{EN}$  pins. The loading effects of the feedback resistors of the disabled amplifier must be considered when multiple amplifier outputs are connected together. The  $\overline{EN}$  pin also has an internal pull-down. If left open, the  $\overline{EN}$  pin will pull to the negative rail and the device will be enabled by default.

**Using Only One Channel**

The ISL28278 and ISL28478 are dual and quad channel op amps. If the application only requires one channel when using the ISL28278 or less than 4 channels when using the ISL28478, the user must configure the unused channel(s) to prevent them from oscillating. The unused channel(s) will oscillate if the input and output pins are floating. This will result in higher than expected supply currents and possible noise injection into the channel being used. The proper way to prevent this oscillation is to short the output to the negative input and ground the positive input (as shown in Figure 36).

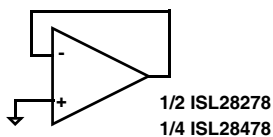


FIGURE 36. PREVENTING OSCILLATIONS IN UNUSED CHANNELS

**Proper Layout Maximizes Performance**

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28278 and ISL28478, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board. When input leakage current is a concern, the use of guard rings around the amplifier inputs will further reduce leakage currents. Figure 37 shows a guard ring example for a unity gain amplifier that uses the low impedance amplifier output at the same voltage as the high impedance input to eliminate surface leakage. The guard ring does not need to be a specific width, but it should

form a continuous loop around both inputs. For further reduction of leakage currents, components can be mounted to the PC board using Teflon standoff insulators.

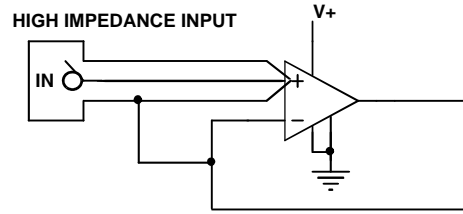


FIGURE 37. GUARD RING EXAMPLE FOR UNITY GAIN AMPLIFIER

**Current Limiting**

The ISL28278 and ISL28478 have no internal current-limiting circuitry. If the output is shorted, it is possible to exceed the Absolute Maximum Rating for output current or power dissipation, potentially resulting in the destruction of the device.

**Power Dissipation**

It is possible to exceed the +150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature ( $T_{JMAX}$ ) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times PD_{MAXTOTAL}) \tag{EQ. 1}$$

where:

- $PD_{MAXTOTAL}$  is the sum of the maximum power dissipation of each amplifier in the package ( $PD_{MAX}$ )
- $PD_{MAX}$  for each amplifier is calculated in Equation 2:

$$PD_{MAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \tag{EQ. 2}$$

where:

- $T_{MAX}$  = Maximum ambient temperature
- $\theta_{JA}$  = Thermal resistance of the package
- $PD_{MAX}$  = Maximum power dissipation of 1 amplifier
- $V_S$  = Supply voltage (Magnitude of  $V_+$  and  $V_-$ )
- $I_{SMAX}$  = Maximum supply current of 1 amplifier
- $V_{OUTMAX}$  = Maximum output voltage swing of the application
- $R_L$  = Load resistance

## Application Circuits

### THERMOCOUPLE AMPLIFIER

Thermocouples are the most popular temperature-sensing device because of their low cost, interchangeability, and ability to measure a wide range of temperatures. The ISL28x88 (see Figure 38) is used to convert the differential thermocouple voltage into single-ended signal with 10x gain. The amplifier's rail-to-rail input characteristic allows the thermocouple to be biased at ground and the amplifier to run from a single 5V supply.

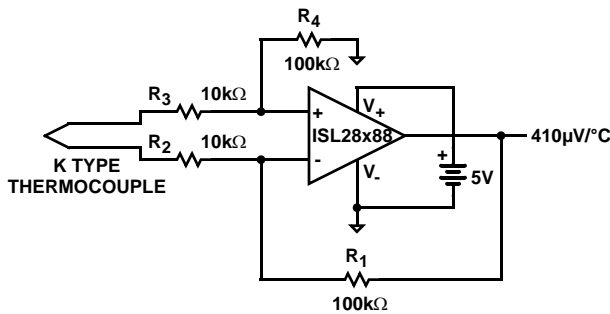


FIGURE 38. THERMOCOUPLE AMPLIFIER

### ECG AMPLIFIER

ECG amplifiers must extract millivolt low frequency AC signals from the skin of the patient while rejecting AC common mode interference and static DC potentials created at the electrode-to-skin interface. In Figure 39, the ISL28278 (U1) forms one of the multiple high gain AC band-pass amplifiers using active feedback. Amplifier U1B and RC RF1, CF1 form a high gain LP filtered amplifier with the corner frequency given by Equation 3:

$$f\text{-HPF}_{-3\text{dB}} = \frac{1}{2 \times \pi \times \text{RF1} \times \text{CF1}} \quad (\text{EQ. 3})$$

Inserting the low pass amplifier, U1B, in U1A's feedback loop results in an overall high-pass frequency response. Voltage divider pairs  $R_1$ - $R_2$  and  $R_3$ - $R_4$  set the overall amplifier pass-band gain. The DC input offset is cancelled by U1B at U1A's inverting input. Resistor divider pair,  $R_3$ - $R_4$  define the maximum input DC level that is cancelled, and is given by Equation 4:

$$V_{\text{INDC}} = V_+ \times \left( \frac{R_4}{R_3 + R_4} \right) \quad (\text{EQ. 4})$$

In the passband range, U1B's gain is +1 and the total signal gain is defined by the divider ratios according to Equation 5:

$$V_{\text{OUTU1 GAIN}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \left( \frac{R_1 + R_2}{R_2} \right) \times \left( \frac{R_3 + R_4}{R_4} \right) \quad (\text{EQ. 5})$$

At frequencies greater than the LPF corner, the  $R_1$ - $C_1$  and  $R_3$ - $C_3$  networks works to roll-off U1A's gain to unity. Setting both R-C time constants to the same value simplifies to Equation 6:

$$f\text{-LPF}_{-3\text{dB}} = \frac{1}{2 \times \pi \times R_1 \times C_1} \quad (\text{EQ. 6})$$

Right leg drive and reference amplifiers U2A and U2B form a DC feedback loop that applies a correction voltage at the Right Leg electrode to cancel out DC and low frequency body interference. The voltage at the  $V_{\text{CM}}$  sense electrode is maintained at the reference voltage set by RF1-RF2.

With the values shown in Figure 39, the ECG circuit performance parameters are:

1. Supply Voltage Range = +2.4V to +5.5V
2. Total Supply Current Draw @ +5V = 500μA (typ)
3. Common-Mode Reference Voltage ( $V_{\text{CM}}$ ) =  $V_+/2$
4. Max DC Input Offset Voltage =  $V_{\text{CM}} \pm 0.18\text{V}$  to  $\pm 0.41\text{V}$
5. Passband Gain = 425V/V
6. Lower -3dB Frequency = 0.05Hz
7. Upper -3dB Frequency = 159Hz

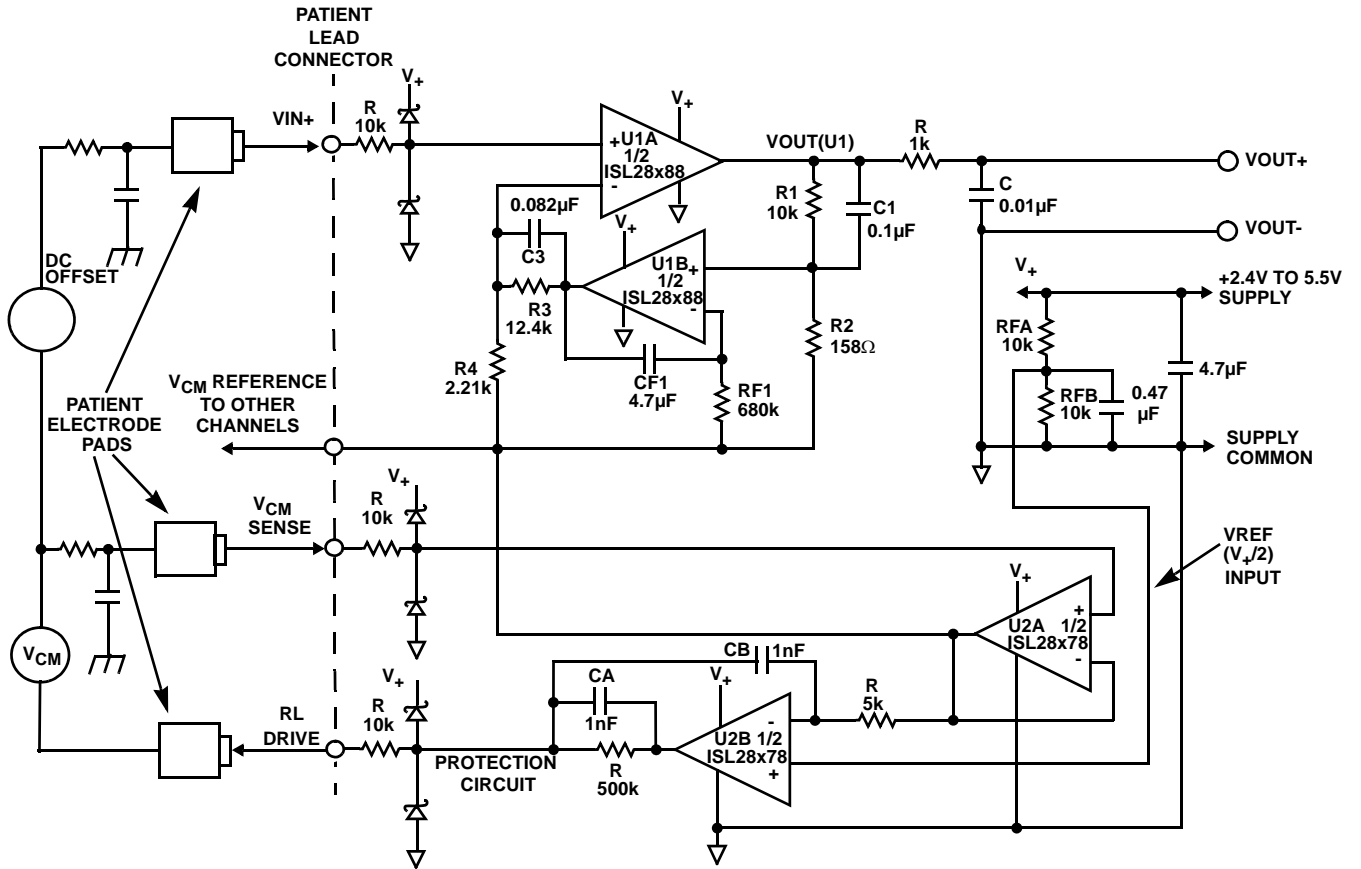
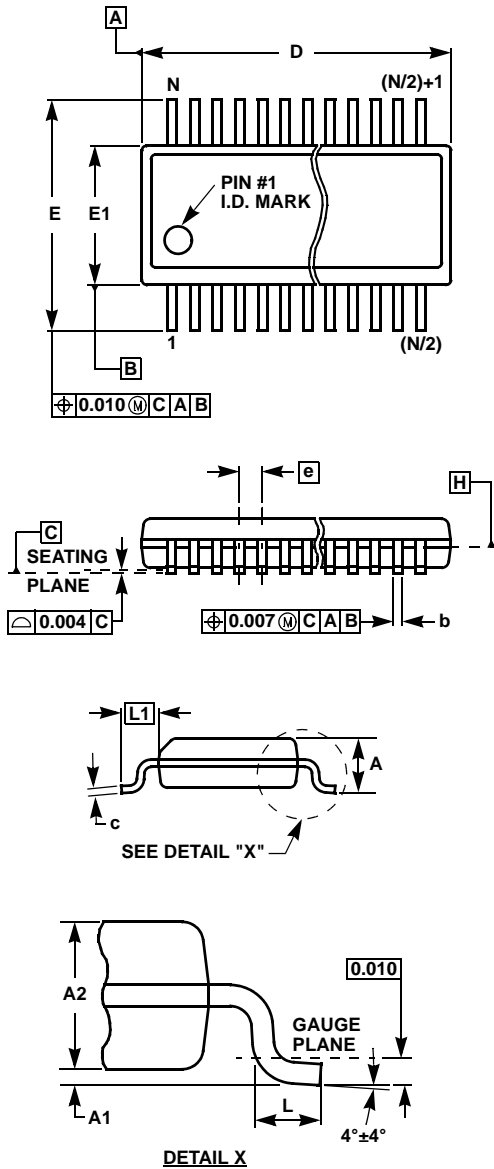


FIGURE 39. ECG AMPLIFIER

Quarter Size Outline Plastic Packages Family (QSOP)



MDP0040

QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY

SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	±0.002	-
A2	0.056	0.056	0.056	±0.004	-
b	0.010	0.010	0.010	±0.002	-
c	0.008	0.008	0.008	±0.001	-
D	0.193	0.341	0.390	±0.004	1, 3
E	0.236	0.236	0.236	±0.008	-
E1	0.154	0.154	0.154	±0.004	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	±0.009	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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