

550MHz Differential Twisted-Pair Drivers

The EL5174 and EL5374 are single and triple high bandwidth amplifiers with an output in differential form. They are primarily targeted for applications such as driving twisted-pair lines in component video applications. The inputs can be in either single-ended or differential form but the outputs are always in differential form.

On the EL5174 and EL5374, two feedback inputs provide the user with the ability to set the gain of each device (stable at minimum gain of one). For a fixed gain of two, please see EL5173 and EL5373.

The output common mode level for each channel is set by the associated REF pin, which have a -3dB bandwidth of over 110MHz. Generally, these pins are grounded but can be tied to any voltage reference.

All outputs are short circuit protected to withstand temporary overload condition.

The EL5174 is available in an 8 Ld SO package and EL5374 is available in a 28 Ld QSOP package. All specified for operation over the full -40°C to +85°C temperature range.

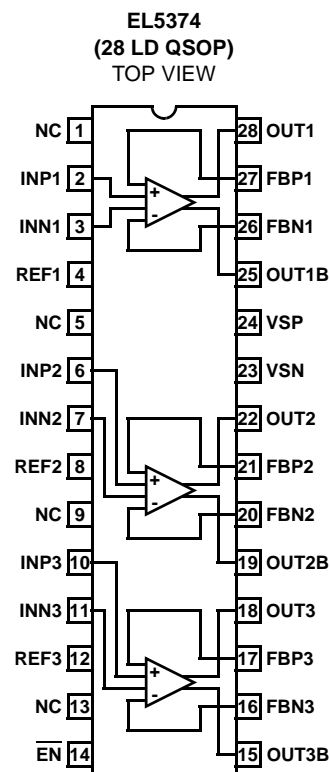
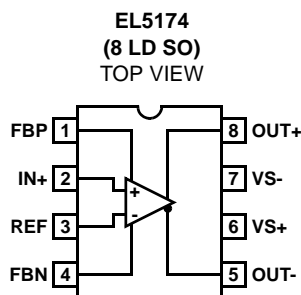
Features

- Fully differential inputs, outputs, and feedback
- Differential input range $\pm 2.3V$
- 550MHz 3dB bandwidth
- 1100V/ μs slew rate
- Low distortion at 5MHz
- Single 5V or dual $\pm 5V$ supplies
- 60mA maximum output current
- Low power - 12.5mA per channel
- Pb-free available (RoHS compliant)

Applications

- Twisted-pair driver
- Differential line driver
- VGA over twisted-pair
- ADSL/HDSL driver
- Single ended to differential amplification
- Transmission of analog signals in a noisy environment

Pinouts



Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
EL5174IS	5174IS	-40 to +85	8 Ld SO	MDP0027
EL5174IS-T7*	5174IS	-40 to +85	8 Ld SO	MDP0027
EL5174IS-T13*	5174IS	-40 to +85	8 Ld SO	MDP0027
EL5174ISZ (See Note)	5174ISZ	-40 to +85	8 Ld SO (Pb-Free)	MDP0027
EL5174ISZ-T7* (See Note)	5174ISZ	-40 to +85	8 Ld SO (Pb-free)	MDP0027
EL5174ISZ-T13* (See Note)	5174ISZ	-40 to +85	8 Ld SO (Pb-free)	MDP0027
EL5374IU	EL5374IU	-40 to +85	28 Ld QSOP	M28.15
EL5374IU-T7*	EL5374IU	-40 to +85	28 Ld QSOP	M28.15
EL5374IU-T13*	EL5374IU	-40 to +85	28 Ld QSOP	M28.15
EL5374IUZ (See Note)	EL5374IUZ	-40 to +85	28 Ld QSOP (Pb-Free)	M28.15
EL5374IUZ-T7* (See Note)	EL5374IUZ	-40 to +85	28 Ld QSOP (Pb-Free)	M28.15
EL5374IUZ-T13* (See Note)	EL5374IUZ	-40 to +85	28 Ld QSOP (Pb-Free)	M28.15

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

EL5174, EL5374

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage (V_{S+} to V_{S-}) 12V
 Maximum Output Current ±60mA

Operating Conditions

Operating Junction Temperature +135°C
 Ambient Operating Temperature -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W)
 8 Lead SOIC Package 120.40
 28 Lead QSOP Package 77.61
 Storage Temperature Range -65°C to +150°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T_J = T_C = T_A

Electrical Specifications V_{S+} = +5V, V_{S-} = -5V, T_A = +25°C, V_{IN} = 0V, R_{LD} = 1kΩ, R_F = 0, R_G = OPEN, C_{LD} = 2.7pF, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A _V = 1, C _{LD} = 2.7pF		550		MHz
		A _V = 2, R _F = 500, C _{LD} = 2.7pF		130		MHz
		A _V = 10, R _F = 500, C _{LD} = 2.7pF		20		MHz
BW	±0.1dB Bandwidth	A _V = 1, C _{LD} = 2.7pF		120		MHz
SR	Slew Rate (EL5174)	V _{OUT} = 3V _{P-P} , 20% to 80%	800	1100		V/μs
	Slew Rate (EL5374)	V _{OUT} = 3V _{P-P} , 20% to 80%	600	850		V/μs
T _{STL}	Settling Time to 0.1%	V _{OUT} = 2V _{P-P}		10		ns
T _{OVR}	Output Overdrive Recovery Time			20		ns
GBWP	Gain Bandwidth Product			200		MHz
V _{REFBW} (-3dB)	V _{REF} -3dB Bandwidth	A _V = 1, C _{LD} = 2.7pF		110		MHz
V _{REFSR+}	V _{REF} Slew Rate - Rise	V _{OUT} = 2V _{P-P} , 20% to 80%		134		V/μs
V _{REFSR-}	V _{REF} Slew Rate - Fall	V _{OUT} = 2V _{P-P} , 20% to 80%		70		V/μs
V _N	Input Voltage Noise	at 10kHz		21		nV/√Hz
I _N	Input Current Noise	at 10kHz		2.7		pA/√Hz
HD2	Second Harmonic Distortion	V _{OUT} = 2V _{P-P} , 5MHz		-95		dBc
		V _{OUT} = 2V _{P-P} , 20MHz		-94		dBc
HD3	Third Harmonic Distortion	V _{OUT} = 2V _{P-P} , 5MHz		-88		dBc
		V _{OUT} = 2V _{P-P} , 20MHz		-87		dBc
dG	Differential Gain at 3.58MHz	R _{LD} = 300Ω, A _V = 2		0.06		%
dθ	Differential Phase at 3.58MHz	R _{LD} = 300Ω, A _V = 2		0.13		°
e _S	Channel Separation - for EL5374 only	at f = 1MHz		90		dB
INPUT CHARACTERISTICS						
V _{OS}	Input Referred Offset Voltage	(EL5174)		±1.4	±25	mV
		(EL5374)		±2.2	±25	mV
I _{IN}	Input Bias Current (V _{IN+} , V _{IN-})		-30	-14	-7	μA
I _{REF}	Input Bias Current (V _{REF})		0.5	2.3	4	μA
R _{IN}	Differential Input Resistance			150		kΩ
C _{IN}	Differential Input Capacitance			1		pF
DMIR	Differential Mode Input Range		±2.1	±2.3	±2.5	V
CMIR+	Common Mode Positive Input Range at V _{IN+} , V _{IN-}			3.4		V
CMIR-	Common Mode Negative Input Range at V _{IN+} , V _{IN-}			-4.3		V

EL5174, EL5374

Electrical Specifications $V_{S+} = +5V$, $V_{S-} = -5V$, $T_A = +25^\circ C$, $V_{IN} = 0V$, $R_{LD} = 1k\Omega$, $R_F = 0$, $R_G = OPEN$, $C_{LD} = 2.7pF$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
V_{REFIN+}	Positive Reference Input Voltage Range (EL5374)	$V_{IN+} = V_{IN-} = 0V$	3.4	3.7		V
V_{REFIN-}	Negative Reference Input Voltage Range (EL5374)	$V_{IN+} = V_{IN-} = 0V$		-3.3	-3	V
V_{REFOS}	Output Offset Relative to V_{REF} (EL5374)			± 50	± 100	mV
CMRR	Input Common Mode Rejection Ratio (EL5374)	$V_{IN} = \pm 2.5V$	65	78		dB
Gain	Gain Accuracy	$V_{IN} = 1V$ (EL5174)	0.980	0.995	1.010	V
		$V_{IN} = 1V$ (EL5374)	0.978	0.993	1.008	V
OUTPUT CHARACTERISTICS						
V_{OUT}	Output Voltage Swing	$R_L = 500\Omega$ to GND (EL5174)		± 3.4		V
		$R_L = 500\Omega$ to GND (EL5374)	± 3.6	± 3.8		V
$I_{OUT(Max)}$	Maximum Output Current	$R_L = 10\Omega$, $V_{IN+} = \pm 3.2V$	± 50	± 60	± 100	mA
R_{OUT}	Output Impedance			130		$m\Omega$
SUPPLY						
V_{SUPPLY}	Supply Operating Range	V_{S+} to V_{S-}	4.75		11	V
$I_{S(ON)}$	Power Supply Current - Per Channel		10	12.5	14	mA
$I_{S(OFF)+}$	Positive Power Supply Current - Disabled (EL5374)	\overline{EN} pin tied to 4.8V		1.7	10	μA
$I_{S(OFF)-}$	Negative Power Supply Current - Disabled (EL5374)		-200	-120		μA
PSRR	Power Supply Rejection Ratio	V_S from $\pm 4.5V$ to $\pm 5.5V$	60	75		dB
ENABLE (EL5374 ONLY)						
t_{EN}	Enable Time			130		ns
t_{DS}	Disable Time			1.2		μs
V_{IH}	\overline{EN} Pin Voltage for Power-Up				$V_{S+} - 1.5$	V
V_{IL}	\overline{EN} Pin Voltage for Shut-Down		$V_{S+} - 0.5$			V
I_{IH-EN}	\overline{EN} Pin Input Current High	At $V_{EN} = 5V$		123	150	μA
I_{IL-EN}	\overline{EN} Pin Input Current Low	At $V_{EN} = 0V$	-10	-8		μA

NOTE:

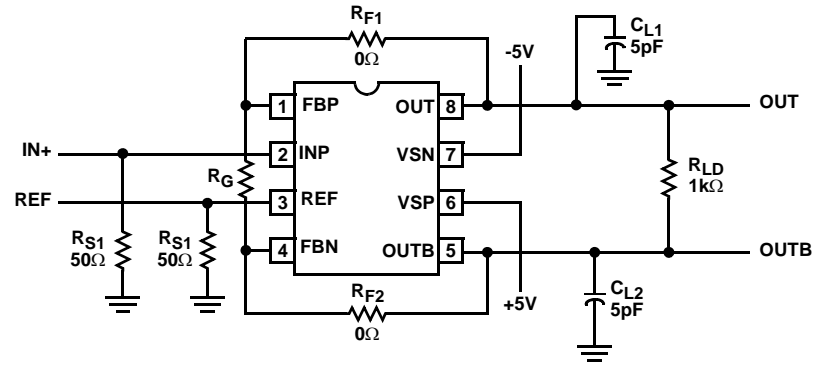
- Parts are 100% tested at $+25^\circ C$. Over-temperature limits established by characterization and are not production tested.

Pin Descriptions

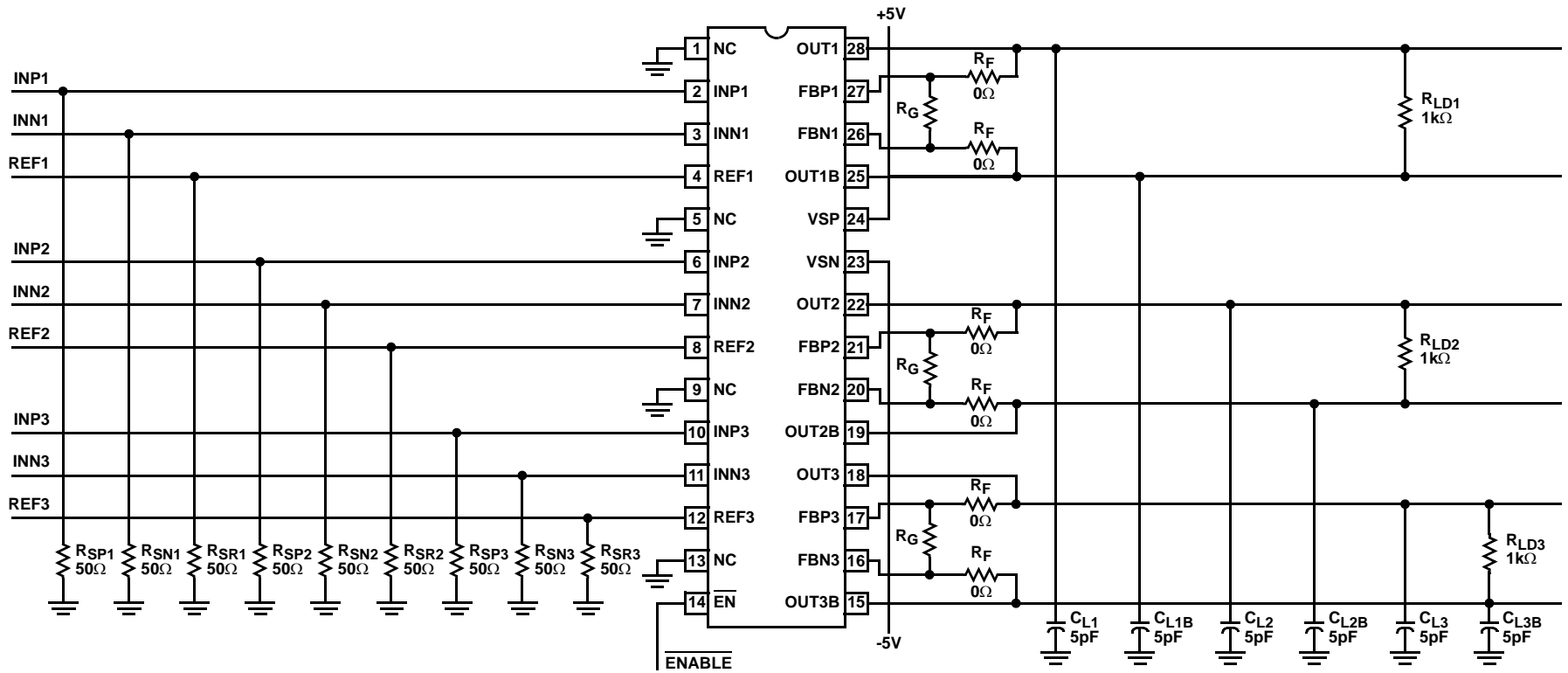
EL5174	EL5374	PIN NAME	PIN FUNCTION
1	17, 21, 27	FBP1, 2, 3	Feedback from non-inverting outputs
2	2, 6, 10	INP1, 2, 3	Non-inverting inputs
3	3, 7, 11	INN1, 2, 3	Inverting inputs, note that on EL5174, this pin is also the REF pin
4	16, 20, 26	FBN1, 2, 3	Feedback from inverting outputs
5	15, 19, 25	OUT1B, 2B, 3B	Inverting outputs
6	24	VSP	Positive supply
7	23	VSN	Negative supply
8	18, 22, 28	OUT1, 2, 3	Non-inverting outputs
	1, 5, 9, 13	NC	No connect; grounded for best crosstalk performance
	4, 8, 12	REF1, 2, 3	Reference inputs, sets common-mode output voltage
	14	\overline{EN}	ENABLE

Connection Diagrams

EL5174



EL5374



EL5174, EL5374

Typical Performance Curves

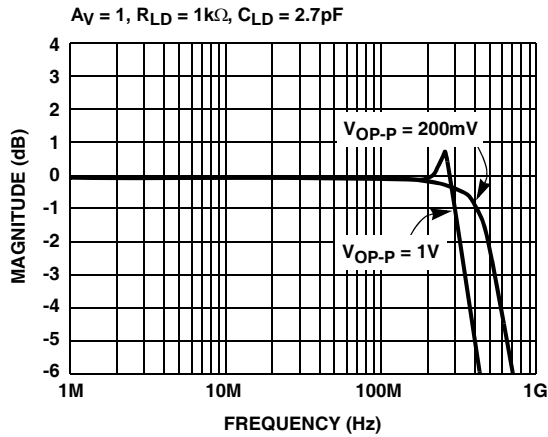


FIGURE 1. FREQUENCY RESPONSE

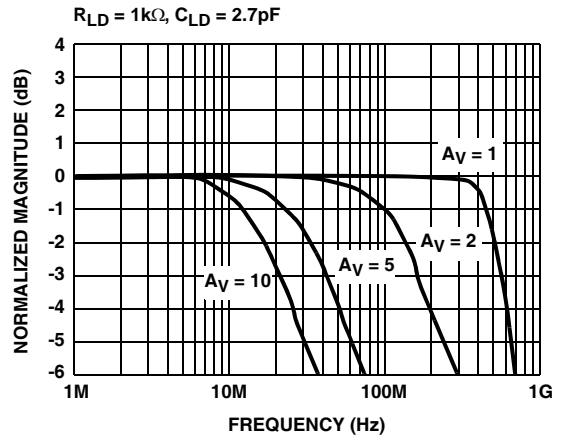


FIGURE 2. FREQUENCY RESPONSE FOR VARIOUS GAIN

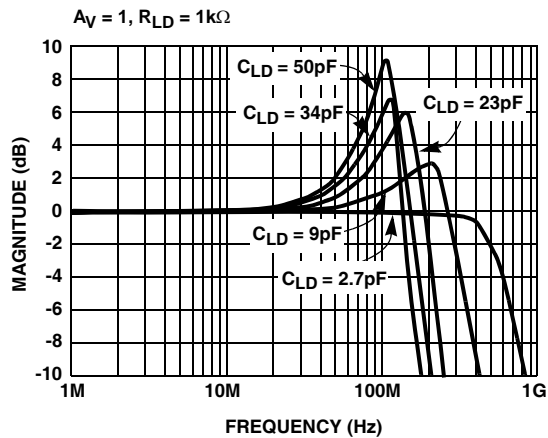


FIGURE 3. FREQUENCY RESPONSE vs C_{LD}

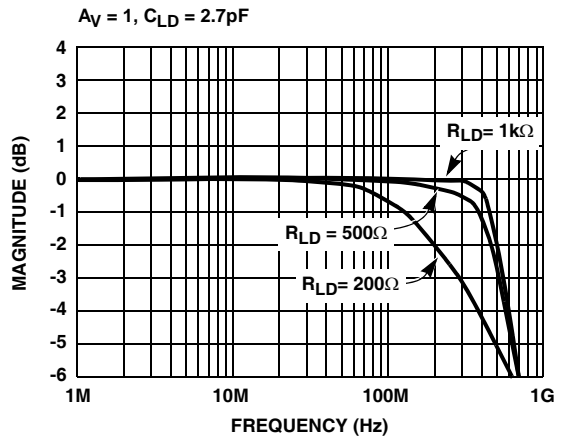


FIGURE 4. FREQUENCY RESPONSE vs R_{LD}

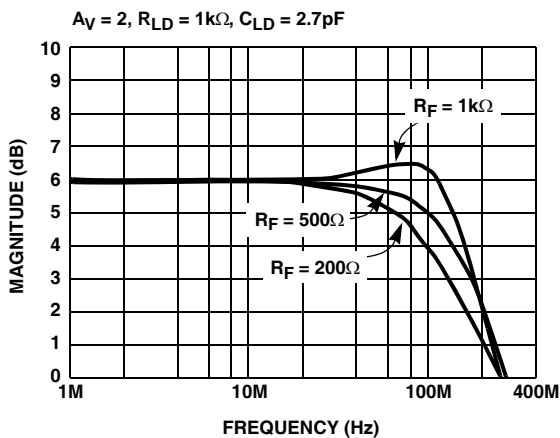


FIGURE 5. FREQUENCY RESPONSE

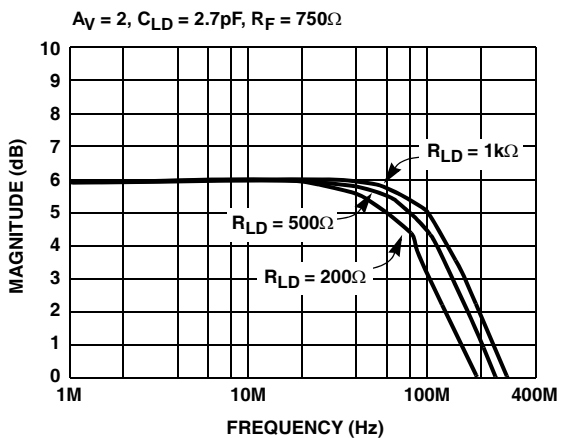


FIGURE 6. FREQUENCY RESPONSE vs R_{LD}

Typical Performance Curves (Continued)

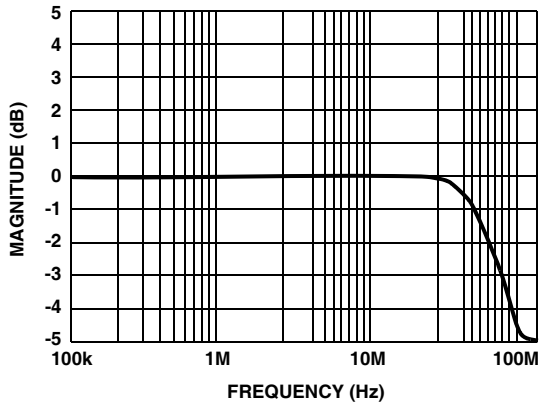


FIGURE 7. FREQUENCY RESPONSE - V_{REF}

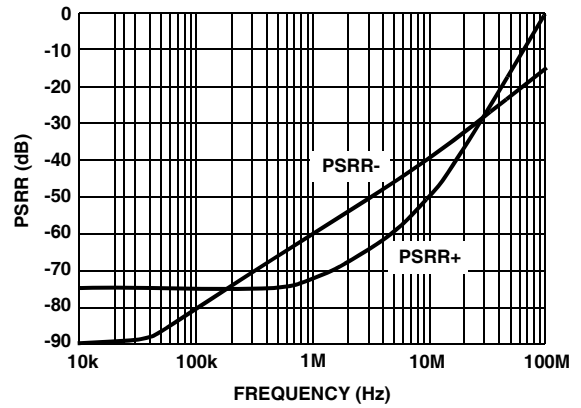


FIGURE 8. PSRR vs FREQUENCY

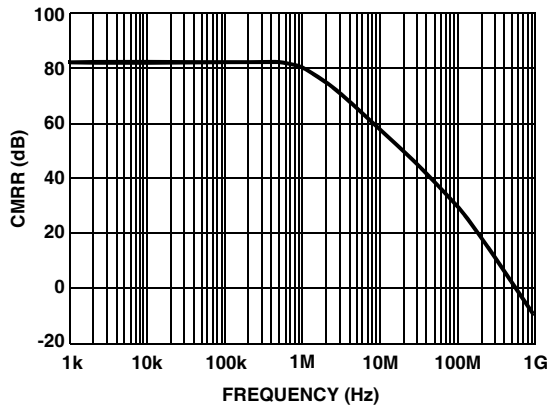


FIGURE 9. CMRR vs FREQUENCY

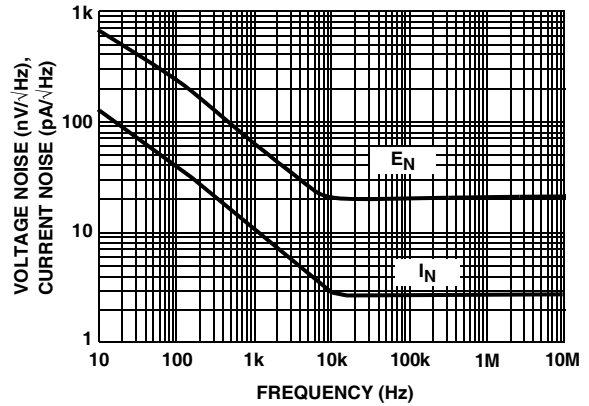


FIGURE 10. VOLTAGE AND CURRENT NOISE vs FREQUENCY

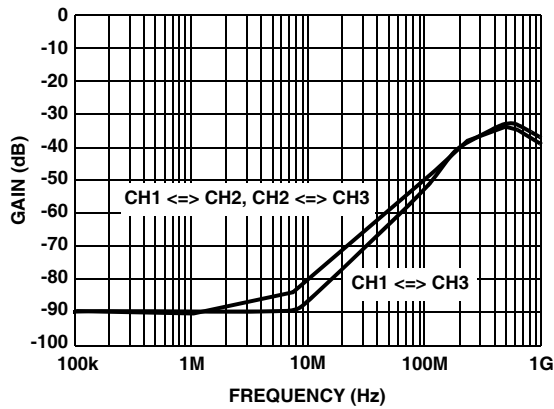


FIGURE 11. CHANNEL ISOLATION (EL5374 ONLY)

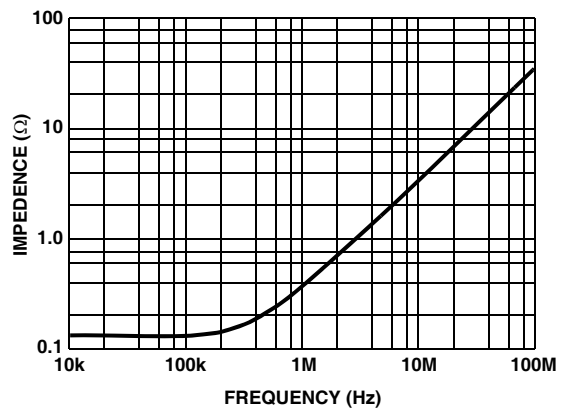


FIGURE 12. OUTPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

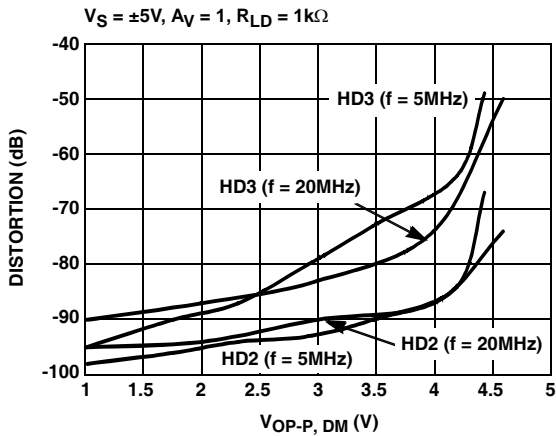


FIGURE 13. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

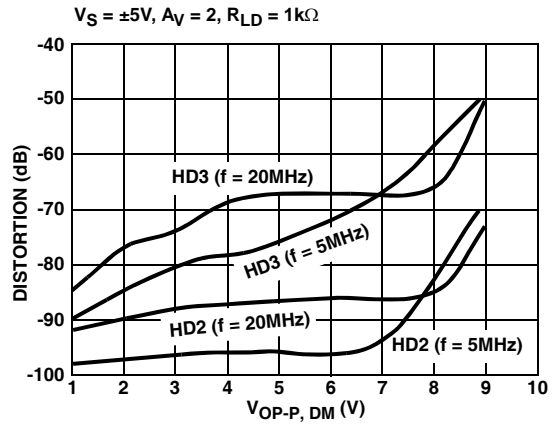


FIGURE 14. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

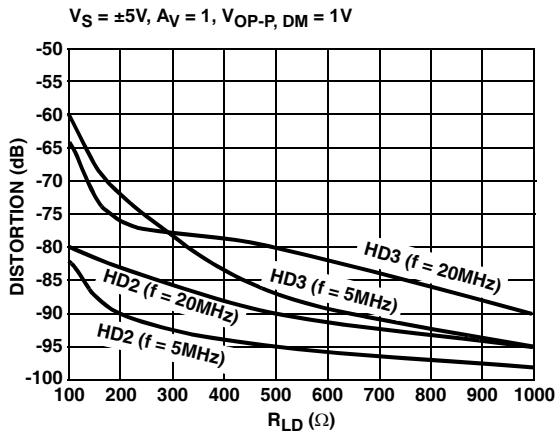


FIGURE 15. HARMONIC DISTORTION vs R_{LD}

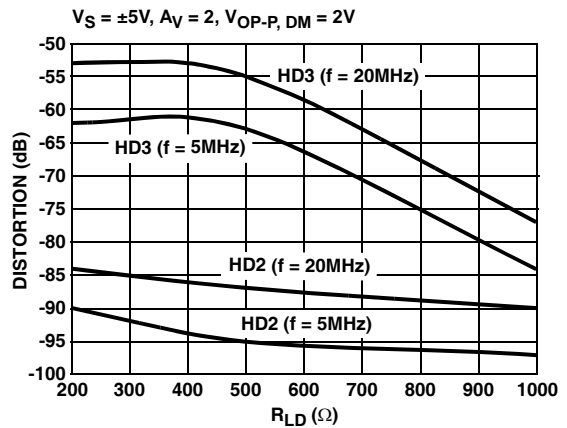


FIGURE 16. HARMONIC DISTORTION vs R_{LD}

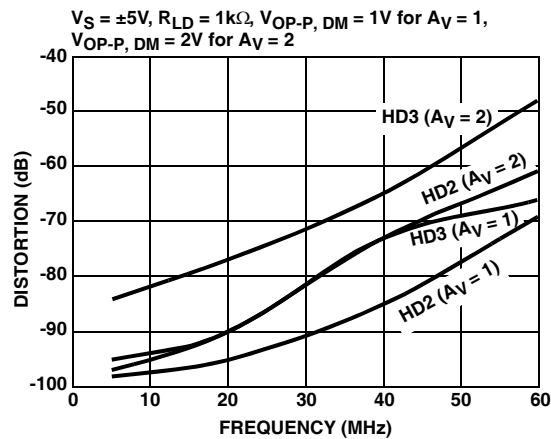


FIGURE 17. HARMONIC DISTORTION vs FREQUENCY

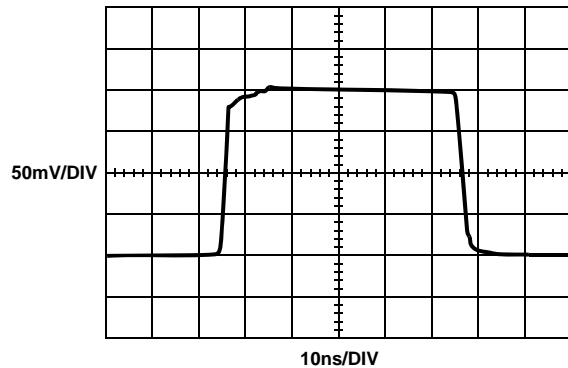


FIGURE 18. SMALL SIGNAL TRANSIENT RESPONSE

Typical Performance Curves (Continued)

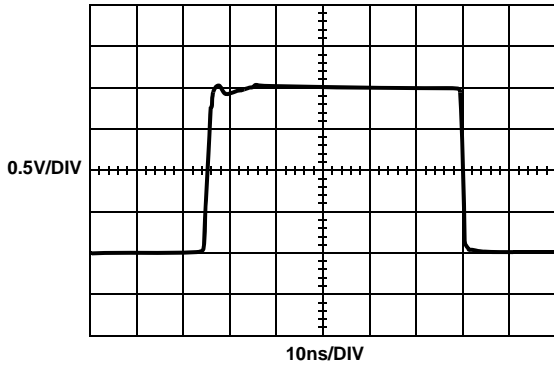


FIGURE 19. LARGE SIGNAL TRANSIENT RESPONSE

M = 400ns, CH1 = 500mV/DIV, CH2 = 5V/DIV

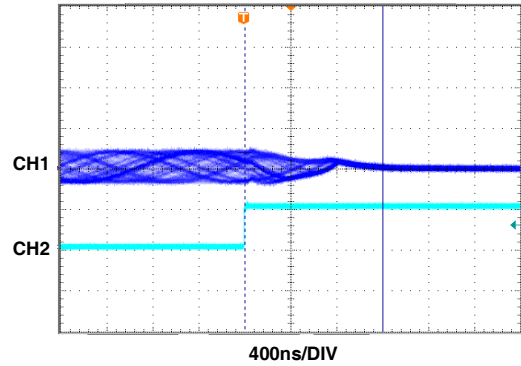


FIGURE 20. ENABLED RESPONSE

M = 400ns, CH1 = 200mV/DIV, CH2 = 5V/DIV

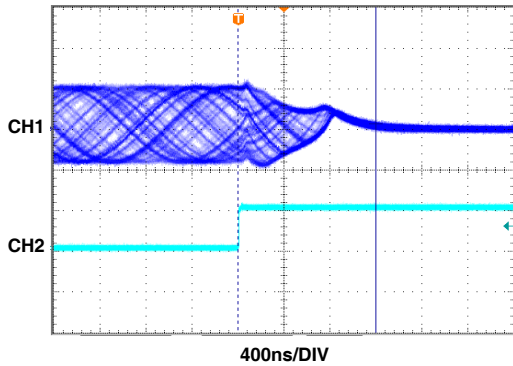


FIGURE 21. DISABLED RESPONSE

JEDEC JESD51-3 LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD

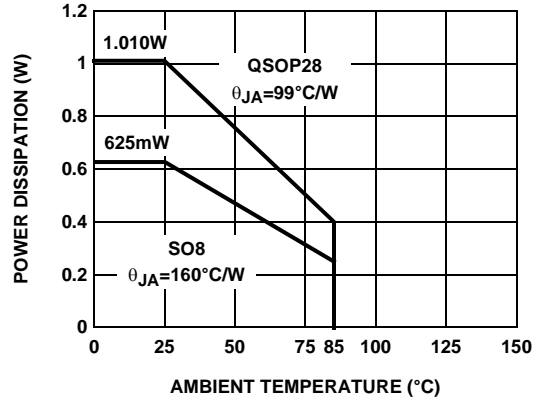


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

JEDEC JESD51-7 HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD

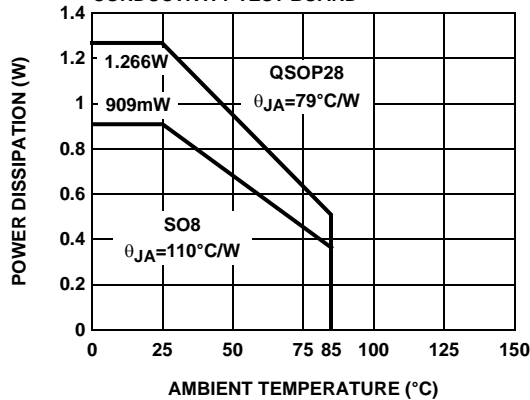
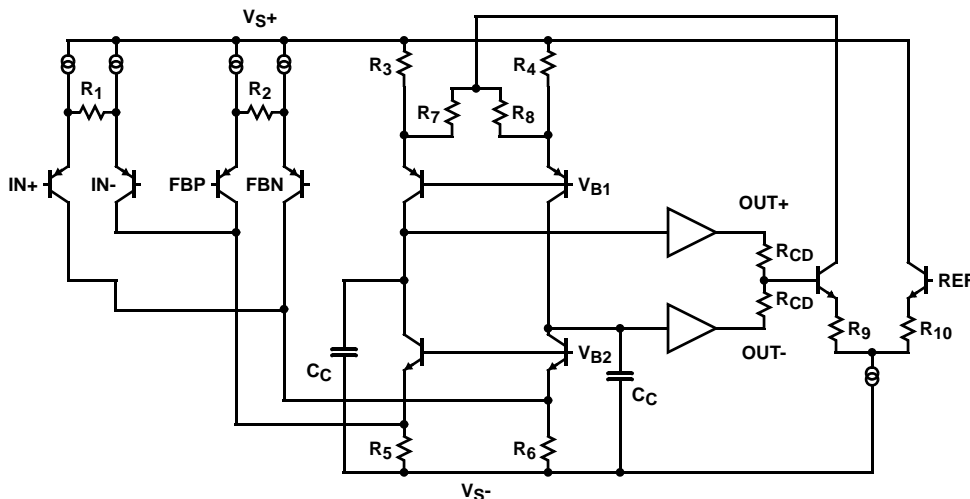


FIGURE 23. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Simplified Schematic



Description of Operation and Application Information

Product Description

The EL5174 and EL5374 are wide bandwidth, low power and single/differential ended to differential output amplifiers. The EL5174 is a single channel differential amplifier. Since the I_{N-} pin and REF pin are tied together internally, the EL5174 can be used as a single ended to differential converter. The EL5374 is a triple channel differential amplifier. The EL5374 have a separate I_{N-} pin and REF pin for each channel. It can be used as single/differential ended to differential converter. The EL5174 and EL5374 are internally compensated for closed loop gain of +1 or greater. Connected in gain of 1 and driving a $1\text{k}\Omega$ differential load, the EL5174 and EL5374 have a -3dB bandwidth of 550MHz. Driving a 200Ω differential load at gain of 2, the bandwidth is about 130MHz. The EL5374 is available with a power down feature to reduce the power while the amplifier is disabled.

Input, Output, and Supply Voltage Range

The EL5174 and EL5374 have been designed to operate with a single supply voltage of 5V to 10V or a split supplies with its total voltage from 5V to 10V. The amplifiers have an input common mode voltage range from -4.3V to 3.4V for $\pm 5\text{V}$ supply. The differential mode input range (DMIR) between the two inputs is from -2.3V to +2.3V. The input voltage range at the REF pin is from -3.3V to 3.7V. If the input common mode or differential mode signal is outside the above-specified ranges, it will cause the output signal distorted.

The output of the EL5174 and EL5374 can swing from -3.8V to +3.8V at $1\text{k}\Omega$ differential load at $\pm 5\text{V}$ supply. As the load resistance becomes lower, the output swing is reduced.

Differential and Common Mode Gain Settings

For EL5174, since the I_{N-} pin and REF pin are bounded together as the REF pin in an 8 Ld package, the signal at the REF pin is part of the common mode signal and also part of the differential mode signal. For the true balance differential outputs, the REF pin must be tied to the same bias level as the I_{N+} pin. For a $\pm 5\text{V}$ supply, just tie the REF pin to GND if the I_{N+} pin is biased at 0V with a 50Ω or 75Ω termination resistor. For a single supply application, if the I_{N+} is biased to half of the rail, the REF pin should be biased to half of the rail also.

The gain setting for EL5174 is:

$$V_{ODM} = V_{IN+} \times \left(1 + \frac{R_{F1} + R_{F2}}{R_G} \right)$$

$$V_{ODM} = V_{IN+} \times \left(1 + \frac{2R_F}{R_G} \right)$$

$$V_{OCM} = V_{REF} = 0\text{V}$$

Where:

$$V_{REF} = 0\text{V}$$

$$R_{F1} = R_{F2} = R_F$$

EL5374 have a separate I_{N-} pin and REF pin. It can be used as a single/differential ended to differential converter. The voltage applied at REF pin can set the output common mode voltage and the gain is one.

The gain setting for EL5374 is:

$$V_{ODM} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{R_{F1} + R_{F2}}{R_G} \right)$$

$$V_{ODM} = (V_{IN+} - V_{IN-}) \times \left(1 + \frac{2R_F}{R_G} \right)$$

$$V_{OCM} = V_{REF}$$

Where:

$$R_{F1} = R_{F2} = R_F$$

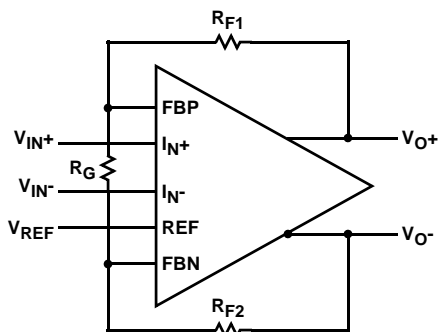


FIGURE 24.

Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the OUT+ pin to FBP pin and OUT- pin to FBN pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value that should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few Pico farad range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

The bandwidth of the EL5174 and EL5374 depends on the load and the feedback network. R_F and R_G appear in parallel with the load for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F also has a minimum value that should not be exceeded for optimum bandwidth performance. For gain of +1, $R_F = 0$ is optimum. For the gains other than +1, optimum response is obtained with R_F between 500Ω to $1k\Omega$.

The EL5174 and EL5374 have a gain bandwidth product of 200MHz for $R_{LD} = 1k\Omega$. For gains ≥ 5 , its bandwidth can be predicted by the following equation:

$$\text{Gain} \times \text{BW} = 200\text{MHz}$$

Driving Capacitive Loads and Cables

The EL5174 and EL5374 can drive 23pF differential capacitor in parallel with $1k\Omega$ differential load with less than 5dB of peaking at gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with each output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make up for any gain loss which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down (for EL5374 only)

The EL5374 can be disabled and placed its outputs in a high impedance state. The turn off time is about $1.2\mu s$ and the turn on time is about 130ns. When disabled, the amplifier's supply current is reduced to $1.7\mu A$ for I_{S+} and $120\mu A$ for I_{S-} typically, thereby effectively eliminating the power consumption. The amplifier's power down can be controlled by standard CMOS signal levels at the EN pin. The applied logic signal is relative to V_{S+} pin. Letting the \overline{EN} pin float or applying a signal that is less than 1.5V below V_{S+} will enable the amplifier. The amplifier will be disabled when the signal at \overline{EN} pin is above $V_{S+} - 0.5V$.

Output Drive Capability

The EL5174 and EL5374 have internal short circuit protection. Its typical short circuit current is $\pm 60mA$. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds $\pm 60mA$. This limit is set by the design of the internal metal interconnections.

Power Dissipation

With the high output drive capability of the EL5174 and EL5374. It is possible to exceed the $135^\circ C$ absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD = i \times \left(V_S \times I_{SMAX} + V_S \times \frac{\Delta V_O}{R_{LD}} \right)$$

Where:

V_S = Total supply voltage

I_{SMAX} = Maximum quiescent supply current per channel

ΔV_O = Maximum differential output voltage of the application

R_{LD} = Differential load resistance

I_{LOAD} = Load current

i = Number of channels

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_{S-} pin is connected to the ground plane, a single 4.7 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor from V_{S+} to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_{S-} pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

Typical Applications

As the signal is transmitted through a cable, the high frequency signal will be attenuated. One way to compensate this loss is to boost the high frequency gain at the receiver side.

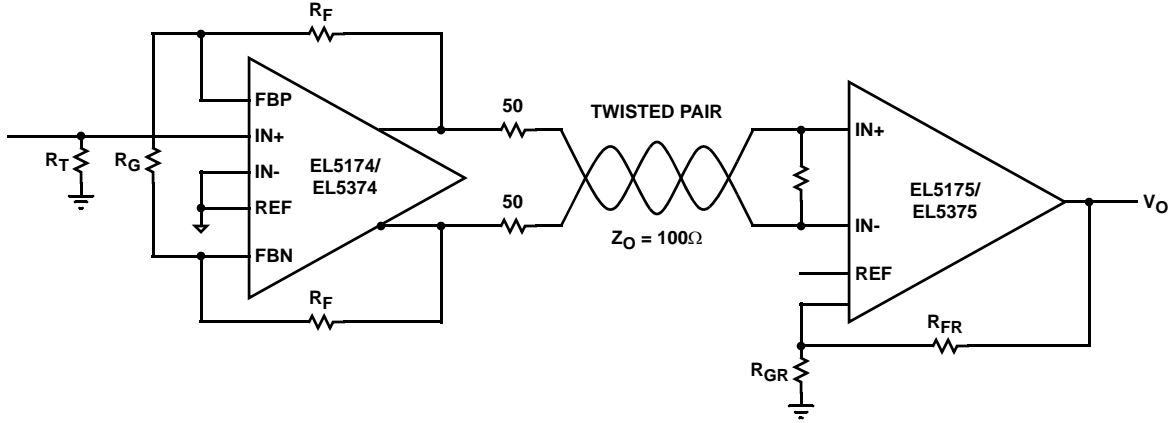
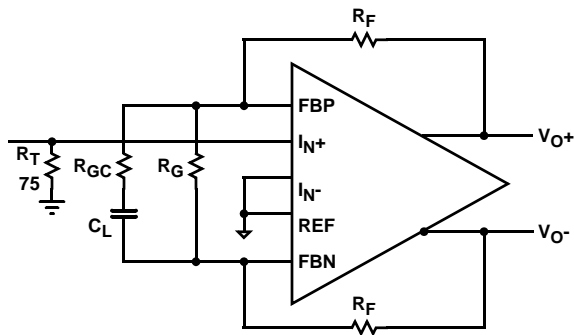
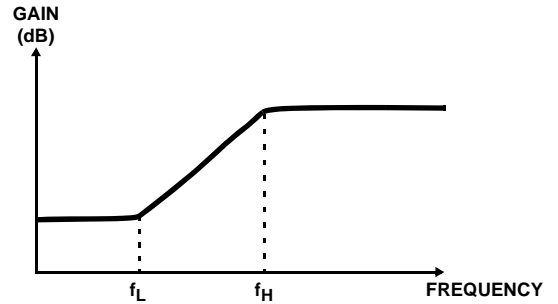


FIGURE 25. TWISTED PAIR CABLE RECEIVER



$$\text{DC Gain} = 1 + \frac{2R_F}{R_G}$$

$$\text{(HF)Gain} = 1 + \frac{2R_F}{R_G \parallel R_{GC}}$$

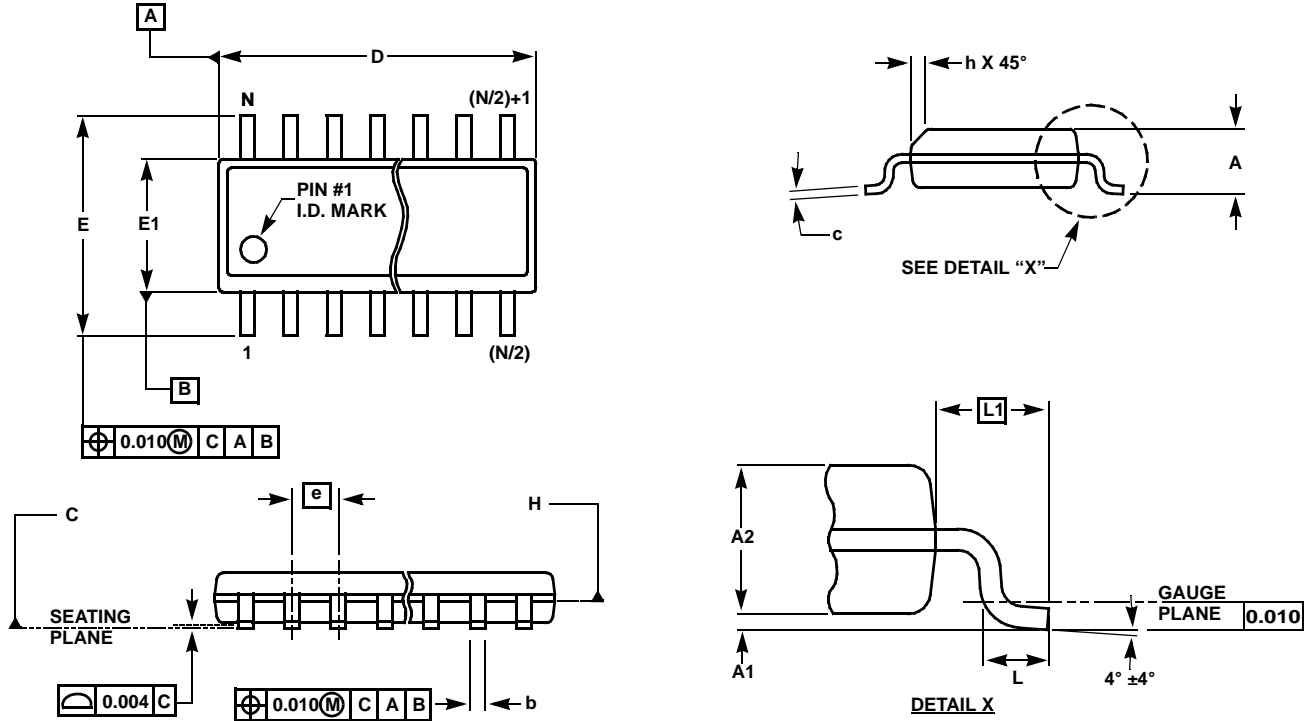


$$f_L \cong \frac{1}{2\pi R_G C_C}$$

$$f_H \cong \frac{1}{2\pi R_{GC} C_C}$$

FIGURE 26. TRANSMIT EQUALIZER

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

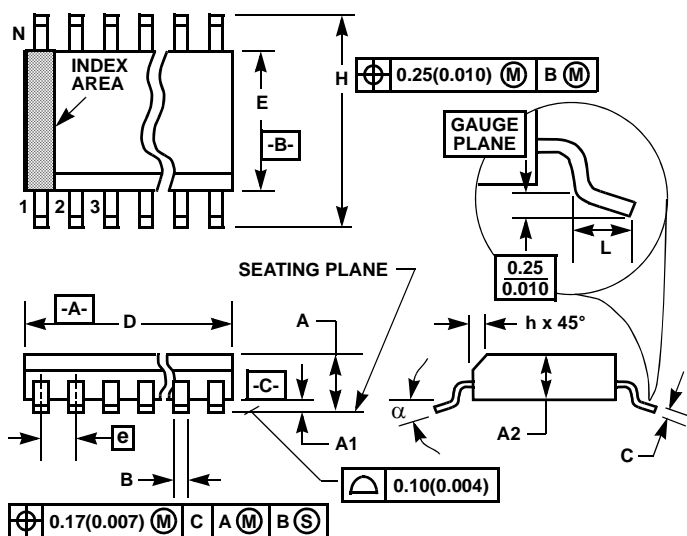
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

**Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)**



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M28.15

**28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE
(0.150" WIDE BODY)**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 1 6/04

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com