Data Sheet | February 20, 2008 | FN6167.2

High Voltage TFT-LCD Logic Driver

The EL5000A is high voltage TFT-LCD logic driver with +40V and -30V output swing capability. Manufactured using the Intersil proprietary monolithic high voltage bipolar process, it is capable of delivering 100mA output peak current into 5nF of capacitive load. To simplify external circuitry, the EL5000A integrates additional logic circuits.

The EL5000A can operate on 3.3V logic supply and high voltage -30V to +40V output supplies. The EL5000A is available in a 16 Ld TSSOP. It is specified for operation over the -20°C to +85°C extended temperature range.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
EL5000AERZ	5000AER Z	16 Ld TSSOP	MDP0044
EL5000AERZ-T7*	5000AER Z	16 Ld TSSOP	MDP0044
EL5000AERZ-T13*	5000AER Z	16 Ld TSSOP	MDP0044

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

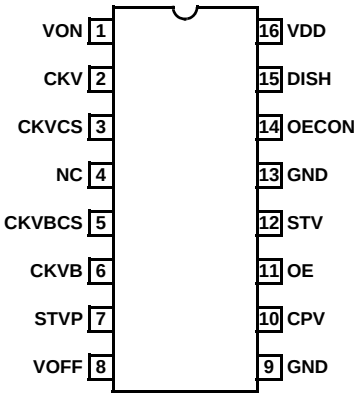
- 3.3V logic supply
- 40V V_{ON} output high level
- -30V V_{OFF} output low level
- 166kHz input logic frequency
- 100mA output peak current
- 10mA output continuous current
- TTL-compatible logic input
- Pb-free (RoHS compliant)

Applications

- TFT-LCD panels

Pinout

EL5000A
(16 LD TSSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

V_{DD} 4.5V
V_{ON} 44V
V_{OFF} . . . . . -33V
V_{CKV}, V_{CKVB}, V_{STVP},
V_{CKVCS}, V_{CKVBCS} . . . . . V_{ON} + 0.3V /V_{OFF} - 0.3V
V_{CPV}, V_{OE}, V_{STV}, V_{OECON} . . . . . V_{DD} + 0.3V /GND - 0.3V
V_{DISH} . . . . . GND + 0.3V /V_{OFF} - 0.3V
I_{OUT} (peak) 100mA
I_{OUT} (continuous), CKV, CKVB, or STVP 30mA
I_{OUT} (continuous, total) 50mA

Thermal Information

$T_{AMBIENT}$ . . . . . .-20°C to +85°C
$T_{JUNCTION}$ . . . . . .-20°C to +150°C
$T_{STORAGE}$ . . . . . .-65°C to +150°C
$P_{DISSIPATION}$ . . . . . See Curves
Maximum Power Dissipation . . . . . See Curves
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_{ON} = 20V, V_{OFF} = -14V, V_{DD} = 3.3V, 4.7nF load on STV, CKV, CKVB, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
I_{VDD}	V_{DD} Supply Current	All inputs low		1.1		mA
		CPV = 3.1V, other inputs low	0.7	1.5	2.5	mA
I_{VON}	V_{ON} Supply Current	All inputs low		0.25		mA
		CPV = 3.1V, other inputs low	0.2	0.45	0.9	mA
I_{VOFF}	V_{OFF} Supply Current	All inputs low		0.25		mA
		CPV = 3.1V, other inputs low	-1.25	-0.7	-0.30	mA
I_{STV}	STV Input Current	STV = 3.1V	25	130	180	µA
		STV = 0.2V	-1	0	1	µA
I_{CPV}	CPV Input Current	CPV = 3.1V	20	60	90	µA
		CPV = 0.2V	-1	0	1	µA
I_{OE}	OE Input Current	OE = 0.2V	-1	0	1	µA
		OE = 3.1V, OECON = 0.2V	200	450	700	µA
		OE = 3.1V, OECON = 3.1V	-1	0	1	µA
I_{OECON}	OECON Input Current	OECON - 0.2V, OE = 3.1V	-40	-25	-5	µA
		OECON - 0.2V, OE = 0.2V	-1	0	1	µA
V_{CKV}^+	CKV Positive Output Swing	V_{ON} = +20V, 1mA output current	19.1	19.3	19.5	V
V_{CKV}	CKV Negative Output Swing	V_{OFF} = -14V, 1mA output current	-13.1	-13.3	-13.5	V
V_{CKVB}^+	CKVB Positive Output Swing	V_{ON} = +20V, 1mA output current	19.1	19.3	19.5	V
V_{CKVB}	CKVB Negative Output Swing	V_{OFF} = -14V, 1mA output current	-13.1	-13.3	-13.5	V
V_{STVP}^+	STVP Positive Output Swing	V_{ON} = +20V, 1mA output current	19.0	19.2	19.4	V
V_{STVP}	STVP Negative Output Swing	V_{OFF} = -14V, 1mA output current	-13.1	-13.3	-13.5	V
R_{IN}	CPV, OE, STV Input Resistance			3		kΩ
C_{IN}	CPV, OE, STV Input Capacitance			1.5		pF
t_R-CKV	CKV Rise Time		0.3	0.5	0.7	µs
t_F-CKV	CKV Fall Time		0.5	0.75	1	µs
t_R-CKVB	CKVB Rise Time		0.3	0.5	0.7	µs
t_F-CKVB	CKVB Fall Time		0.5	0.75	1	µs
t_R-STVP	STVP Rise Time		1.2	1.6	2.4	µs

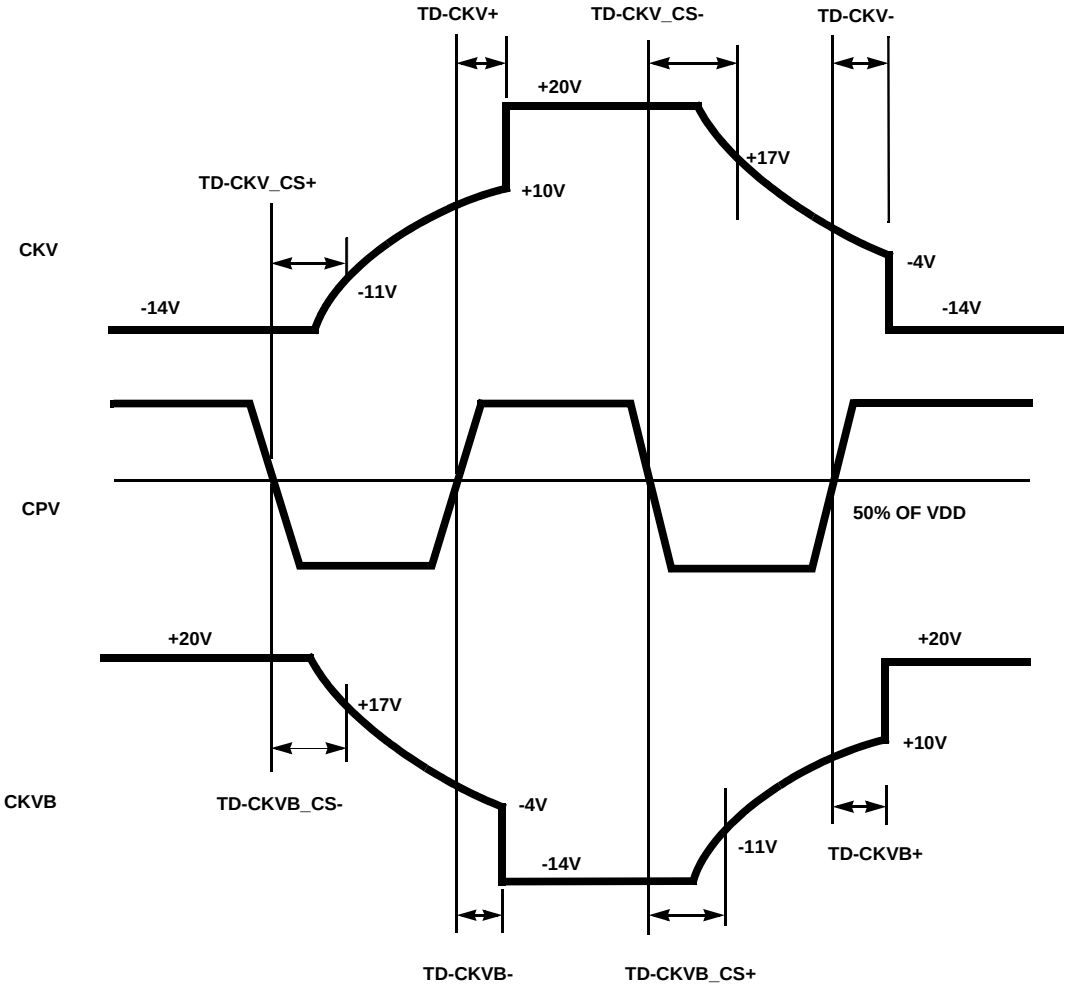
Electrical Specifications V_{ON} = 20V, V_{OFF} = -14V, V_{DD} = 3.3V, 4.7nF load on STV, CKV, CKVB, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
t_F-STVP	STVP Fall Time		1.2	1.6	2.4	µs
t_D-CKV+	CKV Rising Edge Delay Time		0.5	0.9	1.3	µs
t_D-CKV-	CKV Falling Edge Delay Time		0.7	1.1	1.5	µs
t_D-CKVB+	CKVB Rising Edge Delay Time		0.5	0.9	1.3	µs
t_D-CKVB-	CKVB Falling Edge Delay Time		0.7	1.1	1.5	µs
t_D-STVP+	STVP Rising Edge Delay Time		1.3	1.75	2.2	µs
t_D-STVP-	STVP Falling Edge Delay Time		1.2	1.7	2	µs
t_D-CKV_CS+	CKV_CS Rising Edge Delay Time		1.6	2.3	2.9	µs
t_D-CKV_CS-	CKV_CS Falling Edge Delay Time		3.4	4.1	4.8	µs
t_D-CKVB_CS+	CKVB_CS Rising Edge Delay Time		1.6	2.3	2.9	µs
t_D-CKVB_CS-	CKVB_CS Falling Edge Delay Time		3.4	4.1	4.8	µs

NOTE:

1. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

Timing Diagram



Typical Performance Curves

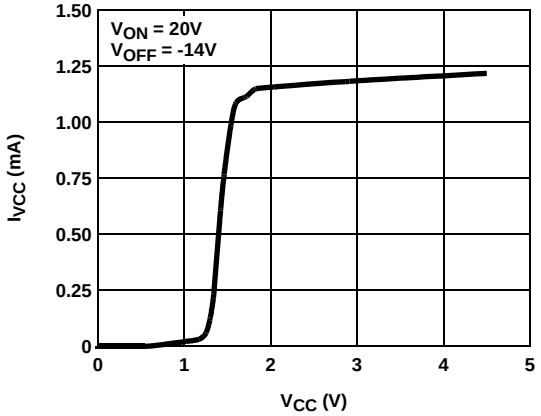


FIGURE 1. V_{SS} SUPPLY CURRENT vs V_{CC}

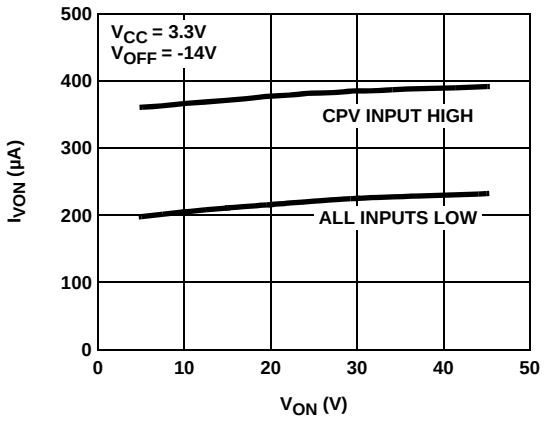


FIGURE 2. V_{ON} DC SUPPLY CURRENT vs V_{ON}

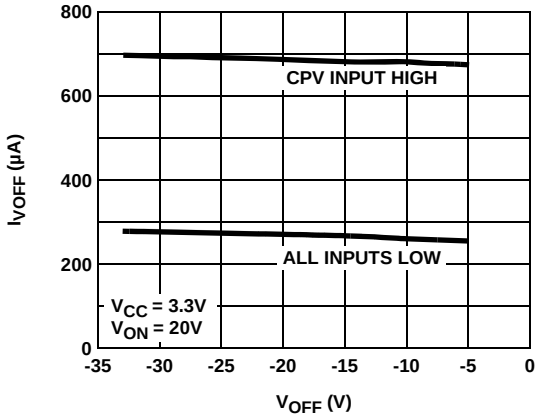


FIGURE 3. V_{OFF} DC SUPPLY CURRENT vs V_{OFF}

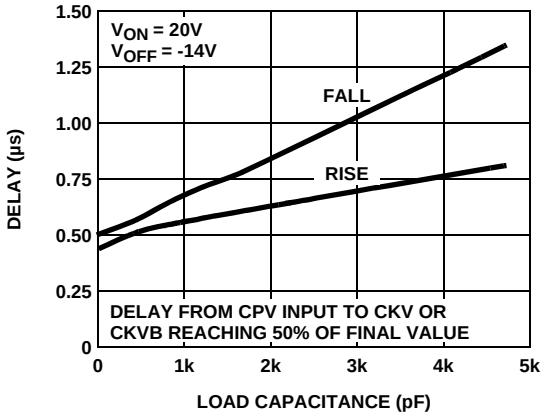


FIGURE 4. CLOCK DELAY vs LOAD CAPACITOR

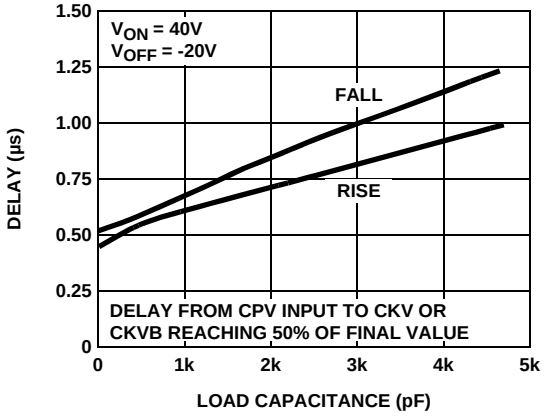


FIGURE 5. CLOCK DELAY vs LOAD CAPACITOR

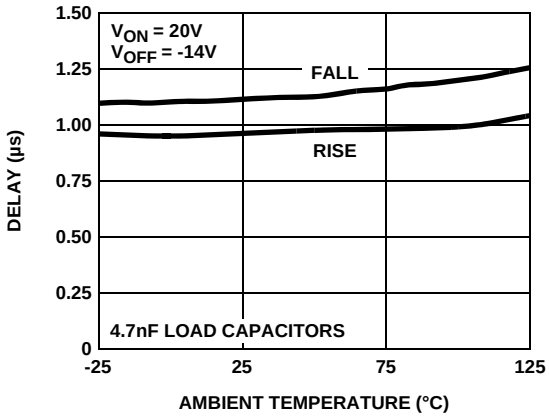


FIGURE 6. CLOCK DELAY vs TEMPERATURE

Typical Performance Curves (Continued)

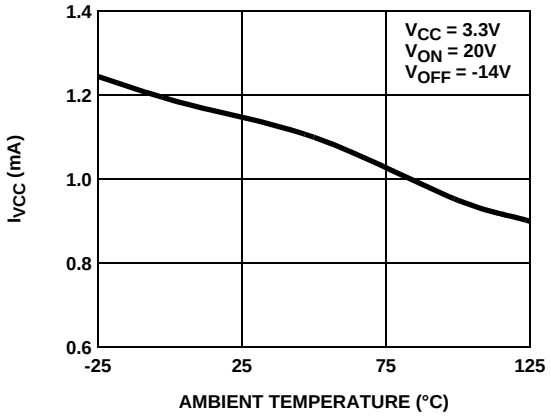


FIGURE 7. V_{CC} SUPPLY CURRENT vs TEMPERATURE

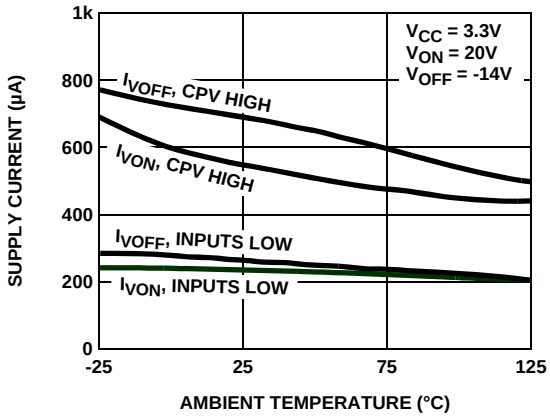


FIGURE 8. DC SUPPLY CURRENTS vs TEMPERATURE

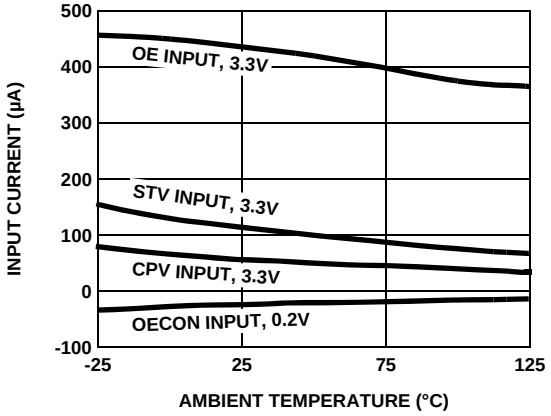


FIGURE 9. INPUT BIAS CURRENTS vs TEMPERATURE

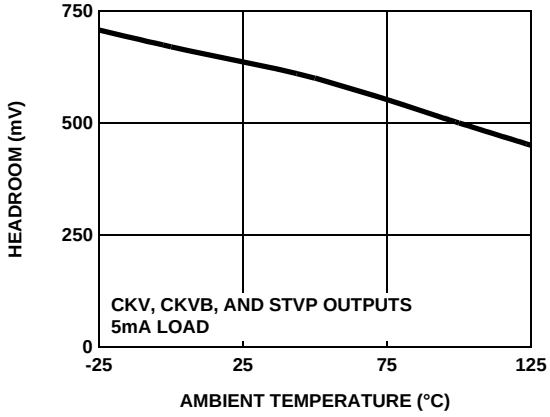


FIGURE 10. OUTPUT SWING HEADROOM vs TEMPERATURE

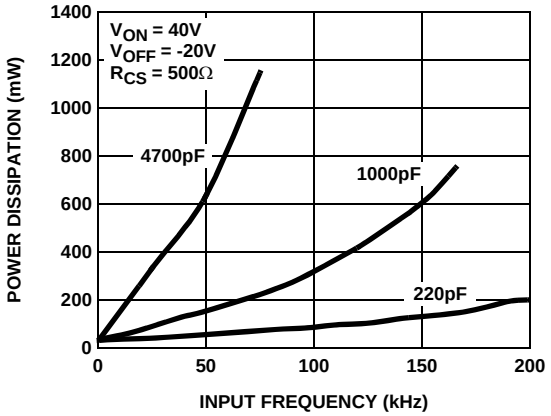


FIGURE 11. POWER CONSUMPTION vs FREQUENCY AND LOAD

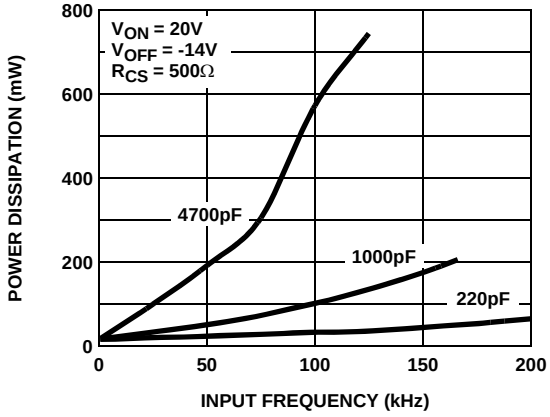


FIGURE 12. POWER CONSUMPTION vs FREQUENCY AND LOAD

Typical Performance Curves (Continued)

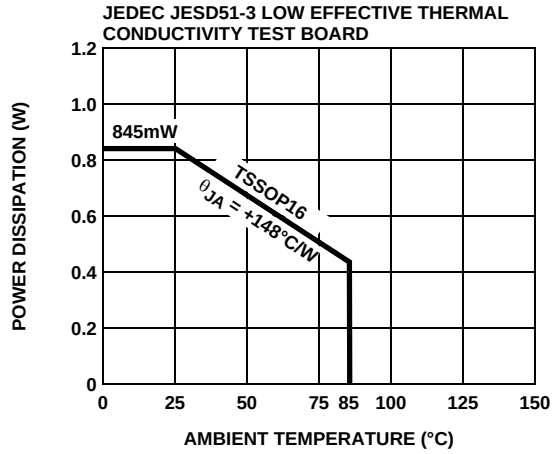


FIGURE 13. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

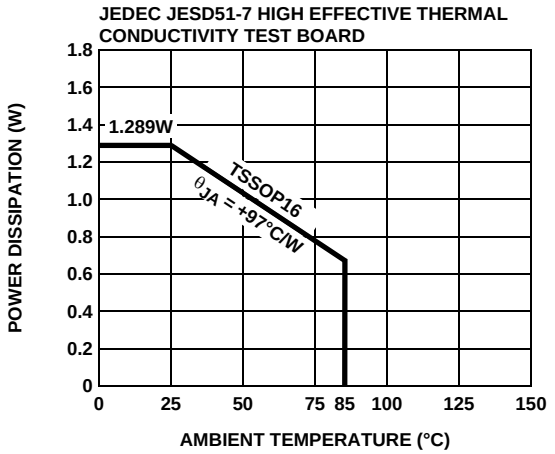


FIGURE 14. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Pin Descriptions

PIN NUMBER (16 LD TSSOP)	PIN NAME	PIN FUNCTION
1	VON	Positive supply
2	CKV	High voltage output, scan clock out
3	CKVCS	Discharge switch input, CKV charge share
4	NC	No connect
5	CKVBCS	Discharge switch input, CKVB charge share
6	CKVB	High voltage output, scan clock even
7	STVP	High voltage output, scan start pulse
8	VOFF	Negative supply
9	GND	Ground
10	CPV	H sync timing, H sync clock 1
11	OE	Writing timing, H sync clock 2
12	STV	V sync timing, V sync
13	GND	Ground, logic return
14	OECON	OE disable input, OE blank
15	DISH	Discharge function input, V_{OFF} discharge
16	VDD	Logic power supply

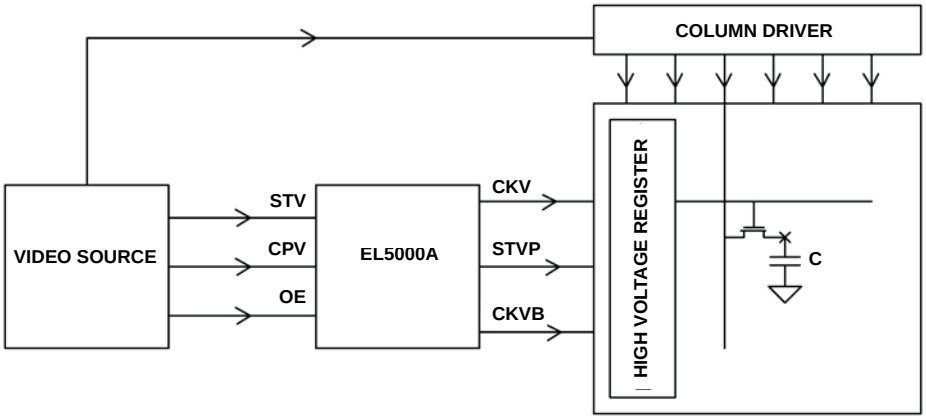


FIGURE 15. EL5000A SYSTEM BLOCK DIAGRAM

Application Information

General Description

The EL5000A is a high performance 70V TFT-LCD row driver. It level shifts TTL level timing signals from the video source into $70V_{P-P}$ output voltage. Its output is capable of delivering 100mA peak current into 1nF of capacitive load. It also incorporates logic to control the output timings. The logic timing control circuit is powered from 3.3V supply. Figure 15 shows the system block diagram.

Input Signals

The device performs beside of level transformation also logic operation between the input signals:

- STV - Vertical Sync Timing signal, frequency range around 60Hz
- CPV - Horizontal Sync Timing signal, frequency range up to 166kHz
- OE - Output Enable Write Signal, frequency range up to 166kHz

Output Signals

The output signals, CKV and CKVB are generated by EL5000A internal switches. Figure 16 depicts the simplified schematic of the output stage and interface.

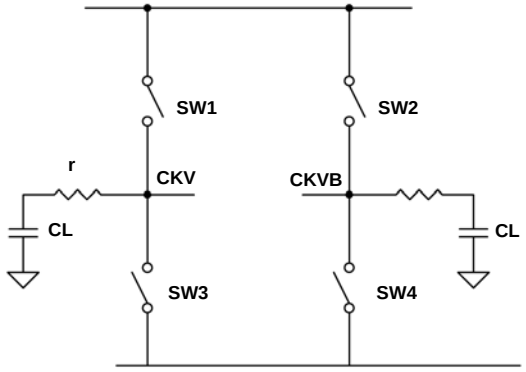


FIGURE 16. SIMPLIFIED SCHEMATIC OF OUTPUT STAGE

C_L capacitors model the capacitive loading appeared at the inputs of the TFT-LCD panel for the CKV and the CKVB signals. The C_L is typically between 1nF and 5nF.

In addition to switches SW1, SW2, SW3, and SW4, a fifth switch is added to reduce the power dissipation and shape the output waveform. Figure 17 shows the location of the additional SW5 switch.

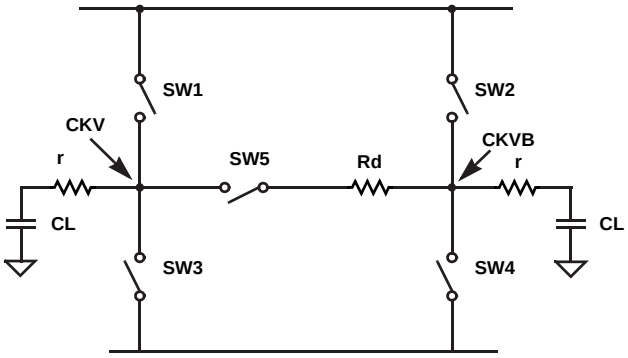


FIGURE 17. BI-DIRECTIONAL SWITCHES

In reality, each switch consists of two such switches, one for the positive discharge and one for the negative discharge, see Figure 18.

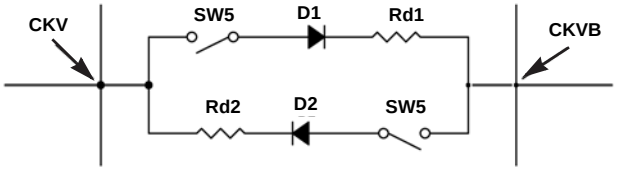


FIGURE 18. BI-DIRECTIONAL SWITCHES

Due to the actual solid-state construction of the switches, the capacitors C_L does not get discharged entirely. The amount of left over charges depends on the value of the voltages of V_{ON} and V_{OFF} on the capacitors.

Internal Logic Block Diagram

Figures 19 and 20 show the internal block diagram. In order to reduce power dissipation, most of the logic circuitry is powered from 3.3V logic supply. The output of the 3.3V logic is level-shifted to drive the output switches.

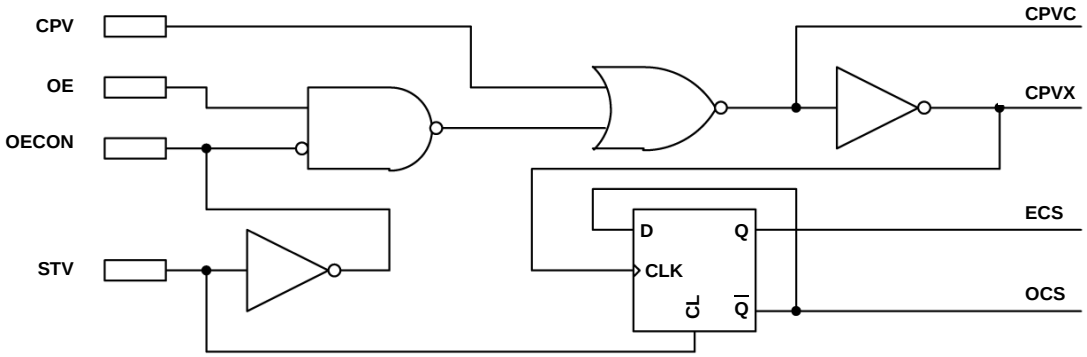


FIGURE 19. INTERNAL LOGIC BLOCK DIAGRAM

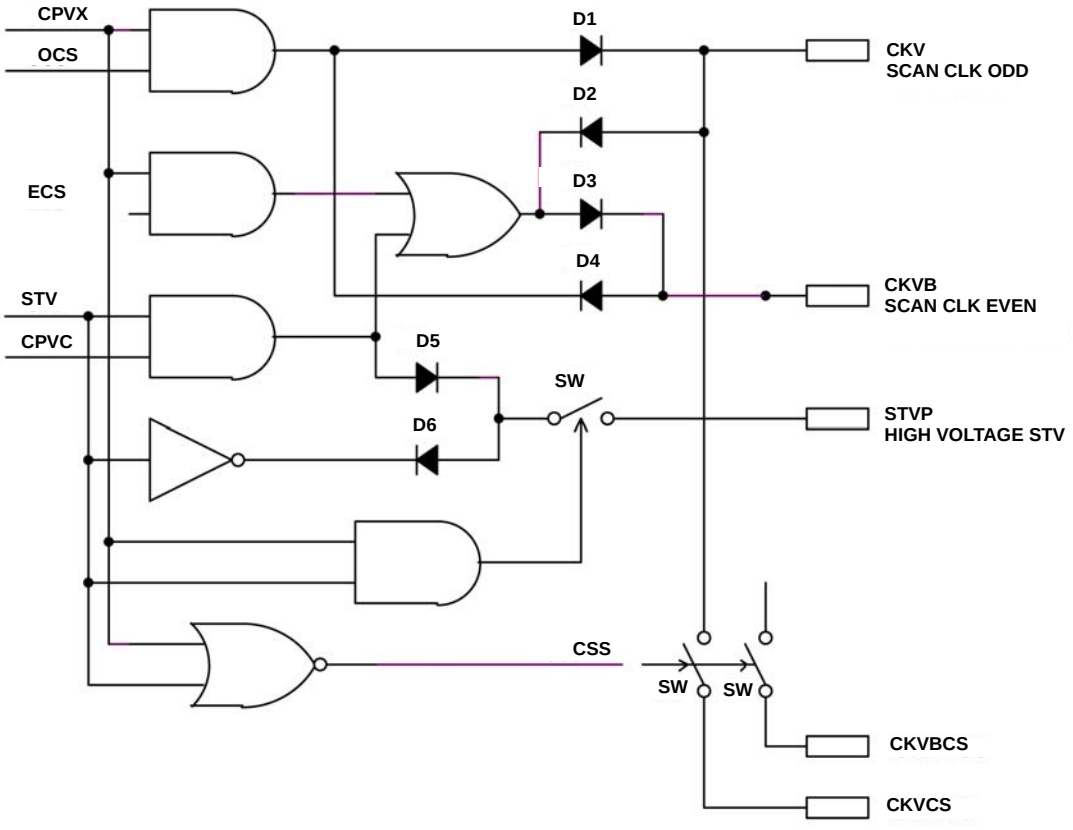


FIGURE 20. INTERNAL LOGIC BLOCK DIAGRAM AND OUTPUT SWITCHES

Output Waveforms

Figure 21 shows a typical CKV and CKVB output waveforms. The output droop rate depends on the external discharge resistor value and the output capacitor load.

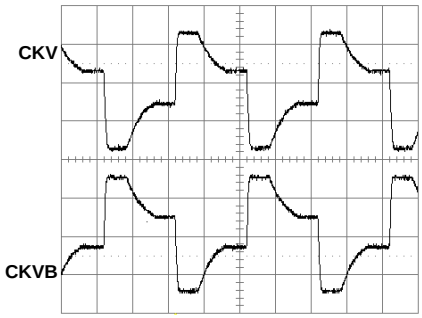


FIGURE 21. CKV AND CKVB OUTPUT WAVEFORMS

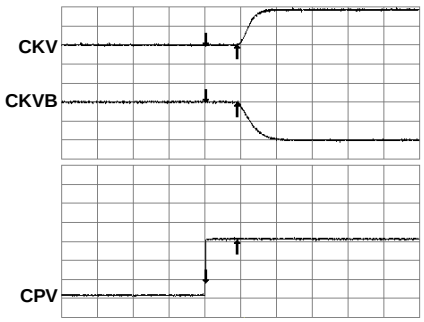


FIGURE 22. CPV TO CKV/CKVB DELAY

Figure 22 shows the delay time between the incoming horizontal sync timing pulse CPV and the generated output pulses. Δt is dependent mainly on the value of C_L. Figure 23 shows the effect of STV.

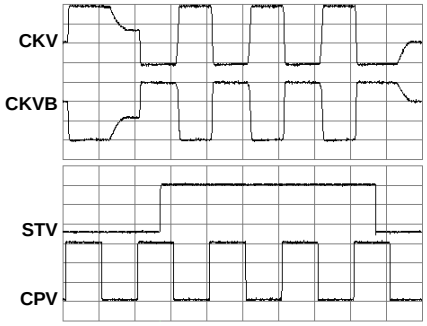


FIGURE 23. EFFECT OF STV

Auxiliary Functions

DISH: It discharges V_{OFF} when the logic power voltage level drops out, when 'DISH' is < -0.6V (V_{CC} system power turns off), V_{OFF} is connected to ground level by 1kΩ.

OECON: It provides continuos polarity changes to the TFT-LCD panel during the vertical blanking.

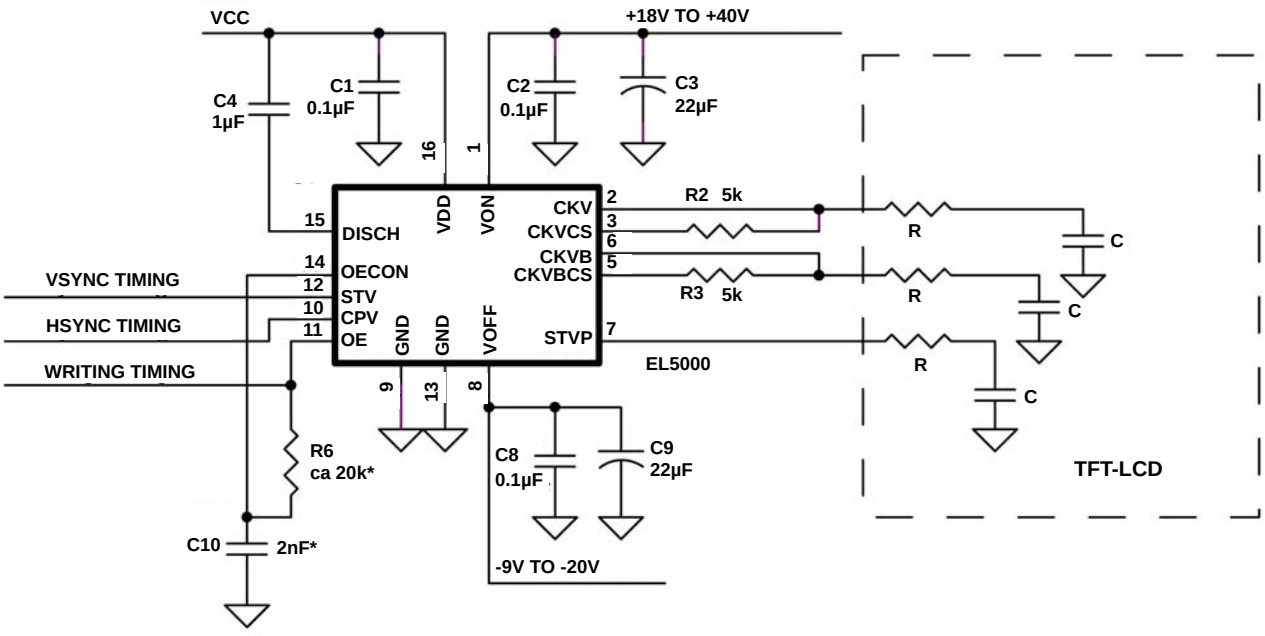


FIGURE 24. TYPICAL APPLICATION CIRCUIT

Power Dissipation

The dissipated power in R_3 and R_6 could be calculated as follows:

We assume that:

- V_{ON} = 40V
- V_{OFF} = -20V
- H sync timing frequency = 60kHz
- C_L = 5nF

The value of V_L (the left over voltage) in the capacitors in that case is 23V for the positive discharge and 3.3V for the negative discharge.

The voltage change across the capacitor is therefore 23V; see Figure 25.

The stored energy in the capacitor is shown in Equation 1:

$$1/2 \times V^2 C = 1/2 \times 23^2 \times 5 \times 10^{-9} = 132\mu J \quad \text{(EQ. 1)}$$

The energy, which is stored in the capacitor, will be dissipated on the resistor; see Figure 26. The switch will close 2 x 60,000 in every second.

The process will be repeated 2 times for the CKV and the CKVB. In 120,000 cycles per second, the power dissipation in R_3 and R_6 becomes Equation 2:

$$2 \times 1.32 \times 10^{-6} \times 60 \times 10^{3} = 160mW \quad \text{(EQ. 2)}$$

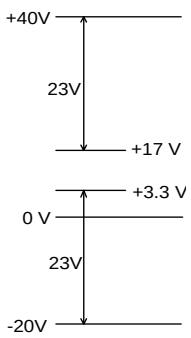


FIGURE 25.

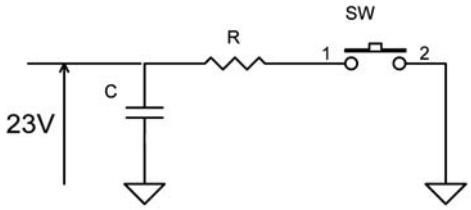
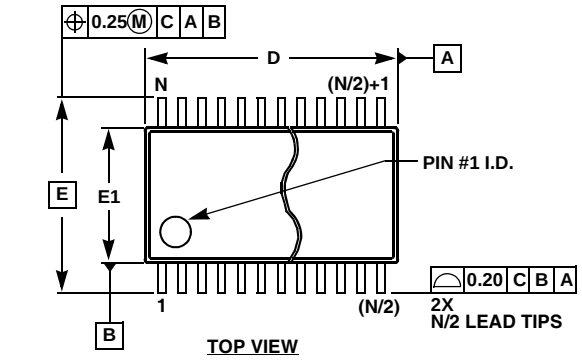


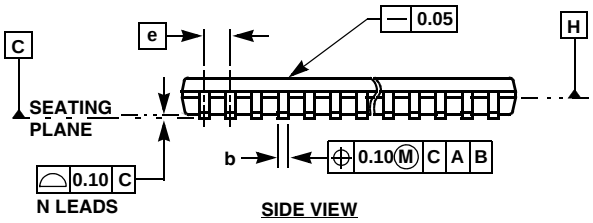
FIGURE 26.

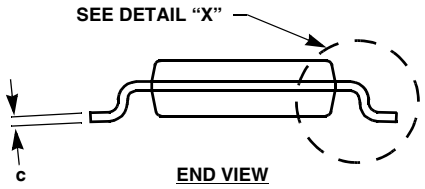
For different values of V_{ON}, V_{OFF}, C_L and H sync timing frequency, the worst case dissipation can be calculated in a similar matter. The value of the R_3 and R_6 must be selected such that the capacitor C_L is discharged via R_3 or R_6 resistor in one half period of the H sync timing.

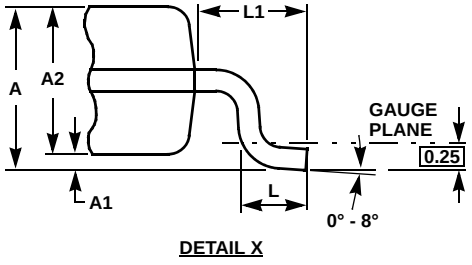
Figures 13 and 14 show the total power dissipation over a range of possible voltages, operating frequencies and loads. Care should be taken to prevent the power from exceeding the maximum rating of the package, as shown in Figure 13.

Thin Shrink Small Outline Package Family (TSSOP)









MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.