ISL78610

Multi-Cell Li-Ion Battery Manager

FN8830
Rev 3.00
May 10, 2018

The automotive grade ISL78610 12-cell battery pack monitor can be used as a stand-alone battery monitor or as a redundant back-up device in an ASIL compliant system. It supervises up to 12 series connected cells and features cell voltage and temperature monitoring along with system diagnostics.

The ISL78610 communicates to a host microcontroller with an SPI interface and to other ISL78610 devices using a robust, proprietary, two-wire daisy chain system.

The ISL78610 is offered in a 64 Ld TQFP package and is specified for operation at a temperature range of -40°C to +105°C.

Applications

- Hybrid Electric Vehicle (HEV), Plug-in Hybrid Electric Vehicle (PHEV) and Electric Vehicle (EV) battery packs
- Electric motorcycle battery packs
- Backup battery and energy storage systems requiring high accuracy management and monitoring
- Portable and semiportable equipment

Features

- Up to 12-cell voltage monitors with support for Li-ion CoO_2, Li-ion Mn_2O_4, and Li-ion $FePO_4$ chemistries
- Cell voltage measurement accuracy of ±10mV
- 13-bit cell voltage measurement
- 14-bit pack voltage and temperature measurements
- Cell voltage scan rate of 19.5µs per cell (234µs to scan 12 cells)
- Internal and external temperature monitoring
- Up to four external temperature inputs
- Robust daisy chain communications system
- Integrated system diagnostics for all key internal functions
- Integrated watchdog shuts down device if communication is lost
- 2Mbps SPI
- AEC-Q100 qualified

Related Literature

For a full list of related documents, visit our website

- ISL78610 product page

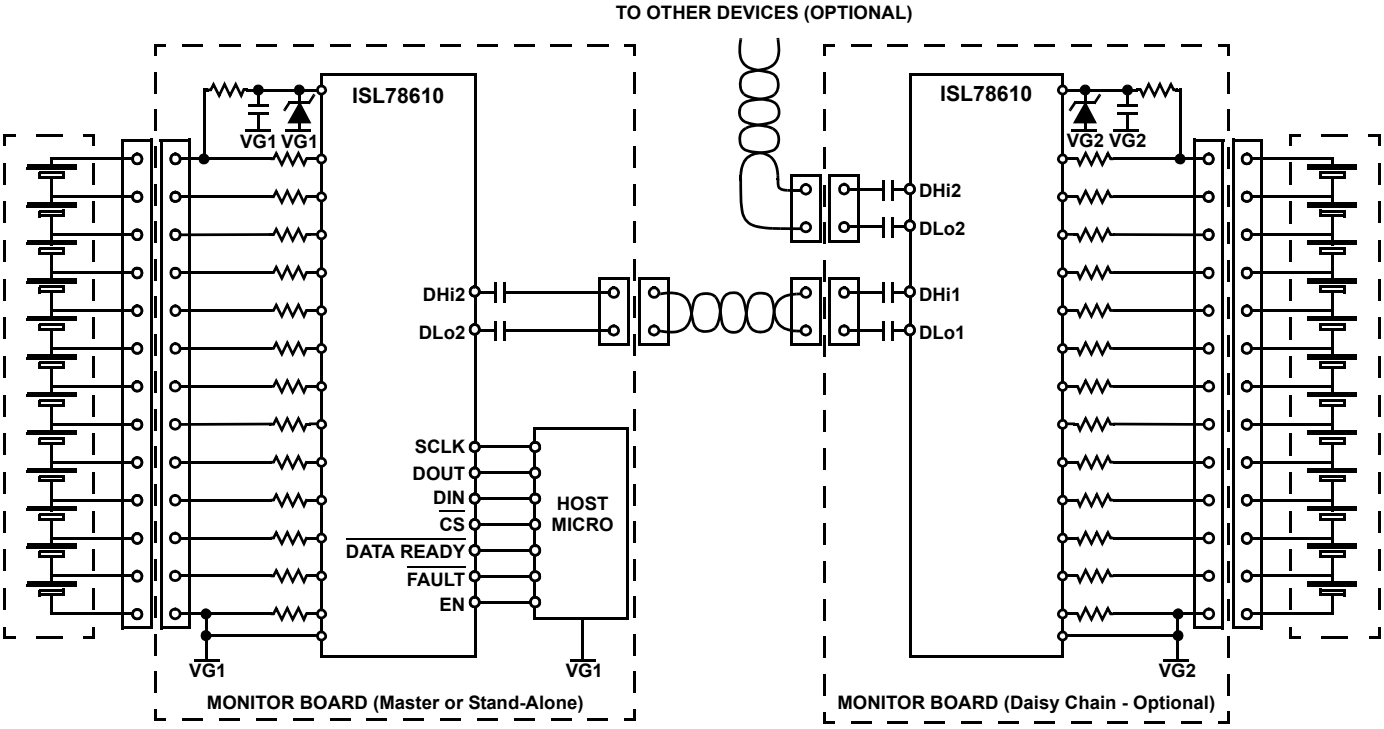

FIGURE 1. TYPICAL APPLICATION

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Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TRIM VOLTAGE, V_{NOM} (V)	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL78610ANZ	ISL78610ANZ	3.3	-40 to +105	-	64 Ld TQFP	Q64.10x10D
ISL78610ANZ-T	ISL78610ANZ	3.3	-40 to +105	1k	64 Ld TQFP	Q64.10x10D
ISL78610EVKIT1Z	Evaluation Kit					

NOTES:

1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL78610 product information page. For more information about handling and processing moisture sensitive devices, see TB363.

TABLE 1. KEY DIFFERENCE BETWEEN FAMILY OF PARTS

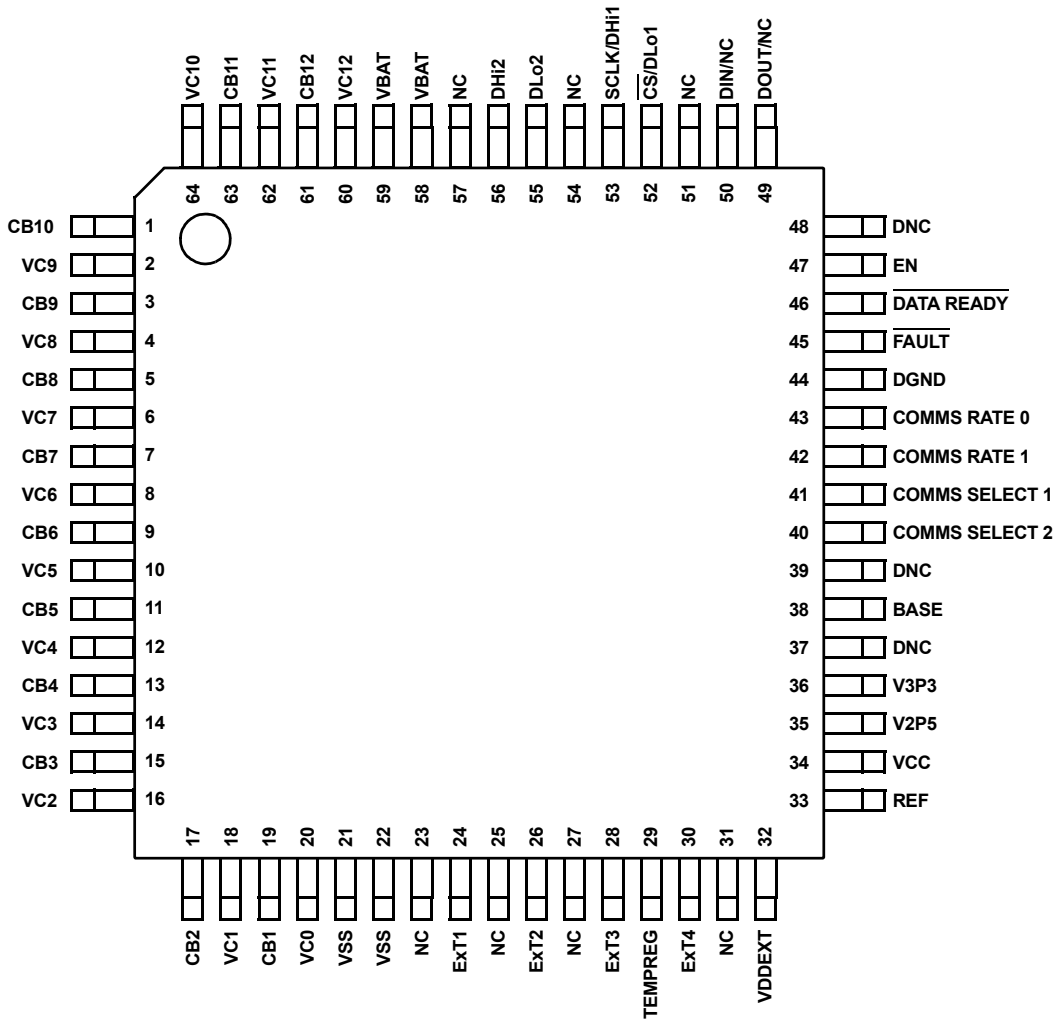
PART NUMBER	INITIAL CELL MONITOR VOLTAGE ERROR (mV) (Note 4)
ISL78610	10.0 (maximum)
ISL78600	2.0 (maximum)

NOTE:

4. Conditions: Temperature = -20°C to +60°C, V_{CELL} = 2.6V to 4.0V, limits applied to a ±3 sigma distribution.

Pin Configuration

ISL78610
(64 LD 10x10 TQFP)
TOP VIEW



Pin Descriptions

SYMBOL	PIN NUMBER	DESCRIPTION
VC0, VC1, VC2, VC3, VC4, VC5, VC6, VC7, VC8, VC9, VC10, VC11, VC12	2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 60, 62, 64	Battery cell voltage inputs. VCn connects to the positive terminal of CELLn and the negative terminal of CELLn+1 (VC12 connects only to the positive terminal of CELL12 and VC0 connects only to the negative terminal of CELL1).
CB1, CB2, CB3, CB4, CB5, CB6, CB7, CB8, CB9, CB10, CB11, CB12	1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 61, 63	Cell balancing FET control outputs. Each output controls an external FET, which provides a current path around the cell for balancing.
VBAT	58, 59	Main IC supply pins. Connect to the most positive terminal in the battery string.
VSS	21, 22	Ground. Connect to the most negative terminal in the battery string.
ExT1, ExT2, ExT3, ExT4	24, 26, 28, 30	External temperature monitor or general purpose inputs. The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements but can also be used as general purpose analog inputs at the user's discretion. 0V to 2.5V input range.
TEMPREG	29	Temperature monitor voltage regulator output. This switched 2.5V output supplies a reference voltage to external NTC thermistor circuits to provide ratiometric ADC inputs for temperature measurement.

Pin Descriptions (Continued)

SYMBOL	PIN NUMBER	DESCRIPTION
VDDEXT	32	External V3P3 supply input/output. This pin is connected to the V3P3 pin by a switch, and can power external circuits from the V3P3 supply. The switch is open when the ISL78610 is placed in Sleep mode.
REF	33	2.5V voltage reference decoupling pin. Connect a 2.0µF to 2.5µF X7R capacitor to VSS. Do not connect any additional external load to this pin.
VCC	34	Analog supply voltage input. Connect to V3P3 with a 33Ω resistor. Connect a 1µF capacitor to ground.
V2P5	35	Internal 2.5V digital supply decoupling pin. Connect a 1µF capacitor to DGND.
V3P3	36	3.3V digital supply voltage input. Connect the emitter of the external NPN regulator transistor to this pin. Connect a 1µF capacitor to DGND.
BASE	38	Regulator control pin. Connect the external NPN transistor's base. Do not let this pin float.
DNC	37, 39, 48	Do not connect. Leave pins floating.
COMMS SELECT 1	41	Communications Port 1 mode select pin. Connect to V3P3 using a 1kΩ resistor for daisy chain communications on Port 1 or to DGND for SPI operation on Port 1.
COMMS SELECT 2	40	Communications Port 2 mode select pin. Connect to V3P3 using a 1kΩ resistor to enable Port 2 or to DGND to disable this port.
COMMS RATE 0, COMMS RATE 1	43, 42	Daisy chain communications data rate setting. Connect to DGND (0) using a 1kΩ resistor or to V3P3 (1) to select between various communication data rates.
DGND	44	Digital Ground.
$\overline{\text{FAULT}}$	45	Logic fault output. Asserted low if a fault condition exists.
$\overline{\text{DATA READY}}$	46	SPI data ready. Asserted low when the device is ready to transmit data to the host microcontroller.
EN	47	Enable input. Tie to V3P3 to enable the part. Tie to DGND to disable (all IC functions are turned off).
DOUT/NC	49	Serial data output (SPI) or NC (daisy chain). 0V to 3.3V push-pull output.
DIN/NC	50	Serial data input (SPI) or NC (daisy chain). 0V to 3.3V input.
$\overline{\text{CS}}$/DLo1	52	Chip-select, active low 3.3V input (SPI) or daisy chain Port 1 Low connection.
SCLK/DHi1	53	Serial-Clock Input (SPI) or daisy chain Port 1 High connection.
DHi2	56	Daisy chain Port 2 High connection.
DLo2	55	Daisy chain Port 2 Low connection.
NC	23, 25, 27, 31, 51, 54, 57	No internal connection.

Block Diagram

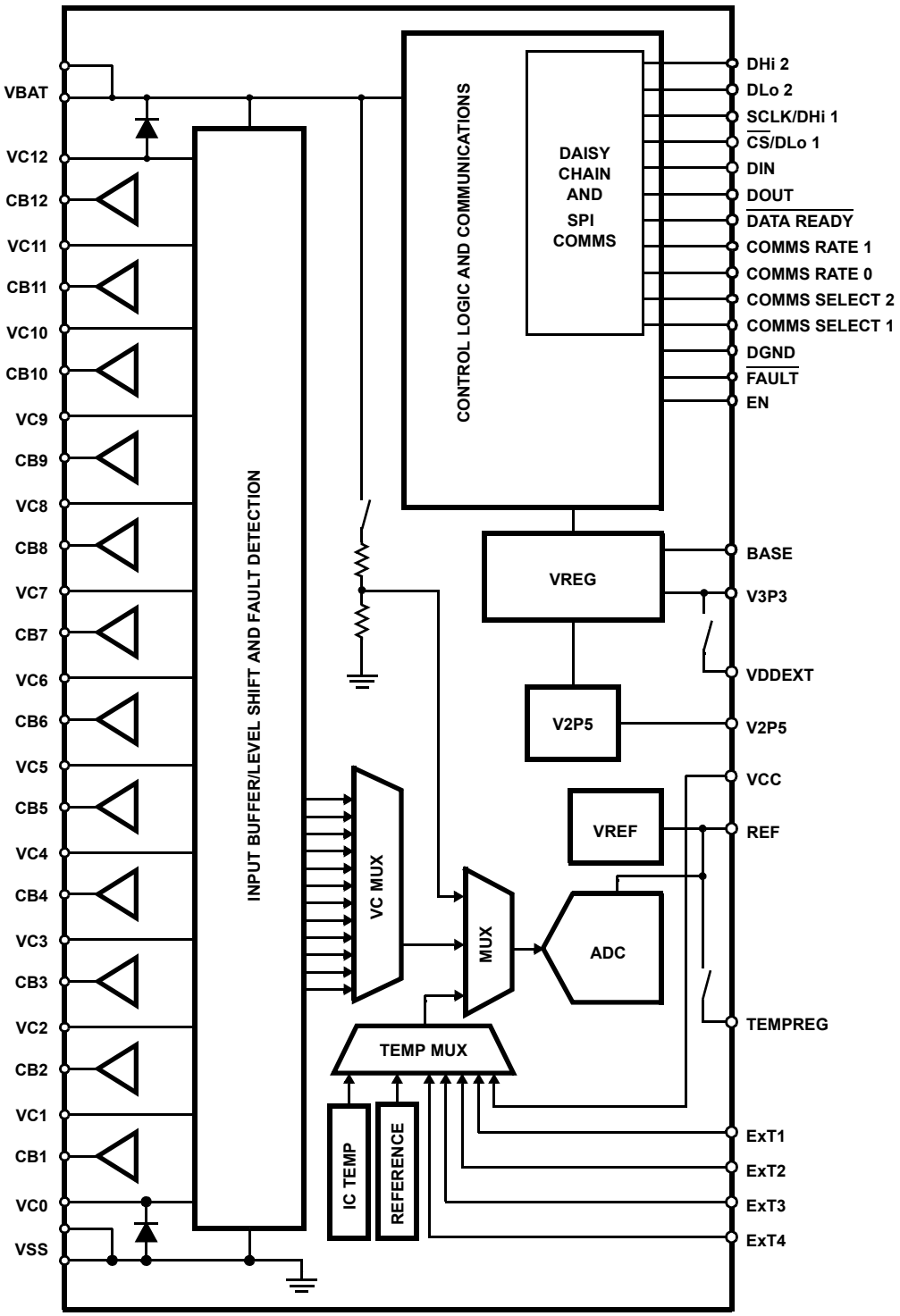


FIGURE 2. BLOCK DIAGRAM

Absolute Maximum Ratings

Unless otherwise specified. With respect to VSS.

BASE, DIN, SCLK, $\overline{CS}$, DOUT, $\overline{DATA\ READY}$, COMMS SELECT n, TEMPREG, REF, V3P3, VCC, $\overline{FAULT}$, COMMS RATE n, EN, VDDEXT . . . . . -0.2V to 5.5V
ExTn . . . . . -0.2V to 4.1V
V2P5. . . . . -0.2V to 2.9V
VBAT . . . . . -0.5V to 63V
Dhi1, DLo1, DHi2, DLo2 . . . . . -0.5V to (V_{BAT} + 0.5V)
VC0 . . . . . -0.5V to +9.0V
VC1, VC2 . . . . . -0.5V to +18V
VC3, VC4 . . . . . -0.5V to +27V
VC5, VC6 . . . . . -0.5V to +36V
VC7, VC8 . . . . . -0.5V to +45V
VC9 . . . . . -0.5V to +54V
VC10, VC11, VC12 . . . . . -0.5V to +63V
VCn (for n = 0 to 12). . . . . -0.5 to VBAT +0.5V
CBn (for n = 1 to 12) . . . . . -0.5 to VBAT +0.5V
CBn (for n = 1 to 9) . . . . . V(VCn-1) -0.5V to V(VCn-1) +9V
CBn (for n = 10 to 12). . . . . V(VCn) -9V to V(VCn) +0.5V
Current into VCn, VBAT, VSS (Latch-Up Test) . . . . . ±100mA
ESD Rating
  Human Body Model (Tested per AECQ100-002) 2kV
  Charged Device Model (Tested per AECQ100-011) 2kV
Latch-Up (Tested per AEC-Q100-004; Class 2, Level A) 100mA

NOTE: DOUT, $\overline{DATA\ READY}$ and $\overline{FAULT}$ are digital outputs and should not be driven from external sources. V2P5, REF, TEMPREG and BASE are analog outputs and should not be driven from external sources.

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (C/W)	θ_{JC} (C/W)
64 Ld TQFP Package (Notes 5, 6)	42	9

Maximum Continuous Package Power Dissipation 400mW
Storage Temperature . . . . . .-55°C to +125°C
Maximum Operating Junction Temperature . . . . . .+125°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

T_A, Ambient Temperature Range . . . . . .-40°C to +105°C
V_{BAT} . . . . . 6V to 60V
V_{BAT} (Daisy Chain Operation) . . . . . 10V to 60V
VCn (for n = 1 to 12) . . . . . .V(VCn-1) to V(VCn-1) + 5V
VC0 . . . . . .-0.1V to 0.1V
CBn (for n = 1 to 9) . . . . . .V(VCn-1) to V(VCn-1) + 9V
CBn (for n = 10 to 12). . . . . V(VCn) -9V to V(VCn)
DIN, SCLK, $\overline{CS}$, COMMS SELECT 1, COMMS SELECT 2, V3P3, VCC, COMMS RATE 0, COMMS RATE 1, EN. . . . . .0V to 3.6V
ExT1, ExT2, ExT3, ExT4 . . . . . .0V to 2.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

V_{BAT} = 6 to 60V, T_A = -20°C to +85°C, unless otherwise specified. Biasing setup as in Figure 45 on page 26 or equivalent.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
MEASUREMENT SPECIFICATIONS						
Cell Voltage Input Measurement Range	V_{CELL}	VC(N) - VC(N-1). For design reference	0		5	V
Cell Monitor Voltage Resolution	$V_{CELLRES}$	[VC(N) - VC(N-1)] LSB step size (13-bit signed number), 5V full scale value		0.61		mV
ISL78610 Cell Monitor Voltage Error (Absolute) For Performance Characteristics, see "Performance Characteristics" on page 15	ΔV_{CELLA}	Cell Measurement Error (Cell measurement error compared with applied voltage with 1k series resistance in line to cell input) Temperature = +25°C, V_{CELL} = 3.3V	-6.5		6.5	mV
		Temperature = +85°C, V_{CELL} = 3.3V	-25.0		25.0	mV
Cell Input Current Note: Cell accuracy figures assume a fixed 1kΩ resistor is placed in series with each VCn pin (n = 0 to 12)	I_{VCELL}	VC0 input, V_{CELL} = 0.5V to 4.95V	-2.0	-1	-0.5	µA
		VC1, VC2, VC3 inputs, V_{CELL} = 0.5V to 4.95V	-3.0	-2	-0.9	µA
		VC4 input, V_{CELL} = 0.5V to 4.95V	-0.8	0	0.9	µA
		VC5, VC6, VC7, VC8, VC9, VC10, VC11 inputs, V_{CELL} = 0.5V to 4.95V	0.5	2	3.2	µA
		VC12 input, V_{CELL} = 0.5V to 4.95V	0.4	1	2.0	µA

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +85°C, unless otherwise specified. Biasing setup as in Figure 45 on page 26 or equivalent. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
V_{BAT} Monitor Voltage Resolution	$VBAT_{RES}$	ADC resolution referred to input (V_{BAT}) level. 14b unsigned number. Full scale value = 79.67V.		4.863		mV
V_{BAT} Monitor Voltage Error	ΔV_{BAT}	Temperature = +25°C, Measured at V_{BAT} = 39.6V	-120		120	mV
		Temperature = +85°C, Measured at V_{BAT} = 39.6V	-320		320	mV
External Temperature Monitoring Regulator	V_{TEMP}	Voltage on TEMPREG output (0 to 2mA load)	2.475	2.500	2.525	V
External Temperature Output Impedance	R_{TEMP}	Output impedance at TEMPREG pin		0.1		Ω
External Temperature Input Range	V_{EXT}	ExTn input voltage range. For design reference	0		2344	mV
External Temperature Input Pull-Up	$R_{EXTTEMP}$	Pull-up resistor to $V_{TEMPREG}$ applied to each input during measurement		10		MΩ
External Temperature Input Offset	V_{EXTOFF}	V_{BAT} = 39.6V	-12		12	mV
External Temperature Input INL	V_{EXTINL}			±0.3		mV
External Temperature Input Gain Error	V_{EXTG}			±8	18.5	mV
Internal Temperature Monitor Error	V_{INTMON}			±10		°C
Internal Temperature Monitor Resolution	T_{INTRES}	Output resolution (LSB/°C). 14b number		31.9		LSB/°C
Internal Temperature Monitor Output	T_{INT25}	Output count at +25°C		9180		Decimal
Power-Up Specifications						
Power-Up Condition Threshold	V_{POR}	V_{BAT} voltage (rising)	4.8	5.1	5.6	V
Power-Up Condition Hysteresis	V_{PORhys}			400		mV
Initial Power-Up Delay	t_{POR}	Time after VPOR condition V_{REF} from 0V to 0.95 x V_{REF}(nom) (EN tied to V3P3) Device can now communicate			27.125	ms
Enable Pin Power-Up Delay	t_{PUD}	Delay after EN = 1 to V_{REF} from 0V to 0.95 x V_{REF}(nom) (V_{BAT} = 39.6V) - Device can now communicate			27.125	ms

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +85°C, unless otherwise specified. Biasing setup as in Figure 45 on page 26 or equivalent. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Supply Current Specifications							
V_{BAT} Supply Current	I_{VBAT}	Non-daisy chain configuration. Device enabled. No communications, ADC, measurement, or open-wire detection activity	6V		35		µA
			39.6V		64		µA
			60V	10	73	96	µA
	$I_{VBATMASTER}$	Daisy chain configuration – master device. Enabled. No communications, ADC, measurement, or open-wire detection activity	6V		530		µA
			39.6V		680		µA
			60V	550	750	1000	µA
		Peak current when daisy chain transmitting			18		mA
	$I_{VBATMID}$	Daisy chain configuration – mid stack device. Enabled. No communications, ADC, measurement, or open-wire detection activity	6V		1020		µA
			39.6V		1250		µA
			60V	1000	1400	1700	µA
		Peak current when daisy chain transmitting			18		mA
	$I_{VBATTOP}$	Daisy chain configuration – top device. Enabled. No communications, ADC, measurement, or open-wire detection activity	6V		530		µA
			39.6V		680		µA
			60V	550	750	1000	µA
		Peak current when daisy chain transmitting			18		mA
	$I_{VBATSLEEP1}$	Sleep mode (EN = 1, daisy chain configuration)		20	35	50	µA
	$I_{VBATSLEEP2}$	Sleep mode (EN = 1, stand-alone, non-daisy chain)		13	20	50	µA
	$I_{VBATSHDN}$	Shutdown. device “off” (EN = 0) (Daisy chain and non-daisy chain configurations)		6	15	54	µA
V_{BAT} Supply Current Tracking. Sleep Mode	$I_{VBATΔSLEEP}$	EN = 1, daisy chain Sleep mode configuration. V_{BAT} current difference between any two devices operating at the same temperature and supply voltage		0		10.5	µA
V3P3 Regulator Voltage (Normal)	V_{3P3N}	EN = 1, Load current range 0 to 5 mA V_{BAT} = 39.6V		3.2	3.35	3.5	V
V3P3 Regulator Voltage (Sleep)	V_{3P3S}	EN = 1, Load current range, no load, (SLEEP) V_{BAT} = 39.6V			2.7		V
V3P3 Supply Current	I_{V3P3}	Device Enabled No measurement activity, normal mode		0.7	1	1.3	mA
V_{REF} Reference Voltage	V_{REF}	EN = 1, no load, normal mode			2.5		V
VDDEXT Switch Resistance	R_{VDDEXT}	Switch “On” resistance, V_{BAT} = 39.6V			12		Ω
VCC Supply Current	I_{VCC}	Device enabled (EN = 1). Stand-alone or daisy configuration. No ADC or daisy chain communications active		2.00	3.25	5.00	mA
	$I_{VCCACTIVE1}$	Device enabled (EN = 1). Stand-alone or daisy configuration. Average current during 16ms Scan Continuous operation. V_{BAT} = 39.6V			6.0		mA
	$I_{VCCSLEEP}$	Device enabled (EN = 1). Sleep mode. V_{BAT} = 39.6V			2.4		µA
	$I_{VCCSHDN}$	Device disabled (EN = 0). Shutdown mode		0	1.2	9.0	µA

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +85°C, unless otherwise specified. Biasing setup as in Figure 45 on page 26 or equivalent. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Over-Temperature Protection Specifications						
Internal Temperature Limit Threshold	T_{INTSD}	Balance stops and auto scan stops. Temperature rising or falling		150		°C
External Temperature Limit Threshold	T_{XT}	Corresponding to 0V (minimum) and $V_{TEMPREG}$ (maximum) External temperature input voltages higher than 15/16 $V_{TEMPREG}$ are registered as open input faults	0		16383	Decimal
Fault Detection System Specifications						
Undervoltage Threshold	V_{UV}	Programmable. Corresponding to 0V (minimum) and 5V (maximum)	0		8191	Decimal
Overvoltage Threshold	V_{OV}	Programmable. Corresponding to 0V (minimum) and 5V (maximum)	0		8191	Decimal
V3P3 Power-Good Window	V_{3PH}	3.3V power-good window high threshold. V_{BAT} = 39.6V		3.90		V
	V_{3PL}	3.3V power-good window low threshold. V_{BAT} = 39.6V		2.65		V
V2P5 Power-Good Window	V_{2PH}	2.5V power-good window high threshold. V_{BAT} = 39.6V		2.7		V
	V_{2PL}	2.5V power-good window low threshold. V_{BAT} = 39.6V		2.0		V
VCC Power-Good Window	V_{VCCH}	V_{CC} power-good window high threshold. V_{BAT} = 39.6V		3.75		V
	V_{VCCL}	VCC power-good window low threshold. V_{BAT} = 39.6V		2.7		V
V_{REF} Power-Good Window	V_{RPH}	V_{REF} power-good window high threshold. V_{BAT} = 39.6V		2.7		V
	V_{RPL}	V_{REF} power-good window low threshold. V_{BAT} = 39.6V		2.30		V
V_{REF} Reference Accuracy Test	V_{RACC}	V_{REF} value calculated using stored coefficients. V_{BAT} = 39.6V (See "Voltage Reference Check Calculation" on page 80)		2.500		V
Voltage Reference Check Timeout	t_{VREF}	Time to check voltage reference value from power-on, enable, or wake-up		20		ms
Oscillator Check Timeout	t_{OSC}	Time to check main oscillator frequency from power-on, enable, or wake-up		20		ms
Oscillator Check Filter Time	t_{OSCF}	Minimum duration of fault required for detection		100		ms
Fast Oscillator		Oscillator frequency	3.4	4	4.6	MHz
Slow Oscillator		Oscillator frequency	27.2	32	36.8	kHz
Cell Open-Wire Detection (See "Scan Wires Command" on page 41 and "Open-wire Test" on page 74)						
Open-Wire Current	I_{OW}	ISCN bit = 0; V_{BAT} = 39.6V	0.125	0.150	0.185	mA
		ISCN bit = 1; V_{BAT} = 39.6V	0.85	1.00	1.15	mA
Open-Wire Detection Time	t_{OW}	Open-wire current source "on" time		4.6		ms
Open VC0 Detection Threshold	V_{VC0}	CELL1 negative terminal (with respect to VSS) V_{BAT} = 39.6V (Note 8)	1.2	1.5	1.8	V

Electrical Specifications

V_{BAT} = 6 to 60V, T_A = -20°C to +85°C, unless otherwise specified. Biasing setup as in Figure 45 on page 26 or equivalent. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Open VC1 Detection Threshold	V_{VC1}	CELL1 positive terminal (with respect to VSS) V_{BAT} = 39.6V (Note 8)	0.6	0.7	0.8	V
Primary Detection Threshold, VC2 to VC12	V_{VC2_12P}	V(VC(n - 1)) - V(VCn), n = 2 to 12 V_{BAT} = 39.6V (Note 8)	-2	-1.5	0	V
Secondary Detection Threshold, VC2 to VC12	V_{VC2_12S}	Via ADC. VC2 to VC12 only V_{BAT} = 39.6V (Note 8)	-100	-30	50	mV
Open V_{BAT} Fault Detection Threshold	V_{VBO}	VC12 - V_{BAT}		200		mV
Open VSS Fault Detection Threshold	V_{VSSO}	VSS - VC0		250		mV
Cell Balance Output Specifications						
Cell Balance Pin Output Impedance	R_{CBL}	CBn output off impedance between CB(n) to VC(n-1): Cells 1 to 9 and between CB(n) to VC(n): Cells 10 to 12	2	4	5	MΩ
Cell Balance Output Current	I_{CBH1}	CBn output on. (CB1 - CB9); V_{BAT} = 39.6V; device sinking current	-28	-25	-21	µA
	I_{CBH2}	CBn output on. (CB10 - CB12); V_{BAT} = 39.6V; device sourcing current	21	25	28	µA
Cell Balance Output Leakage in Shutdown	I_{CBSD}	EN = GND. V_{BAT} = 39.6V	-500	10	700	nA
External Cell Balance FET Gate Voltage	VGS	CBn Output on; External 320kΩ between VCn and CBn (n = 10 to 12) and between CBn and VCn-1 (n = 1 to 9)	7.04	8.00	8.96	V
Internal Cell Balance Output Clamp	VCBCL	I_{CB} = 100µA	8.94			V
Logic Inputs: SCLK, $\overline{CS}$, DIN						
Low Level Input Voltage	V_{IL}				0.8	V
High Level Input Voltage	V_{IH}		1.75			V
Input Hysteresis	V_{HYS}			250		mV
Input Current	I_{IN}	0V < V_{IN} < V3P3	-1		1	µA
Input Capacitance (Note 8)	C_{IN}				10	pF
Logic Inputs: EN, COMMS SELECT1, COMMS SELECT2, COMMS RATE 0, COMMS RATE 1						
Low Level Input Voltage	V_{IL}				0.3*V3P3	V
High Level Input Voltage	V_{IH}		0.7*V3P3			V
Input Hysteresis	V_{HYS}	(Note 8)	0.05*V3P3			V
Input Current	I_{IN}	0V < V_{IN} < V3P3	-1		1	µA
Input Capacitance (Note 8)	C_{IN}				10	pF
Logic Outputs: DOUT, $\overline{FAULT}$, $\overline{DATA\ READY}$						
Low Level Output Voltage	V_{OL1}	At 3mA sink current	0		0.4	V
	V_{OL2}	At 6mA sink current	0		0.6	V
High Level Output Voltage	V_{OH1}	At 3mA source current	V3P3 – 0.4		V3P3	V
	V_{OH2}	At 6mA source current	V3P3 – 0.6		V3P3	V
SPI Interface Timing See Figures 3 and 4						
SCLK Clock Frequency	f_{SCLK}				2	MHz

Electrical Specifications V_{BAT} = 6 to 60V, T_A = -20°C to +85°C, unless otherwise specified. Biasing setup as in Figure 45 on page 26 or equivalent. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Pulse Width of Input Spikes Suppressed	t_{IN1}		50		200	ns
Enable Lead Time	t_{LEAD}	Chip select low to ready to receive clock data	200			ns
Clock High Time	t_{HIGH}		200			ns
Clock Low Time	t_{LOW}		200			ns
Enable Lag Time	t_{LAG}	Last data read clock edge to Chip Select high	250			ns
Slave Access Time	t_A	Chip Select low to DOUT active			200	ns
Data Valid Time	t_V	Clock low to DOUT valid			350	ns
Data Output Hold Time	t_{HO}	Data hold time after falling edge of SCLK	0			ns
DOUT Disable Time	t_{DIS}	DOUT disabled following rising edge of $\overline{CS}$			240	ns
Data Setup Time	t_{SU}	Data input valid prior to rising edge of SCLK	100			ns
Data Input Hold Time	t_{HI}	Data input to remain valid following rising edge of SCLK	80			ns
$\overline{\text{Data Ready}}$ Start Delay Time	$t_{DR:ST}$	Minimum chip select high to $\overline{\text{Data Ready}}$ low		100		ns
$\overline{\text{Data Ready}}$ Stop Delay Time	$t_{DR:SP}$	Maximum chip select high to $\overline{\text{Data Ready}}$ high		750		ns
$\overline{\text{Data Ready}}$ High Time	$t_{DR:WAIT}$	Minimum time between bytes		1.0		µs
Chip Select High Time	$t_{CS:WAIT}$	Minimum high time for $\overline{CS}$ between bytes		200		ns
SPI Communications Timeout	$t_{SPI:TO}$	Maximum time the $\overline{CS}$ remains high before SPI communications time out - requiring the start of a new command		100		µs
DOUT Rise Time	t_R	Up to 50pF load			30	ns
DOUT Fall Time	t_F	Up to 50pF load			30	ns
Daisy Chain Communications Interface: DHi1, DLo1, DHi2, DLo2						
Daisy Chain Clock Frequency		Comms Rate (0, 1) = 11	450	500	550	kHz
		Comms Rate (0, 1) = 10	225	250	275	kHz
		Comms Rate (0, 1) = 01	112.5	125	137.5	kHz
		Comms Rate (0, 1) = 00	56.25	62.5	68.75	kHz
Common-Mode Reference Voltage				$V_{BAT}/2$		V

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design. Limits are 100% tested, unless declared otherwise.
8. These MIN and/or MAX values are based on characterization data and are not 100% tested.
9. Stresses may be induced in the ISL78610 during soldering or other high temperature events that affect measurement accuracy. Initial accuracy does not include effects due to this. See Figure 8 on page 16 for cell reading accuracy obtained after soldering to Renesas evaluation boards. When soldering the ISL78610 to a customized circuit board with a layout or construction significantly differing from the Renesas evaluation board, design verification tests should be applied to determine drift due to soldering and over lifetime.

Timing Diagrams

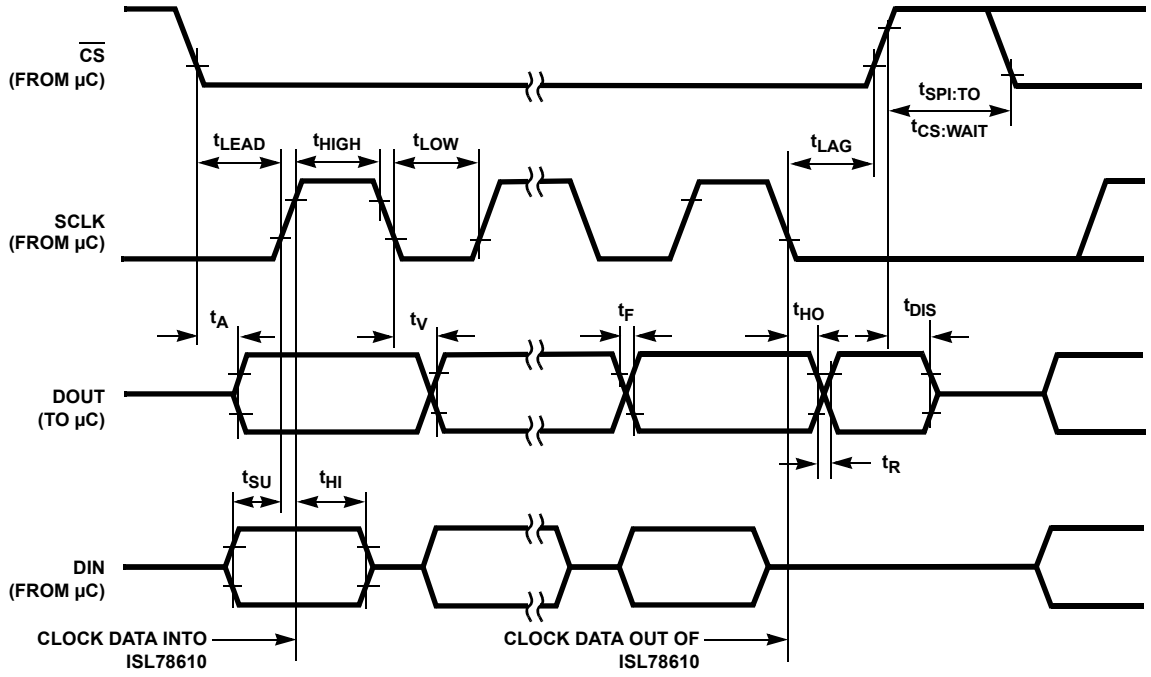


FIGURE 3. SPI FULL DUPLEX (4-WIRE) INTERFACE TIMING

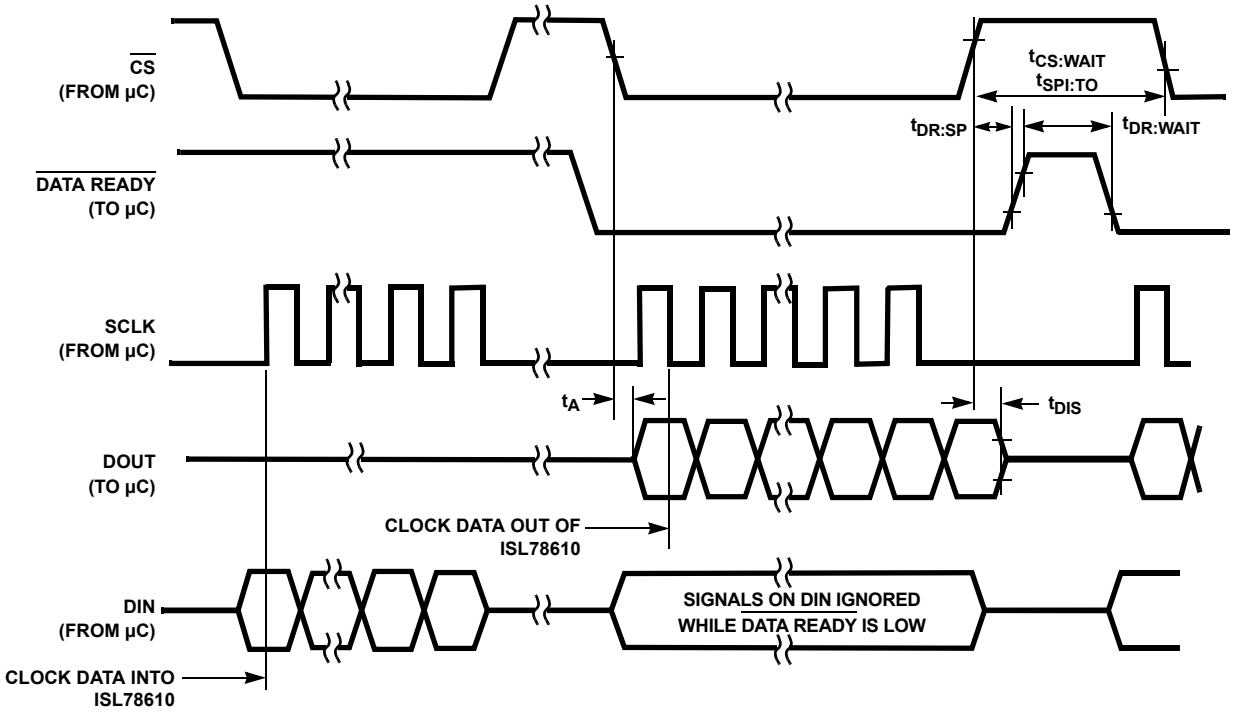


FIGURE 4. SPI HALF DUPLEX (3-WIRE) INTERFACE TIMING

Performance Characteristics

Cell/V_{BAT} Reading Error - 3 Sigma

PARAMETER	SYMBOL	TEST CONDITIONS	-3 SIGMA (Note 10)	TYP	+3 SIGMA (Note 10)	UNIT
ISL78610 Initial Cell Reading Error (Absolute)	ΔV_{CELLA}	Temperature = +25°C V_{CELL} = 3.3V Limits applied to a ±3 sigma distribution	-3.2		3.2	mV
		Temperature = -20°C to +60°C V_{CELL} = 2.6V to 4.0V Limits applied to a ±3 sigma distribution	-10		10	mV
		Temperature = -40°C to -20°C V_{CELL} = 2.6V to 4.0V Limits applied to a ±3 sigma distribution	-15		15	mV
		Temperature = +60°C to +85°C V_{CELL} = 2.6V to 4.0V Limits applied to a ±3 sigma distribution	-15		15	mV
ISL78610 Initial V_{BAT} Reading Error (Absolute)	ΔV_{BAT}	Temperature = -20°C to +60°C V_{BAT} = 31.2V to 48V Limits applied to a ±3 sigma distribution	-175		175	mV
		Temperature = -40°C to +105°C V_{BAT} = 31.2V to 48V Limits applied to a ±3 sigma distribution	-300		300	mV
Voltage Reference Long Term Drift				-0.31		mV/ log (days)

Cell/V_{BAT} Reading Error - 5 Sigma

PARAMETER	SYMBOL	TEST CONDITIONS	-5 SIGMA (Note 10)	TYP	+5 SIGMA (Note 10)	UNIT
ISL78610 Initial Cell Monitor Voltage Error (Absolute)	ΔV_{CELLA}	Temperature = +25°C V_{CELL} = 3.3V Limits applied to a ±5 sigma distribution	-5		5	mV
		Temperature = -20°C to +60°C V_{CELL} = 2.6V to 4.0V Limits applied to a ±5 sigma distribution	-12		12	mV
		Temperature = -40°C to -20°C V_{CELL} = 2.6V to 4.0V Limits applied to a ±5 sigma distribution	-20		20	mV
		Temperature = +60°C to +85°C V_{CELL} = 2.6V to 4.0V Limits applied to a ±5 sigma distribution	-25		25	mV
		Temperature = +85°C to +105°C V_{CELL} = 2.6V to 4.0V Limits applied to a ±5 sigma distribution	-45		45	mV
ISL78610 Initial V_{BAT} Reading Error (Absolute)	ΔV_{BAT}	Temperature = -20°C to +60°C V_{BAT} = 31.2V to 48V Limits applied to a ±5 sigma distribution	-250		250	mV
		Temperature = -40°C to +105°C V_{BAT} = 31.2V to 48V Limits applied to a ±5 sigma distribution	-425		425	mV

NOTE:

10. These distribution values are based on characterization of devices mounted on evaluation boards and are not 100% tested.

Performance Curves

These performance curves are based on characterization of devices mounted on evaluation boards.

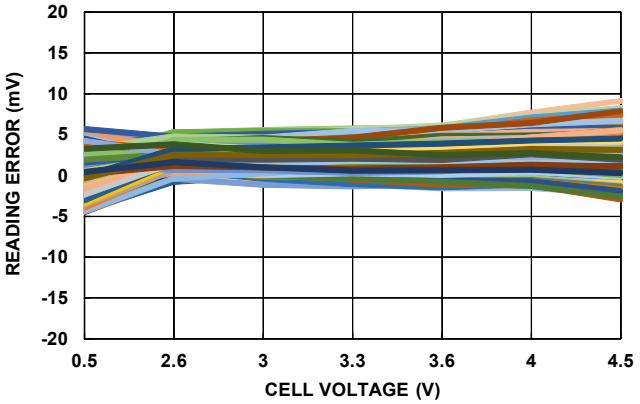


FIGURE 5. CELL VOLTAGE READING ERROR FROM -20°C TO +60°C

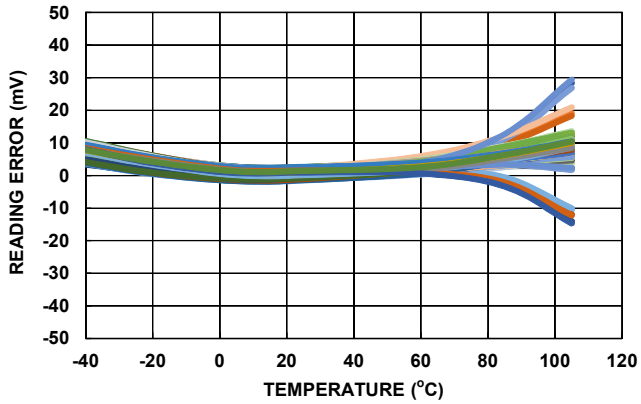


FIGURE 6. CELL VOLTAGE READING ERROR 3.0V TO 3.6V PER CELL

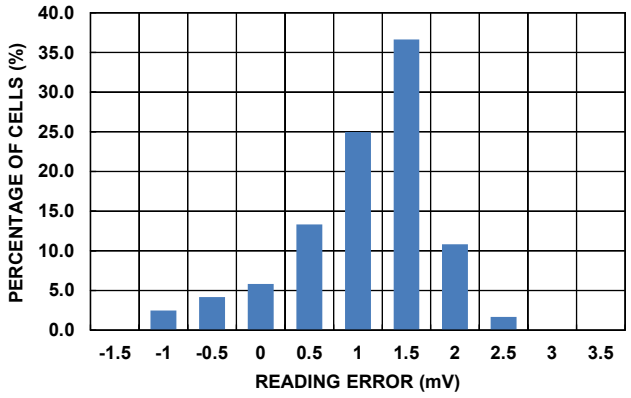


FIGURE 7. INITIAL CELL VOLTAGE ACCURACY FROM EVALUATION BOARDS AT 3.3V, +25°C HISTOGRAM

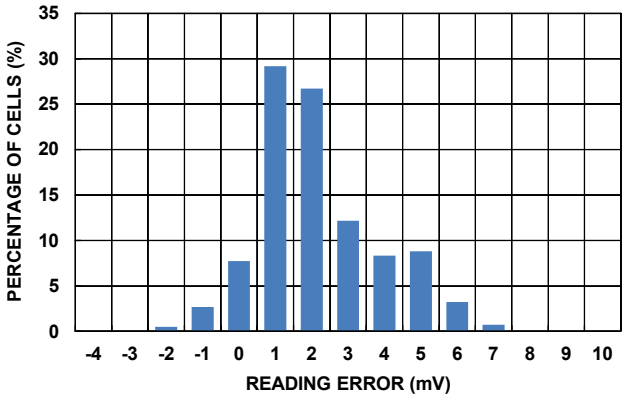


FIGURE 8. CELL READING ERROR FROM EVALUATION BOARDS AT CELL VOLTAGE FROM 2.6V TO 4.0V, AND -20°C TO +60°C HISTOGRAM

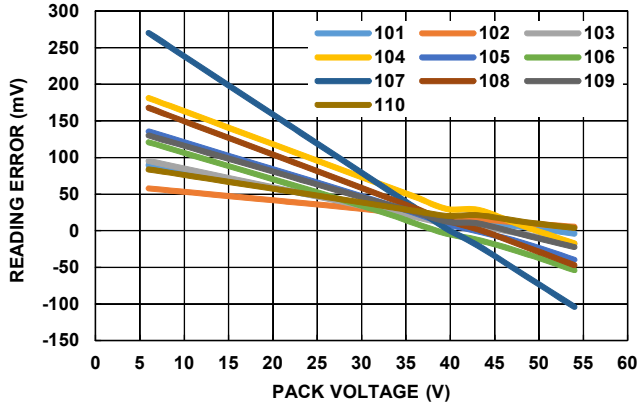


FIGURE 9. PACK VOLTAGE READING ERROR AT +25°C (MULTIPLE BOARDS)

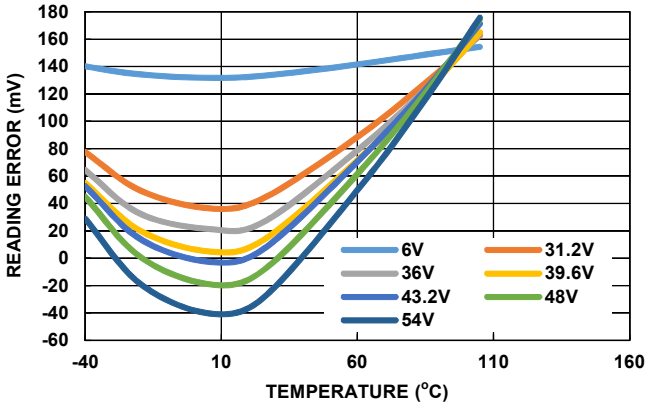


FIGURE 10. AVERAGE PACK VOLTAGE READING ERROR AT 6V TO 54V PACK VOLTAGE

Performance Curves

These performance curves are based on characterization of devices mounted on evaluation boards. **(Continued)**

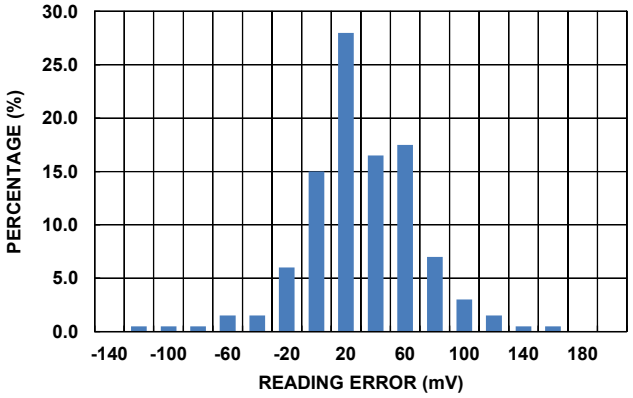


FIGURE 11. INITIAL PACK VOLTAGE ACCURACY 31.2V TO 48V, -20°C TO +60°C HISTOGRAM

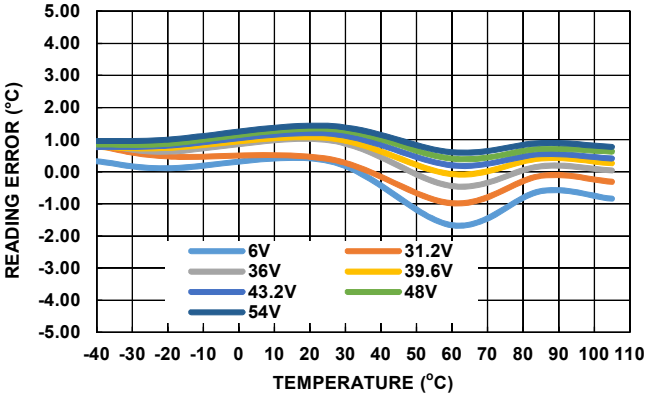


FIGURE 12. IC TEMPERATURE READING ERROR vs TEMPERATURE

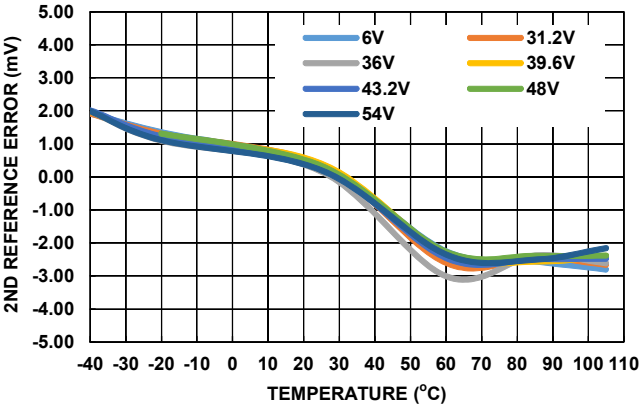


FIGURE 13. VOLTAGE REFERENCE CHECK VOLTAGE ERROR OVER VBAT = 6V TO 54V AND TEMPERATURE

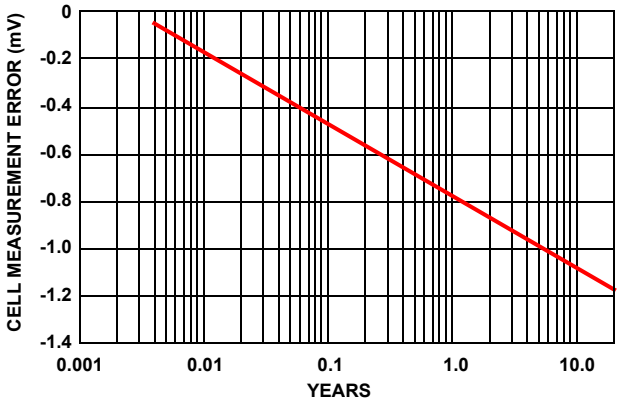


FIGURE 14. LONG TERM DRIFT

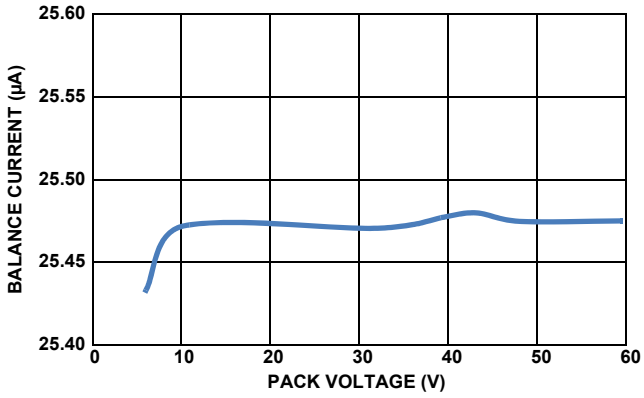


FIGURE 15. BALANCE CURRENT vs PACK VOLTAGE

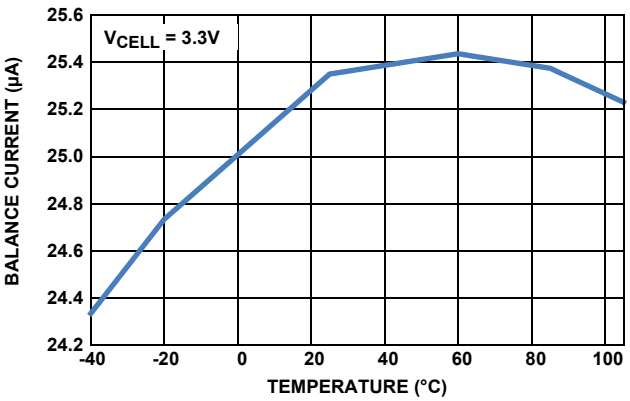


FIGURE 16. BALANCE CURRENT vs TEMPERATURE

Performance Curves

These performance curves are based on characterization of devices mounted on evaluation boards. **(Continued)**

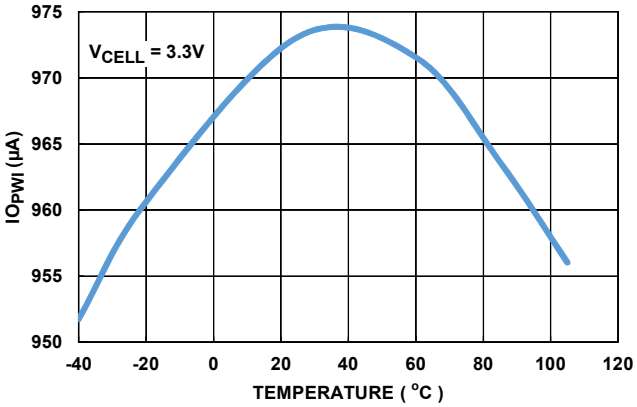


FIGURE 17. OPEN-WIRE TEST CURRENT vs TEMPERATURE (1mA SETTING)

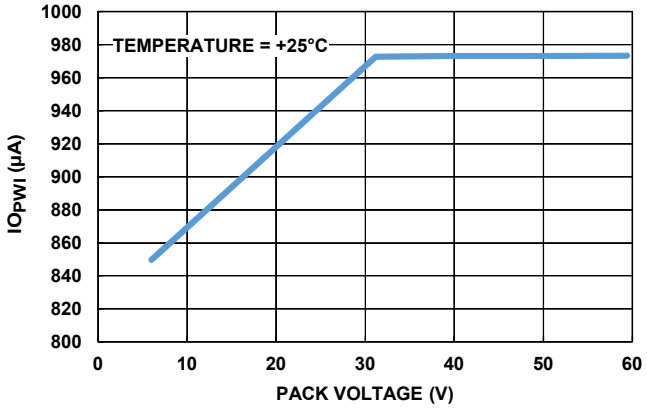


FIGURE 18. OPEN-WIRE TEST CURRENT vs PACK VOLTAGE (1mA SETTING)

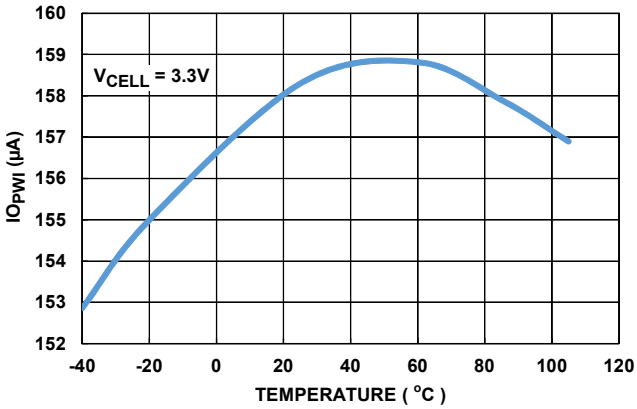


FIGURE 19. OPEN-WIRE TEST CURRENT vs TEMPERATURE (150µA SETTING)

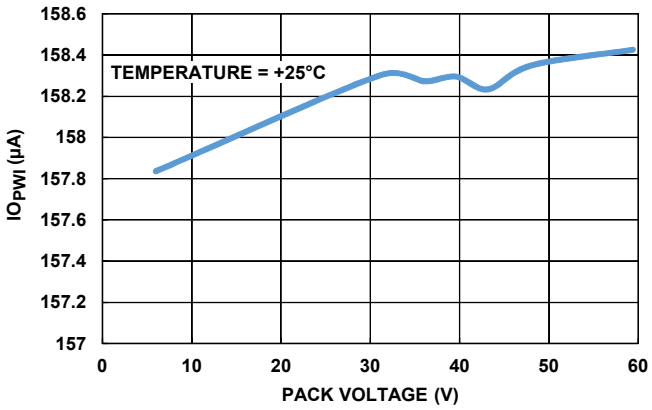


FIGURE 20. OPEN-WIRE TEST CURRENT vs PACK VOLTAGE (150µA SETTING)

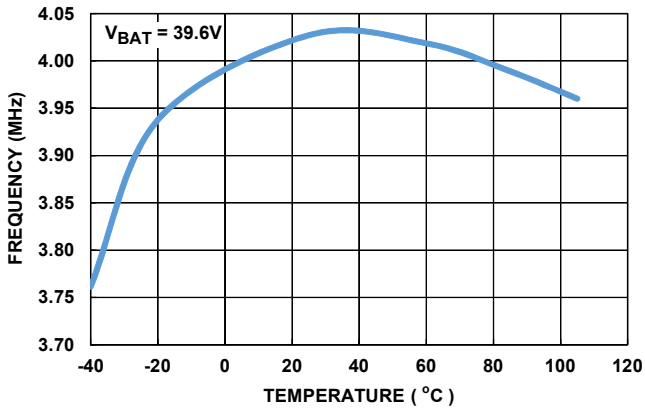


FIGURE 21. 4MHz OSCILLATOR FREQUENCY vs TEMPERATURE

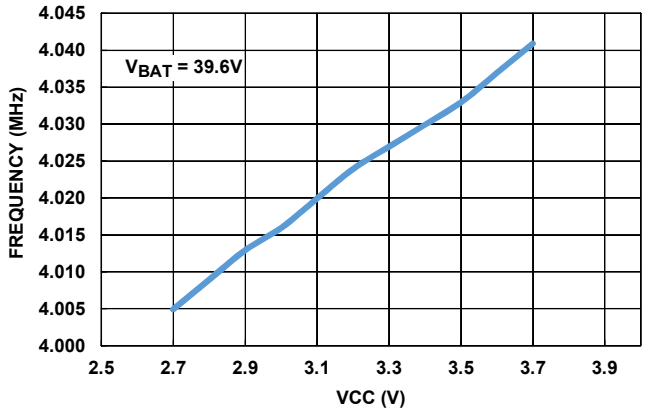


FIGURE 22. 4MHz OSCILLATOR FREQUENCY vs V_{CC}

Performance Curves

These performance curves are based on characterization of devices mounted on evaluation boards. **(Continued)**

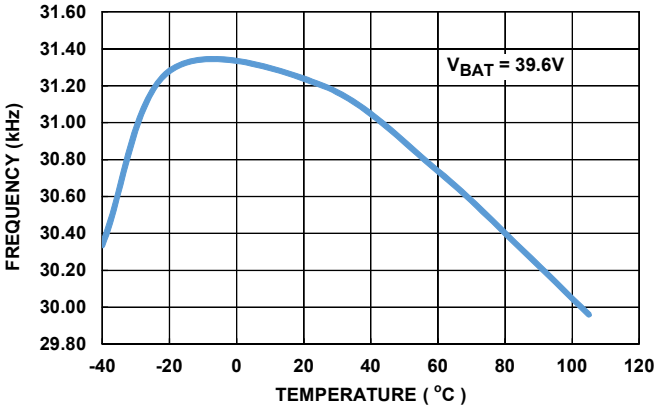


FIGURE 23. 32kHz OSCILLATOR FREQUENCY vs TEMPERATURE

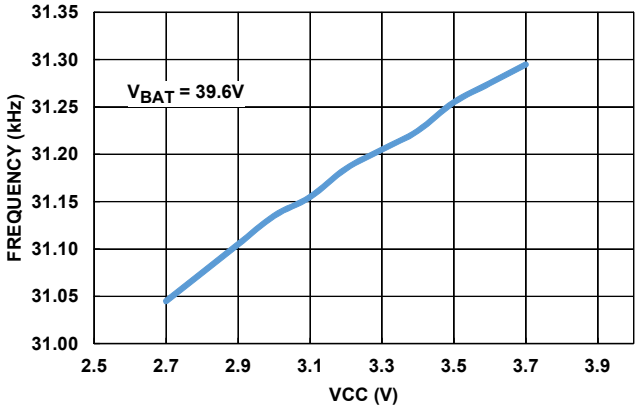


FIGURE 24. 32kHz OSCILLATOR FREQUENCY vs V_{CC}

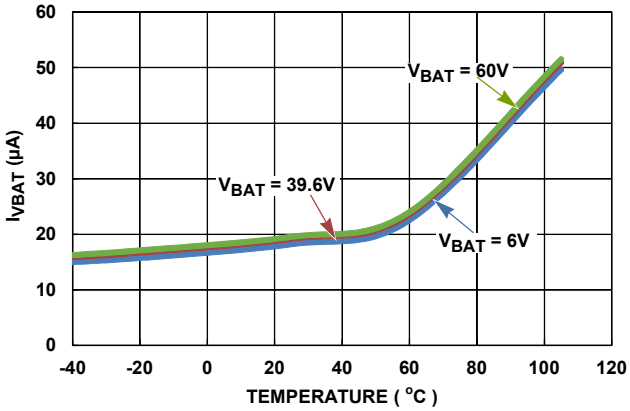


FIGURE 25. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (STAND-ALONE MODE)

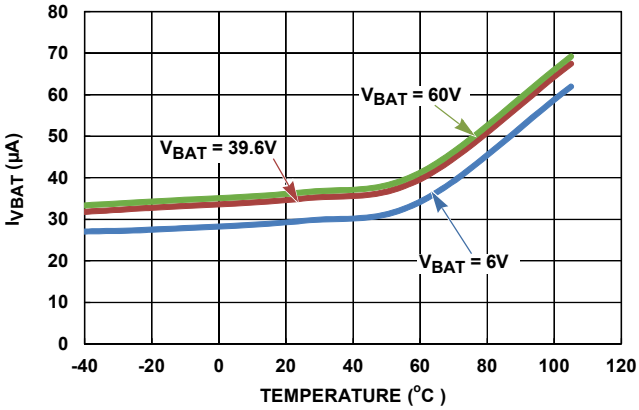


FIGURE 26. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MASTER)

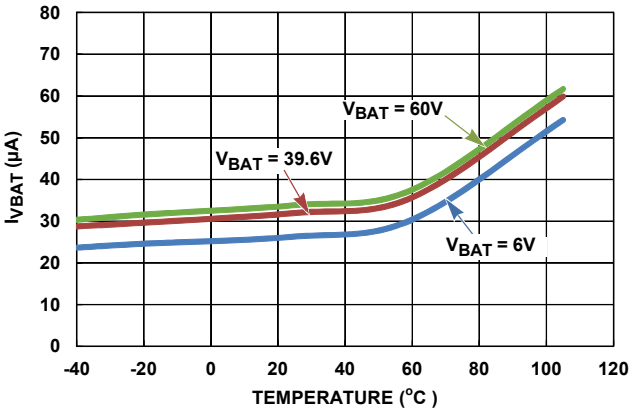


FIGURE 27. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MIDDLE)

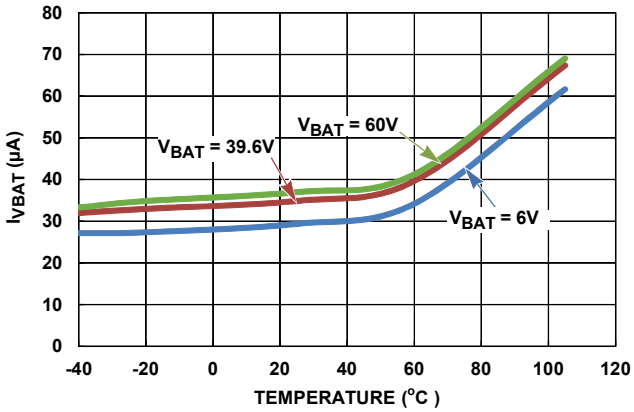


FIGURE 28. PACK VOLTAGE SLEEP CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN TOP)

Performance Curves

These performance curves are based on characterization of devices mounted on evaluation boards. **(Continued)**

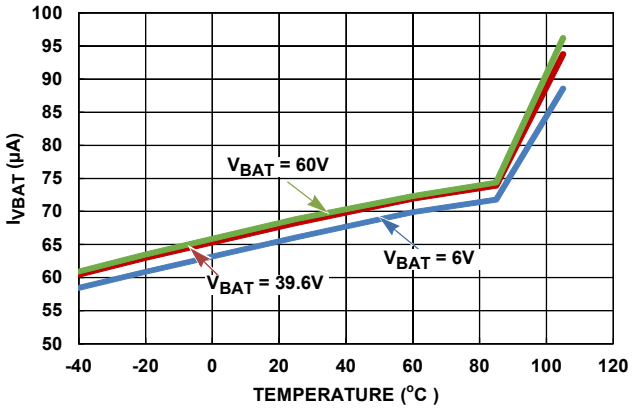


FIGURE 29. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (STAND-ALONE MODE)

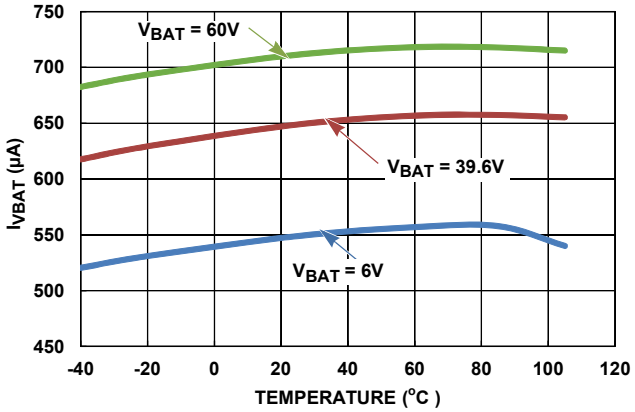


FIGURE 30. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MASTER)

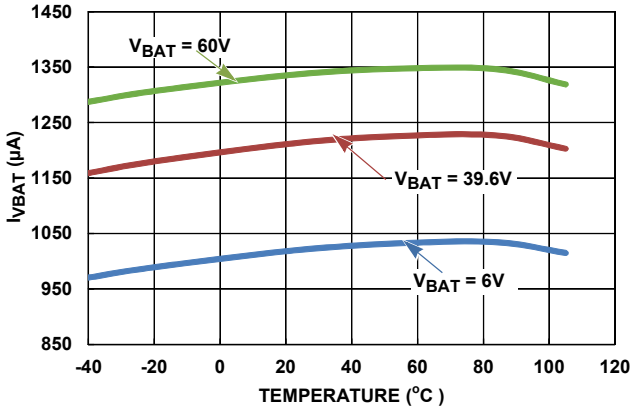


FIGURE 31. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN MIDDLE)

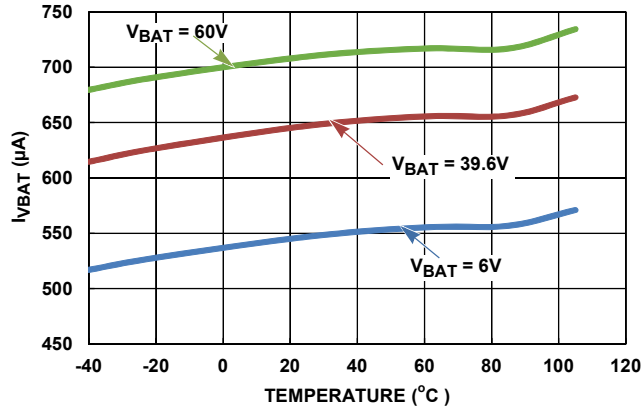


FIGURE 32. PACK VOLTAGE SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V (DAISY CHAIN TOP)

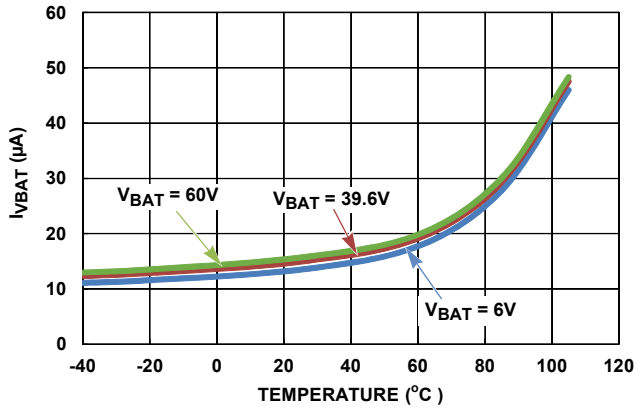


FIGURE 33. PACK VOLTAGE SHUTDOWN CURRENT vs TEMPERATURE (EN = 0) AT 6V, 39.6V, 60V

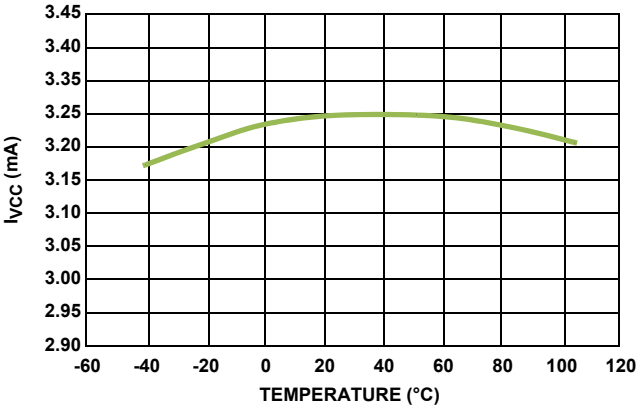


FIGURE 34. V_{CC} SUPPLY CURRENT vs TEMPERATURE AT 6V, 39.6V, 60V

Performance Curves

These performance curves are based on characterization of devices mounted on evaluation boards. **(Continued)**

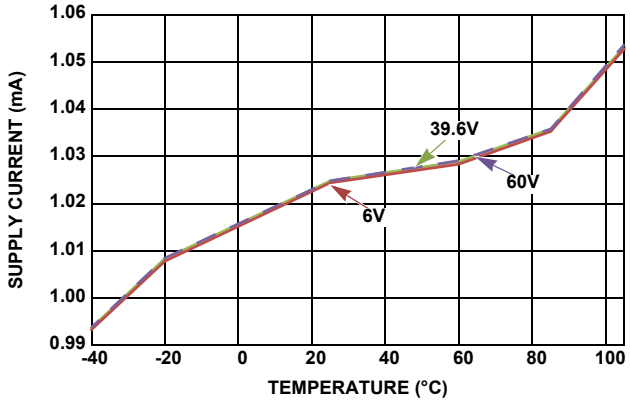


FIGURE 35. V3P3 SUPPLY CURRENT vs TEMPERATURE

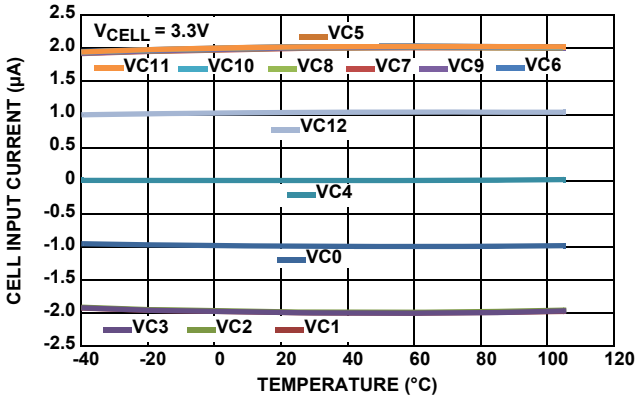


FIGURE 36. CELL INPUT CURRENT vs TEMPERATURE

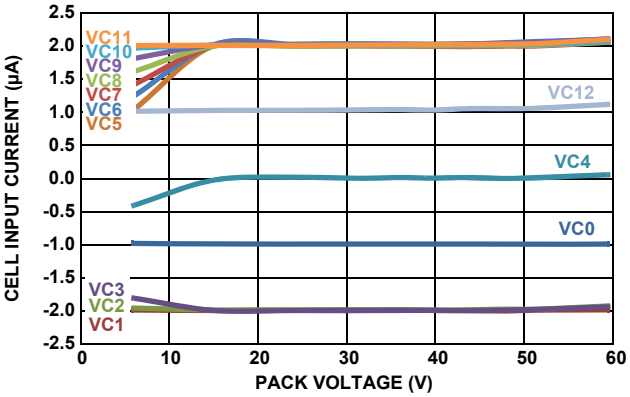


FIGURE 37. CELL INPUT CURRENT vs PACK VOLTAGE (+25°C)

Device Description and Operation

The ISL78610 is a Li-ion battery manager IC that supervises up to 12 series connected cells. Up to 14 ISL78610 devices can be connected in series to support systems with up to 168 cells. The ISL78610 provides accurate monitoring, cell balance control, and diagnostic functions. The ISL78610 includes a voltage reference, 14-bit A/D converter, and registers for control and data.

When multiple ISL78610 devices are connected to a series of cells, their power supply domains are normally non-overlapping. The lower (VSS) supply of each ISL78610 nominally connects to the same potential as the upper (V_{BAT}) supply of the ISL78610 device below.

Within each device, the cell voltage monitoring system has two basic elements: a level shift to eliminate the cell common-mode voltage and an analog-to-digital conversion of the cell voltage.

Each ISL78610 is calibrated at a specific cell input voltage value, V_{NOM}. Cell voltage measurement error data is given in "MEASUREMENT SPECIFICATIONS" on page 8 for various voltage and temperature ranges with voltage ranges defined with respect to V_{NOM}. Plots showing the typical error distribution over the full input range are included in the "Performance Curves" section beginning on page 16.

To collect cell voltage and temperature measurements, the ISL78610 provides two multiple parameter measurement "scanning" modes in addition to single parameter direct measurement capability. The scanning modes provide pseudo simultaneous measurement of all cell voltages in the stack.

The ISL78610 does not measure current. The system does this separately using other measurement systems.

The only filtering applied to the ADC measurements is that resulting from external protection circuits and the limited bandwidth of the measurement path. No additional filtering is performed within the part. This arrangement is typically needed to maintain timing integrity between the cell voltage and pack current measurements. However, the ISL78610 does apply filtering to the fault detection systems.

Cell balancing is an important function in a battery pack consisting of a stack of multiple Li-ion cells. As the cells charge and discharge, differences in each cell's ability to take on and give up charge typically leads to cells with different states of charge. The problem with a stack of cells having different states of charge is that Li-ion cells have a maximum voltage above which it should not be charged, and a minimum voltage below which it should not be discharged. Extreme cases, in which one cell in the stack is at the maximum voltage and one cell is at the minimum voltage, result in a nonfunctional battery stack, because the battery stack cannot be charged or discharged.

The ISL78610 provides multiple cell balance modes: Manual Balance mode, Timed Balance mode, and Auto Balance mode. These modes are described in more detail in "Alarm Response" on page 76.

The ISL78610 incorporates extensive fault diagnostics functions including cell overvoltage and undervoltage, regulator and oscillator operation, open cell input detection, and communication faults. The current status of most faults is accessible using the ISL78610 registers. Some communication faults are reported by special responses to system commands and some as "unprompted" responses from the device detecting the fault to the host microcontroller through the daisy chain.

To conserve power, the ISL78610 has three main power modes: Normal mode, Sleep mode, and "off" (Shutdown mode).

The devices enters Sleep mode in response to a Sleep command or after a watchdog timeout (see "Watchdog Function" on page 76). Only the communications input circuits, low speed oscillator, and internal registers are active in Sleep mode, allowing the part to perform timed scan and balancing activity and to wake up in response to communications.

The device is in Shutdown mode when the Enable pin is low. In this mode, the internal bias for most of the IC is powered down except digital core, Sleep mode regulators, and digital input buffers. When exiting, the device powers up and does not reload the factory programmed configuration data from the EEPROM.

Normal mode consists of an Active state and a Standby state. In the Standby state, all systems are powered and the device is ready to perform an operation in response to commands from the host microcontroller. In the Active state, the device is performing an operation, such as ADC conversion, open-wire detection, etc.

System Hardware Connection

Battery and Cell Balance Connection

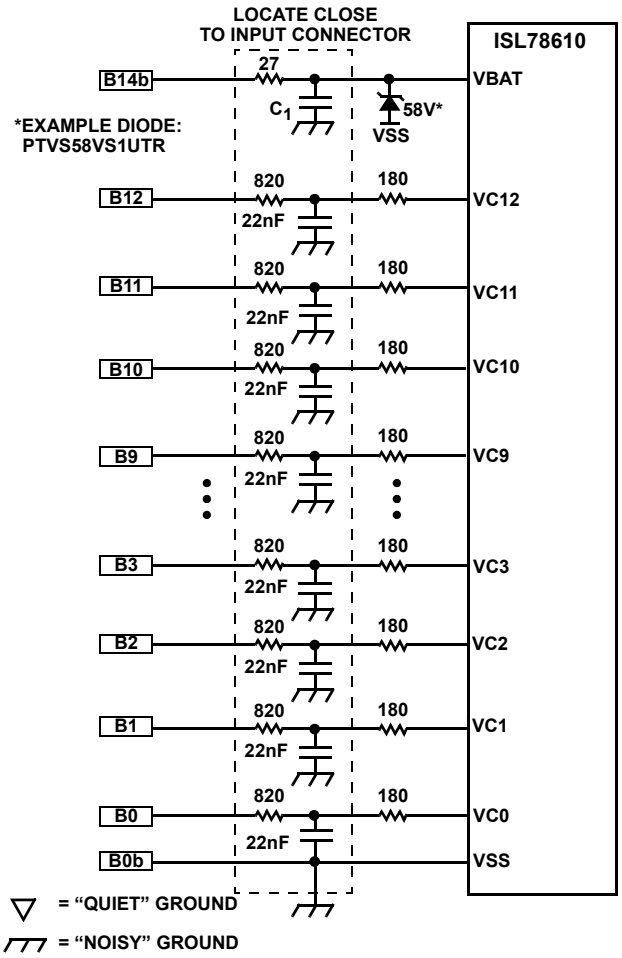
The first consideration in designing a battery system around the ISL78610 is the connection of the cells to the IC.

The battery connection elements are split between the cell monitor connections (VCn) and the cell balance connections (CBn).

BATTERY CONNECTION

All inputs to the ISL78610 VCn pins are protected against battery voltage transients by external RC filters. The basic input filter structure, with capacitors to the local ground, provides protection against transients and EMI for the cell inputs. They carry the loop currents produced by EMI and should be placed as close to the battery connector as possible. The ground terminals of the capacitors must be connected directly to a solid ground plane. Do not use vias to connect these capacitors to the input signal path or to ground. Any vias should be placed in line to the signal inputs so that the inductance of these forms a low pass filter with the grounded capacitors.

The resistors on the input filter provide a current limit function during hot plug events. The ISL78610 is calibrated for use with 1kΩ series protection resistors at the VCn inputs. The VBAT connection uses a lower value input resistor to accommodate the supply current of the ISL78610. As much as possible, the time constant produced by the filtering applied to VBAT should be matched to that applied to the VCn monitoring inputs. See Figure 38.



CELL BALANCE CIRCUITS NOT SHOWN IN THIS FIGURE

FIGURE 38. TYPICAL INPUT FILTER CIRCUITS

The filtered battery voltage connects to the internal cell voltage monitoring system. The monitoring system comprises three basic elements; a level shifter to eliminate the cell common-mode voltage, a multiplexer to select a specific input, and an analog-to-digital conversion of the cell voltage.

Each ISL78610 is calibrated at a specific cell input voltage value, V_{NOM} with an expected input series resistance of 1kΩ. Cell voltage measurement error data is given in "MEASUREMENT SPECIFICATIONS" on page 8 for various voltage and temperature ranges with voltage ranges defined with respect to V_{NOM}. Plots showing the typical error distribution over the full input range are included in the "Performance Curves" section beginning on page 16.

Another important consideration is the connection of cells in a stacked (non-overlapping) configuration. This mainly involves connecting the supply and ground pins at the junction of two devices. The diagram in Figure 39 shows the recommended minimum connection to the pack. Renesas recommends using four connection wires at the intersection of two devices, but this does pose a cost constraint. To minimize the connections, the power and monitor pins are connected separately, as shown in Figure 39. Do not connect all four wires together with a single wire to the pack - first, the power supply current for the devices might affect the accuracy of the cell voltage readings. Second, if the single wire breaks, it is very difficult for the system to tell specifically what happened through normal diagnostic methods.

An alternative circuit in Figure 40 shows the connection of one (or two) wires with additional Schottky diodes to provide supply current paths to allow the device to detect a connection fault and to minimize the effects on cell voltage measurements when there is an open connection to the battery.

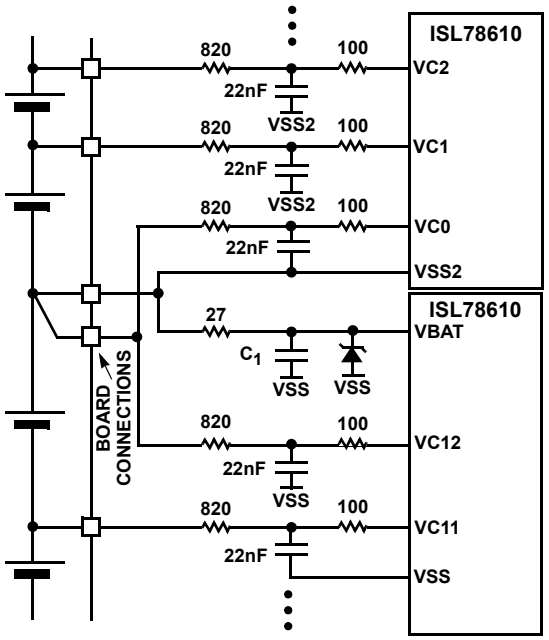


FIGURE 39. BATTERY CONNECTION BETWEEN STACKED DEVICES (OPTION 1)

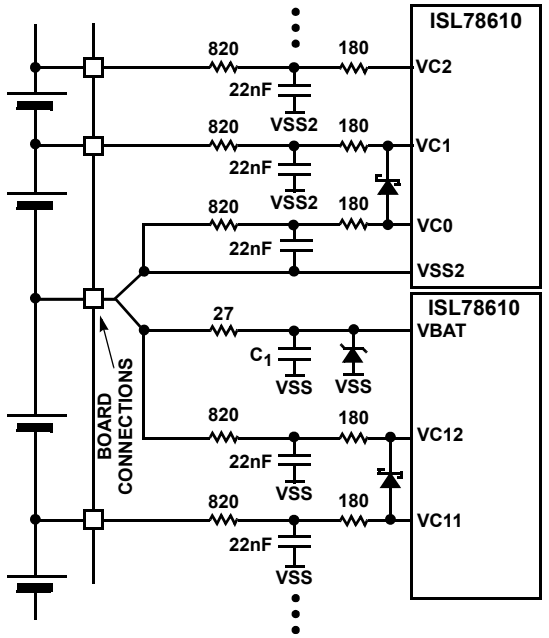


FIGURE 40. BATTERY CONNECTION BETWEEN STACKED DEVICES (OPTION 2)

CELL BALANCE CONNECTION

The ISL78610 uses external MOSFETs for cell balancing. The gate drive for these is derived from on-chip current sources on the ISL78610, which are 25µA nominally. The current sources are turned on and off as needed to control the external MOSFET devices. The current sources are turned off when the device is in Shutdown mode or Sleep mode. The ISL78610 uses a mix of N-channel and P-channel MOSFETs for the external balancing function. The top three cell locations, Cells 10, 11, and 12 are configured to use P-channel MOSFETs, while the remaining cell locations, Cells 1 through 9, use N-channel MOSFETs. The mix of N-channel and P-channel devices are used for the external FETs in order to remove the need for a charge pump, while providing a balance FET gate voltage that is sufficient to drive the FET on, regardless of the cell voltages.

Figures 41 and 42 show the circuit detail for the recommended balancing and cell voltage monitoring system. In this configuration, the cell voltage is monitored after the cell balance resistor. This allows the system to monitor the operation of the external balance circuits and is part of the fault detection system. However, this connection prevents monitoring the cell voltage while cell balance is enabled for that cell.

Figure 41 shows the connection for VC12 to VC9. This connection for the upper three cells uses P-channel FETs, while VC9 and below use N-channel FETs. Similarly, Figure 42 shows the connection for VC1 to VC3 using an N-channel FETs. The connections for VC3 through VC9 are similar. See Figure 51 on page 31 for a more complete example.

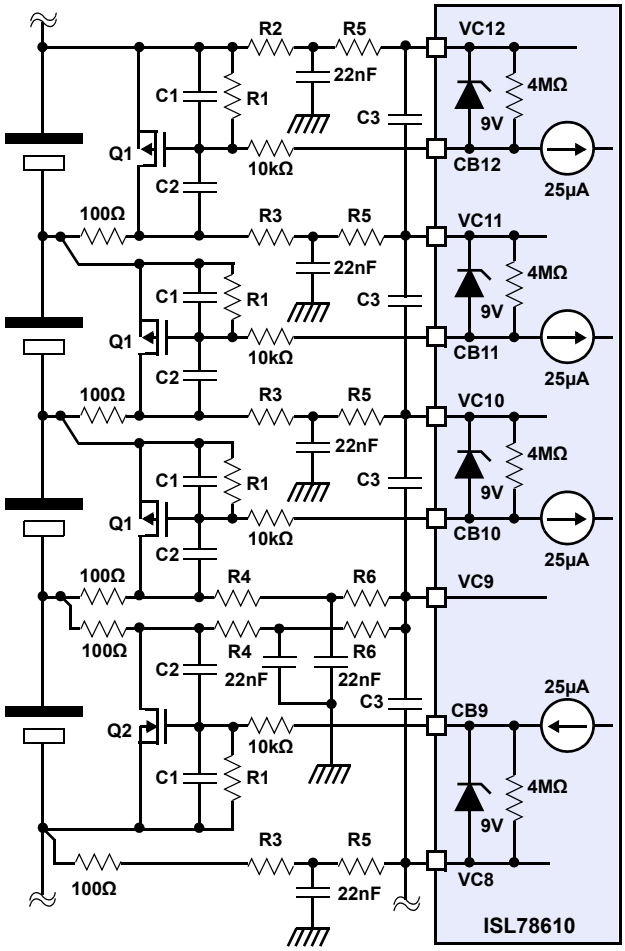


FIGURE 41. CELL MONITOR AND BALANCE CIRCUIT ARRANGEMENT (VC8 TO VC12)

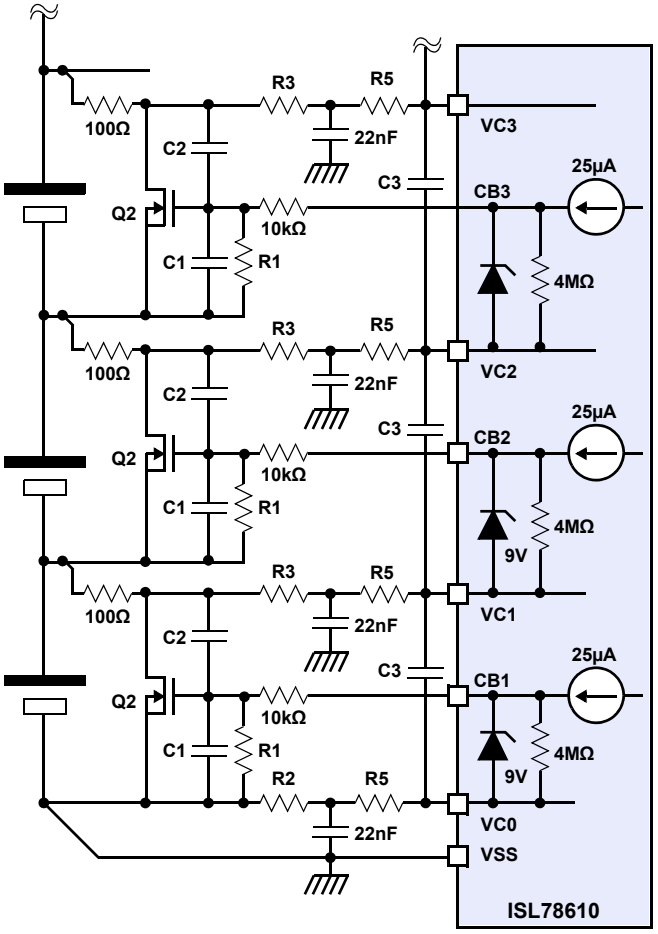


FIGURE 42. CELL MONITOR AND BALANCE CIRCUIT ARRANGEMENT (VC0 TO VC3)

TABLE 2. ISL78610 INPUT FILTER COMPONENT OPTIONS

Q1 (P-channel) with examples		Q2 (N-channel) with examples		C1	C2	C3	R1	R2	R3	R4	R5	R6
30V	A&O Semi AO3401	30V	A&O Semi AO3402	1nF	10nF	Not populated	100k	820	720	1.54k	180	360
30V	A&O Semi AO3401	30V	A&O Semi AO3402	1nF	10nF	100nF	100k	100	0	0	910	1900
60V	Fairchild FDN5618	60V	Diodes DMN6140L-7	Not needed	10nF	Not populated	330k	820	720	1.54k	180	360
60V	Fairchild FDN5618	60V	Diodes DMN6140L-7	Not needed	10nF	100nF	330k	100	0	0	910	1900

Note: Q1 and Q2 should have low RdsON specifications (<100mOhm) to function properly in this fault diagnostic configuration.

Figures 43 and 44 show an alternative balancing and cell voltage monitoring arrangement. The diagram in Figure 43 shows the connection for VC9 through VC12, using P-channel FETs for the upper three inputs. Figure 44 shows the connection for VC1 through VC3 using N-channel FETs. With this alternative circuit it is possible to monitor the cell voltages during cell balancing (even though the voltage will likely drop a little when measuring a cell that is being balanced). However, this circuit connection does not allow the system to check for all potential external component failures. See Figure 54 on page 34 for a more complete example.

The gate of the N-channel MOSFET (cell locations 1 through 9) and P-channel MOSFETs (Cells 10 through 12) are normally protected against excessive voltages during cell voltage transients by the action of the parasitic Cgs and Cgd capacitances. These momentarily turn on the FET in the event of a large transient, thus limiting the Vgs values to reasonable levels. A 10nF capacitor is included between the MOSFET gate and source terminals to protect against EMI effects. This capacitor provides a low impedance path to ground at high frequencies and prevents the MOSFET turning on in response to high frequency interference.

The 10k and 330k resistors prevent the 9V clamp at the output from the ISL78610 from activating.

Reduced cell counts for fewer than 12 cells are accommodated by removing connections to the cells in the middle of the stack first. The top and bottom cell locations are always occupied. See "Operating with Reduced Cell Counts" on page 30 for suggested cell configurations when using fewer than 12 cells.

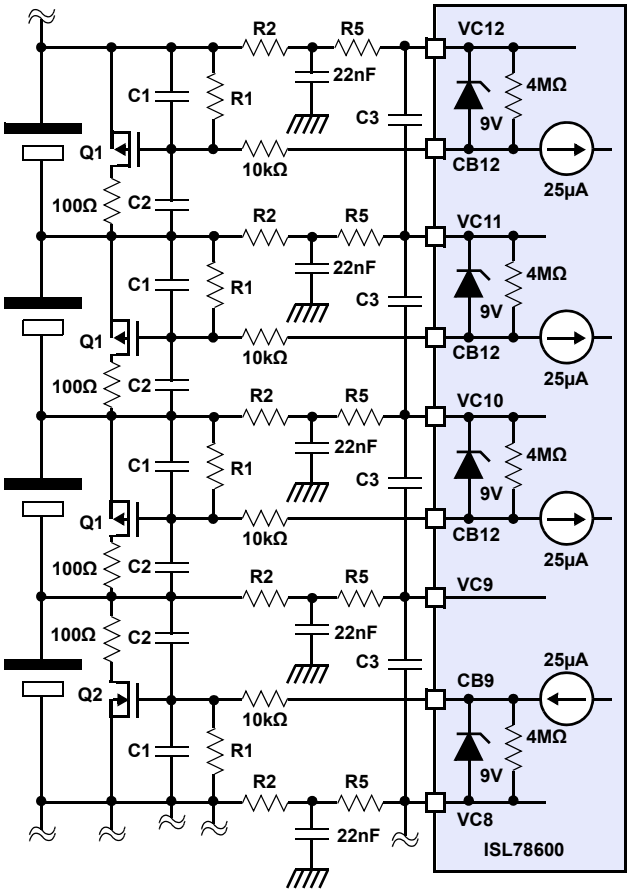


FIGURE 43. ALTERNATE CELL MONITOR AND BALANCE CIRCUIT ARRANGEMENT (VC8 to VC12)

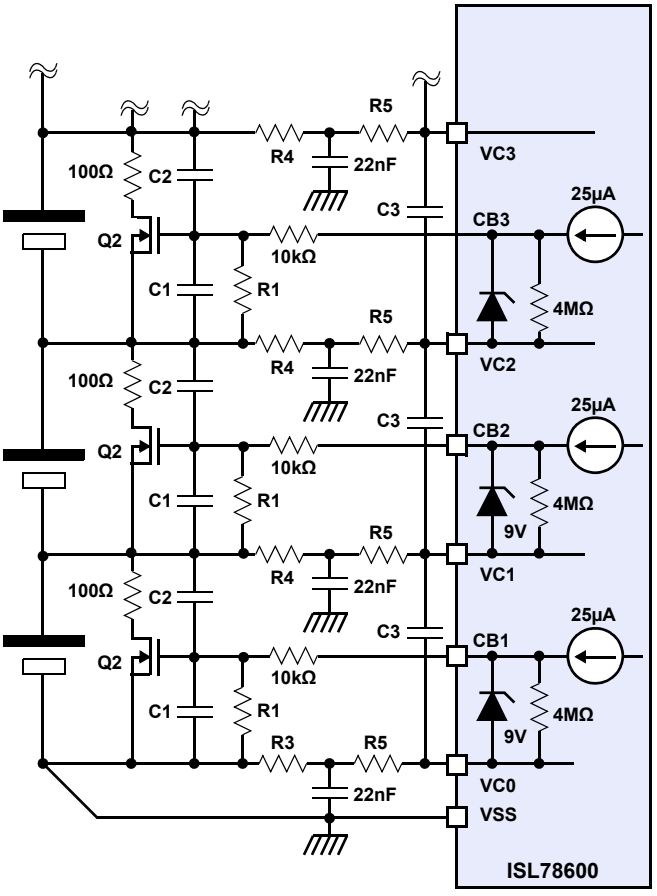


FIGURE 44. ALTERNATE CELL MONITOR AND BALANCE CIRCUIT ARRANGEMENT (VC1 TO VC3)

TABLE 3. ISL78610 INPUT FILTER COMPONENT OPTIONS

Q1 (P-channel) with examples		Q2 (N-channel) with examples		C1	C2	C3	R1	R2	R3	R4	R5	R6
30V	Diodes DMP32D4S-13	30V	Diodes DMN63D8L-7	10nF	1nF	Not populated	100k	820	720	1.54k	180	360
30V	Diodes DMP32D4S-13	30V	Diodes DMN63D8L-7	10nF	1nF	100nF	100k	100	0	0	910	1900
60V	Fairchild NDS0605	60V	Fairchild NDS7002	10nF	Not needed	Not populated	330k	820	720	1.54k	180	360
60V	Fairchild NDS0605	60V	Fairchild NDS7002	10nF	Not needed	100nF	330k	100	0	0	910	1900

Note: Q1 and Q2 RdsON specification is not critical, since fault diagnostics are not performed in this configuration.

CELL VOLTAGE MEASUREMENTS DURING BALANCING

The standard cell balancing circuit (Figures 41 and 42 on page 24 and Figure 51 on page 31) is configured so the cell measurement is taken from the drain connection of the balancing MOSFET. When balancing is enabled for a cell, the resulting cell measurement is then the voltage across the balancing MOSFET (VGS voltage). This system provides a diagnostic function for the cell balancing circuit. The input voltage of the cell adjacent to the MOSFET drain connection is also affected by this mechanism: the input voltage for this cell increases by the same amount that the voltage of the balance cell decreases.

For example, if Cells 2 and 3 are both at 3.6V and balancing is enabled for Cell 2, the voltage across the balancing MOSFET may be only 50mV. In this case, the input voltage on the VC2 pin would be VC1 + 50mV and Cell 3 would be VC2 + 7.15V. The VC3 value in this case is outside the measurement range of the cell input. VC3 would then read full scale voltage, which is 4.9994V. This full scale voltage reading will occur if the sum of the voltages on the two adjacent cells is greater than the total of 5V plus the “balancing on” voltage of the balanced cell. Table 4 shows the cell affected when each cell is balanced.

The cell voltage measurement is affected by impedances in the cell connectors and any associated wiring. The balance current passes through the connections at the top and bottom of the balanced cell. This effect further reduces the voltage measured on the balanced cell and increases the voltage measured on cells above and below the balanced cell. For example, if Cell 4 is balanced with 100mA, and the total impedance of the connector and wiring for each cell connection is 0.1Ω, then Cell 4 would read low by an additional 20mV (10mV due to each pin) while Cells 3 and 5 would both read high by 10mV.

TABLE 4. CELL READINGS DURING BALANCING

CELL BALANCED	CELL WITH LOW READING	CELL WITH HIGH READING
1	1	2
2	2	3
3	3	4
4	4	5
5	5	6
6	6	7
7	7	8
8	8	9
9	9*	10*
10	10*	9*
11	11	10
12	12	11

NOTE: *Cells 9 and 10 produce a different result from the other cells. Cell 9 uses an N-channel MOSFET while Cell 10 uses a P-channel MOSFET. The circuit arrangement used with these devices produces approximately half the normal cell voltage when balancing is enabled. The adjacent cell then sees an increase of half the voltage of the balanced cell.

Power Supplies and Reference

VOLTAGE REGULATORS

The two VBAT pins, along with V3P3, VCC, and VDDEXT, supply power to the ISL78610. The VBAT pins provide power for the high voltage circuits and Sleep mode internal regulators. V3P3 supplies the logic circuits and VCC similarly supplies the low voltage analog circuits. The V3P3 and VCC pins must not be connected to external circuits other than those associated with the ISL78610 main voltage regulator. The VDDEXT pin is provided for use with external circuits.

The ISL78610 main low voltage regulator uses an external NPN pass transistor to supply 3.3V power for the V3P3 and VCC pins. This regulator is enabled whenever the ISL78610 is in Normal mode and can also power external circuits through the VDDEXT pin. An internal switch connects the VDDEXT pin to the V3P3 pin. Both the main regulator and the switch are off when the part is placed in Sleep mode or Shutdown mode (EN pin LOW.) The pass transistor’s base is connected to the ISL78610 BASE pin. A suitable configuration for the external components associated with the V3P3, VCC, and VDDEXT pins is shown in Figure 45 on page 26.

The external pass transistor is required. **Do not allow the BASE pin to float.**

VOLTAGE REFERENCE

A bypass capacitor is required between REF (pin 33) and the analog ground VSS. The total value of this capacitor should be in the range of 2.0µF to 2.5µF. Use X7R type dielectric capacitors for this function. The ISL78610 continuously performs a power-good check on the REF pin voltage starting 20ms after a power-up, Enable, or Wake-up condition. If the REF capacitor is too large, then the reference voltage may not reach its target voltage range before the power-good check starts and result in a REF fault. If the capacitor is too small, then it may lead to inaccurate voltage readings.

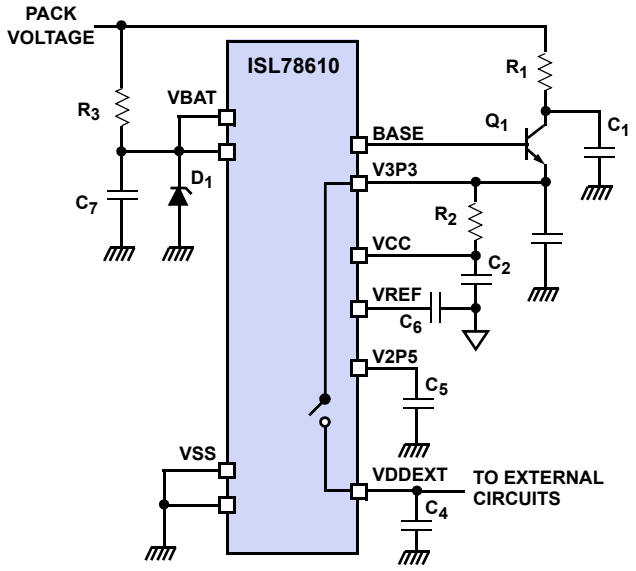


FIGURE 45. ISL78610 REGULATOR AND EXTERNAL CIRCUIT SUPPLY ARRANGEMENT

TABLE 5. COMPONENT SELECTION FOR CRICUIT IN Figure 45

COMPONENT	VALUE
R_1	Sized to pass the maximum supply current at the minimum specified battery pack voltage.
R_2	33Ω
R_3	27Ω
C_1	Selected to produce a time constant with R_1 of a few milliseconds. C_1 and R_1 provide transient protection for the collector of Q_1. Obtain component values and voltage ratings by simulating measurement of the worst case transient expected on VBAT.
C_2, C_3, C_4, C_5	1µF
C_6	2.2µF
C_7	220nF/100V
D_1	PTVS54VS1UTR
Q_1	Selected for power dissipation at the maximum specified battery voltage and load current. The load current includes the V_{3P3} and V_{CC} currents for the ISL78610 and the maximum current drawn by external circuits supplied through VDDEXT. The voltage rating should be determined by the worst case transient expected on VBAT.

Communications Circuits

The ISL78610 operates as a stand-alone monitor for up to 12 series connected cells or in a daisy chain configuration for multiple series connected ISL78610 monitoring devices. For stand-alone (non-daisy chain) systems, only a synchronous SPI is needed for communications between a host microcontroller and the ISL78610.

Both the SPI port and daisy chain ports are needed for communication in systems with more than one ISL78610.

A daisy chain consists of a bottom device, a top device, and up to 12 middle devices. The ISL78610 device located at the bottom of the stack is called the master and communicates to the host microcontroller using SPI communications and to other ISL78610 devices using the daisy chain port. Each middle device provides two daisy chain ports: one is connected to the ISL78610 above in the stack and the other to the ISL78610 below. Communications between the SPI and daisy chain interfaces are buffered by the master device to accommodate timing differences between the two systems.

The daisy chain ports are fully differential, DC balanced, bidirectional, and AC coupled to provide maximum immunity to EMI and other system transients while requiring only two wires for each port.

The addressed device, the top device, and the bottom device act as master devices for controlling command and response communications. All other devices are repeaters, passing data up or down the chain.

The communications setup is controlled by the COMMS SELECT 1 and COMMS SELECT 2 pins on each device. These pins specify whether the ISL78610 is a stand-alone device, the daisy chain master, the daisy chain top, or a middle position in the daisy chain. See Figures 46 and 47 and Table 6. This configuration also specifies the use of SPI or daisy chain on the communication ports.

TABLE 6. COMMUNICATIONS MODE CONTROL

COMMS SELECT 1	COMMS SELECT 2	PORT 1 COMM	PORT 2 COMM	COMMUNICATIONS CONFIGURATION
0	0	SPI (Full Duplex)	Disabled	Stand-alone
0	1	SPI (Half Duplex)	Enabled	Daisy chain, master device setting
1	0	Daisy Chain	Disabled	Daisy chain, top device setting
1	1	Daisy Chain	Enabled	Daisy chain middle device setting

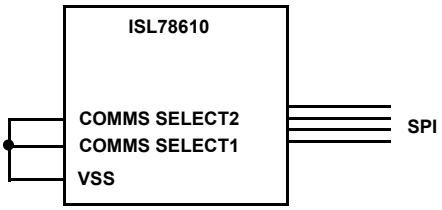


FIGURE 46. NON-DAISY CHAIN COMMUNICATIONS CONNECTIONS AND SELECTION

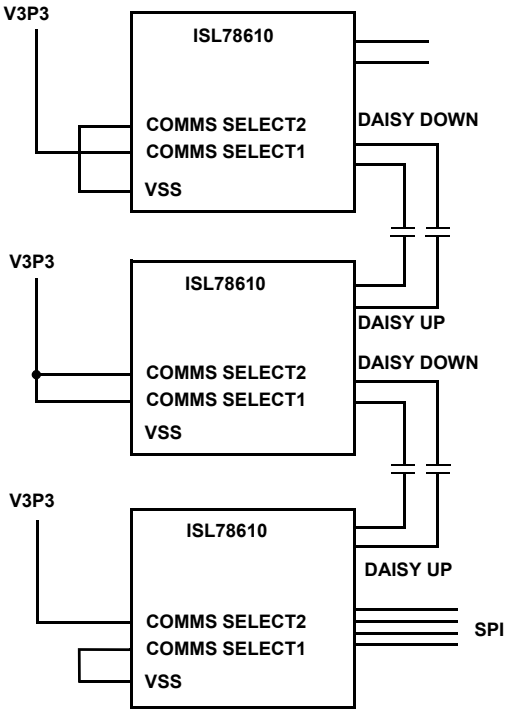


FIGURE 47. DAISY CHAIN COMMUNICATIONS CONNECTIONS AND SELECTION

Four daisy chain data rates are available and are configurable by pin selection using the COMMS RATE 0 and COMMS RATE 1 pins (see Table 7).

TABLE 7. DAISY CHAIN COMMUNICATIONS DATA RATE SELECTION

COMMS RATE 0	COMMS RATE 1	DATA RATE (kHz)
0	0	62
0	1	125
1	0	250
1	1	500

Daisy Chain Circuits

The ISL78610 daisy chain communications system external circuit arrangement is symmetrical to provide the bidirectional communications function. The performance of the system under transient voltage and EMI conditions is enhanced by the use of a capacitive load. A schematic of the daisy chain circuit for board to board connection is shown in Figure 48.

The basic circuit elements are the series resistor and capacitor elements R_1 and C_1, which provide the transient current limit and AC coupling functions, and the line termination components C_2, which provide the capacitive load. Capacitors C_1 and C_2 should be located as closely as possible to the board connector.

The AC coupling capacitors C_1 need to be rated for the maximum voltage, including transients, that will be applied to the interface. Specific component values are needed for correct operation with each daisy chain data rate and are given in Table 8 on page 28.

The daisy chain operates with standard unshielded twisted pair wiring. The component values given in Table 8 accommodate cable capacitance values from 0pF to 50pF when operating at the 500kHz data rate. Higher cable capacitance values can be accommodated by either reducing the value of C_2 or operating at lower data rates.

The values of components in Figure 48 are given in Table 8 for various daisy chain operating data rates.

The circuit and component values of Figure 48 and Table 8 will accommodate cables with differential capacitance values in the ranges given. This allows a range of cable lengths to be accommodated through careful selection of cable properties.

The circuit of Figure 48 provides full isolation when used with off board wiring. The daisy chain external circuit can be simplified in cases in which the daisy chain system is contained within a single board. Figure 49 on page 29 and Table 9 on page 29 show the circuit arrangement and component values for single board use. In this case, the AC coupling capacitors C_1 need to be rated only for the maximum transient voltage expected from device to device.

The value for C2 in Table 8 is ideally 220pF. This creates a 3:1 ratio in the transmit vs. received signal. However, additional capacitance on the board due to device pin, board layout, and connector capacitance forces the use of a lower value capacitor. In practical terms, using the “ideal” capacitor and ignoring real additional capacitance on the board reduces the signal level at the receiver. Renesas recommends that the board layout minimize distance on daisy chain traces and to isolate them as much as possible from each other and from ground planes. Expect at least 50pF to 90pF of additional board capacitance, depending on the layout and connectors

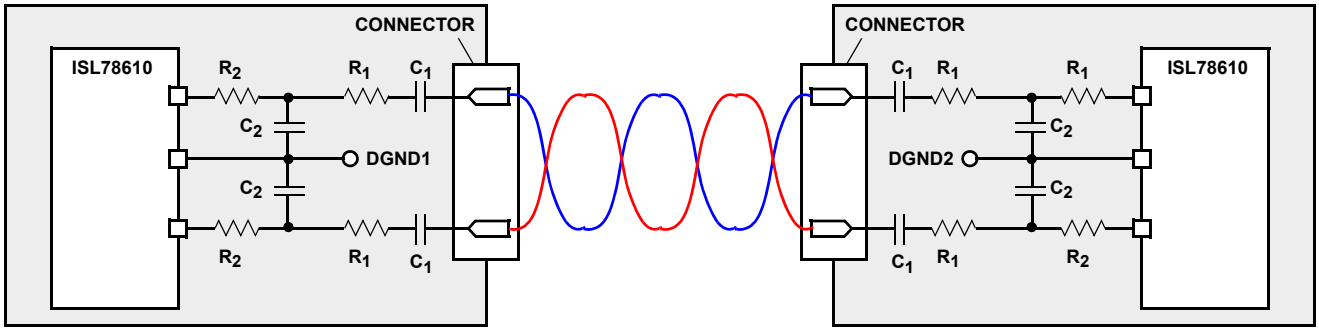


FIGURE 48. ISL78610 DAISY CHAIN CIRCUIT IMPLEMENTATION

TABLE 8. COMPONENT VALUES IN FIGURE 48 FOR VARIOUS DAISY CHAIN DATA RATES

COMPONENT	DAISY CHAIN CLOCK RATES				COMMENTS
	500kHz	250kHz	125kHz	62.5kHz	
C_1	4	220pF	470pF	1nF	2.2nF
C_2	4	150pF (Note)	400pF	960pF	2nF
R_1	4	470Ω	470Ω	470Ω	470Ω
R_2	4	100Ω	100Ω	100Ω	100Ω
Cable Capacitance Range	N/A	0 to 50pF	0 to 100pF	0 to 200pF	0 to 400pF

NOTE: Can be accommodated using two 100pF capacitors in parallel.

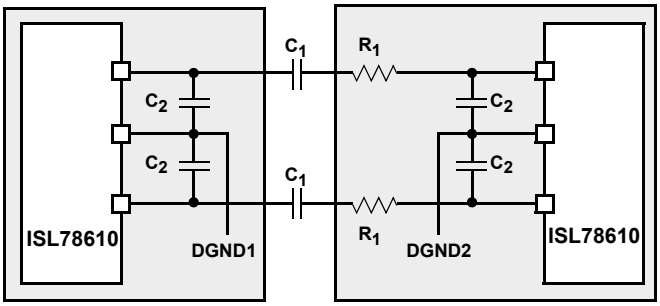


FIGURE 49. ISL78610 DAISY CHAIN – BOARD LEVEL IMPLEMENTATION CIRCUIT

TABLE 9. DAISY CHAIN COMPONENT VALUES FOR BOARD LEVEL IMPLEMENTATION

COMPONENT	QUANTITY (ea.)	TOLERANCE	DAISY CHAIN DATA RATE (kHz)			
			500	250	125	62.5
C_1	2	5%	100pF	220pF	470pF	1nF
C_2	4	5%	150pF	400pF	960pF	2nF
R_1	2		1kΩ	1kΩ	1kΩ	1kΩ

External Inputs

The ISL78610 provides four external inputs for use either as general purpose analog inputs or for NTC type thermistors.

The arrangement of the external inputs is shown in Figure 50 using the ExT4 input as an example. It is important that the components are connected in the sequence shown in Figure 50. For example, C_1 must be connected so the trace from this capacitor's positive terminal connects to R_2 before connecting to R_1. This guarantees the correct operation of the various fault detection functions.

Each of the external inputs has an internal pull-up resistor, which is connected by a switch to the VCC pin whenever the TEMPREG output is active. This arrangement results in an open input being pulled up to the V_{CC} voltage.

Inputs above 15/16 of full scale are registered as open inputs and cause the relevant bit in the Over-Temperature Fault register and the OT bit in the Fault Status register to be set on condition of the respective temperature test enable bit in the Fault Setup register. The user must then read the register value associated with the faulty input to determine if the fault was due to an open input (value above 15/16 full scale) or an over-temperature condition (value below the External Temperature Limit setting).

The function of each of the components in Figure 50 is listed in Table 10 with the diagnostic result of an open or short fault in each component.

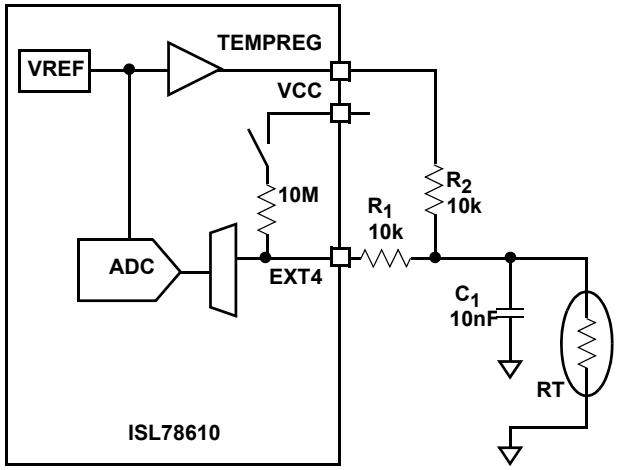


FIGURE 50. CONNECTION OF NTC THERMISTOR TO INPUT EXT4

TABLE 10. COMPONENT FUNCTIONS AND DIAGNOSTIC RESULTS FOR CIRCUIT OF FIGURE 50

COMPONENT	FUNCTION	DIAGNOSTIC RESULT
R_1	Protection from wiring shorts to external HV connections.	Open: Open-wire detection Short: No diagnostic result
R_2	Measurement high-side resistor	Open: Low input level (over-temperature indication) Short: High input level (open-wire indication).
Thermistor		Open: High input level (open-wire indication). Short: Low input level (over-temperature indication)
C_1	Noise Filter. Connects to measurement ground VSS.	Open: No diagnostic result. Short: Low input level (over-temperature indication)

Typical Applications Circuits

Typical applications circuits are shown in Figures 51 to 57. Table 11 on page 38 contains recommended component values. All external (off-board) inputs to the ISL78610 are protected against battery voltage transients by RC filters. They also provide a current limit function during hot plug events. The ISL78610 is calibrated for use with 1kΩ series protection resistors at the cell inputs. V_{BAT} uses a lower value resistor to accommodate the V_{BAT} supply current of the ISL78610. A value of 27Ω is used for this component. As much as possible, the time constant produced by the filtering applied to V_{BAT} should be matched to that applied to the Cell 12 monitoring input. Component values given in Table 11 produce the required matching characteristics.

Figure 51 on page 31 shows the standard arrangement for connecting the ISL78610 to a stack of 12 cells. The cell input filter is designed to maximize EMI suppression. These components should be placed close to the connector with a well controlled ground to minimize noise for the measurement inputs. The balance circuits shown in Figure 51 provide normal cell monitoring when the balance circuit is turned off and a near zero cell voltage reading when the balance circuit is turned on. This is part of the diagnostic function of the ISL78610.

Figure 52 on page 32 shows connections for the daisy chain system, setup pins, power supply, and external voltage inputs for daisy chain devices other than the master (stack bottom) device.

Figure 53 on page 33 shows the daisy chain system, setup pins, microcontroller interface, power supply, and external voltage inputs for the daisy chain master device. Figure 53 is also applicable to stand-alone (non-daisy chain) devices, although in this case, the daisy chain components connected to DHi2 and DLo2 are omitted.

Figure 54 on page 34 shows an alternate arrangement for the battery connections in which the cell input circuits are connected directly to the battery terminal and not through the balance resistor. In this condition, the balance diagnostic function capability is removed.

Operating with Reduced Cell Counts

When using the ISL78610 with fewer than 12 cells, ensure that each used cell has a normal input circuit connection to the top and bottom monitoring inputs for that cell. The simplest way to use the ISL78610 with any number of cells is to always use the full input circuit arrangement for all inputs and short together the unused inputs at the battery terminal. In this way, each cell input sees a normal source impedance independent of whether or not it is monitoring a cell.

The cell balancing components associated with unconnected cell inputs are not required and can be removed. Unused cell balance outputs should be tied to the adjacent cell voltage monitoring pin.

The input circuit component count can be reduced in cases where fewer than 10 cells are being monitored. It is important that cell inputs that are being used are not connected to other (unused) cell inputs as this would affect measurement accuracy. Figures 55, 56, and 57 (starting on page 35) show examples of systems with 10 cells, 8 cells, and 6 cells, respectively.

The component notations and values used in Figures 56 and 57 are the same as those used in Figures 51 to 54.

In Figure 57 the resistor associated with the input filter on VC9 is noted as R_5, rather than R_{5U}. This value change is needed to maintain the correct input network impedance in the absence of the Cell 9 balance circuits.

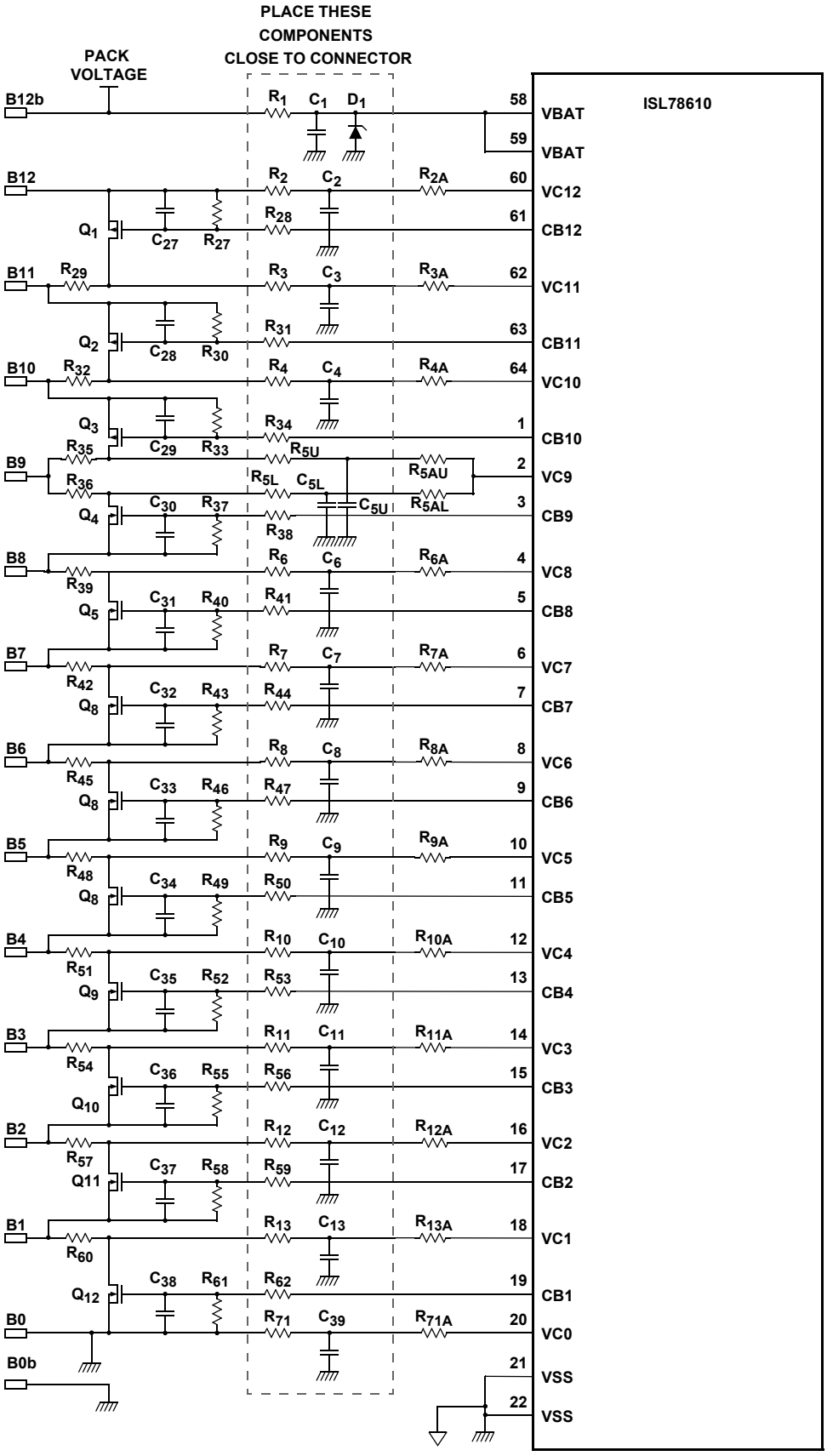


FIGURE 51. TYPICAL APPLICATIONS CIRCUIT – BATTERY CONNECTION CIRCUITS

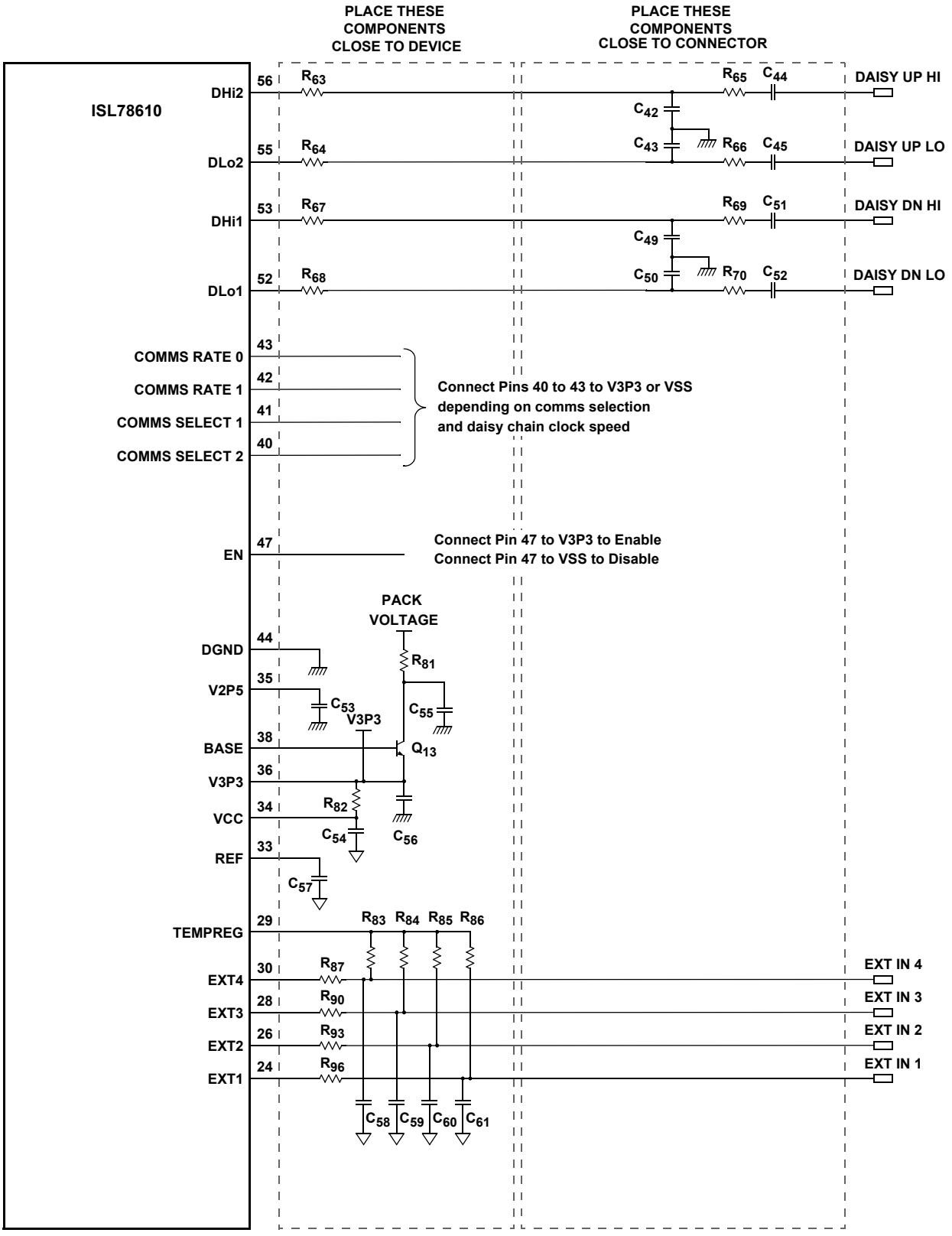


FIGURE 52. TYPICAL APPLICATIONS CIRCUIT – NON BATTERY CONNECTIONS, MIDDLE AND TOP DAISY CHAIN DEVICES

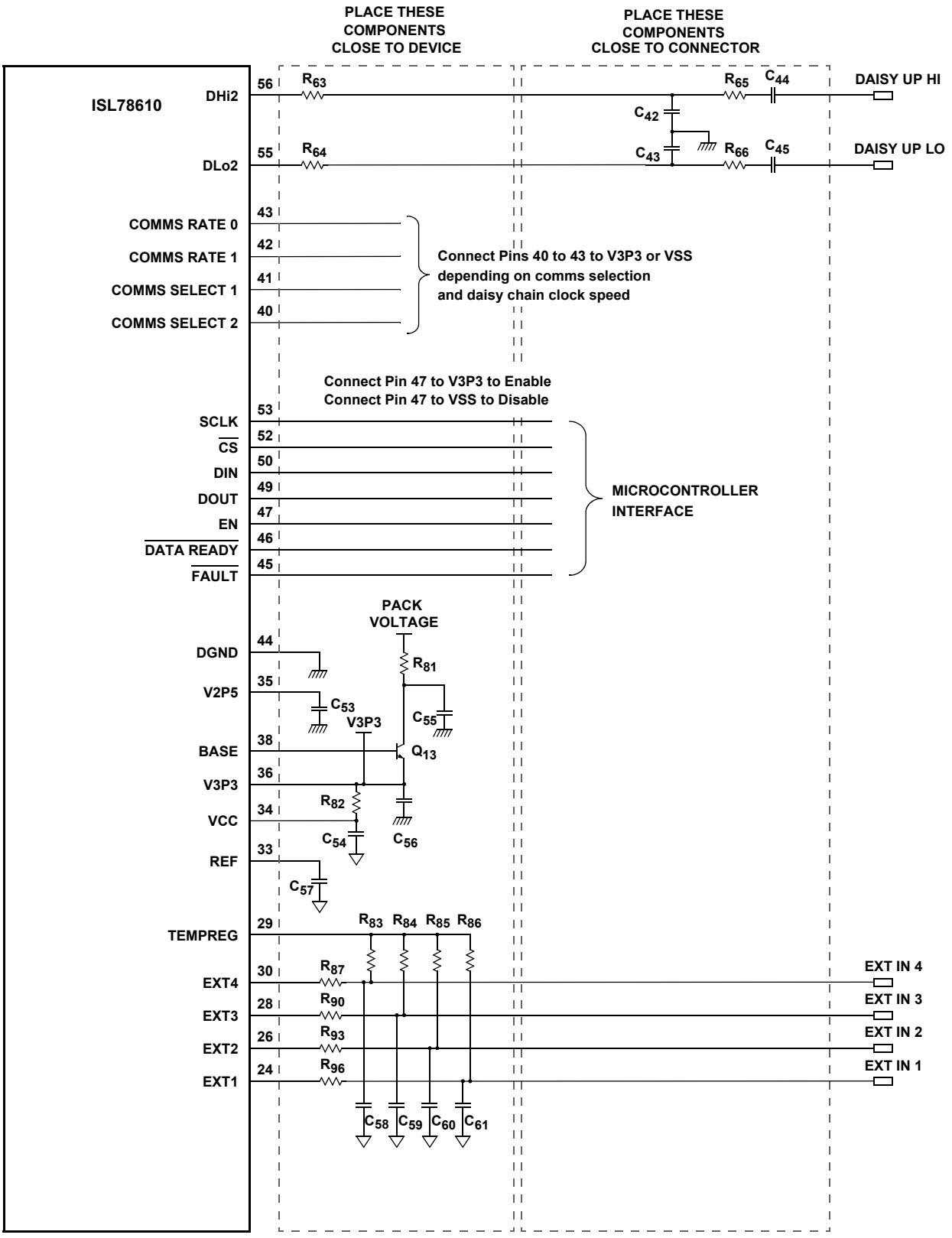


FIGURE 53. TYPICAL APPLICATIONS CIRCUIT – NON BATTERY CONNECTIONS, MASTER DAISY CHAIN DEVICE

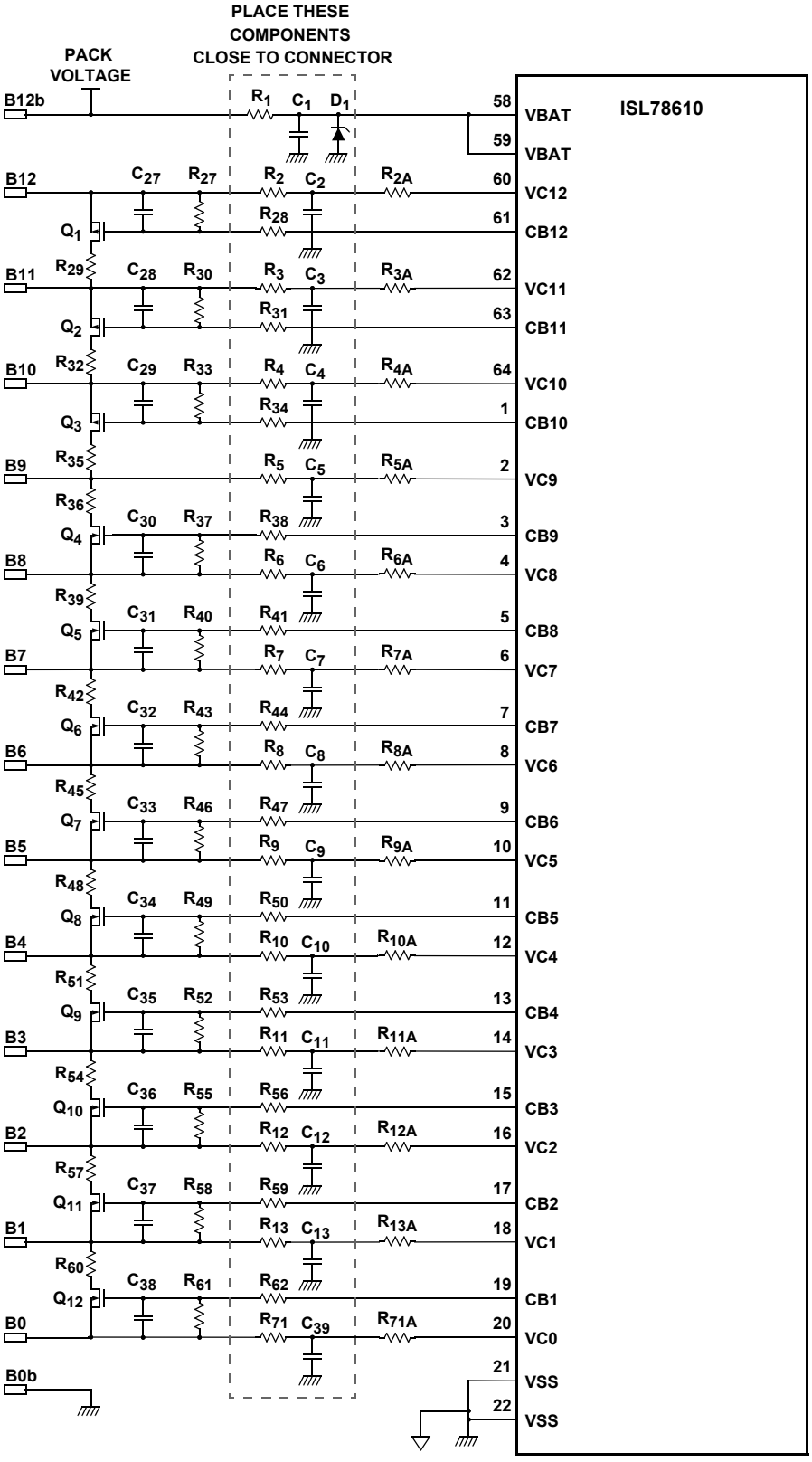


FIGURE 54. TYPICAL APPLICATIONS CIRCUIT – BATTERY CONNECTION CIRCUITS ALTERNATIVE CONFIGURATION

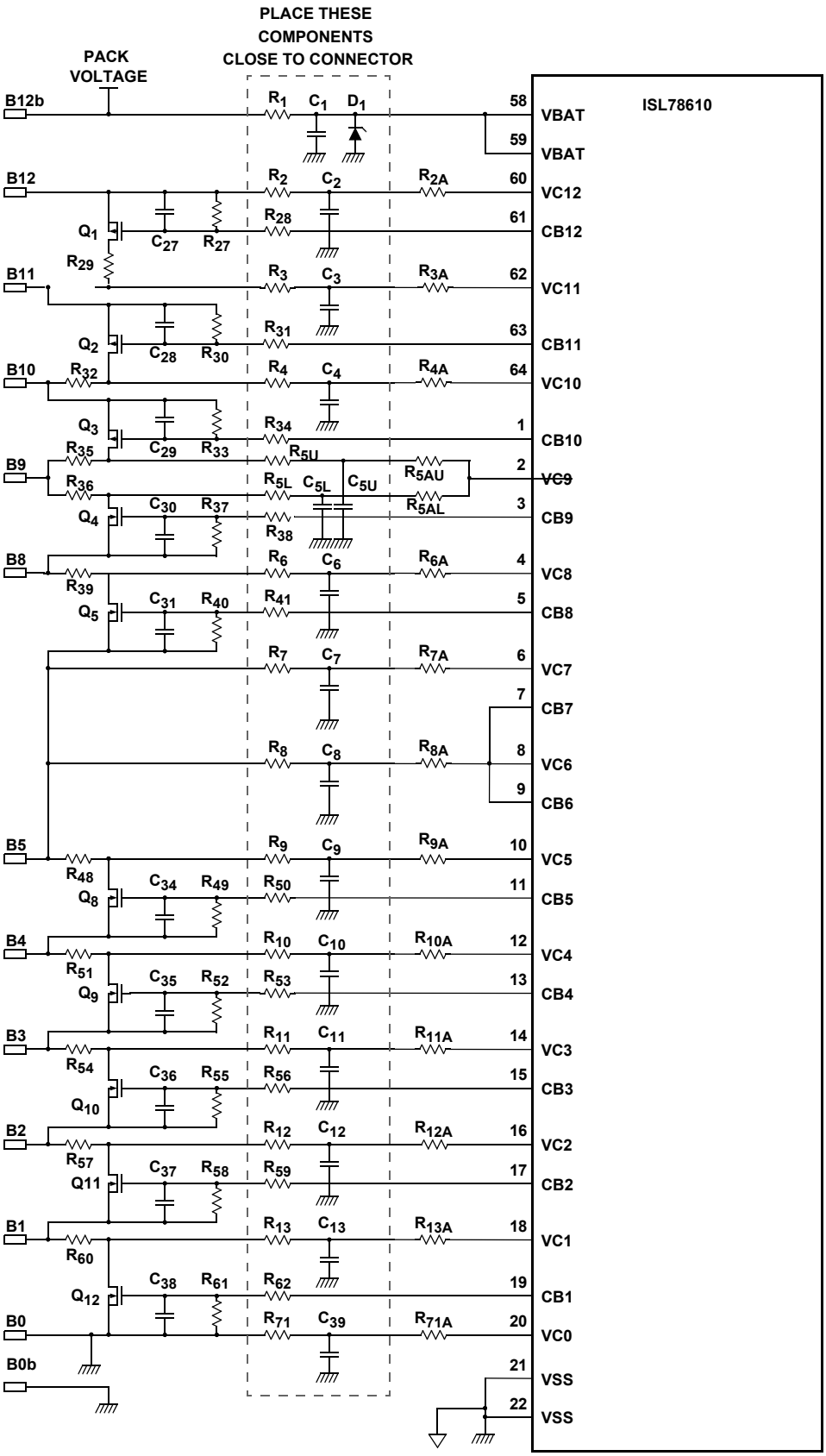


FIGURE 55. TYPICAL APPLICATIONS CIRCUIT – BATTERY CONNECTION CIRCUITS, SYSTEM WITH 10 CELLS

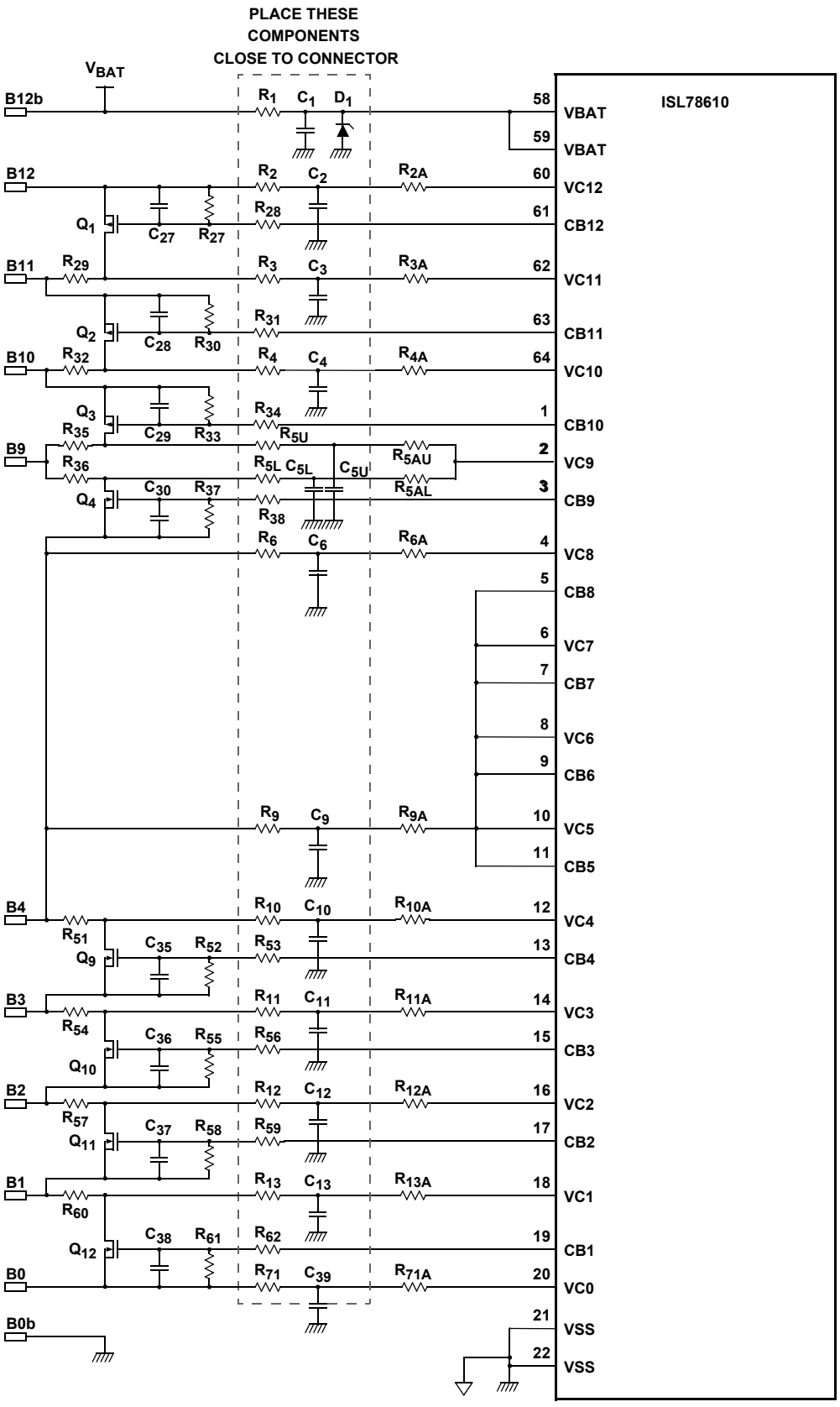


FIGURE 56. TYPICAL APPLICATIONS CIRCUIT – BATTERY CONNECTION CIRCUITS, SYSTEM WITH 8 CELLS

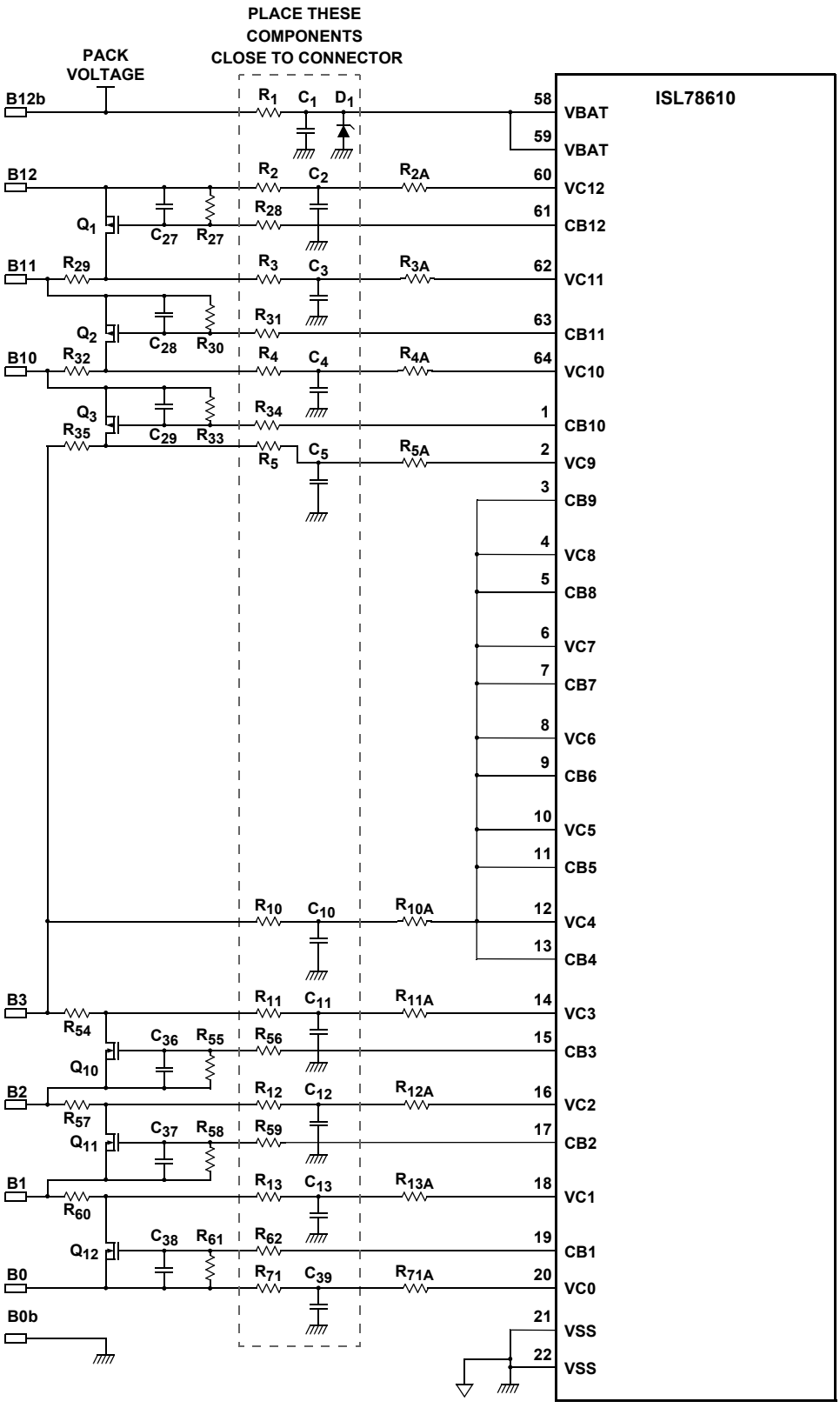


FIGURE 57. TYPICAL APPLICATIONS CIRCUIT – BATTERY CONNECTION CIRCUITS, SYSTEM WITH 6 CELLS

TABLE 11. RECOMMENDED COMPONENT VALUES FOR FIGURES (Figures 51 through 57)

VALUE		COMPONENTS
RESISTORS		
0		R_{101}
27		R_1
33		R_{82}
820		R_2, R_{71}
720	Figure 51 on page 31, Figure 55 on page 35, Figure 56 on page 36	R_3, R_4, R_6, R_7, R_8, R_9, R_{10}, R_{11}, R_{12}, R_{13}
1.54k		R_{5U}, R_{5L}
180		R_{2A}, R_{3A}, R_{4A}, R_{6A}, R_{7A}, R_{8A}, R_{9A}, R_{10A}, R_{11A}, R_{12A}, R_{13A}
360		R_{5AU}, R_{5AL}
910	Figure 54 on page 34	R_3, R_4, R_5, R_6, R_7, R_8, R_9, R_{10}, R_{11}, R_{12}, R_{13}
180		R_{2A}, R_{3A}, R_{4A}, R_{5A}, R_{6A}, R_{7A}, R_{8A}, R_{9A}, R_{10A}, R_{11A}, R_{12A}, R_{13A}
100	1/2W (or larger)	R_{29}, R_{32}, R_{35}, R_{36}, R_{39}, R_{42}, R_{45}, R_{48}, R_{51}, R_{54}, R_{57}, R_{60}
1.3k		R_{81} (assumes minimum pack voltage of 12V and maximum supply current of 6.5mA. Higher current or lower minimum pack voltage requires the use of a smaller resistor)
100		R_{63}, R_{64}, R_{67}, R_{68}
1.4k		R_{5U}, R_{5L}
470		R_{65}, R_{66}, R_{69}, R_{70}
10k		R_{28}, R_{31}, R_{34}, R_{38}, R_{41}, R_{44}, R_{47}, R_{50}, R_{53}, R_{56}, R_{59}, R_{62}, R_{83}, R_{84}, R_{85}, R_{86}, R_{87}, R_{90}, R_{93}, R_{96}, R_{100a}, R_{100b}, R_{100c}, R_{100d}
330k		R_{27}, R_{30}, R_{33}, R_{37}, R_{40}, R_{43}, R_{46}, R_{49}, R_{52}, R_{55}, R_{58}, R_{61}
CAPACITORS		
VALUE	**VOLTAGE**	**COMPONENTS**
200p	100	C_{42}, C_{43}, C_{49}, C_{50}
220p	500	C_{44}, C_{45}, C_{51}, C_{52}
10n	50	C_{27}, C_{28}, C_{29}, C_{30}, C_{31}, C_{32}, C_{33}, C_{34}, C_{35}, C_{36}, C_{37}, C_{38}, C_{58}, C_{59}, C_{60}, C_{61}
22n	100	C_2, C_3, C_4, C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{39}
220n	100	C_1
1µ	10	C_{53}, C_{54}, C_{56}
1µ	100	C_{55}
2.2µ	10	C_{57}
ZENER DIODES		
VALUE	**EXAMPLE**	**COMPONENTS**
54V	PTVS54VS1UTR	D_1 - DIODE-TVS, SMD, 2P, SOD-123W, 54VWM, 87.1VC

Notes on Board Layout

Referring to Figure 51 on page 31 (battery connection circuits), the basic input filter structure is composed of resistors R_2 to R_{13}, R_{71}, and capacitors C_2 to C_{13} and C_{39}. These components provide protection against transients and EMI for the cell inputs. They carry the loop currents produced by EMI and should be placed as close to the connector as possible. The ground terminals of the capacitors must be connected directly to a solid ground plane. Do not use vias to connect these capacitors to the input signal path or to ground. Place any vias in line to the signal inputs so that the inductance of these forms a low pass filter with the grounded capacitors.

Referring to Figure 52 on page 32, the daisy chain components are shown to the top right of the drawing. These are split into two sections. Components to the right of this section should be placed close to the board connector with the ground terminals of capacitors connected directly to a solid ground plane. This is the same ground plane that serves the cell inputs. Components to the left of this section should be placed as close to the device as possible.

The battery connector and daisy chain connectors should be placed closely to each other on the same edge of the board to minimize any loop current area.

Two grounds are identified on the circuit diagram. These are nominally referred to as noisy and quiet grounds. The noisy ground, denoted by an “earth” symbol, carries the EMI loop currents and digital ground currents. The quiet ground defines the decoupling voltage for voltage reference and the analog power supply rail. Join the quiet and noisy grounds at the VSS pin. Keep the quiet ground area as small as possible.

The circuits shown to the bottom right of Figure 52 on page 32 provide signal conditioning and EMI protection for the external temperature inputs. These inputs are designed to operate with external NTC thermistors.

Each of the external inputs has an internal pull-up resistor, which is connected by a switch to the VCC pin whenever the TEMPREG output is active. This arrangement results in an open input being pulled up to the V_{CC} voltage.

Component Selection

Certain failures associated with external components can lead to unsafe conditions in electronic modules. A good example of this is a component that is connected between high energy signal sources failing short. Such a condition can easily lead to the component overheating and damaging the board and other components in its proximity.

One area to consider with the external circuits on the ISL78610 is the capacitors connected to the cell monitoring inputs. These capacitors are normally protected by the series protection resistors but can be a safety hazard in the event of a dual point fault in which both the capacitor and associated series resistor fail short. Also, a short in one of these capacitors would dissipate the charge in the battery cell if left uncorrected for an extended period of time. Renesas recommends selecting capacitors C_1 to C_{13} to be “fail safe” or “open mode” types. An alternative strategy is to replace each of these capacitors with two devices in series, each with double the value of the single capacitor.

A dual point failure in the balancing resistor (R_{29}, R_{32}, R_{35}, etc.) of Figure 51 on page 31 and associated balancing MOSFET (Q_1 to Q_{12}) can also cause a shorted cell condition. Renesas recommends replacing the balancing resistor with two resistors in series.

Board Level Calibration

For best accuracy, the ISL78610 can be recalibrated after soldering to a board using a simple resistor trim. The adjustment method involves obtaining the average cell reading error for the cell inputs at a single temperature and cell voltage value and applying a select-on-test resistor to zero the average cell reading error.

The adjustment system uses a resistor placed either between VDDEXT and V_{REF} or V_{REF}, and VSS as shown in Figure 58. The value of resistor R_1 or R_2 is then selected based on the average error measured on all cells at 3.3V per cell and room temperature; for example, with 3.3V on each cell input, scan the voltage values using the ISL78610 and record the average reading error (ISL78610 reading – cell voltage value). Table 12 shows the value of R_1 and R_2 required for various measured errors.

To use Table 12, find the measured error value closest to the result obtained with measurements using the ISL78610 and select the corresponding resistor value. For finer adjustment resolution, this value can be obtained by interpolation using Table 12.

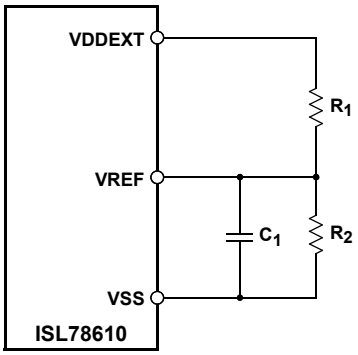


FIGURE 58. CELL READING ACCURACY ADJUSTMENT SYSTEM

TABLE 12. COMPONENT VALUES FOR ACCURACY CALIBRATION ADJUSTMENT OF FIGURE 58

MEASURED ERROR AT VC = 3.3V $V_{78610} - V_{CELL}$ (mV)	R_1 (kΩ)	R_2 (kΩ)
4	205	DNP
3	274	DNP
2	412	DNP
1	825	DNP
0	DNP	DNP
-1	DNP	2550
-2	DNP	1270
-3	DNP	866
-4	DNP	649

DNP = Do Not Populate

System Commands

The ISL78610 has a series of commands available to the host microcontroller to control operation of the ISL78610 system, to read and write data to any individual device, and to check system status. These following sections describe each commands, along with the commands' characteristics.

The attributes associated with each command are: the device response, whether the command can address all devices with a single command, and whether there is a response from the target device.

Device Response

In a stand-alone configuration, the host should only expect a response when reading data from a register. In all other cases, no response is expected.

In a daisy chain configuration, all commands except any Scan, Measure, Sleep, Wake, and Reset commands require a response from either the stack top device or the target device (see Table 13). Each device in the stack waits for a response from the stack device above. Correct receipt of a command is indicated by the correct response. Failure to receive a response within a timeout period indicates a communications fault. The timeout value is stack position dependent. The device that detects the fault then transmits the Communications Failure response, which includes its stack address.

The host microcontroller should build in handlers for commands that might be delayed within the communication structure and look for a Communications Failure response if the wait time expires. For more detail, see "Communication Faults" on page 75.

An Acknowledge (ACK) response indicates that the command was successfully received by the target device. A Not Acknowledged (NAK) indicates an error in decoding the command.

Address All

Address All is used only in a daisy chain configuration. To address a particular device, the host microcontroller specifies the address of that device (1 through 14) for each of the maximum of 14 devices. To address all devices in a daisy chain stack, the host microcontroller uses an address of 15 (Hex '1111') to cause all stack devices to perform functions simultaneously. Only some commands recognize Address All.

Read and Write Commands

Read and Write commands are the primary communication mechanisms in the ISL78610 system. All commands use the read and write operations. Refer to "Communications" on page 52 for a detailed description of these operations' protocols, timing, and interactions.

Table 13 describes the commands and how they control the system.

TABLE 13. COMMAND ATTRIBUTES

COMMAND	VALID IN STAND-ALONE OR DAISY CHAIN	NORMAL DEVICE RESPONSE			DEVICE WAITS FOR A RESPONSE? (Daisy Chain Only)	"ADDRESS ALL" COMPATIBLE (Daisy Chain Only)
		STAND-ALONE	TOP	TARGET		
Read	Both	Data	ACK	Data	Yes	No
Write	Both	-	ACK	ACK	Yes	No
Scan Voltages	Both	-	-	-	No	Yes
Scan Temperatures	Both	-	-	-	No	Yes
Scan Mixed	Both	-	-	-	No	Yes
Scan Wires	Both	-	-	-	No	Yes
Scan All	Both	-	-	-	No	Yes
Scan Continuous	Both	-	ACK	ACK	Yes	Yes
Scan Inhibit	Both	-	ACK	ACK	Yes	Yes
Sleep	Both	-	ACK	NAK	No	Yes
Wake-up	Both	-	ACK	NAK	No	Yes
Balance Enable	Both	-	ACK	ACK	Yes	Yes
Balance Inhibit	Both	-	ACK	ACK	Yes	Yes
Measure	Both	-	-	-	No	No
Identify (special command)	Daisy chain only	-	ACK	NAK	No	Special address
NAK	Daisy chain only	-	ACK	ACK	Yes	No
ACK	Daisy chain only	-	ACK	ACK	Yes	No
Reset	Both	-	-	-	No	No
Calculate Register Checksum	Both	-	ACK	ACK	Yes	No
Check Register Checksum	Both	-	ACK	ACK	Yes	No

Scan Voltages Command

When a device receives the Scan Voltages command to its stack address (or an Address All stack address), it increments the scan counter (see "Scan Counter" on page 43) and begins a scan of the cell voltage inputs. It sequences through the cell voltage inputs in order from Cell 12 (top) to Cell 1 (bottom). This operation is followed by a scan of the Pack Voltage.

The scan operation forces a sample and hold on each input, an analog-to-digital conversion of the voltage, and the storage of the value in its appropriate register. The IC temperature is also recorded for use with the internal calibration routines.

The Scan Voltages command performs cell overvoltage and undervoltage comparisons on each cell input and checks the VBAT and VSS connections for open-wire at the end of the scan. If a fault condition is present (see "Fault Diagnostics" on page 77 for what constitutes a fault condition), the device sets the specific fault bit, sets the device $\overline{\text{FAULT}}$ pin active, and sends an "unprompted fault response" to the host down the daisy chain communication link (a stand-alone device sets the $\overline{\text{FAULT}}$ pin only). The Unprompted Response is identical to a "Read Status Register" command.

Devices revert to the Standby state on completion of the scan activity.

Cell voltage, Pack voltage data, and any fault conditions are stored in local memory ready for reading by the system host microcontroller.

Scan Temperatures Command

When a device receives the Scan Temperatures command to its stack address (or an Address All stack address), it increments the scan counter (see "Scan Counter" on page 43) and begins a scan of the temperature inputs.

The Scan Temperatures command causes the addressed device (or all devices with an Address All stack address) to scan through the internal and four external temperature signals followed by multiplexer loopback and reference measurements. The loopback and reference measurements are part of the internal diagnostics function. Over-temperature compares are performed on each temperature measurement depending on the condition of the appropriate bit in the Fault Setup register.

Temperature data and any fault conditions are stored in local memory ready for reading by the system host microcontroller. If is a fault condition is present, the device sets its $\overline{\text{FAULT}}$ pin active and sends an "unprompted fault response" to the host down the daisy chain communication link on completion of a scan (a stand-alone device sets the $\overline{\text{FAULT}}$ pin only). The Unprompted Response is identical to a "Read Status Register" command.

Devices revert to the Standby state on completion of the scan activity.

See "Temperature Monitoring Operation" on page 43 for more information.

Scan Mixed Command

When a device receives the Scan Mixed command to its stack address (or an Address All stack address), it increments the Scan counter (see "Scan Counter" on page 43) and begins a Scan Mixed operation.

The Scan Mixed command causes the addressed device (or all devices with an Address All stack address) to scan through the cell voltage inputs in order from Cell 12 (top) to Cell 7. Then the external input ExT1 is measured, followed by a scan of Cell 6 to Cell 1. These operations are followed by a scan of the Pack Voltage and the IC temperature. The IC temperature is recorded for use with the internal calibration routines.

The Scan Mixed command also performs cell overvoltage and undervoltage comparisons on each cell voltage sampled. The VBAT and VSS pins are also checked for open conditions at the end of the scan.

ExT1 is sampled in the middle of the cell voltage scan so that half the cells are sampled before ExT1 and half after ExT1. This mode allows ExT1 to be used for an external voltage measurement, such as a current sensing, so it is performed with the cell voltage measurements, reducing the latency between measurements.

The Scan Mixed command is intended for use in stand-alone systems, or by the master device in stacked applications, and typically measures a single system parameter, such as battery current or Pack voltage.

Cell voltage, Pack voltage, ExT1 data, and any fault conditions are stored in local memory ready for reading by the system host microcontroller. Access the data from the ExT1 measurement by a direct Read ET1 Voltage command or by the All Temperatures read command.

If a fault condition is present, (see "Fault Diagnostics" on page 77 for what constitutes a fault condition), the device sets the $\overline{\text{FAULT}}$ pin active and sends an "unprompted fault response" to the host down the daisy chain communication link on completion of a scan (a stand-alone device sets the $\overline{\text{FAULT}}$ pin only). The unprompted response is identical to a "Read Status Register" command.

Devices revert to the Standby state on completion of the scan activity.

Scan Wires Command

When a device receives the Scan Wires command to its stack address (or an Address All stack address), it increments the Scan counter (see "Scan Counter" on page 43) and begins a Scan Wires operation.

The Scan Wires command causes the addressed device (or all devices with an Address All stack address) to measure all the VCn pin voltages while applying load currents to each input pin in turn. This is part of the fault detection system.

If is a fault condition is present, the device sets the $\overline{\text{FAULT}}$ pin and returns a fault signal (sent down the stack) on completion of a scan.

No cell voltage data is sent as a result of the Scan Wires command. Devices revert to the standby state on completion of this activity.

Scan All Command

When a device receives the Scan All command to its stack address (or an Address All stack address), it increments the Scan counter (see "Scan Counter" on page 43) and begins a Scan All operation.

The Scan All command causes the addressed device (or all devices with an Address All stack address) to execute the Scan Voltages, Scan Wires, and Scan Temperatures commands in sequence one time (see Figure 59 on page 44 for example timing).

Scan Continuous Command

Scan Continuous mode is used primarily for fault monitoring and incorporates the Scan Voltages, Scan Temperatures, and Scan Wires commands. See "Temperature Monitoring Operation" on page 43 for more information.

The Scan Continuous command causes the addressed device (or all devices with an Address All stack address) to set the SCAN bit in the Device Setup register and performs a succession of scans at a predetermined scan rate. Each device operates asynchronously on its own clock. This is similar to the Scan All command except that the scans are repeated at intervals determined by the SCN0-3 bits in the Fault Setup register.

The ISL78610 provides an option that pauses cell balancing activity while measuring cell voltages in Scan Continuous mode. This is controlled by the BDDS bit in the Device Setup register. If BDDS is set, cell balancing is inhibited during cell voltage measurement and for 10ms before the cell voltages are scanned. Balancing is re-enabled at the end of the scan to allow balancing to continue. This function applies during the Scan Continuous and while either the Timed or Auto Balance functions are active. This "BDDS" action allows the implementation of a circuit arrangement that can be used to diagnose the condition of external balancing components. See "Cell Voltage Measurements during Balancing" on page 26. During Manual Balance this external circuit arrangement does not allow Scan Continuous without generating a fault condition. It is up to the host microcontroller to stop balancing functions when performing a Scan or Measure command, as BDDS only works in conjunction with Scan Continuous.

The Scan Continuous scan interval is set using the SCN3:0 bits (lower nibble of the Fault Setup register.) The temperature and wire scans occur at slower rates and depend on the value of the scan interval selected. The scan system is synchronized so that the wire and temperature scans always follow a voltage scan. The three scan sequences, depending on the scans required at a particular instance, are as follows:

- Scan Voltages
- Scan Voltages, Scan Wires
- Scan Voltages, Scan Wires, Scan Temperatures

The temperature and wire scans occur at 1/5 the voltage scan rate for voltage scan intervals above 128ms. Below this value, the temperature scan interval is fixed at 512ms.

The behavior of the wire scan interval is determined by the WSCN bit in the Fault Setup register. A bit value of '1' causes the wire scan to be performed at the same rate as the temperature scan. A bit value of '0' causes the wire scan rate to track the voltage scan rate for voltage scan intervals above 512ms. The wire scan is performed at a fixed 512ms rate at and below this value. Table 14 shows the various scan rate combinations available.

Data is not automatically returned while devices are in Scan Continuous mode except when a fault condition is detected. The results of voltage and temperature scans are stored in local volatile memory and can be accessed at any time by the system host microcontroller. However, because the scan continuous operation is running asynchronously to any communications, Renesas recommends stopping the continuous scan before reading the registers.

Devices can be operated in Scan Continuous mode while in Normal mode or in Sleep mode. Devices revert to Sleep mode or remain in Normal mode as applicable on completion of each scan.

The response to a detected fault condition is to send the Fault signal, either immediately in the case of stand-alone devices or daisy chain devices in Normal mode, or following transmission of the Wake-up signal if the device is being used in a daisy chain configuration and is in Sleep mode.

To operate the "Scan Continuous" function in Sleep mode, the host microcontroller configures the ISL78610, starts Scan Continuous mode, and sends the Sleep command. The ISL78610 then wakes itself up each time a scan is required. Note that for the fastest scan settings (scan interval codes 0000, 0001, and 0010) the main measurement functions do not power down between scans because the ISL78610 remains in Normal mode.

TABLE 14. SCAN CONTINUOUS TIMING MODES

SCAN INTERVAL SCN3:0	SCAN INTERVAL (ms)	TEMP SCAN (ms)	WIRE SCAN WSCN = 0 (ms)	WIRE SCAN WSCN = 1 (ms)
0000	16	512	512	512
0001	32	512	512	512
0010	64	512	512	512
0011	128	512	512	512
0100	256	1024	512	1024
0101	512	2048	512	2048
0110	1024	4096	1024	4096
0111	2048	8192	2048	8192
1000	4096	16384	4096	16384
1001	8192	32768	8192	32768
1010	16384	65536	16384	65536
1011	32768	131072	32768	131072
1100	65536	262144	65536	262144

Scan Inhibit Command

The Scan Inhibit command stops a Continuous scan (that is, receipt of the command by the target device resets the SCAN bit and stops the Scan Continuous function).

Measure Command

When a device receives the Measure command to its stack address, it increments the scan counter (see "Scan Counter" on page 43) and begins a Measure operation.

This command initiates the voltage measurement of a single cell voltage, internal temperature, any of the four external temperature inputs, or the secondary voltage reference. The command incorporates a 6-bit suffix that contains the address of the required measurement element. See Table 15 on page 43 and Figure 64B on page 55.

The device matching the target address responds by conducting the single measurement and loading the result to local memory. The host microcontroller then reads from the target device to obtain the measurement result. All devices revert to the Standby state on completion of this activity.

TABLE 15. MEASURE COMMAND TARGET ELEMENT ADDRESSES

MEASURE COMMAND (SUFFIX)	DESCRIPTION
6'h00	V_{BAT} Voltage
6'h01	Cell 1 Voltage
6'h02	Cell 2 Voltage
6'h03	Cell 3 Voltage
6'h04	Cell 4 Voltage
6'h05	Cell 5 Voltage
6'h06	Cell 6 Voltage
6'h07	Cell 7 Voltage
6'h08	Cell 8 Voltage
6'h09	Cell 9 Voltage
6'h0A	Cell 10 Voltage
6'h0B	Cell 11 Voltage
6'h0C	Cell 12 Voltage
6'h10	Internal temperature reading
6'h11	External temperature Input 1 reading
6'h12	External temperature Input 2 reading
6'h13	External temperature Input 3 reading
6'h14	External temperature Input 4 reading
6'h15	Reference voltage (raw ADC) value. Use this value to calculate corrected reference voltage using reference coefficient data

Scan Counter

Because the Scan and Measure commands do not have a response, the scan counter is provided to allow confirmation of receipt of the Scan and Measure commands. This 4-bit counter located in the Scan Count register (Page 1, address 6'h16) increments each time a Scan or Measure command is received. This allows the host microcontroller to compare the counter value before and after the Scan or Measure command was sent to verify receipt. The counter wraps to zero when overflowed.

The scan counter increments whenever the ISL78610 receives a Scan or Measure command. The ISL78610 does not perform a requested Scan or Measure function if a Scan or Measure function is already in progress, but it still increments the scan counter.

Temperature Monitoring Operation

One internal and four external temperature inputs are provided together with a switched bias voltage output (TEMPREG, pin 29). The voltage at the TEMPREG output is nominally equal to the ADC reference voltage so that the external voltage measurements are ratiometric to the ADC reference (see Figure 50 on page 29).

The temperature inputs are intended for use with external resistor networks using NTC type thermistor sense elements but can also be used as general purpose analog inputs. Each temperature input is applied to the ADC through a multiplexer. The ISL78610 converts the voltage at each input and loads the 14-bit result to the appropriate register.

The TEMPREG output is turned "on" in response to a Scan Temperatures or Measure Temperature command. A dwell time of 2.5ms is provided to allow external circuits to settle, after which the ADC measures each external input in turn. The TEMPREG output turns "off" after measurements are completed.

Figure 59 on page 44 shows an example temperature scan with the ISL78610 operating in Scan Continuous mode with a scan interval of 512ms. The preceding voltage and wire scans are shown for comparison.

The external temperature inputs are designed so that an open connection results in the input being pulled up to the full scale input level. This function is provided by a switched 10MΩ pull-up from each input to VCC. This feature is part of the fault detection system and is used to detect open pins.

The internal IC temperature, Auxiliary Reference Voltage, and multiplexer loopback signals are sampled in sequence with the external signals using the Scan Temperatures command.

The converted value from each temperature input is also compared to the external over-temperature limit and open connection threshold values on condition of the [TST4:1] bits in the Fault Setup register (see "Fault Setup:" on page 86.) If a TSTn bit is set to "1", the temperature value is compared to the External Temperature threshold and a Fault occurs if the measured value is lower than the threshold value. If a TSTn bit is set to "0", then the temperature measurement is not compared to the threshold value and no fault occurs. The [TST4:1] bits are "0" by default.

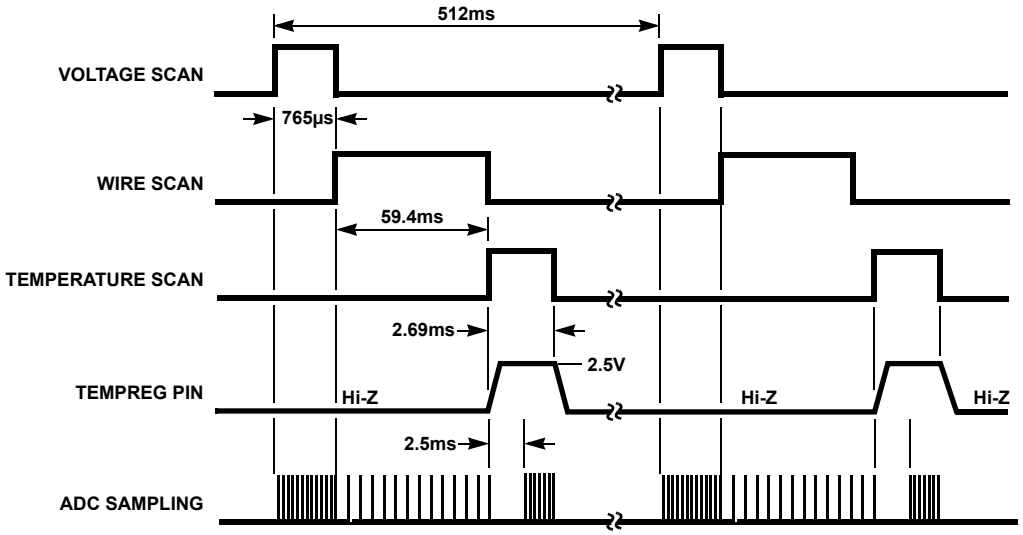


FIGURE 59. SCAN TIMING EXAMPLE DURING SCAN CONTINUOUS MODE AND SCAN ALL MODE

Sleep Command

Sleep mode is entered in response to a Sleep command. Only the communications input circuits, low speed oscillator, and internal registers are active in Sleep mode, allowing the part to perform timed scan and balancing activity and to wake up in response to communications.

Using a Sleep command does not require that the devices in a daisy chain stack be identified first. They do not need to know their position in the stack.

In a daisy chain system, the Sleep command must be written using the Address All stack address. The command is not recognized if sent with an individual device address and causes the addressed device to respond NAK. The top stack device responds ACK on receiving a valid Sleep command.

After receiving a valid Sleep command, the devices wait before entering Sleep mode. This is to allow time for the top stack device in a daisy chain to respond ACK, or for all devices that do not recognize the command to respond NAK, and for the host microcontroller to respond with another command. Receipt of any valid communications on Port 1 of the ISL78610 before the wait period expires cancels the Sleep command. Receipt of another Sleep command restarts the wait timers. Table 16 provides the maximum wait time for various daisy chain data rates. The communications fault checking timeout is not applied to the Sleep command. A problem with the communications is indicated by a lack of response to the host microcontroller. The host microcontroller may choose to do nothing if no response is received, in which case devices that received the Sleep command go to sleep when the wait time expires. Devices that do not receive the message go to sleep when their watchdog timer expires (if this is enabled).

Devices exit Sleep mode on receipt of a valid Wake-up command.

TABLE 16. MAXIMUM WAIT TIME FOR DEVICES ENTERING SLEEP MODE

	MAXIMUM WAIT TIME FROM TRANSMISSION OF SLEEP COMMAND (DAISY CHAIN ONLY)			
DAISY CHAIN DATA RATE (kHz)	500	250	125	62.5
Time to Enter Sleep mode (µs)	500	1000	2000	4000

Wake-Up Command

The communications pins are monitored when the device is in Sleep mode, allowing the part to respond to communications.

The host microcontroller wakes up a sleeping device, or a stack of sleeping devices, by sending the Wake-up command to a stand-alone or a master stack device. In a daisy chain configuration, the Wake-up command must be written using the Address All stack address. The command is not recognized if sent with an individual device address and causes the master device to respond NAK.

Using a Wake-up command does not require that the devices in a stack be identified first. They do not need to know their position in the stack.

The master exits Sleep mode on receipt of a valid Wake-up command and transmits the Wake-up signal to the next device in the stack. The Wake-up signal is a few cycles of a 4kHz clock. Each device in the chain wakes up on receipt of the Wake-up signal and sends the signal to the next device.

Any communications received on Port 1 by a device that is transmitting the Wake-up signal on Port 2 are ignored.

The top stack device, after waking up, waits for some time before sending an ACK response to the master. This wait time is necessary to allow receipt of the Wake-up signal being originated by a stack device other than the master. See "Fault Response in Sleep Mode" on page 77 for more information.

The master device passes the ACK on to the host microcontroller to complete the Wake-up sequence. The total time required to wake up a complete stack of devices is dependent on the number of devices in the stack. Table 17 gives the maximum time from Wake-up command transmission to receipt of ACK response ($\overline{\text{DATA READY}}$ asserted low) for stacks of 8 and 14 devices at various daisy chain data rates (interpolate linearly for different number of devices).

TABLE 17. MAXIMUM WAKE-UP TIMES FOR STACKS OF 8 DEVICES AND 14 DEVICES (WAKE-UP COMMAND TO ACK RESPONSE)

	MAXIMUM WAKE-UP TIMES			
DAISY CHAIN DATA RATE (kHz)	500	250	125	62.5
Stack of 8 Devices (ms)	63	63	63	63
Stack of 14 Devices (ms)	100	100	100	100

There is no additional checking for communications faults while devices are waking up. A communications fault is indicated by the host microcontroller not receiving an ACK response within the expected time.

Reset Command

All digital registers can be reset to their power-up condition using the Reset Command.

Daisy chain devices must be reset in sequence from the stack top device to the stack bottom (master) device. Sending the Reset command to all devices using the Address All stack address has no effect. There is no response from the stack when sending a Reset command.

All stack address and stack size information is set to zero in response to a Reset command. When all devices have been reset it is necessary to reprogram the stack address and stack size information using the Identify command.

A Reset command should be issued following a “hard reset” in which the EN pin is toggled.

Balance Enable Command

The Balance Enable command sets the BEN bit, which starts the balancing operation. However, before this command becomes operational and before balancing can commence, the balance operation needs to be specified. See “Cell Balancing Functions”.

The Balance Enable command can be sent to all devices with one command using Address All addressing.

Balance Inhibit Command

The Balance Inhibit command clears the BEN bit, which stops the balancing operation. The Balance Inhibit command can be sent to all devices with one command using Address All addressing.

CELL BALANCING FUNCTIONS

Cell balancing is performed using external MOSFETs and external current balancing resistors (see Figure 51 on page 31). Each MOSFET is controlled independently by the CB1 to CB12 pins of the ISL78610. The CB1 to CB12 outputs are controlled either directly, or indirectly by an external microcontroller through bits in various control registers.

The three cell balance modes are Manual, Timed, and Auto.

TABLE 18. REGISTERS CONTROLLING BALANCE

REGISTER	BALANCE MODE	REFERENCE
Balance Setup	Manual, Timed, Auto	Table 19 on page 46
Balance Status	Manual, Timed, Auto	Table 19 on page 46
Watchdog/Balance Time	Timed, Auto	Table 21 on page 47
Device Setup	Timed, Auto	“Set-Up Registers” on page 88
Balance Value	Auto only	Table 22 on page 49

BALANCE MODE

Set the Balance mode with the BMD1 and BMD0 bits in the Balance Setup Register (see Table 19).

In Manual mode, the host microcontroller directly controls the state of each MOSFET output.

In Timed mode, the host microcontroller programs a balance duration value and selects which cells are to be balanced, then starts the balance operation. The ISL78610 turns all the FETs off when the balance duration has been reached.

In Auto Balance mode, the host microcontroller programs the ISL78610 to control the balance MOSFETs to remove a programmed “charge delta” value from each cell. The ISL78610 does this by controlling the amount of charge removed from each cell over a number of cycles, rather than trying to balance all cells to a specific voltage.

BALANCE WAIT TIME

The balance wait time is the interval between balancing operations in Auto Balance mode (see Table 19).

BALANCE ENABLE

When all of the other balance control bits are properly set, setting the balance Enable bit to “1” starts the balance operation. The BEN bit can be set by writing directly to the Balance Setup register or by sending a Balance Enable command. See Table 19.

TABLE 19. BALANCE SETUP REGISTER

REGISTER BITS													
9		8	7	6	5		4	3	2		1	0	
BEN	BALANCE	BSP3	BSP2	BSP1	BSP0	POINT TO REGISTER	BWT2	BWT1	BWT0	SECONDS BETWEEN BALANCE CYCLES	BMD1	BMD0	BALANCE MODE
0	Off	0	0	0	0	Balance Status 0 12 11 10 9 8 7 6 5 4 3 2 1 Set bit to 1 to enable balance	0	0	0	0	0	0	Off
1	On	0	0	0	1	Balance Status 1	0	0	1	1	0	1	Manual
		0	0	1	0	Balance Status 2	0	1	0	2	1	0	Timed
		0	0	1	1	Balance Status 3	0	1	1	4	1	1	Auto
		0	1	0	0	Balance Status 4	1	0	0	8			
		0	1	0	1	Balance Status 5	1	0	1	16			
		0	1	1	0	Balance Status 6	1	1	0	32			
		0	1	1	1	Balance Status 7	1	1	1	64			
		1	0	0	0	Balance Status 8							
		1	0	0	1	Balance Status 9							
		1	0	1	0	Balance Status 10							
		1	0	1	1	Balance Status 11							
		1	1	0	0	Balance Status 12							

Manual/Timed

Auto Balance Mode Only

BALANCE STATUS POINTER

The Balance Status register is a “multiple instance” register (see “Balance Status Register” on page 46. There are 13 locations within this register and only one location can be accessed at a time. The Balance Status Pointer points to one of these 13 locations (see Table 19).

Manual Balance mode and Timed Balance mode requires a balance status pointer value of ‘0’. In this case, the bits in the Balance Status Register directly select the cells to be balanced.

The Auto Balance mode uses Balance Status register locations 1 to 12 (see Table 19). In Auto Balance mode, the ISL78610 increments the Balance Status pointer on each auto balance cycle to step through Balance Status register locations 1 to 12. This allows the programming of up to twelve different balance profiles for each Auto Balance operation. When the operation encounters a zero value at a pointer location, the auto balance operation returns to the pattern at location 1 and resumes balancing with that pattern.

More information about the Auto Balance mode is provided in “Auto Balance Mode” on page 47. Example balancing setup information is provided in “Auto Balance Mode Cell Balancing Example” on page 81.

BALANCE STATUS REGISTER

The Balance Status register contents control which external balance FET is turned on during a balance event. Each of the 12 bits in the Balance Status register controls one external balancing FET, such that bit 0 [BAL1] controls the Cell 1 FET and bit 11 [BAL12] controls the FET for Cell 12. Bits are set to ‘1’ to enable the balancing for that cell and cleared to ‘0’ to disable balancing.

Manual Balance Mode

In Manual Balance mode, the host microcontroller specifies which cell is balanced and controls when balancing starts and stops.

To manually control the cells to be balanced:

- Set the Balance Mode bits to ‘01’ for “Manual”
- Set the balance status pointer to zero
- Set bits in the Balance Status register to program the cells to be balanced (e.g., to balance Cell 5, set the BAL5 bit to 1)
- Enable balancing, either by setting the BEN bit in the Balance Setup register or by sending a Balance Enable command
- Disable balancing either by resetting the BEN bit or by sending a Balance Inhibit command

The Balance Enable and Balance Inhibit commands can be used with the “Address All” device address to control all devices in a stack simultaneously.

Manual Balance mode cannot operate while the ISL78610 is in Sleep mode. If the watchdog timer is off and the Sleep command is received during Manual balance, balancing stops immediately and the device goes into Sleep mode.

TABLE 20. BALANCE, SLEEP, WAKE, WATCHDOG TIMER OPERATION

OPERATING IN	WATCHDOG TIMER	RECEIVE SLEEP COMMAND	WATCHDOG TIMES OUT	RECEIVE WAKE COMMAND		
		ALL BALANCE MODES	ALL BALANCE MODES	MANUAL BALANCE	TIMED BALANCE	AUTO BALANCE
Normal Mode	Off	Stop balancing Device enters the Sleep mode.	N/A	N/A	N/A	N/A
	On	Stop balancing. Device enters the Sleep mode. Set the WDTM bit when the watchdog timer expires.	Stop balancing. Device enters the Sleep mode. Set the WDTM bit.	N/A	N/A	N/A
Sleep Mode	N/A	N/A	N/A	Resume Balancing	Resume Balancing, Balance time reduced by the time spent in Sleep	Resume Balancing with Auto Balance settings suspended during Sleep

If the watchdog timer is active during manual balance and the device receives the Sleep command, balancing stops immediately and the device goes into Sleep mode, but the WDTM bit is set when the watchdog timer expires (see Table 20).

The ISL78610 has a watchdog timer function that protects the battery from excess discharge due to balancing. If communications are lost, the watchdog begins a count down. If the timeout value is exceeded while the part is in Manual Balance mode, all balancing ceases and the device goes into Sleep mode. See Table 20.

If the device was performing a manual balance operation before a Sleep command, receiving a Wake command resumes balancing.

Timed Balance Mode

In Timed Balance mode, the host microcontroller specifies which cell is balanced and sets a balance time-out period. Balancing starts by control of the microcontroller and stops at the end of a time-out period (or by a command from the microcontroller.)

To set up a timed balance operation:

- Set the Balance mode bits to ‘10’ for “Timed”
- Set the Balance Status Pointer to zero
- Set bits in the Balance Status register to program the cells to be balanced (for example to balance Cells 7 and 10, set the BAL7 and BAL10 bits to 1)
- Set the balance on time. The balance on time is programmable in 20 second intervals from 20 seconds to 42.5 minutes using the BTM[6:0] bits. See Table 21
- Enable balancing, either by setting the BEN bit in the Balance Setup register or by sending a Balance Enable command. When BEN is reasserted, or when a new Balance Enable command is received, balancing resumes, using the full time specified by the BTM[6:0] bits
- Disable balancing either by resetting the BEN bit or by sending a Balance Inhibit command. Resetting BEN stops the balancing functions and resets the timer values.
- When the balance timeout period is met, the End Of Balance (EOB) bit in the Device Setup register is set and BEN is reset.

TABLE 21. WATCHDOG/BALANCE TIME REGISTER

REGISTER BITS							
13	12	11	10	9	8	7	
BTM6	BTM5	BTM4	BTM3	BTM2	BTM1	BTM0	BALANCE TIME (MINUTES)
0	0	0	0	0	0	0	Disabled
0	0	0	0	0	0	1	0.33
0	0	0	0	0	1	0	0.67
0	0	0	0	0	1	1	1.00
• • •							-
1	1	1	1	1	0	1	41.67
1	1	1	1	1	1	0	42.00
1	1	1	1	1	1	1	42.33

Timed Balance mode cannot operate while the ISL78610 is in Sleep mode. If the watchdog timer is off and the Sleep command is received during Manual balance, then balancing stops immediately and the device goes into Sleep mode.

If the watchdog timer is active during Timed balance and the device receives the Sleep command, balancing stops immediately and the device goes into Sleep mode, but the WDTM bit is set when the watchdog timer expires (see Table 20).

If the watchdog timeout value is exceeded while the part is in Manual Balance mode, all balancing ceases and the device goes into Sleep mode (see Table 20).

If the device was performing a Timed balance operation before a Sleep command, receiving a Wake command resumes balancing. However, the balance timer continues during the Sleep mode, so if the Balance timer expires before a Wake command, then Balance will not resume until the host microcontroller starts another balance cycle.

Auto Balance Mode

In Auto Balance mode, the host microcontroller specifies an amount of charge to be removed from each cell to be balanced. Balancing starts by control of the microcontroller and stops when all cells have had the specified charge removed (or by command from the microcontroller.)

Auto Balance mode performs balancing autonomously and in an intelligent manner. Thermal issues are accommodated by the provision of auto balance sequencing (see "Auto Balance Sequencing" on page 48), a multiple instance Balance Status register, and a balance wait time.

During Auto Balance mode the ISL78610 cycles through each Balance Status register instance, which turns on the balancing outputs corresponding to the bits set in each Balance Status register instance. While each cell is being balanced, the amount of charge withdrawn is calculated. Balancing stops for a cell when the specified amount of charge has been removed. See "Auto Balance SOC Adjustment value" on page 48.

When Auto Balancing is complete, the End Of Balance (EOB) bit in the Device Setup register is set and BEN bit is reset.

To set up an auto balance operation:

- Set the Balance Mode bits to '11' for Auto
- Set the Balance Status Pointer to '1'
- Set the bits in the Balance Status register to program the cells to be balanced in the first cycle (for example, to balance odd cells, set Bits 1, 3, 5, 7, 9, and 11)
- Set the Balance Status Pointer to '2'
- Set bits in the Balance Status register to program the cells to be balanced in the second cycle (for example, to balance even cells, set Bits 2, 4, 6, 8, 10, and 12)
- Set the Balance Status Pointer to '3'
- Set the bits in the Balance Status register at this location to zero to terminate the sequence. The next cycle will go back to balance at status pointer = 1.
- Write the B values into the Balance Value Registers for each cell to be balanced.
- Enable balancing, either by setting the BEN bit in the Balance Setup register or by sending a Balance Enable command. When enabled, the ISL78610 cycles through each instance of the Balance Status register for the duration given by the balance timeout. Between each Balance Status register instance, the device does a Scan All operation and inserts a delay equal to the balance wait time. The process continues with the balance status pointer wrapping back to 1, until all the Balance Value registers equal zero. If one cell Balance Value register reaches zero before the others, balancing for that cell stops, but the others continue.
- Disable balancing either by resetting the BEN bit or by sending a Balance Inhibit command. Resetting BEN, either directly or by using the Balance Inhibit command, stops the balancing functions but maintains the current Balance Value register contents. Auto Balancing continues from Balance Status register location 1 when BEN is reasserted.

AUTO BALANCE SEQUENCING

The first cycle of the auto balance operation begins with the balance status pointer at location 1, specifying the first Balance Status register instance. For the next auto balance cycle, the balance status pointer increments to location 2. For each subsequent cycle, the pointer increments to the next Balance Status register instance, until a zero value instance is encountered. At this point the sequence repeats from the Balance Status register instance at balance status pointer location 1.

For example, using two Balance Status registers, the ISL78610 can balance odd numbered cells during the first cycle and even numbered cells on the second cycle.

There is a delay time between each cycle. This delay is set by the balance wait time bits (see Table 19 on page 46)

Cells are balanced with periodic measurements performed during the balance time interval (see Table 21). These measurements are used to calculate the reduction in State of Charge (SOC) with each balancing cycle.

As individual cells reach their programmed SOC adjustment, that cell balance terminates, but the balance operation continues cycling through all instances until all cells reach their SOC adjustment value.

AUTO BALANCE SOC ADJUSTMENT VALUE

The balance value (delta SOC) is the difference between the present charge in a cell and the desired charge for that cell.

The method for calculating the state of charge for a cell is left to the system designer. Typically, determining the state of charge is dependent on the chosen cell type and manufacturer, and is dependent on cell voltage, charge and discharge rates, temperature, age of the cell, number of cycles, and other factors. Tables for determining SOC are often available from the battery cell manufacturer.

The balance value itself is a function of the current SOC, required SOC, balancing leg impedance, and sample interval. This value is calculated by the host microcontroller for each cell. The balancing leg impedance is made up of the external balance FET and balancing resistor. The sample interval is equal to the balance cycle on-time period (for example, each cell voltage is sampled at the end of the balance on-time).

The balancing value B for each cell is calculated using the formula shown in Equation 1 (see also "Balance Value Calculation Example" on page 81):

$$B = \frac{8191}{5} \times (CurrentSOC - TargetSOC) \times \frac{Z}{dt} \quad \text{(EQ. 1)}$$

where:

B = The balance register value
CurrentSOC = The present SOC of the cell (Coulombs)
TargetSOC = The required SOC value (Coulombs)
Z = The balancing leg impedance (Ω)
dt = The sampling time interval (Balance cycle on time in seconds)
8191/5 = A voltage to Hex conversion value

The balancing leg impedance is normally the sum of the balance FET $r_{DS(ON)}$ and the balance resistor.

The balancing value (B) can also be defined as in the set of equations following. Auto balance is guided by Equations 2 and 3:

$$SOC = I \times t = \frac{V}{Z} \times t \quad \text{(EQ. 2)}$$

$$B = SOC \times \frac{Z}{dt} = \frac{V}{Z} \times t \times \frac{Z}{dt} = \frac{V}{dt} \times t \quad \text{(EQ. 3)}$$

where:

dt = Balance cycle on time
t = Total balance time

Equations 2 and 3 show that the impedance drops out of the equation, leaving only the voltage and time elements. So, B becomes a collection of voltages that integrates during the balance cycle on time, and accumulates over the total balance time period to equal the programmed delta capacity.

Twelve 28-bit registers are provided for the balance value for each cell. The balance values are programmed for all cells as needed using Balance Value registers 6'h20 to 6'h37 (see Table 22 for the contents of the Cell 1 and Cell 2 Balance Values registers).

TABLE 22. BALANCE VALUES REGISTER CELL1 AND CELL2

ADDR	13	12	11	10	9	8	7	6	5	4	3	2	1	0
6'20	Cell 1 Balance Value Bits [13:0]													
6'21	Cell 1 Balance Value Bits [27:14]													
6'22	Cell 2 Balance Value Bits [13:0]													
6'23	Cell 2 Balance Value Bits [27:14]													

At the end of each balance cycle on time interval the ISL78610 measures the voltage on each of the cells that were balanced during that interval. The measured values are then subtracted from the balance values for those cells. This process continues until the balance value for each cell is zero, at which time the auto balancing process is complete.

Auto Balance mode cannot operate while the ISL78610 is in Sleep mode. If the Sleep command is received while the device is auto balancing (and the watchdog timer is off), balancing continues until it is finished and the device enters Sleep mode. If the watchdog timer is active during the Auto Balance mode and the device receives the Sleep command, balancing stops immediately and the device enters Sleep mode immediately. The WDTM bit is set when the watchdog timer expires (see Table 20).

If the device was performing an Auto balance operation before a Sleep Command, receiving a Wake command resumes balancing with the same SOC calculations that were in place when the device entered Sleep Mode.

BALANCING IN SCAN CONTINUOUS MODE

Cell balancing may be active while the ISL78610 is operating in Scan Continuous mode. In Scan Continuous mode the ISL78610 scans cell voltages, temperatures, and open-wire conditions at a rate determined by the Scan Interval bits in the Fault Setup register (see Table 14 on page 42). The behavior of the balancing functions while operating in Scan Continuous mode is controlled by the BDDS bit in the Device Setup register. If BDDS is set, cell balancing is inhibited during cell voltage measurements and for 10ms before the cell voltage scan to allow the balance devices to turn off. Balancing is re-enabled automatically at the end of the scan. The Scan Continuous and BDDS function are available during both Timed and Auto Balance modes, but not during Manual Balance.

MONITORING CELL BALANCE

To facilitate system monitoring of the cell balance operation, the ISL78610 has a Cells Balanced Enabled register that shows the present state of the balance drivers. A "1" bit indicates that the CBn output is enabled. A "0" indicates that the CBn output is disabled. This register is valid only in a Stand-Alone configuration. Reading this register in any other mode results in a NAK response.

TABLE 23. CELLS BEING BALANCED REGISTER

11	10	9	8	7	6	5	4	3	2	1	0
CBEN12	CBEN11	CBEN10	CBEN9	CBEN8	CBEN7	CBEN6	CBEN5	CBEN4	CBEN3	CBEN2	CBEN1

Daisy Chain Commands

Daisy chain devices require some special commands that are not needed by a stand-alone device. These commands are Identify, ACK, and NAK. Identify is needed to enumerate the devices in the stack. ACK is used as a command to check the communications hardware and to indicate proper communications status. A NAK response indicates a problem with the addressed device recognizing the command.

Identify Command

Identify mode is a special case mode that must be executed before any other communications to daisy chained devices, except for the Sleep command and Wake-up command. The Identify command initiates address assignments to the devices in the daisy chain stack.

Devices determine their stack position while in Identify mode. Identify mode is entered on receipt of the "base" Identify command (this is the Identify command with the device address set to 6'h00). The top stack device responds ACK after receiving the base Identify command and enters the Identify mode. Other stack devices wait to allow the ACK response to be relayed to the host microcontroller, then enter Identify mode. When in Identify mode, all stack devices except the master load address 4'h0 to their stack address register. The master (identified by the state of the Comms Select pins = 2'b01) loads 4'h1 to its stack address.

After receiving the ACK response the host microcontroller sends the Identify command with stack address 6'h2 (that is, 24'h0000 0011 0010 0100 **0010** 0110; the stack address is bolded). The last four bits are the corresponding CRC value. The master passes the command onto the stack. The device at stack position 2 responds by setting the stack address bits (ADDR[3:0]) and stack size bits (SIZE[3:0]) in the Comms Setup register to 4'h2 and returns the Identify response with CRC and an address of 6'h32 (that is, 32'b0000 0011 0010 0**111 0010** 0000 0000 1111; the address bits are bolded). The address bits contains the

normal stack address (2'h0010) and the state of the Comms Select pins (2'b11). Note that the in an Identify response, the data LSBs are always zero.

The host microcontroller then sends the Identify command with stack address 6'h3. Device 3 responds by setting its stack address and stack size information to 4'h3 and returning the Identify response with address 6'h33. Devices 1 and 2 set their stack size information to 4'h3.

The process continues with the host microcontroller incrementing the stack address until all devices in the stack receive their stack address. Identified devices update their stack size information with each new transmission. The stack top device (identified by the state of the Comms Select pins = 10) loads the stack address and stack size information and returns the Identify response with address 6'h2x, where x corresponds to the stack position of the top device. The host microcontroller recognizes the top stack response and loads the total number of stack devices to local memory. The host microcontroller then sends the Identify command with data set to 6'h3F. Devices exit Identify mode on receipt of this command. The stack top device responds ACK. An example Identify transmit and receive sequence for a stack of three devices is shown in Figure 60.

When in Normal mode, only the base Identify command is recognized by devices. Any other Identify command variant or an Identify command sent with a nonzero stack address causes a NAK response from the addressed device(s).

Send Identify Command	Tx				0000	0011	0010	0100	0000	0100		03 24 04
	Rx		0000	0011	0011	0000	0000	0000	0000	1100		03 30 00 0C
Send Identify Device 2	Tx				0000	0011	0010	0100	0010	0110		03 24 26
	Rx		0000	0011	0010	0111	0010	0000	0000	1111		03 27 20 0F
Send Identify Device 3	Tx				0000	0011	0010	0100	0011	0111		03 24 37
	Rx		0000	0011	0010	0110	0011	0000	0000	0101		03 26 30 05
Send Identify Complete	Tx				0000	0011	0010	0111	1111	1110		03 27 FE
	Rx		0011	0011	0011	0000	0000	0000	0000	0001		33 30 00 01

FIGURE 60. IDENTIFY EXAMPLE, STACK OF 3 DEVICES

IDENTIFY TIMING

Refer to Table 24 to determine the time required to complete an Identify operation. The table's two SPI Command columns show the time required to send the Identify command and receive the response (with a 1MHz SPI clock). The master has no daisy chain clocks, so all three bytes of the send and four bytes of the receive are accumulated. For the daisy chain devices, the daisy communication overlaps with two of the SPI send bytes and with three of the SPI receive bytes, so no extra time is needed for these bits.

When the device receives the Identify command, it adds a Delay time before sending the response back to the master. After receiving the daisy response, the master sends the response to the host through the SPI port.

The "Time for Each Device" column shows the time for the Identify commands to be sent and propagate through each numbered device. The "Identify Total Time" column shows the total accumulated time required for Identify commands to be sent and propagate through all devices in the battery stack configuration. The "Identify + Identify Complete Time" columnadds the identify complete timing to the total. The Identify Complete command takes the same number of clock cycles as the last Identify command.

TABLE 24. IDENTIFY TIMING WITH DAISY CHAIN OPERATING AT 500kHz

NUMBER OF DEVICES (2 MINIMUM)	SPI COMMAND SEND TIME (µs)	DAISY TRANSMIT TIME (µs)	RESPONSE DELAY (µs)	DAISY RECEIVE TIME (µs)	SPI COMMAND RECEIVE TIME (µs)	TIME FOR EACH DEVICE (µs)	IDENTIFY TOTAL TIME (µs)	IDENTIFY + IDENTIFY COMPLETE TIME (µs)
1 (Master)	24	0	0	0	32	56	56	56
2	8	50	18	66	8	150	206	356
3	8	52	18	68	8	154	360	514
4	8	54	18	70	8	158	518	676
5	8	56	18	72	8	162	680	842
6	8	58	18	74	8	166	846	1012
7	8	60	18	76	8	170	1016	1186
8	8	62	18	78	8	174	1190	1364
9	8	64	18	80	8	178	1368	1546
10	8	66	18	82	8	182	1550	1732
11	8	68	18	84	8	186	1736	1922
12	8	70	18	86	8	190	1926	2116
13	8	72	18	88	8	194	2120	2314
14	8	74	18	90	8	198	2318	2516

TABLE 25. IDENTIFY TIMING WITH DAISY CHAIN OPERATING AT 250kHz

NUMBER OF DEVICES (2 MINIMUM)	SPI COMMAND SEND TIME (µs)	DAISY TRANSMIT TIME (µs)	RESPONSE DELAY (µs)	DAISY RECEIVE TIME (µs)	SPI COMMAND RECEIVE TIME (µs)	TIME FOR EACH DEVICE (µs)	IDENTIFY TOTAL TIME (µs)	IDENTIFY + IDENTIFY COMPLETE TIME (µs)
1 (Master)	24	0	0	0	32	56	56	56
2	8	100	34	132	8	282	338	620
3	8	104	34	136	8	290	628	918
4	8	108	34	140	8	298	926	1224
5	8	112	34	144	8	306	1232	1538
6	8	116	34	148	8	314	1546	1860
7	8	120	34	152	8	322	1868	2190
8	8	124	34	156	8	330	2198	2528
9	8	128	34	160	8	338	2536	2874
10	8	132	34	164	8	346	2882	3228
11	8	136	34	168	8	354	3236	3590
12	8	140	34	172	8	362	3598	3960
13	8	144	34	176	8	370	3968	4338
14	8	148	34	180	8	378	4346	4724

ACK (Acknowledge) Command

The daisy chain devices use the ACK command to acknowledge receipt of a valid command. ACK is also useful as a communications test command: the stack top device returns ACK in response to successful receipt of the ACK command. No other action is performed in response to an ACK.

NAK (Not Acknowledge) Command

Receipt of an unrecognized command by either the target device or the top stack device results in a NAK being returned by that device. If a command addressed to all devices using the Address All stack address 1111 or the identify stack address 0000 is not recognized by any devices, then all devices not recognizing the command respond NAK. In this case, the host microcontroller receives the NAK response from the lowest stack device that failed to recognize the command. An incomplete command (for example, one that is less than the length required) also causes a NAK to be returned.

Communications

All communications are conducted through the SPI port in single 8-bit byte increments. The MSB is transmitted first and the LSB is transmitted last.

Maximum operating data rates are 2Mbps for the SPI interface. When using the daisy chain communications system it is recommended that the synchronous communications data rate be at least twice that of the daisy chain system (see Table 7).

In stand-alone applications (non-daisy chain) data is sent without additional address information. This maximizes the throughput for full duplex SPI operation.

In daisy chain applications all measurement data is sent with the corresponding device stack address (the position within the daisy chain), parameter identifier, and data address. Daisy chain communication throughput is maximized by allowing streamed data (accessed by a “read all data” address).

SPI Interface

The ISL78610 operates as an SPI slave capable of bus speeds up to 2Mbps. Four lines make up the SPI interface: SCLK, DIN, DOUT, and $\overline{CS}$. The SPI interface operates in either full duplex or half duplex mode depending on the daisy chain status of the part.

The DOUT line is normally tri-stated (high impedance) to allow use in a multidrop bus. DOUT is active only when $\overline{CS}$ is low.

An additional output $\overline{\text{DATA READY}}$ is used in the daisy chain configuration to notify the host microcontroller that responses have been received from a device in the chain.

FULL DUPLEX (STAND-ALONE) SPI OPERATION

In non-daisy chain applications, the SPI bus operates as a standard, full duplex SPI port. Read and write commands are sent to the ISL78610 in 8-bit blocks. $\overline{CS}$ is taken high between each block.

Data flow is controlled by interpreting the first bit of each transaction and counting the requisite number of bytes. The host microcontroller ensures that commands are correctly formulated. An incorrect formulation, (for example, a read bit instead of a write bit), causes the port to lose synchronization.

A timeout period associated with the $\overline{CS}$ inactive (high) condition resets all the communications counters. This effectively resets the SPI port to a known starting condition. If $\overline{CS}$ stays high for more than 100µs, the SPI state machine resets.

A pending device response from a previous command is sent by the ISL78610 during the first two bytes of the 3-byte Write transaction. The third byte from the ISL78610 is then discarded by the host microcontroller. This maintains sequencing during 3-byte (Write) transactions.

Figure 3 on page 14 shows interface timing for full duplex SPI transfers.

HALF DUPLEX (DAISY CHAIN) OPERATION

The SPI operates in half duplex mode when configured as a daisy chain application (see Table 6 on page 27). Data flow is controlled by a handshake system using the $\overline{\text{DATA READY}}$ and $\overline{CS}$ signals. $\overline{\text{DATA READY}}$ is controlled by the ISL78610. $\overline{CS}$ is controlled by the host microcontroller. This handshake accommodates the delay between command receipt and device response due to the latency of the daisy chain communications system.

A timeout period associated with the $\overline{CS}$ inactive (high) condition resets all the communications counters. This effectively resets the SPI port to a known starting condition. If $\overline{CS}$ stays high for more than 100µs, the SPI state machine resets.

Responses from stack devices are received by the stack master (stack bottom device). The stack master then asserts its $\overline{\text{DATA READY}}$ output when the first full data byte is available. The host microcontroller responds by asserting $\overline{CS}$ and clocking the data out of the DOUT port. The $\overline{\text{DATA READY}}$ line is then cleared and DOUT is tri-stated in response to $\overline{CS}$ being taken high. The DIN and DOUT lines can be connected externally in this mode.

Half duplex communications are conducted using the $\overline{\text{DATA READY}}/\overline{CS}$ handshake as follows:

1. The host microcontroller sends a command to the ISL78610 using the $\overline{CS}$ line to select the ISL78610 and clocking data into the ISL78610 DIN pin.
2. The ISL78610 asserts $\overline{\text{DATA READY}}$ low when it is ready to send data to the host microcontroller. When $\overline{\text{DATA READY}}$ is low, the ISL78610 is in transmit mode and will ignore any data on DIN.
3. The host microcontroller asserts $\overline{CS}$ low and clocks 8 bits of data out of DOUT using SCLK.
4. The host microcontroller then raises $\overline{CS}$. The ISL78610 responds by raising $\overline{\text{DATA READY}}$ and tri-stating DOUT.
5. The ISL78610 reasserts $\overline{\text{DATA READY}}$ for the next byte, and so on.

The host microcontroller must service the ISL78610 if $\overline{\text{DATA READY}}$ is low before sending further commands. The ISL78610 ignores any data sent to DIN while $\overline{\text{DATA READY}}$ is low.

The ISL78610 $\overline{\text{DATA READY}}$ output is not asserted if $\overline{\text{CS}}$ is already asserted. It is possible for the microcontroller to interrupt a sequential data transfer by asserting $\overline{\text{CS}}$ before the ISL78610 asserts $\overline{\text{DATA READY}}$. This causes a conflict with the communications and is not recommended. A conflict created in this manner would be recognized by the microcontroller either not receiving the expected response or receiving a communications failure notification.

Figure 4 on page 14 shows interface timing for half duplex SPI transfers.

Non-Daisy Chain Communications

In non-daisy chain (Stand-Alone) systems, all communications sent from the master are 2 or 3 bytes in length. Data read and action commands are 2 bytes. Data writes are 3 bytes. Device responses are 2 bytes in length and contain data only.

Write commands in non-daisy chain systems consist of a $\overline{\text{read}}$/write bit, page address (3 bits), data address (6 bits), and data (14 bits) - three bytes.

Read commands in non-daisy chain systems are composed of a $\overline{\text{read}}$/write bit, page address (3 bits), data address (6 bits), fill (6 bits), and 16 bits of returned data (ignore the first most significant bits of data returned) - four bytes.

The ISL78610 responds to read commands by loading the requested data to its output buffer. The output buffer contents are then loaded to the shift register when $\overline{\text{CS}}$ goes low and are shifted out on the DOUT line on the falling edges of SCLK. This sequence continues until all the requested data has been sent.

Commands and data are memory mapped to 14-bit data locations. The memory map is arranged in pages. Pages 1 and 2 are used for volatile data. Page 3 contains the action and communications administration commands. Page 4 accesses nonvolatile memory. Page 5 is used for factory test.

Action commands, such as scan and communications administration operations are treated as reads.

Non-daisy chain devices do not generate a response to write or system level commands. Data integrity can be verified by reading register contents after writing. The ISL78610 does nothing in response to a write or administration command that is not recognized. An unrecognized read command returns 16'h0000. An incomplete command, such as may occur if communications are interrupted, is registered as an unrecognized command either when $\overline{\text{CS}}$ is taken high or after a timeout period. The communications interface is reset after the timeout period.

Non-daisy chain communications are conducted without CRC (Cyclical Redundancy Check) error detection. The following commands have no meaning in non-daisy chain systems: Identify, ACK, and NAK.

The rules for non-daisy chain installations are shown in Table 26.

Examples of full duplex SPI read and write sequences are shown in Figures 61, 62, and 63. An example Device Read (Cell 7), with response, is shown in Figure 63.

TABLE 26. ISL78610 DATA INTERPRETATION RULES FOR NON-DAISY CHAIN INSTALLATIONS

FIRST BIT IN SEQUENCE	PAGE ADDR	DATA ADDRESS	INTERPRETATION
0	011	001000	Measure command. The last six bits of the transmission contain the element address.
0	Any	All other	Device read or action command. The last six bits of the transmission are zero.
1	Any	Any	Device write command.

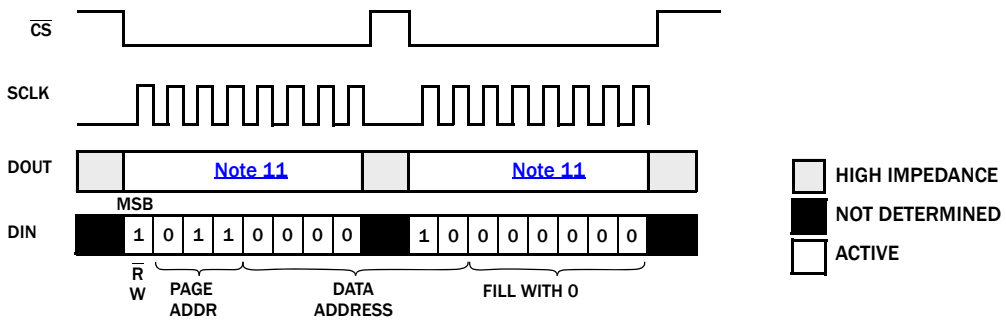
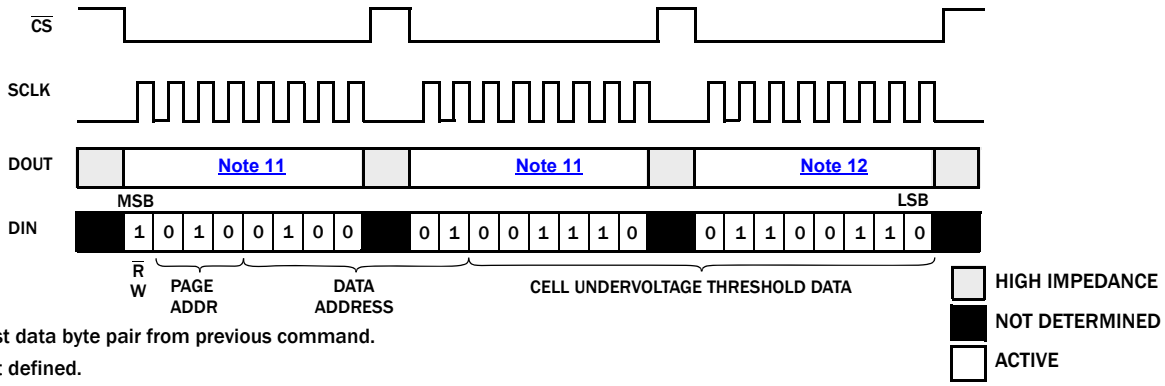


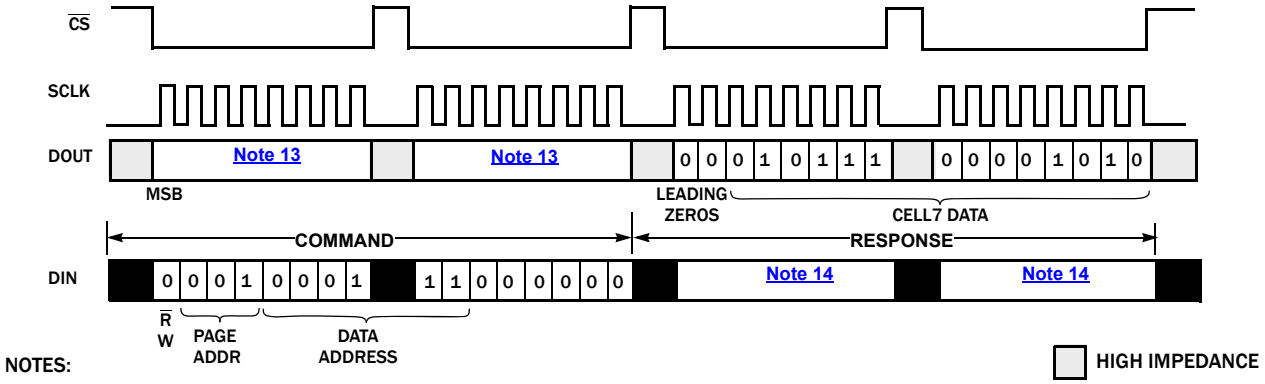
FIGURE 61. SPI FULL DUPLEX (STAND-ALONE) MEASURE COMMAND EXAMPLE: EXT4 VOLTAGE



NOTES:

11. Last data byte pair from previous command.
12. Not defined.

FIGURE 62. SPI FULL DUPLEX (STAND-ALONE) WRITE COMMAND EXAMPLE: WRITE UNDERVOLTAGE THRESHOLD DATA



NOTES:

13. Last data byte pair from previous command.
14. Next command (or 8'h00 if no command).

FIGURE 63. SPI FULL DUPLEX (STAND-ALONE) READ COMMAND EXAMPLE: READ CELL 7 DATA

EXAMPLE NON-DAISY COMMUNICATIONS

Examples of the various command structures for non-daisy chain installations are shown in Figures 64A through 64E.

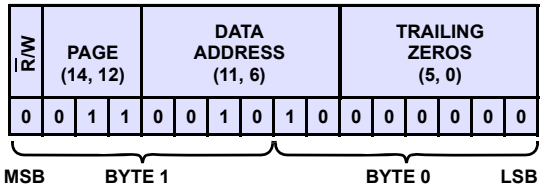


FIGURE 64A. DEVICE LEVEL COMMAND: SLEEP

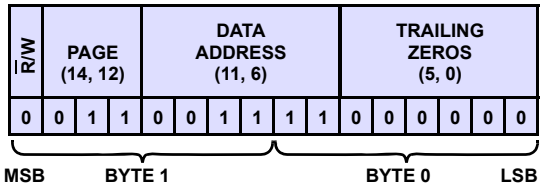


FIGURE 64B. DEVICE LEVEL COMMAND: WAKE-UP

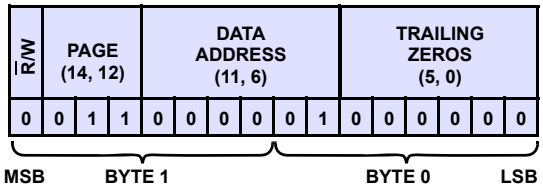


FIGURE 64C. DEVICE LEVEL COMMAND: SCAN VOLTAGES

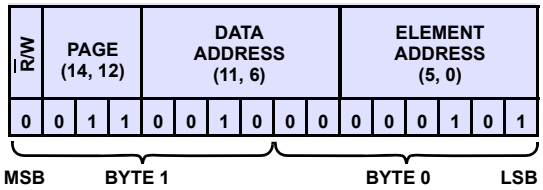


FIGURE 64D. DEVICE LEVEL COMMAND: MEASURE CELL 5 VOLTAGE

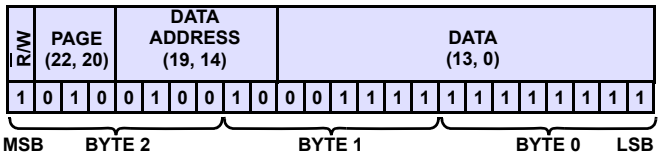


FIGURE 64E. DEVICE WRITE: WRITE EXTERNAL TEMPERATURE LIMIT = 14'h0FFF

FIGURE 64. NON-DAISY CHAIN DEVICE COMMAND AND WRITE EXAMPLES

Daisy Chain Communications

Commands in daisy chain systems are transmitted and received through the SPI port and are composed of a device address (4 bits), a read/write bit, page address (3 bits), data address (6 bits), data (6 bits), and CRC (4 bits).

Device commands and data are memory mapped to 14-bit data locations. The memory map is arranged in pages. Pages 1 and 2 are used for volatile data. Page 3 contains the action and communications administration commands. Page 4 accesses nonvolatile memory. Page 5 is used for factory test.

The daisy chain communication is intended for use with large stacks of battery cells with many ISL78610 devices.

Communications Protocol

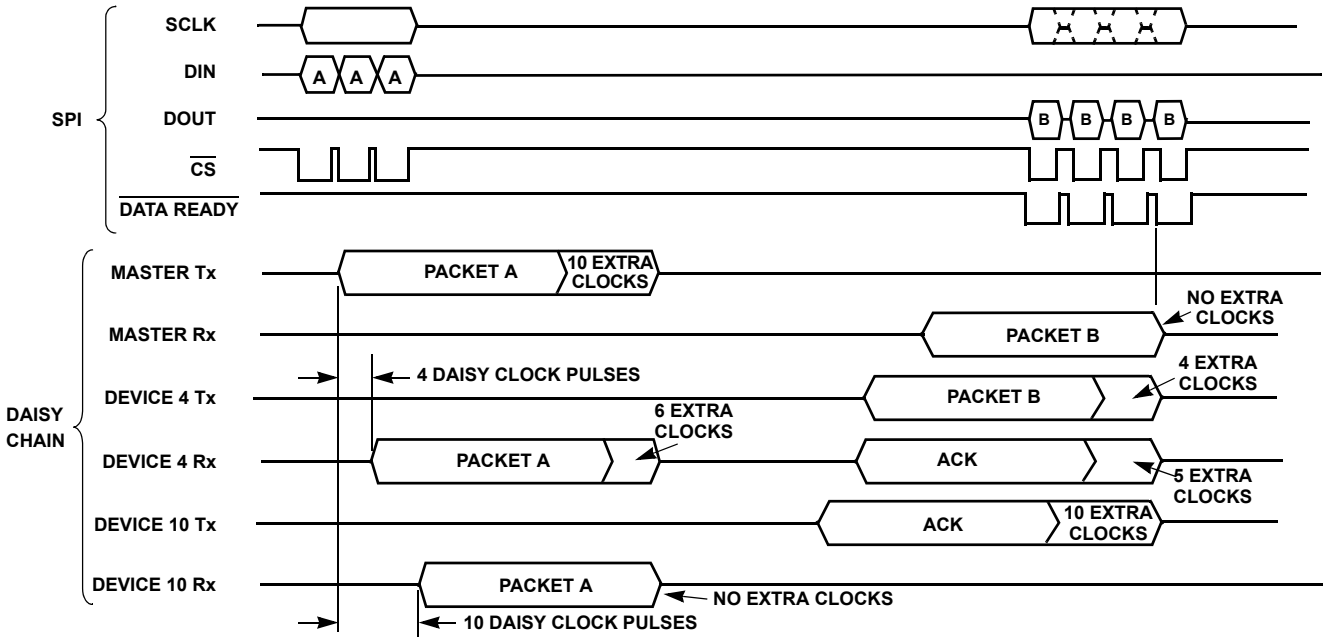
All daisy chain communications are passed from device to device so that all devices in the stack receive the same information. Each device then decodes the message and responds as needed. The originating device (master in the case of commands, addressed device or top stack device in the case of responses) generates the system clock and data stream. Each device delays the data stream by one clock cycle. Each device knows its stack location (see the Identify command on page 49) and the total number of devices in the stack. Each originating device adds a number of clock pulses to the daisy chain data stream to allow transmission through the stack.

All communications from the host microcontroller are passed from device to device to the last device in the chain (top device). The top device responds to read and write messages with an "ACK" (or with the requested data if this is the addressed device and the message was a read command). The addressed device then waits to receive the "ACK" before responding, either with data, in the case of a read, or with an "ACK" in the case of a write. Action commands such as the Scan commands do not require a response.

A read or write communications transmission is only considered to be complete following receipt of a response from the target device or the identification of a communications fault condition. The host microcontroller should not transmit further data until either a response has been received from the target stack device or a communications fault condition has been identified. Figure 65 on page 56 shows a typical communication sequence to "Read Device 4, Cell 7" data from a stack of 10 devices. The maximum response time (the time from the rising edge of $\overline{CS}$ at the end of the first byte of a read/write command, sent by the host microcontroller, to the assertion of $\overline{DATA\ READY}$ by the master device) is given in Table 27 for various daisy chain data rates.

TABLE 27. MAXIMUM RESPONSE TIMES FOR DAISY CHAIN READ AND WRITE COMMANDS. STACK OF 10 DEVICES

	MAXIMUM TIME TO ASSERTION OF DATA READY				
DAISY CHAIN DATA RATE (kHz)	500	250	125	62.5	UNIT
Response time	240	480	960	1920	µs



- Host microcontroller sends “Read Device 4, Cell 7” = Packet A
- Master begins relaying Packet A following receipt of the first byte of A. Master adds 10 extra clock cycles to allow all stack devices to relay the message.
- Device 4 receives and decodes “Read Device 4, Cell 7” and waits for a response from top stack device.
- Top of stack (device 10) receives and decodes Packet A.
- Device 10 responds “ACK”. Device 10 adds 10 clock cycles to allow all stack devices to relay the message.
- Device 4 receives and decodes ACK.
- Device 4 transmits the Cell 7 data = Packet B. Device 4 subtracts one clock cycle to synchronize timing for lower stack devices to relay the message.
- Master asserts DATA READY after receiving the first byte of Packet B.
- Host responds by asserting $\overline{CS}$ and clocking out 8 bits of data from DOUT. $\overline{CS}$ is taken high following the 8th bit. The master responds by taking $\overline{DATA\ READY}$ high and tri-stating DOUT. Master asserts $\overline{DATA\ READY}$ after receiving the next byte and so on.

FIGURE 65. DAISY CHAIN READ EXAMPLE “READ DEVICE 4, CELL 7”. STACK OF 10 DEVICES

TABLE 28. ISL78610 DATA INTERPRETATION RULES FOR DAISY CHAIN INSTALLATIONS

FIRST 4 BITS IN SEQUENCE	5TH BIT ($\overline{R}$/W)	PAGE	DATA ADDRESS	INTERPRETATION
Stack address [3:0] (nonzero)	0	011	001000	Measure command. Data address is followed by 6-bit element address.
0000	0	011	001001	Identify command. Data address is followed by device count data.
Stack address [3:0] (nonzero)	0	Any	All other	Device Read command. Data address is followed by 6 zeros.
Stack address [3:0] (nonzero)	1	Any	Any	Device Write command.

DAISY CHAIN RECEIVE BUFFER

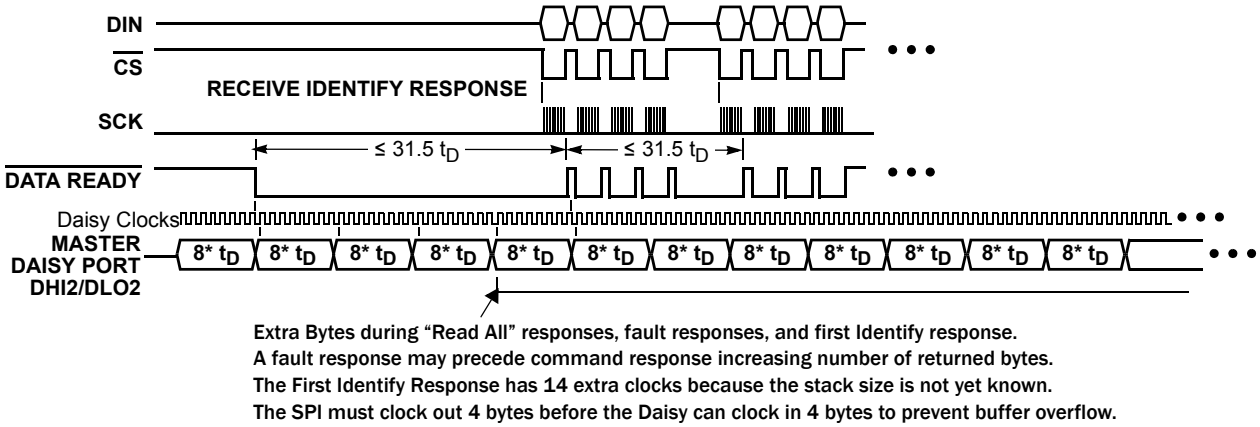


FIGURE 66. EXAMPLE WORST CASE TIMING TO AVOID DAISY BUFFER OVERFLOW

A 4-byte data buffer is provided between the Daisy Chain and SPI communications. This accommodates all single transaction responses. Multiple byte responses, such as Identify, Read All Voltages, Read All Temperatures, Read All Faults, and responses that may include a fault response from a device detecting an error, would overflow this buffer. Therefore, it is important that the host microcontroller completes a read of the first byte of data before a fifth byte arrives on the Master device’s daisy chain port and to clock data out from the SPI port faster than data is clocked in through the Daisy port to prevent data loss.

For example, when performing the first step in an IDENTIFY operation (see “Identify Command” on page 49) the daisy chain top device returns a 4-byte response plus 14 extra zeros (because it does not yet know how many devices are in the stack.) If the Host does not read the first byte from the Master before the 32nd daisy clock, the extra zeros will overwrite the first byte of the response. In another example, a “Read All Faults” returns 22 bytes. It is important for the Host to read data from the ISL78610 faster than 4 bytes every 31.5 Daisy clocks (see Figure 66).

COMMUNICATION SEQUENCES

All daisy chain device responses are 4-byte sequences, except for the responses to the Read All command. All responses start with the device stack address and use a 4-bit CRC. The response to the “Read All Commands” is to send a normal 4-byte data response for the first data segment and continue sending the remaining data segments in 3-byte sections composed of the data address, data, and CRC. This creates an anomaly with the normal CRC usage in that the first four bytes have a 4-bit CRC at the end (operating on 3.5 bytes of data) while the remaining bytes have a CRC which only operates on 2.5 bytes. The host microcontroller, having requested the data, must be prepared for this.

Daisy chain devices require device stack address information to be added to the basic command set. Daisy chain writes are 4-byte sequences. Daisy chain reads are 3 bytes. Action commands, such as scan and communications administration commands, are treated as reads. Daisy chain communications employ a 4-bit CRC (Cyclic Redundancy Check) using a polynomial of the form $1 + X + X^4$. The first four bits of each daisy chain transmission contain the stack address, which can be any number from 0001 to 1110. All devices respond to the Address All (1111) and Identify (0000) stack addresses. The fifth bit is set to ‘1’ for write and ‘0’ for read. The rules for daisy chain installations are shown in Table 28 on page 56.

CRC Calculation

Daisy chain communications use a 4-bit CRC with a polynomial of the form $1 + X + X^4$. The polynomial is implemented as a 4-stage internal XOR standard linear feedback shift register as shown in Figure 67. The CRC value is calculated using the base command data only. The CRC value is not included in the calculation.

The host microcontroller calculates the CRC when sending commands or writing data. The calculation is repeated in the ISL78610 and checked for compliance. The ISL78610 calculates the CRC when responding with data (device reads). The host microcontroller then repeats the calculation and checks for compliance.

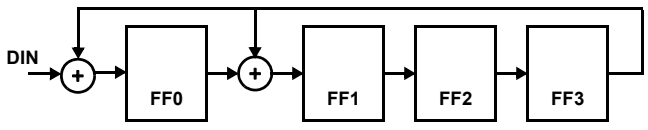


FIGURE 67. 4-BIT CRC CALCULATION

```
Attribute VB_Name = "isl78610evb_crc4_lib"
' File - isl78610evb_crc4_lib.bas
' Copyright (c) 2010
' ----------------------------------------------------------------------------
Option Explicit
'*****************************************************************
' CRC4 Routines
'*****************************************************************
 Public Function CheckCRC4(myArray() As Byte) As Boolean
    'returns True if CRC4 checksum (low nibble of last byte in myarray)
    'is good. Array can be any length

    Dim crc4 As Byte
    Dim lastnibble As Byte

    lastnibble = myArray(UBound(myArray)) And &HF
    crc4 = CalculateCRC4(myArray)

    If lastnibble = crc4 Then
        CheckCRC4 = True
    Else
        CheckCRC4 = False
    End If

End Function

Public Sub AddCRC4(myArray() As Byte)
    'adds CRC4 checksum (low nibble in last byte in array)
    'array can be any length

    Dim crc4 As Byte

    crc4 = CalculateCRC4(myArray)
    myArray(UBound(myArray)) = (myArray(UBound(myArray)) And &HF0) Or
crc4

End Sub

Public Function CalculateCRC4(ByRef myArray() As Byte) As Byte
    'calculates/returns the CRC4 checksum of array contents excluding
    'last low nibble. Array can be any length

    Dim size As Integer
    Dim i As Integer
    Dim j As Integer
    Dim k As Integer
    Dim bit0 As Boolean, bit1 As Boolean, bit2 As Boolean, bit3 As Boolean
    Dim ff0 As Boolean, ff1 As Boolean, ff2 As Boolean, ff3 As Boolean
    Dim carry As Boolean
    Dim arraycopy() As Byte
    Dim result As Byte

    'copy data so we do not clobber source array
    ReDim arraycopy(LBound(myArray) To UBound(myArray)) As Byte
    For i = LBound(myArray) To UBound(myArray)
        arraycopy(i) = myArray(i)
    Next

    'initialize bits
    bit0 = False
    bit1 = False
    bit2 = False
    bit3 = False

    'simple implementation of CRC4 (using polynomial 1 + X + X^4)
    For i = LBound(arraycopy) To UBound(arraycopy)

        'last nibble is ignored for CRC4 calculations
        If i = UBound(arraycopy) Then
            k = 4
        Else
            k = 8
        End If

        For j = 1 To k
            'shift left one bit
            carry = (arraycopy(i) And &H80) > 0
            arraycopy(i) = (arraycopy(i) And &H7F) * 2

            'see ISL78610 datasheet, Fig 11: 4-bit CRC calculation
            ff0 = carry Xor bit3
            ff1 = bit0 Xor bit3
            ff2 = bit1
            ff3 = bit2
            bit0 = ff0
            bit1 = ff1
            bit2 = ff2
            bit3 = ff3
        Next j
    Next i

    'combine bits to obtain CRC4 result
    result = 0
    If bit0 Then
        result = result + 1
    End If
    If bit1 Then
        result = result + 2
    End If
    If bit2 Then
        result = result + 4
    End If
    If bit3 Then
        result = result + 8
    End If

    CalculateCRC4 = result

End Function
```

FIGURE 68. EXAMPLE CRC CALCULATION ROUTINE (VISUAL BASIC)

Daisy Chain Addressing

When used in a daisy chain system, each individual device dynamically assigns itself a unique address (see "Identify Command" on page 49). In addition, all daisy chain devices respond to a common address, allowing them to be controlled simultaneously (for example, when using the Scan Voltages and Balance Enable commands). See "Communication Timing" on page 61.

The state of the COMMS SELECT 1, COMMS SELECT 2, COMMS RATE 0, and COMMS RATE 1 pins can be checked by reading the CSEL[2:1] and CRAT[1:0] bits in the Comms Setup register (see Table 29). The SIZE[3:0] bits show the number of devices in the daisy chain and the ADDR[3:0] bits indicate the location of a device within the daisy chain.

Examples of the various read and write command structures for daisy chain installations are shown in Figures 70C to 70G. The MSB is transmitted first and the LSB is transmitted last.

TABLE 29. COMMS SETUP REGISTER (ADDRESS 6'h18)

11	10	9	8	7	6	5	4	3	2	1	0
CRAT1	CRAT0	CSEL2	CSEL1	SIZE3	SIZE2	SIZE1	SIZE0	ADDR3	ADDR2	ADDR1	ADDR0
These bits show the status of the COMMS RATE 1 and COMMS RATE 0 pins		These bits show the status of the COMMS SEL 2 and COMMS SEL 1 pins		These bits show the daisy chain stack size (that is, the total number of stacked devices)				These bits show this devices position within the daisy chain stack			

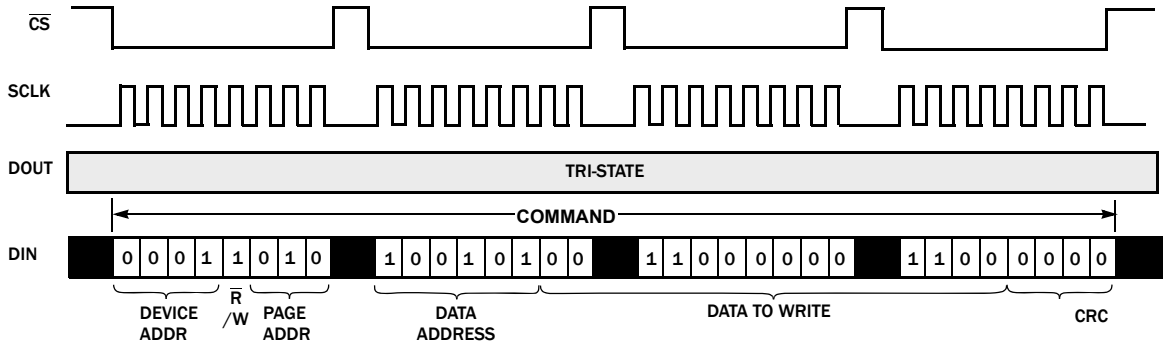


FIGURE 69. SPI HALF DUPLEX (DAISY CHAIN) WRITE REGISTER COMMAND EXAMPLE: WRITE DEVICE 1, DEVICE SETUP REGISTER

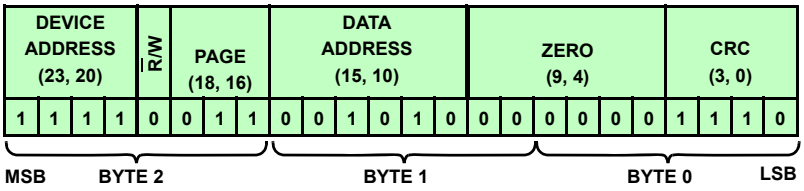


FIGURE 70A. DEVICE LEVEL COMMAND: SLEEP

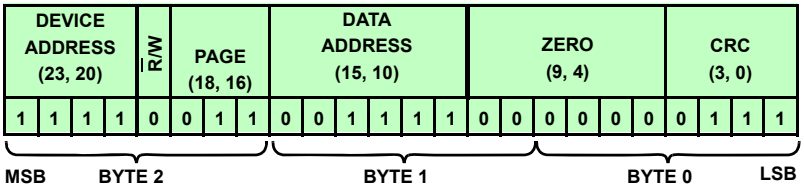


FIGURE 70B. DEVICE LEVEL COMMAND: WAKE-UP

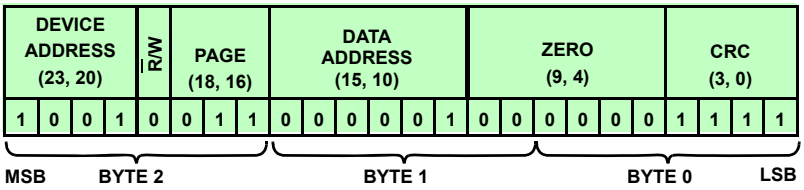


FIGURE 70C. DEVICE LEVEL COMMAND: DEVICE 9, SCAN VOLTAGES

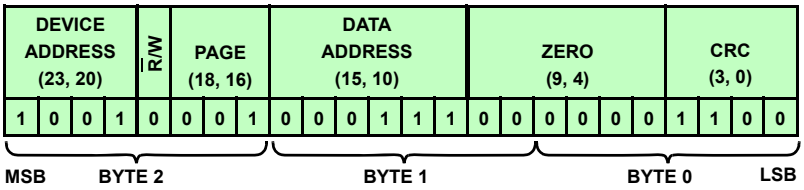


FIGURE 70D. DEVICE READ: DEVICE 9, GET CELL 7 DATA

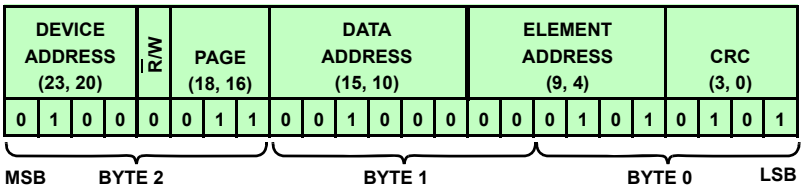


FIGURE 70E. ELEMENT LEVEL COMMAND: DEVICE 4, MEASURE CELL 5 VOLTAGE

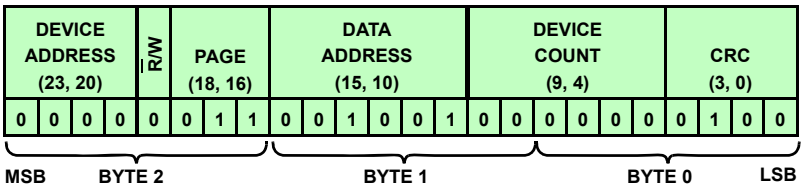


FIGURE 70F. IDENTIFY COMMAND

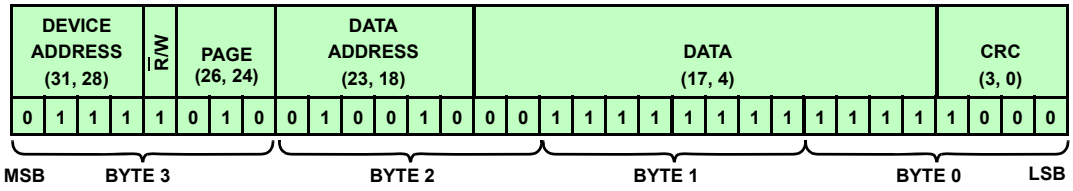


FIGURE 70G. DEVICE WRITE: DEVICE 7, WRITE EXTERNAL TEMPERATURE LIMIT = 14'h0FFF

FIGURE 70. DAISY CHAIN DEVICE READ AND WRITE EXAMPLES

Response examples are shown in Figures 71A to 71D.

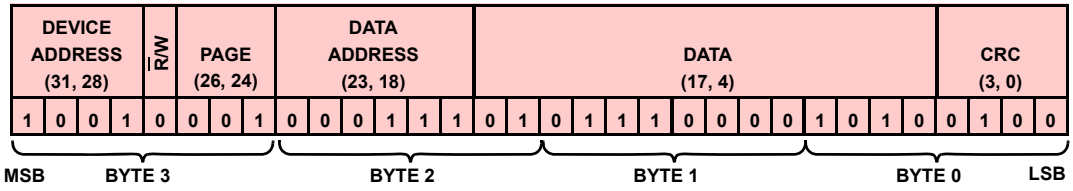


FIGURE 71A. DEVICE DATA RESPONSE: DEVICE 9, CELL 7 VOLTAGE = 14'h170A (3.6V)

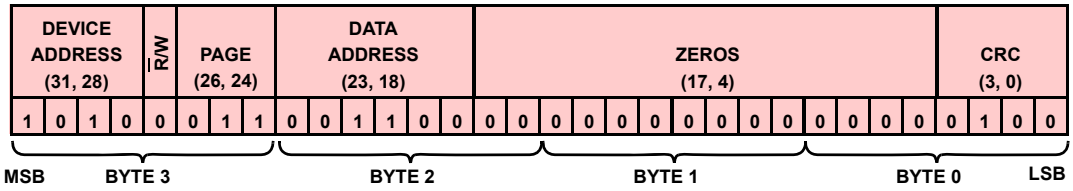


FIGURE 71B. DEVICE COMMUNICATIONS ADMINISTRATION RESPONSE: DEVICE 10, ACK

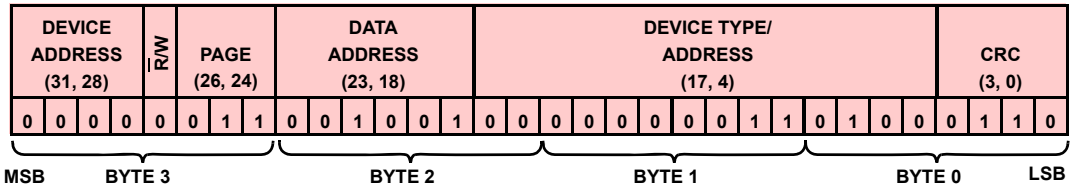


FIGURE 71C. DEVICE COMMUNICATIONS ADMINISTRATION RESPONSE: *IDENTIFY*, DEVICE 4, MIDDLE STACK DEVICE

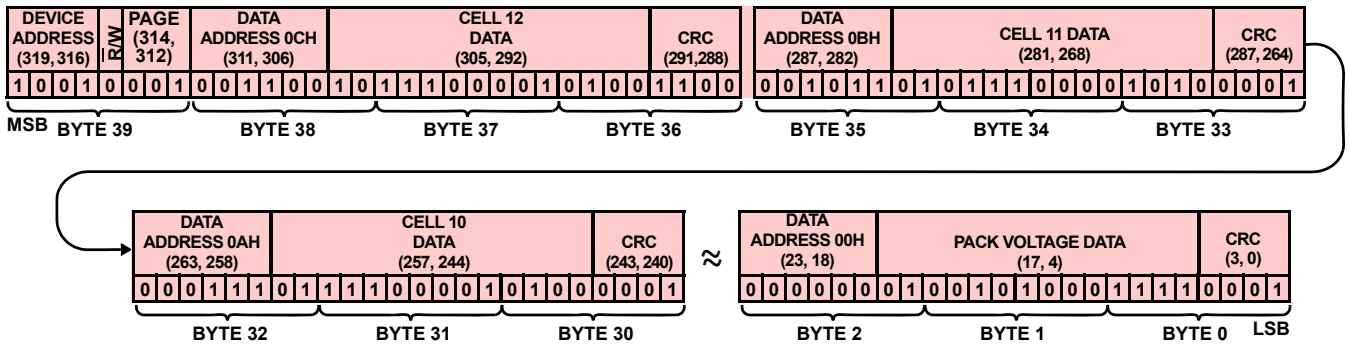


FIGURE 71D. DEVICE DATA RESPONSE: DEVICE 9, READ ALL CELL VOLTAGE DATA

FIGURE 71. DAISY CHAIN DEVICE RESPONSE EXAMPLES

Communication Timing

Collecting voltage and temperature data from daisy chained ISL78610 devices consists of three separate types of operations: A command to initiate measurement, the measurement itself, and a command and response to retrieve data.

Commands are the same for all types of operations, but the timing is dependent on the number of devices in the stack, the daisy chain clock rate, and the SPI clock rate.

Actual measurement operations occur within the device and start with the last bit of the command byte and end with data being placed in a register. Measurement times are dependent on the ISL78610 internal clock. This clock has the same variations (and is related to) the daisy chain clock.

Responses have different timing calculations, based on the position of the addressed device in the daisy chain stack and the daisy chain and SPI clock rates.

Measurement Timing Diagrams

All measurement timing is derived from the ISL78610's internal oscillators. The following typical figures are those obtained with the oscillators operating at their nominal frequencies and with any synchronization timing also at nominal value. Maximum figures are those obtained with the oscillators operating at their minimum frequencies and with the maximum time for any synchronization timing.

Measurement timing begins with a Start Scan signal. This signal is generated internally by the ISL78610 at the last clock falling edge of the Scan or Measure command (this is the last falling edge of the SPI clock in the case of a stand-alone or master device, or the last falling edge of the daisy chain clock, in the case of a daisy chain device). Daisy chain middle or top devices impose additional synchronization delays. Communications sent on the SPI port are passed on to the master device's daisy chain port at the end of the first byte of data. Then, for each device, there is an additional delay of one daisy chain clock cycle.

After receiving the Start Scan signal, the device initializes measurement circuits and performs the requested measurement(s). When the measurements are made, some devices perform additional operations, such as checking for overvoltage conditions. The measurement command ends when the registers are updated. At this time, the registers can be read using a separate command. A detailed timing breakdown is provided for each measurement type below.

See Figure 72 for the measurement timing for a Stand-Alone device. See Figure 73 for the measurement timing for daisy chain devices.

Tables 33 through 38 starting on page 68 give the typical and maximum timing for the critical elements of measurement process. Each table shows the timing from the last edge of the Scan command clock.

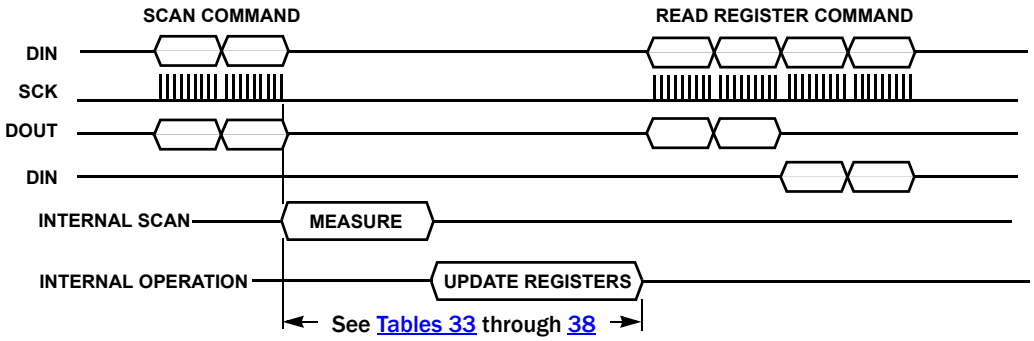


FIGURE 72. SCAN/MEASURE COMMAND TIMING WITH RESPONSE (STAND-ALONE)

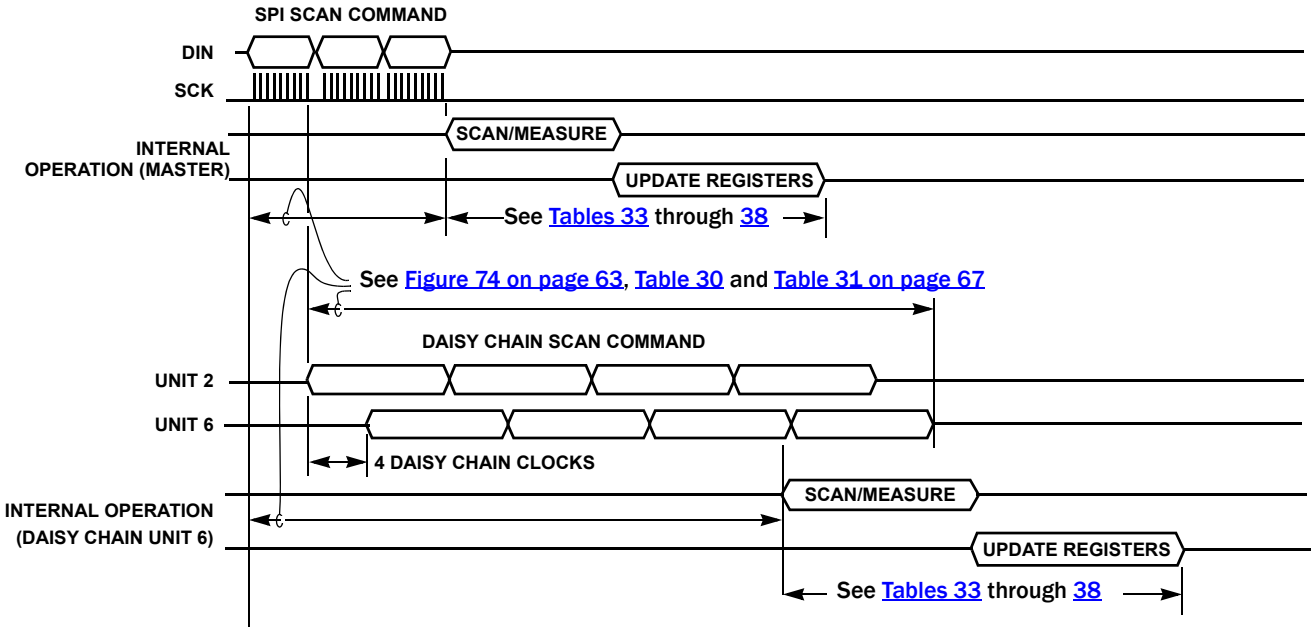
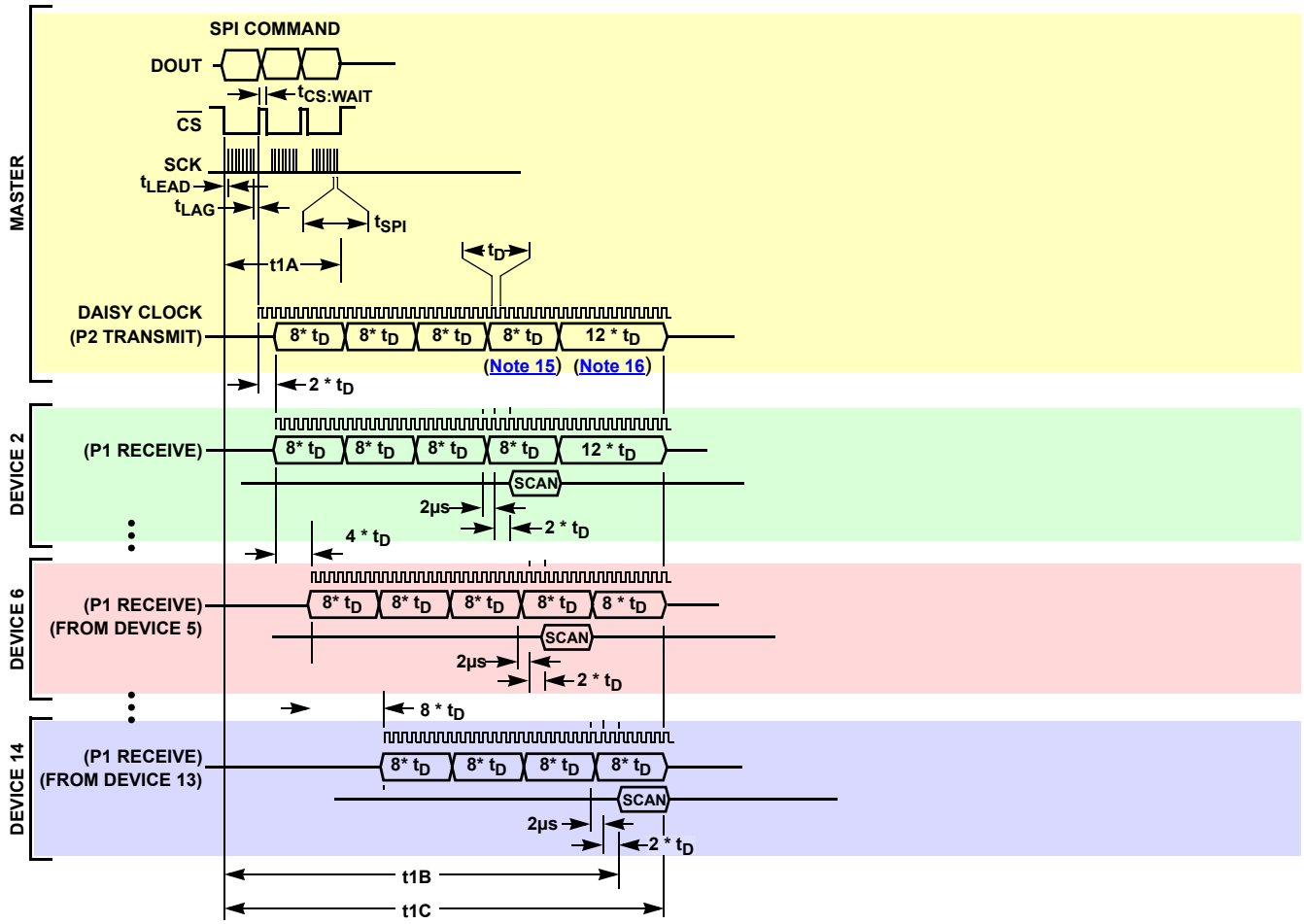


FIGURE 73. MEASUREMENT TIMING (6 DEVICE DAISY CHAIN)

Command Timing Diagram



To Start of Scan (master)

$$t1A = t_{SPI} \times 8 + t_{LEAD} + t_{LAG} \times 3 + 2 \times t_{CSWAIT}$$

To Start of Scan (top/middle)

$$t1B = t_{SPI} \times 8 + t_{LEAD} + t_{LAG} + t_D \times (28 + n - 2) + 2\mu s$$

To End of command

$$t1C = t_{SPI} \times 8 + t_{LEAD} + t_{LAG} + t_D \times (34 + N - 2)$$

where:
t_{SPI} = SPI clock period
t_D = Daisy chain clock period
$t_{CS:WAIT}$ = $\overline{CS}$ High time
t_{LEAD} = $\overline{CS}$ Low to first SPI Clock
t_{LAG} = Last SPI Clock $\overline{CS}$ High
n = stack position of target device
N = stack position of TOP device

COMMANDS:

- Scan Voltages
- Scan Temperatures
- Scan Mixed
- Scan Wires
- Scan All
- Measure
- Read
- Write
- Scan Continuous
- Scan Inhibit
- Sleep

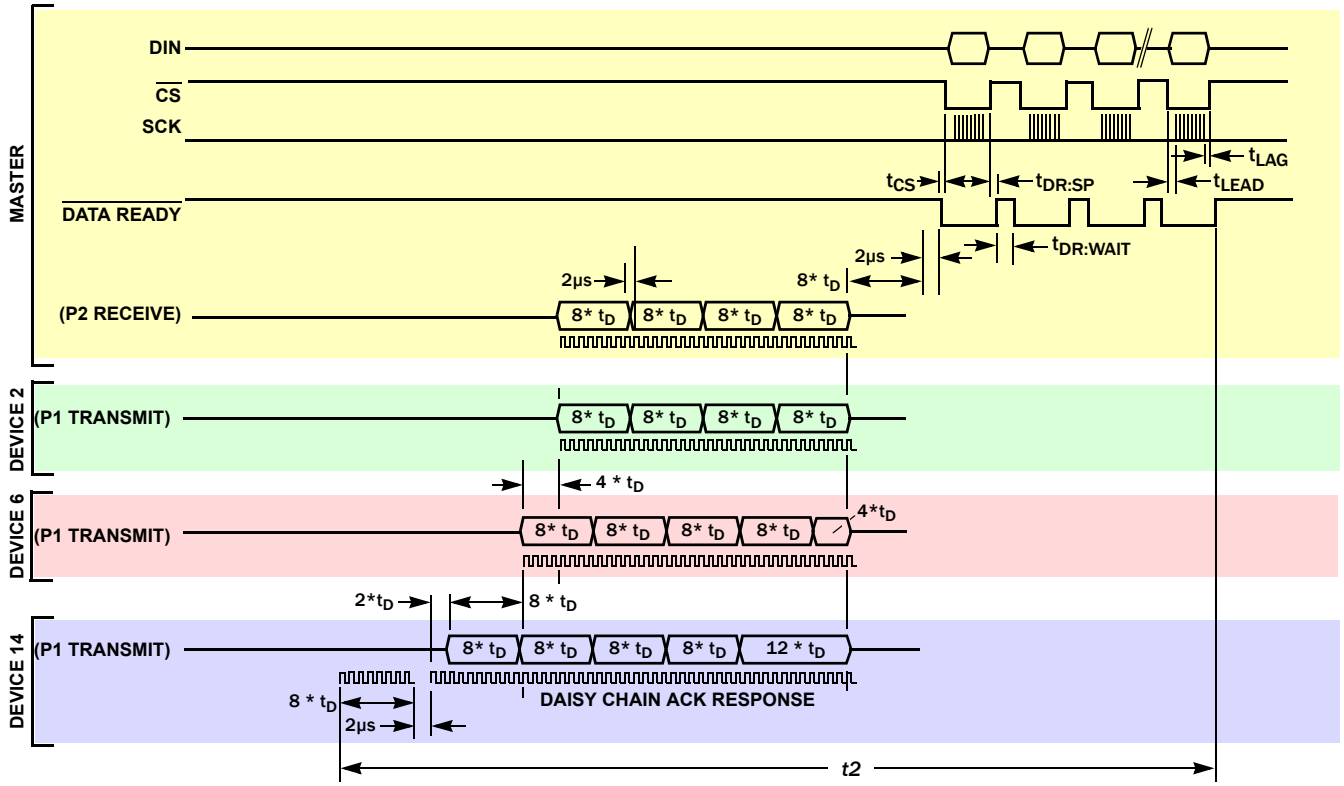
NOTES:

15. Master adds extra byte of zeros as part of daisy protocol.
16. Master adds N-2 clocks to allow communication to the end of the chain.

FIGURE 74. COMMAND TIMING

Response Timing Diagrams

Responses are different for master, middle, and top devices. The response timings are shown in Figures 75, 76, and 77.



$$t2 = (8 \times t_{SPI} + t_{DRSP} + t_{DRWAIT} + t_{CS} + t_{LEAD} + t_{LAG}) \times D - t_{DRSP} + t_D \times (42 + N - 2 + 8) + 4\mu s$$

where:

t_{SPI} = SPI clock period

t_D = Daisy chain clock period

t_{CS} = Host delay from $\overline{\text{DATA READY}}$ Low to the $\overline{\text{CS}}$ Low

t_{DRSP} = $\overline{\text{CS}}$ High to $\overline{\text{DATA READY}}$ High

t_{DRWAIT} = $\overline{\text{DATA READY}}$ High time

t_{LEAD} = $\overline{\text{CS}}$ Low to first SPI Clock

t_{LAG} = Last SPI clock $\overline{\text{CS}}$ High

N = Stack position of top device

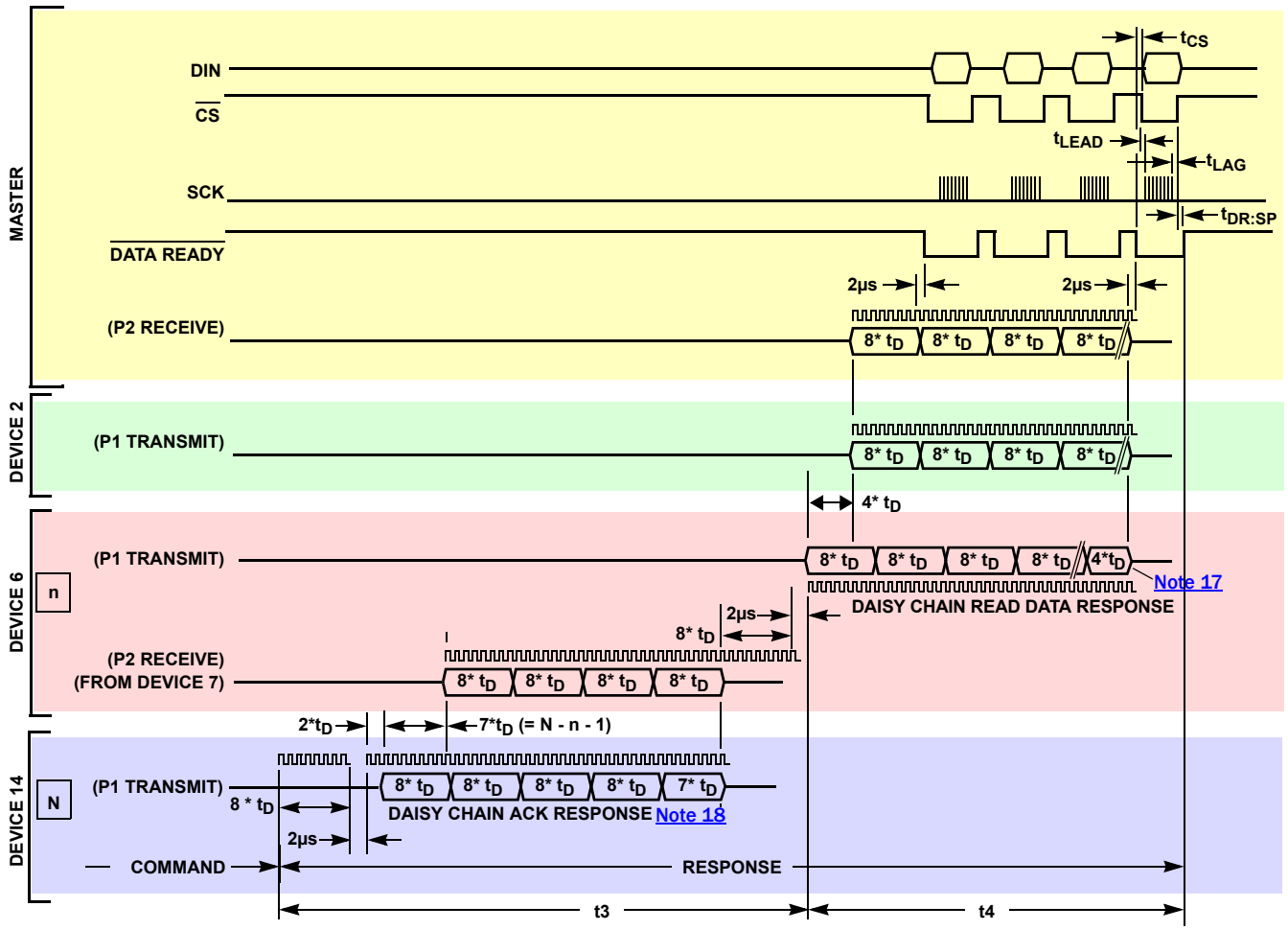
D = Number of data bytes

- D = 4 for one register read (or ACK/NAK response)
- D = 40 for read all voltages
- D = 22 for read all temperatures
- D = 22 for read all faults
- D = 43 for read all setup

FIGURE 75. RESPONSE TIMING (MASTER DEVICE)

Response Timing Diagrams

Responses are different for master, middle, and top devices. The response timings are shown in Figures 75, 76, and 77. **(Continued)**



$$t3 = t_D \times (50 + N - n - 1) + 4\mu s$$

$$t4 = t_{SPI} \times 8 + t_{CS} + t_{LEAD} + t_{LAG} + t_{DRSP} + t_D \times (D \times 8 + n - 2) + 2\mu s$$

where:
t_D = Daisy chain clock period
t_{SPI} = SPI Clock Period
N = Stack position of top device
n = Stack position of middle stack device
t_{CS} = Delay imposed by host from $\overline{DATA\ READY}$ to the first SPI clock cycle
D = Number of bytes in the middle stack device response e.g. read all cell data = 40 bytes, Register or *ACK* response = 4 bytes.

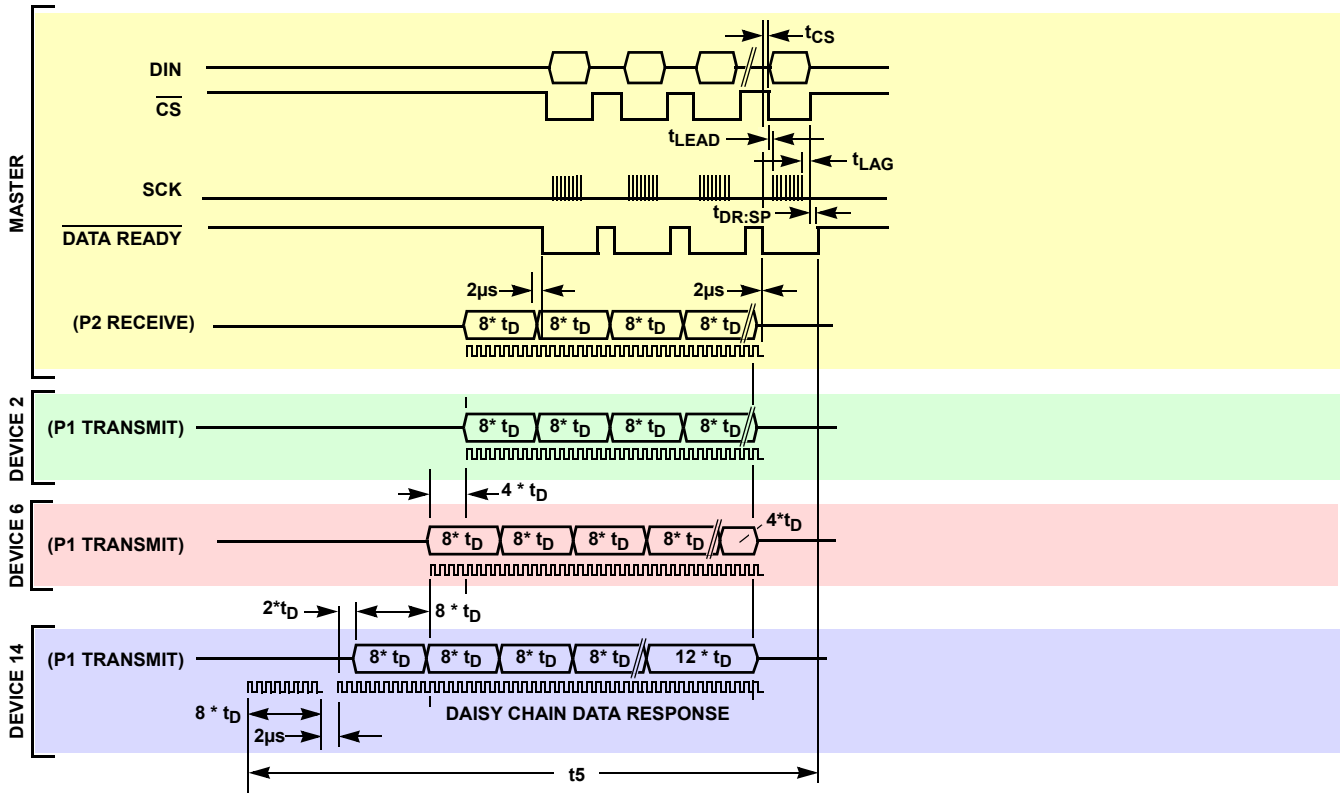
NOTES:

17. Top device adds (N - n - 1) daisy clocks to allow communications to the targeted middle stack device.
18. Middle stack device adds (n - 2) daisy clocks to allow communications to the master device.

FIGURE 76. RESPONSE TIMING (MIDDLE STACK DEVICE)

Response Timing Diagrams

Responses are different for master, middle, and top devices. The response timings are shown in Figures 75, 76, and 77. **(Continued)**



$$t5 = t_{SPI} \times 8 + t_{LEAD} + t_{LAG} + t_{DRSP} + t_{CS} + t_D \times (D \times 8 + 10 + N - 2) + 4\mu s$$

where:
t_{SPI} = SPI clock period
t_D = Daisy chain clock period
t_{CS} = Host delay from $\overline{\text{DATA READY}}$ to the first SPI clock
t_{DRSP} = $\overline{\text{CS}}$ High to $\overline{\text{DATA READY}}$ High
t_{LEAD} = $\overline{\text{CS}}$ Low to first SPI Clock
t_{LAG} = Last SPI Clock $\overline{\text{CS}}$ High
N = Stack position of top device
D = Number of bytes in response

FIGURE 77. RESPONSE TIMING (TOP DEVICE)

System Timing Tables

Command Timing Tables

The command timing (Table 30) includes the time from the start of the command to the start of an internal operation for each device in a stack. Table 31 shows the time required for the command to complete. For a stand-alone device, the two values are the same, because the internal operation starts at the end of the command. For a daisy chain operation, the internal operation begins before the end of the command.

When calculating overall timing for a command, start with the time from the start of the command to the start of the internal operation for the target device. Add to this the time for the internal operation (see "Measurement Timing Tables" on page 68). Add to this the time it takes to read back the data. See times shown in "Response Timing Tables" on page 69. Also needed is a wait time between sending each command (see Table 32).

When using the Address All option, the command timing for the top device in the stack determines when the command ends, but use the Time to Start of Scan for each device to determine when that device begins its internal operation. For example, in a stack of six devices, the command takes 90.9µs to complete, but internal operations start at 13.8µs for the master, 68.7µs for device 2, 70.9µs for device 3, etc.

In Tables 30 and 31, the calculation assumes a daisy chain (and internal) clock that is 10% slower than the nominal and an SPI clock that is running at the nominal speed (because the SPI clock is normally crystal controlled). For the 500kHz daisy setting, timing assumes a 450kHz clock.

TABLE 30. TIME TO START OF INTERNAL OPERATION

TARGET DEVICE	TIME TO START OF INTERNAL OPERATION FOR TARGET DEVICE (µs)	
	SPI CLOCK = 2MHz	
	DAISY CLOCK = 500kHz	DAISY CLOCK = 250kHz
1	17.5	17.5
2	68.7	130.9
3	70.9	135.4
4	73.2	139.8
5	75.4	144.3
6	77.6	148.7
7	79.8	153.2
8	82.1	157.6
9	84.3	162.1
10	86.5	166.5
11	88.7	170.9
12	90.9	175.4
13	93.2	179.8
14	95.4	184.3

TABLE 31. COMMAND TIMING

NUMBER OF DEVICES	TIME TO END OF COMMAND FOR NUMBER OF DEVICES (µs)	
	SPI CLOCK = 2MHz	
	DAISY CLOCK = 500kHz	DAISY CLOCK = 250kHz
1	17.5	17.5
2	82.0	157.6
3	84.2	162.0
4	86.5	166.5
5	88.7	170.9
6	90.9	175.3
7	93.1	179.8
8	95.3	184.2
9	97.6	188.7
10	99.8	193.1
11	102.0	197.6
12	104.2	202.0
13	106.5	206.5
14	108.7	210.9

SEQUENTIAL DAISY CHAIN COMMUNICATIONS

When sending a sequence of commands to the master device, the host must allow time after each response and before sending the next command for the daisy chain ports of all stack devices (other than the master) to switch to receive mode. This wait time is equal to eight daisy chain clock cycles and is imposed from the time of the last edge on the master's input daisy chain port to the last edge of the first byte of the subsequent command on the SPI (see Figure 78). Table 32 shows the minimum recommended wait time between the host receiving the last edge of a response and sending the first edge of the next command for the various daisy chain data rates.

TABLE 32. MINIMUM RECOMMENDED COMMUNICATIONS WAIT TIME

	MAXIMUM TIME FOR DAISY CHAIN PORTS TO CLEAR				UNIT
DAISY CHAIN DATA RATE	500	250	125	62.5	kHz
Communications Wait Time	18	36	72	144	µs

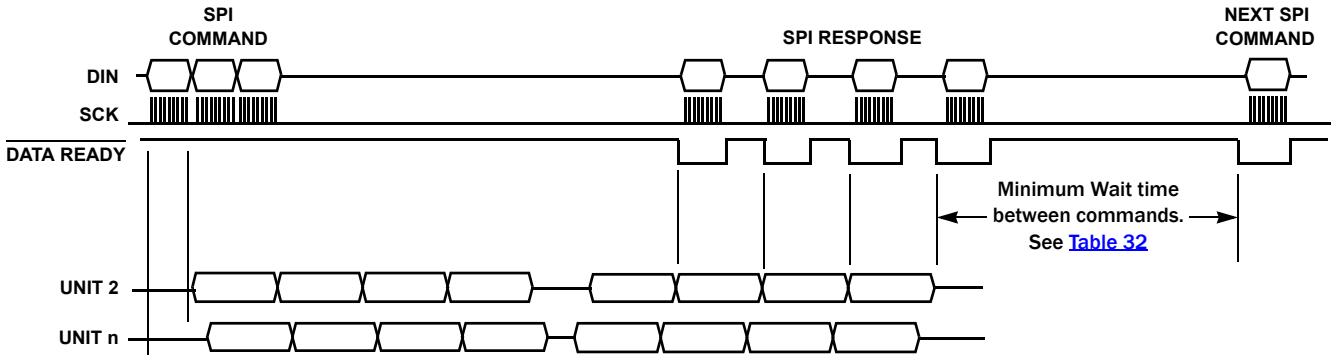


FIGURE 78. MINIMUM WAIT BETWEEN COMMANDS (DAISY CHAIN RESPONSE - TOP DEVICE)

Measurement Timing Tables

SCAN VOLTAGES

The Scan Voltages command initiates a sequence of measurements starting with a scan of each cell input from Cell 12 to Cell 1, followed by a measurement of pack voltage. Additional measurements are then performed for the internal temperature and to check the connection integrity test of the VSS and VBAT inputs. The process completes with the application of calibration parameters and the loading of registers. Table 33 shows the times after the start of scan that the cell voltage inputs are sampled. The voltages are held until the ADC completes its conversion.

TABLE 33. SCAN VOLTAGES FUNCTION TIMING - DAISY CHAIN MASTER OR STAND-ALONE DEVICE

EVENT	TYP (µs)	MAX (µs)
Sample Cell 12	17	19
Sample Cell 11	38	42
Sample Cell 10	59	65
Sample Cell 9	81	89
Sample Cell 8	102	112
Sample Cell 7	123	135
Sample Cell 6	144	159
Sample Cell 5	166	182
Sample Cell 4	187	206
Sample Cell 3	208	229
Sample Cell 2	229	252
Sample Cell 1	251	276
Complete Cell Voltage Capture (ADC complete) Sample VBAT	304	334
Complete VBAT Voltage Capture	318	349
Measure Internal Temperature	423	465
Complete VSS Test	550	605
Complete V_{BAT} Test	726	799
Load Registers	766	842

SCAN TEMPERATURES

The Scan Temperatures command turns on the TEMPREG output and samples the ExT1 to ExT4 inputs after a 2.5ms settling interval. TEMPREG turns off at completion of the ExT4 measurement. The Reference voltage, IC Temperature, and Multiplexer loopback function are also measured. The sequence is completed with respective registers being loaded.

TABLE 34. SCAN TEMPERATURES FUNCTION TIMING – DAISY CHAIN MASTER OR STAND-ALONE DEVICE

EVENT	ELAPSED TIME (µs)	
	TYP	MAX
Turn On TEMPREG	2	2
Sample ExT1	2518	2770
~		
Sample ExT4	2564	2820
Sample Reference	2584	2842
Measure Internal Temperature	2689	2958
Load Registers	2689	2958

SCAN MIXED

The Scan Mixed command performs all the functions of the Scan Voltages command but interposes a measurement of the ExT1 input between the Cell 7 and Cell 6 measurements.

TABLE 35. SCAN MIXED FUNCTION TIMING – DAISY CHAIN MASTER OR STAND-ALONE DEVICE

EVENT	TYP (µs)	MAX (µs)
Sample Cell 12	17	19
Sample Cell 11	38	42
Sample Cell 10	59	65
Sample Cell 9	80	88
Sample Cell 8	101	111
Sample Cell 7	122	134
Complete Cell Voltage Capture 12-7 Sample Ext1	176	194
Complete Ext1 Capture	192	211
Sample Cell 6	207	228
Sample Cell 5	228	251
Sample Cell 4	249	274
Sample Cell 3	270	297
Sample Cell 2	291	321
Sample Cell 1	312	344
Complete Cell Voltage Capture 6-1 Sample V_{BAT}	367	404
Complete V_{BAT} Voltage Capture	381	419
Load Registers	829	911

SCAN WIRES

The Scan Wires command initiates a sequence in which each input is loaded in turn with a test current for a duration of 4.5ms (default). At the end of this time the input voltage is checked and the test current is turned off. The result of each test is recorded and the Open-wire Fault and Fault Status registers are updated (data latched) at the conclusion of the tests.

TABLE 36. SCAN WIRES FUNCTION TIMING – DAISY CHAIN MASTER OR STAND-ALONE DEVICE

EVENT	ELAPSED TIME (ms)	
	TYP	MAX
Turn On VC0 Current	0.03	0.05
Test VC0	4.5	5.0
Turn On Vc1 Current	4.6	5.1
Test VC1	9.1	10.0
~		
Turn On VC12 Current	54.9	60.3
Test VC12	59.4	65.3
Load Registers	59.4	65.3

SCAN ALL

The Scan All command combines the Scan Voltages, Scan Wires, and Scan Temperatures commands into a single scan function.

TABLE 37. SCAN ALL FUNCTION TIMING – DAISY CHAIN MASTER OR STAND-ALONE DEVICE

EVENT	ELAPSED TIME (ms)	
	TYP	MAX
Start Scan Voltages	0	0
Start Scan Wires	0.8	0.9
Start Scan Temperatures	60.1	66.2
Complete Sequence	62.8	69.1

MEASURE COMMAND

Single parameter measurements of the cell voltages, pack voltage, ExT1 to ExT4 inputs, IC temperature and reference voltage are performed using the Measure command.

TABLE 38. VARIOUS MEASURE FUNCTION TIMINGS – DAISY CHAIN MASTER OR STAND-ALONE DEVICE

EVENT	ELAPSED TIME (µs)	
	TYP	MAX
Measure Cell Voltage	178	196
Measure Pack Voltage	122	134
Measure ExT input	2517	2768
Measure IC Temperature	106	116
Measure Reference Voltage	106	116

Response Timing Tables

Response timing depends on the number of devices in the stack, the position of the device in the stack, and how many bytes are read back. There are four “sizes” of read responses. The four types of responses are:

1. Single register read or ACK/NAK responses, where four bytes are returned by the Read Command
2. Read All Voltage response, which returns 40 bytes
3. Read all Temps or Read All Faults responses, which returns 22 bytes
4. Read All Setup Registers response, which returns 43 bytes

In Tables 39 through 44, the master, middle, and top device response times for any number of daisy chain devices are included with the command timing for that configuration. The right hand column shows the total time to complete the read operation. This is calculated as follows:

$$(N \times T_{COMMAND}) + ((N-2) \times T_{MID}) + T_{TOP} + T_{MASTER} \quad \text{(EQ. 4)}$$

where N = Number of devices in the stack.

In the following tables, internal and daisy clocks are assumed to be slow by 10% and the SPI clock is assumed to be at the stated speed.

For example, consider a stack of six devices. To get the full scan time with a daisy clock of 500kHz and SPI clock of 2MHz, it takes 77.6µs from the start of the *Scan All* command to the start of the internal scan of the top device (see Table 30), 842µs to complete an internal scan of all voltages (see Table 33 on page 68), 5.337ms to read all cell voltages from all devices (see Table 41 on page 71), and 18µs delay before issuing another command.

In this case, all cell voltages in the host controller can be updated every 6.28ms.

4-BYTE RESPONSE

Tables 39 and 40 show the calculated timing for read operations for 4-byte responses. This is the timing for an ACK or NAK, as well as a Read Register command.

TABLE 39. READ TIMING (MAX): 4-BYTE RESPONSE, DAISY CLOCK = 500kHz, SPI CLOCK = 2MHz

TOP STACK DEVICE	COMMAND TIME TO START OF RESPONSE (EACH DAISY DEVICE) (µs)	TIME TO COMPLETE RESPONSE (DAISY CHAIN)				COMMAND + RESPONSE ALL DEVICES (µs)
		MASTER DEVICE (µs)	MIDDLE DEVICE (µs)	TOP DEVICE (µs)	ALL DEVICES (µs)	
2	80	139		110	250	410
3	82	142	201	113	455	702
4	85	144	203	115	666	1004
5	87	146	206	117	880	1314
6	89	148	208	119	1099	1633
7	91	151	210	121	1323	1961
8	93	153	212	124	1550	2298
9	96	155	215	126	1783	2643
10	98	157	217	128	2020	2998
11	100	159	219	130	2261	3361
12	102	162	221	133	2506	3734
13	105	164	223	135	2757	4115
14	107	166	226	137	3011	4505

TABLE 40. READ TIMING (MAX): 4-BYTE RESPONSE, DAISY CLOCK = 250kHz, SPI CLOCK = 2MHz

TOP STACK DEVICE	COMMAND TIME TO START OF RESPONSE (EACH DAISY DEVICE) (µs)	TIME TO COMPLETE RESPONSE (DAISY CHAIN)				COMMAND + RESPONSE ALL DEVICES (µs)
		MASTER DEVICE (µs)	MIDDLE DEVICE (µs)	TOP DEVICE (µs)	ALL DEVICES (µs)	
2	156	228		204	432	743
3	160	233	383	208	824	1304
4	165	237	388	213	1226	1884
5	169	242	392	217	1636	2480
6	173	246	397	221	2055	3095
7	178	251	401	226	2483	3727
8	182	255	406	230	2919	4378
9	187	259	410	235	3365	5045
10	191	264	415	239	3820	5731
11	196	268	419	244	4283	6435
12	200	273	423	248	4755	7156
13	205	277	428	253	5237	7895
14	209	282	432	257	5727	8652

40-BYTE RESPONSE

Tables 41 and 42 show the calculated timing for read operations for 40-byte responses. Specifically, this is the timing for a Read All Voltages command.

TABLE 41. READ TIMING (MAX): 40-BYTE RESPONSE, DAISY CLOCK = 500kHz, SPI CLOCK = 2MHz

TOP STACK DEVICE	COMMAND TIME TO START OF RESPONSE (EACH DAISY DEVICE) (µs)	TIME TO COMPLETE RESPONSE (DAISY CHAIN)				COMMAND + RESPONSE ALL DEVICES (µs)
		MASTER DEVICE (µs)	MIDDLE DEVICE (µs)	TOP DEVICE (µs)	ALL DEVICES (µs)	
2	80	643		750	1394	1554
3	82	646	841	753	2239	2486
4	85	648	843	755	3090	3428
5	87	650	846	757	3944	4378
6	89	652	848	759	4803	5337
7	91	655	850	761	5667	6305
8	93	657	852	764	6534	7282
9	96	659	855	766	7407	8267
10	98	661	857	768	8284	9262
11	100	663	859	770	9165	10265
12	102	666	861	773	10050	11278
13	105	668	863	775	10941	12299
14	107	670	866	777	11835	13329

TABLE 42. READ TIMING (MAX): 40-BYTE RESPONSE, DAISY CLOCK = 250kHz, SPI CLOCK = 2MHz

TOP STACK DEVICE	COMMAND TIME TO START OF RESPONSE (EACH DAISY DEVICE) (µs)	TIME TO COMPLETE RESPONSE (DAISY CHAIN)				COMMAND + RESPONSE ALL DEVICES (µs)
		MASTER DEVICE (µs)	MIDDLE DEVICE (µs)	TOP DEVICE (µs)	ALL DEVICES (µs)	
2	156	732		1484	2216	2527
3	160	737	1663	1488	3888	4368
4	165	741	1668	1493	5570	6228
5	169	746	1672	1497	7260	8104
6	173	750	1677	1501	8959	9999
7	178	755	1681	1506	10667	11911
8	182	759	1686	1510	12383	13842
9	187	763	1690	1515	14109	15789
10	191	768	1695	1519	15844	17755
11	196	772	1699	1524	17587	19739
12	200	777	1703	1528	19339	21740
13	205	781	1708	1533	21101	23759
14	209	786	1712	1537	22871	25796

22-BYTE RESPONSE

Tables 43 and 44 show the calculated timing of read operations for 22-byte responses. This is the timing for Read All Temperature or Read All Faults command.

TABLE 43. READ TIMING (MAX): 22-BYTE RESPONSE, DAISY CLOCK = 500kHz, SPI CLOCK = 2MHz

TOP STACK DEVICE	COMMAND TIME TO START OF RESPONSE (EACH DAISY DEVICE) (µs)	TIME TO COMPLETE RESPONSE (DAISY CHAIN)				COMMAND + RESPONSE ALL DEVICES (µs)
		MASTER DEVICE (µs)	MIDDLE DEVICE (µs)	TOP DEVICE (µs)	ALL DEVICES (µs)	
2	80	391		430	822	982
3	82	394	521	433	1347	1594
4	85	396	523	435	1878	2216
5	87	398	526	437	2412	2846
6	89	400	528	439	2951	3485
7	91	403	530	441	3495	4133
8	93	405	532	444	4042	4790
9	96	407	535	446	4595	5455
10	98	409	537	448	5152	6130
11	100	411	539	450	5713	6813
12	102	414	541	453	6278	7506
13	105	416	543	455	6849	8207
14	107	418	546	457	7423	8917

TABLE 44. READ TIMING (MAX): 22-BYTE RESPONSE, DAISY CLOCK = 250kHz, SPI CLOCK = 2MHz

TOP STACK DEVICE	COMMAND TIME TO START OF RESPONSE (EACH DAISY DEVICE) (µs)	TIME TO COMPLETE RESPONSE (DAISY CHAIN)				COMMAND + RESPONSE ALL DEVICES (µs)
		MASTER DEVICE (µs)	MIDDLE DEVICE (µs)	TOP DEVICE (µs)	ALL DEVICES (µs)	
2	156	480		844	1324	1635
3	160	485	1023	848	2356	2836
4	165	489	1028	853	3398	4056
5	169	494	1032	857	4448	5292
6	173	498	1037	861	5507	6547
7	178	503	1041	866	6575	7819
8	182	507	1046	870	7651	9110
9	187	511	1050	875	8737	10417
10	191	516	1055	879	9832	11743
11	196	520	1059	884	10935	13087
12	200	525	1063	888	12047	14448
13	205	529	1068	893	13169	15827
14	209	534	1072	897	14299	17224

System Diagnostics Functions

The system uses the following four types of faults to determine the overall health of the system:

1. Automatic Fault detection within the IC.
2. Fault detection that is automatic, but requires the host microcontroller to initiate an operation.
3. Faults that are detected by the host microcontroller during normal communication. This includes lack of response or responses that indicate a fault condition.
4. Faults that are detected by the host microcontroller following a series of commands and responses that check various internal and external circuits.

Hardware Fault Detection

The ISL78610 is always checking the internal V3P3, V2P5, and VREF power supplies using window comparators. If any of these voltages exceed a programmed limit (either too high or too low), a REG fault occurs. This immediately starts an alarm response. See "Alarm Response" on page 76.

The ISL78610 also checks the two oscillators continually. The high speed and low speed oscillators are compared against limits and against each other. If there is a deviation greater than programmed, then an OSC fault exists. This immediately starts an alarm response. See "Alarm Response" on page 76.

System Out of Limit Detection

Bits are set in the fault data registers for detection of:

- Overvoltage
- Undervoltage
- Open-wires
- Over-temperature
- Open VBAT
- Open VSS

The Overvoltage, undervoltage, over-temperature, and open-wire conditions have individual fault bits for each cell input. These bits are OR'd and reflected to bits in the Fault Status register (one bit per data register). The Open VBAT and Open VSS have one bit each in the Fault Status register.

These conditions are not detected unless the host initiates a scan operation. The cell overvoltage, cell undervoltage, V_{BAT} open, and V_{SS} open faults are sampled at the same time at the end of a Scan Voltages command. The cell undervoltage and cell overvoltage signals are also checked following a Measure Cell Voltage command. These conditions are also checked during a Scan Continuous operation. If the host initiates a Scan Continuous operation, the status is checked automatically every scan cycle, without further host involvement. For any other Scan command, the host needs to periodically send the command to perform another check of the system.

FAULT SIGNAL FILTERING

Filtering is provided for the cell overvoltage, cell undervoltage, V_{BAT} open, and V_{SS} open tests. These fault signals use a totalizing method in which an unbroken sequence of positive results is required to validate a fault condition. The sequence length (number of sequential positive samples) is set by the [TOT2:0] bits in the Fault Setup register. See Table 46 on page 74.

If the host sends a Scan Continuous command, the Scan Interval and the Totalizer value set the Fault Detection time. See Table 45.

Each cell input, VBAT, and VSS open circuit has separate filter functions. The filter is reset whenever a test results in a negative result (no fault). All filters are reset when the Fault Status register bits are changed. When a fault is detected, the bits must be rewritten.

Any out of limit condition generates an Alarm response. See "Alarm Response" on page 76.

TABLE 45. FAULT DETECTION TIME AS A FUNCTION OF SCAN INTERVAL AND NUMBER OF TOTALIZED SAMPLES

SCAN INTERVAL CODE	SCAN INTERVAL (ms)	FAULT DETECTION TIME								
		000	001	010	011	100	101	110	111	FAULT SETUP REGISTER
		1	2	4	8	16	32	64	128	TOTALIZER VALUE
0000	16	16	32	64	128	256	512	1024	2048	
0001	32	32	64	128	256	512	1024	2048	4096	
0010	64	64	128	256	512	1024	2048	4096	8192	
0011	128	128	256	512	1024	2048	4096	8192	16384	
0100	256	256	512	1024	2048	4096	8192	16384	32768	
0101	512	512	1024	2048	4096	8192	16384	32768	65536	
0110	1024	1024	2048	4096	8192	16384	32768	65536	131072	
0111	2048	2048	4096	8192	16384	32768	65536	131072	262144	
1000	4096	4096	8192	16384	32768	65536	131072	262144	524288	
1001	8192	8192	16384	32768	65536	131072	262144	524288	1048576	
1010	16384	16384	32768	65536	131072	262144	524288	1048576	2097152	
1011	32768	32768	65536	131072	262144	524288	1048576	2097152	4194304	
1100	65536	65536	131072	262144	524288	1048576	2097152	4194304	8388608	

TABLE 46. FAULT SETUP REGISTER

REGISTER BITS																	
12	11	10	9		8		7	6	5		4		3	2	1	0	
TST4	TST3	TST2	TST1	ENABLE	TST0	INTERNAL TEMP	TOT2	TOT1	TOT0	TOTALIZER COUNT	WSCN	SCAN WIRES	SCN1	SCN0	SCN1	SCN0	SCAN INTERVAL TIME (ms)
0	0	0	0	None	0	Disable	0	0	0	1	0	Track Voltage Scan	0	0	0	0	16
x	x	x	1	ExT1	1	Enable	0	0	1	2	1	Track Temp Scan	0	0	0	1	32
x	x	1	x	ExT2			0	1	0	4			0	0	1	0	64
x	1	x	x	ExT3			0	1	1	8			0	0	1	1	128
1	x	x	x	ExT4			1	0	0	16			0	1	0	0	256
							1	0	1	32			0	1	0	1	512
							1	1	0	64			0	1	1	0	1024
							1	1	1	128			0	1	1	1	2048
													1	0	0	0	4096
													1	0	0	1	8192
													1	0	1	0	16384
													1	0	1	1	32768
													1	1	0	0	65536

Diagnostic Activity Settling Time

The majority of diagnostic functions within the ISL78610 do not affect other system activity and there is no requirement to wait before conducting further measurements. The exceptions to this are the open-wire test and cell balancing functions.

OPEN-WIRE TEST

The open-wire test loads each VCn pin in turn with 150µA or 1mA current. This disturbs the cell voltage measurement while the test is being applied. For example, a 1mA test current applied with an input path resistance of 1kΩ reduces the pin voltage by 1V. The time required for the cell voltage to settle following the open-wire test is dependent on the time constant of components used in the cell input circuit. The standard input circuit (Figure 51 on page 31) with the components given in Table 11 on page 38 provide settling to within 0.1mV in approximately 2.8ms. This time should be added at the end of each open-wire scan to allow the cell voltages to settle.

CELL BALANCING

The standard applications circuit (Figure 51 on page 31) configures the balancing circuits so that the cell input measurement reads close to 0V when balancing is activated. There are time constants associated with the turn-on and turn-off characteristics of the cell balancing system that must be allowed for when conducting cell voltage measurements.

The turn-on time of the balancing circuit is primarily a function of the 25µA drive current of the cell balancing output and the gate charge characteristic of the MOSFET and needs to be determined for a particular setup. Turn-on settling times to within 2mV of final “on” value are typically less than 5ms.

The turn-off time is a function of the MOSFET gate charge and the VGS connected resistor and capacitor values (for example, R_{27} and C_{27} in Figure 51 on page 31) and is generally longer than the turn-on time. As with the turn-on case, the turn-off time needs to be determined for the particular components used. Turn-off settling times in the range 10ms to 15ms are typical for settling to within 0.1mV of final value.

Memory Checksum

Two checksum operations are available to the host microcontroller for checking memory integrity - one for the EEPROM and one for the Page 2 registers.

Two registers are provided to verify the contents of EEPROM memory. The first (Page 4, address 6’h3F) contains the correct checksum value, which is calculated during factory testing at Renesas. The other (Page 5, address 6’h00) contains the checksum value calculated each time the nonvolatile memory is loaded to shadow registers, either after a power cycle or after a device reset. An inequality between these two numbers indicates corruption of the shadow register contents (and possible corruption of EEPROM data). The external microcontroller needs to compare the two registers because it is not automatic. Resetting the device (using the Reset command) reloads the shadow registers. A persistent difference between these two register values indicates EEPROM corruption.

All Page 2 registers (device configuration registers) are subject to a checksum calculation. A Calculate Register Checksum command calculates the Page 2 checksum and saves the value internally (it is not accessible). The Calculate Register Checksum command can be run any time, but should be sent whenever a Page 2 register is changed.

A Check Register Checksum command recalculates the Page 2 checksum and compares it to the internal value. The occurrence of a Page 2 checksum error sets the PAR bit in the Fault Status register and causes a Fault response accordingly. The normal response to a PAR error is for the host microcontroller to rewrite the Page 2 register contents. A PAR fault also causes the device to cease any scanning or cell balancing activity.

See items 42 through 49 in Table 50 on page 77.

Communication Faults

There is no specific flag to indicate a communications fault. A fault is indicated by receiving an abnormal communications response or by an absence of all communications.

Non-daisy chain device commands and responses use CRC (Cyclical Redundancy Check) error detection (stand-alone systems do not use the CRC). If a CRC is not recognized by a target device, a command includes an Address All when it is not allowed, or if there are too few bits in the sequence there is a NAK response. The host can tell where this fault occurred by reading the Device address.

No response indicates a communications failure.

Communication Failure

All commands except the Scan, Measure, and Reset commands require a response from either the stack top device or the target device (see Table 13 on page 40). Each device in the stack waits for a response from the stack device above. Correct receipt of a command is indicated by the correct response. Failure to receive a response within a timeout period indicates a communications failure. The timeout value is stack position dependent. The device that detects the fault, then transmits the communications failure response which includes its stack address.

If the target device receives a communications failure response from the device above, the target device relays the communications failure followed by the requested data (in the case of a read) or simply relays the communications failure only (in the case of a Write, Balance command, etc). The maximum time required to return the communications failure response to the host microcontroller (the time from the falling edge of the 24th clock pulse of an SPI command to receiving a $\overline{\text{DATA READY}}$ low signal) is given for various data rates in Table 47.

TABLE 47. MAXIMUM TIME TO COMMUNICATIONS FAILURE RESPONSE

	MAXIMUM TIME TO ASSERTION OF $\overline{\text{DATA READY}}$				
DAISY CHAIN DATA RATE (kHz)	500	250	125	62.5	UNIT
Communications Failure Response	5.8	11.6	23.2	46.4	ms

A communications fault can be caused by one of three circumstances:

1. The communications system has been compromised
2. The device causing the fault is in Sleep mode
3. A daisy chain input port is in the wrong idle state

This latter condition is unlikely but could arise in response to external influence, such as a large transient event. The daisy chain ports are forced to the correct idle condition at the end of each communication. An external event has the potential to “flip” the input so that the port settles in the inverse state.

A flipped input condition recovers during the normal course of communications. If a flipped input is suspected, having received notification of a communications fault condition for example, the user can send a sequence of all 1s (for example, FF FF FF FF) to clear the fault. Wait for the resulting NAK response, then send an ACK to the device that reported the fault. The “all 1” sequence allows a device to correct a flipped condition through the normal end of the communication process. The command FB FF FF FF also works and contains the correct CRC value (should this be a consideration in the way the control software is set up).

If the process above results in a communications failure response, the next step is for the host microcontroller to send a Sleep command, wait for all stack devices to go to sleep, then send a Wake-up command. If successful, the host microcontroller receives an ACK when all devices are awake. If a single stack device is asleep, the devices above the sleeping device do not receive the Sleep command and respond to the Wake-up sequence with a NAK due to incomplete communications. The host microcontroller then sends a command (for example, ACK) to check that all devices are awake. This process can be repeated as often as needed to wake up sleeping devices.

If the Wake-up command does not generate a response, this likely indicates that the communications have been compromised. The host microcontroller may send a Sleep command to all units. If the communications watchdog is enabled, all parts go to Sleep mode automatically when the watchdog period expires as long as there is no valid communications activity. Table 13 on page 40 provides a summary of the normal responses and an indication if the device waits for a response from the various communications commands.

Daisy Chain Communications Conflicts

Conflicts in the daisy chain system can occur if both a stack device and the host microcontroller are transmitting at the same time, or if more than one stack device transmits at the same time. Conflicts caused by a stack device transmitting at the same time as the host microcontroller are recognized by the absence of the required response (for example, an ACK response to a write command), or by the scan counter not being incremented in the case of Scan and Measure commands.

Conflicts that arise from more than one device transmitting simultaneously can occur if two devices detect faults at the same time. This can occur when the stack is operating normally (for example, if two devices register an undervoltage fault in response to a Scan Voltages command sent to all devices). It is recommended that the host microcontroller checks the Fault Status register contents of all devices whenever a Fault response is received from one device.

Loss of Signal from Host

A watchdog timer is provided as part of the daisy chain communications fault detection system. The watchdog has no effect in non-daisy chain systems.

Each device must receive a valid communications sequence before its watchdog timeout period is exceeded. A valid communications sequence requires an action or response from the device. Address All commands, such as the Scan and Balance commands, provide a simple way to reset the watchdog timers on all devices with a single communication. Single device communications (for example, ACK) must be sent individually to each device to reset the watchdog timer in that device. A read of the Fault Status register of each device is also a good way to reset the watchdog timer on each device. This functionality guards against situations in which a runaway host microcontroller might continually send data.

Failure to receive valid communications within the required time causes the WDGF bit to be set in the Fault Status register and the device to be placed in Sleep mode, with all measurement and balancing functions disabled. Daisy chain devices assert the $\overline{\text{FAULT}}$ output in response to a watchdog fault and maintain this asserted state while in Sleep mode. Note that no watchdog fault response is automatically sent on the daisy chain interface.

WATCHDOG FUNCTION

The watchdog timeout is settable in two ranges using the lower seven bits of the Watchdog/Balance time register (see Table 48). The low range (7'b0000001 to 7'b0111111) provides timeout settings in 1 second increments from 1 second to 63 seconds. The high range (7'b1000000 to 7'b1111111) provides timeout settings in 2 minute intervals from 2 minutes to 128 minutes (see Table 48 for details).

TABLE 48. WATCHDOG/BALANCE TIME REGISTER

REGISTER BITS							
6	5	4	3	2	1	0	
WDG6	WDG5	WDG4	WDG3	WDG2	WDG1	WDG0	WATCHDOG TIMEOUT
0	0	0	0	0	0	0	Disabled
0	0	0	0	0	0	1	1s
0	0	0	0	0	1	0	2s
• • •							-
0	1	1	1	1	1	0	62s
0	1	1	1	1	1	1	63s
1	0	0	0	0	0	0	2min
1	0	0	0	0	0	1	4min
• • •							-
1	1	1	1	1	1	0	126min
1	1	1	1	1	1	1	128min

A zero setting (7'b0000000) disables the watchdog function. A watchdog password function is provided to guard against accidental disabling of the watchdog function. The upper six bits of the Device Setup register must be set to 6'h3A (111010) to allow the watchdog to be set to zero. The watchdog is disabled by first writing the password to the Device Setup register (see "Set-Up Registers" on page 88) and then writing zero to the lower bits of the Watchdog/Balance time register. The password function does not prevent changing the watchdog timeout setting to a different nonzero value.

The watchdog continues to function when the ISL78610 is in Sleep mode. Parts in Sleep mode assert the $\overline{\text{FAULT}}$ output when the watchdog timer expires.

WATCHDOG PASSWORD

Before writing a zero to the watchdog timer, which turns off the timer, write a password to the [WP5:0] bits. The password value is 6'h3A.

Alarm Response

If any of the fault bits are set, the $\overline{\text{FAULT}}$ logic output is asserted low in response to the fault condition. The output then remains low until the bits of the Fault Status register are reset. Individual bits in the fault data registers must be cleared before the associated bits in the Fault Status register can be cleared.

If the device is in a daisy chain, the Fault logic also sends an "unprompted" response down the daisy chain to the master, which notifies the host microcontroller that a problem exists.

The daisy chain fault response is immediate as long as there is no communications activity on the device ports, and comprises the normal Fault Status register read response. As such, it includes the contents of the Status Register and includes the device address that is reporting the fault.

The Fault response is sent only for the first fault occurrence. Subsequent faults do not activate the Fault response until after the Fault Status register has been cleared. If multiple devices report a fault, the response shows the results from the lowest stack device.

If a fault occurs while the device ports are active, the device waits until communications activity ceases before sending the Fault response. The host microcontroller has the option to wait for this response before sending the next message. Alternately, the host microcontroller can send the next message immediately (after allowing the daisy chain ports to clear – see "Sequential Daisy Chain communications" on page 67). Any conflicts resulting from additional transmissions from the stack are recognized by the lack of response from the stack.

Table 49 provides the maximum time from $\overline{\text{DATA READY}}$ going low for the last byte of the normal response to $\overline{\text{DATA READY}}$ going low for the first byte of the Fault response when a Fault response is delayed by active communications.

TABLE 49. MAXIMUM TIME BETWEEN DATA READY SIGNALS – DELAYED FAULT RESPONSE

	MAXIMUM TIME BETWEEN $\overline{\text{DATA READY}}$ ASSERTIONS				
DAISY CHAIN DATA RATE (kHz)	500	250	125	62.5	UNIT
Fault Response	68	136	272	544	µs

Further read communications to the device return the Fault response followed by the requested data. Write communications return only the Fault response. Action commands return nothing. The host microcontroller resets the register bits corresponding to the fault by writing 14'h0000 to the Fault Status register, having first cleared the bits in the Fault Data register(s) if these are set. The device then responds ACK as with a normal write response because the fault status bits are now cleared. This also prevents further Fault responses unless the fault reappears, in which case the Fault response is repeated.

Additionally, the fault status of each part can be obtained at any time by reading the Fault Status register.

The $\overline{FAULT}$ logic output is asserted in Sleep mode if a fault has been detected and has not been cleared.

FAULT RESPONSE IN SLEEP MODE

When a stand-alone device is in Sleep mode, the device may still detect faults if operating in Scan Continuous mode. If an error occurs, the $\overline{FAULT}$ output pin is asserted low.

Devices may detect faults if operating in Scan Continuous mode while also in Sleep mode.

Daisy chain devices registering a fault in Sleep mode wake up the other devices in the stack (for example, middle devices send the Wake-up signal on both ports). Any communications received by a device on one port while it is transmitting the Wake-up signal on its other port are ignored. After receiving the Wake-up signal, the top stack device waits before sending an ACK response on Port 1. This is to allow other stack devices to wake up. The total wait time is dependent on the number of devices in the stack. The time from a device detecting a fault to receipt of the ACK response is also dependent on the stack position of the device. See Table 17 for maximum response times for stacks of 8 and 14 devices.

The normal host microcontroller response to receiving an ACK while the stack is in Sleep mode is to read the Fault Status register contents of each device in the stack to determine which device (or devices) has a fault.

Fault Diagnostics

Table 50 shows a summary of commands and responses for the various fault diagnostics functions.

TABLE 50. SUMMARY OF FAULT DIAGNOSTICS COMMANDS AND RESPONSES

ITEM	DIAGNOSTIC FUNCTION	ACTION REQUIRED	REGISTER READ/WRITE	COMMENTS
1	Static fault detection functions	Check Fault Status (or look for normal fault response)	Read Fault Status register	The main internal functions of the ISL78610 are monitored continuously. Bits are set in the Fault Status register in response to faults being detected in these functions.
2	Oscillator check function	Check for device in Sleep mode if stack returns a Communications Failure response		Oscillator faults are detected as part of the Static Fault detection functions. The response to an oscillator fault detection is to set the OSC bit in the Fault Status register and to enter Sleep mode. A sleeping device does not respond to normal communications, producing a Communications Failure notification from the next device down the stack. The normal recovery procedure is to send repeated Sleep and Wake-up commands to ensure all devices are awake.
3	Cell overvoltage	Set cell overvoltage limit	Write Overvoltage Limit register	Full scale value 14'h1FFF = 5V
4		Set fault filter sample value	Write TOT bits in Fault Setup register	Default is 3'b011 (eight samples) - (see "Fault Setup:" on page 86)
5		Identify which inputs have cells connected	Write Cell Setup register	A '0' bit value indicates the cell is connected. A '1' bit value indicates no cell is connected to this input. The overvoltage test is not applied to unconnected cells.
6		Scan cell voltages	Send Scan Voltages command	A cell overvoltage condition is flagged after a number of sequential overvoltage conditions are recorded for a single cell. The number is programmed in item 4.
7		Check fault status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected and if the register value is zero before the fault is detected.
8		Check overvoltage fault register	Read Overvoltage Fault register	Required only if the Fault Status register returns a fault condition.
9		Reset fault bits		Reset the bits in Overvoltage Fault register followed by the bits in Fault Status register.
10		Reset fault filter		Change the value of the [TOT2:0] bits in the Fault Setup register, then change back to the required value. This resets the filter. The filter is also reset if a false overvoltage test is encountered.

TABLE 50. SUMMARY OF FAULT DIAGNOSTICS COMMANDS AND RESPONSES (Continued)

ITEM	DIAGNOSTIC FUNCTION	ACTION REQUIRED	REGISTER READ/WRITE	COMMENTS
11	Cell Undervoltage	Set cell undervoltage limit	Write Undervoltage Limit register	Full scale value 14'h1FFF = 5V
12		Set fault filter sample value	Write TOT Bits in Fault Setup register	Default is 3'b011 (eight samples)
13		Identify which inputs have cells connected	Write Cell Setup register	A '0' bit value indicates the cell is connected. A '1' bit value indicates no cell is connected to this input. The undervoltage test is not applied to unconnected cells.
14		Scan cell voltages	Send Scan Voltages command	A cell undervoltage condition is flagged after a number of sequential undervoltage conditions are recorded for a single cell. The number is programmed in item 12.
15		Check fault status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected and if the register value is zero before the fault is detected.
16		Check undervoltage fault register	Read Undervoltage Fault register	Required only if the Fault Status register returns a fault condition.
17		Reset fault bits		Reset the bits in Undervoltage Fault register followed by the bits in Fault Status register.
18		Reset fault filter		Change the value of the [TOT2:0] bits in the Fault Setup register, then change back to the required value. This resets the filter. The filter is also reset if a false undervoltage test is encountered.
19	V_{BAT} or VSS Connection Test	Set fault filter sample value	Write TOT bits in Fault Setup register	Default is 3'b011 (eight samples)
20		Scan cell voltages	Send Scan Voltages command	A open condition on V_{BAT} or VSS is flagged after a number of sequential open conditions are recorded for a single cell. The number is programmed in item 19.
21		Check Fault Status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected and if the register value is zero before the fault is detected.
22		Reset fault bits		Reset bits in the Fault Status register.
23		Reset fault filter		Change the value of the [TOT2:0] bits in the Fault Setup register, then change back to the required value. This resets the filter. The filter is also reset if a false open test is encountered.
24	Open-Wire Test	Set Scan current value	Write Device Setup register: ISCN = 1 or 0	Sets scan current to 1mA (recommended) by setting ISCN = 1. Or, set the scan current to 150µA by setting ISCN = 0.
25		Identify which inputs have cells connected	Write Cell Setup register	A '0' bit value indicates the cell is connected. A '1' bit value indicates no cell is connected to this input. Cell inputs VC2 to VC12: the open-wire detection system is disabled for cell inputs with a '1' setting in the Cell Setup register. Cell inputs VC0 and VC1 are not affected by the Cell Setup register.
26		Activate Scan Wires function	Send Scan Wires command	Wait for Scan Wires to complete.
27		Check Fault Status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected and if the register value is zero before the fault is detected.
28		Check Open-Wire Fault register	Read Open-Wire Fault register	Required only if the Fault Status register returns a fault condition.
29		Reset fault bits		Reset the bits in Open-Wire Fault register followed by the bits in Fault Status register.
30	Over-Temperature Indication	Set external temperature limit	Write External Temp Limit register	Full scale value 14'h3FFF = 2.5V

TABLE 50. SUMMARY OF FAULT DIAGNOSTICS COMMANDS AND RESPONSES (Continued)

ITEM	DIAGNOSTIC FUNCTION	ACTION REQUIRED	REGISTER READ/WRITE	COMMENTS
31		Identify which inputs are required to be tested	Write Fault Setup register Bits TST1 to TST4	A '1' bit value indicates the input is tested. A '0' bit value indicates the input is not tested.
32		Scan temperature inputs	Send Scan Temperatures command	An over-temperature condition is flagged immediately if the input voltage is below the limit value.
33		Check Fault Status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected and if the register value is zero before the fault is detected.
34		Check Over-temperature Fault register	Read Over-temperature Fault register	Required only if the Fault Status register returns a fault condition.
35		Reset fault bits		Reset the bits in Over-temperature Fault register followed by the bits in Fault Status register.
36	Reference Check Function	Read reference coefficient A	Read Reference Coefficient A register	
37		Read reference coefficient B	Read Reference Coefficient B register	
38		Read reference coefficient C	Read Reference Coefficient C register	
39		Scan temperature inputs	Send Scan Temperatures command	
40		Read reference voltage value	Read Reference Voltage register	
41		Calculate voltage reference value		See Voltage Reference Check Calculation in the Worked Examples section of this datasheet (see "Voltage Reference Check Calculation" on page 80).
42	Register Checksum	Calculate register checksum value	Send Calculate Register Checksum command	Causes the ISL78610 to calculate a checksum based on the current contents of the Page 2 registers. This action must be performed each time a change is made to the register contents. The checksum value is stored for later comparison.
43		Check register checksum value	Send Check Register Checksum command	The checksum value is recalculated and compared to the value stored by the previous Calculate Register Checksum command. The PAR bit in the Fault Status register is set if these two numbers are not the same.
44		Check Fault Status	Read Fault Status register	The device sends the Fault Status register contents automatically if a fault is detected and if the register value is zero before the fault is detected.
45		Re-write registers	Load all Page 2 registers with their correct values.	This is required only if a PAR fault is registered. It is recommended that the host reads back the register contents to verify values prior to sending a Calc Register Checksum command.
46		Reset fault bits		Reset the bits in the Fault Status register.
47	EEPROM MISR Checksum	Read checksum value stored in EEPROM	Read the EEPROM MISR Register	
48		Read checksum value calculated by ISL78610	Read the MISR Checksum register	The checksum value is calculated each time the EEPROM contents are loaded to registers, either following the application of power, cycling the EN pin followed by a host initiated Reset command, or simply the host issuing a Reset command.
49		Compare checksum values		Correct function is indicated by the two values being equal. Memory corruption is indicated by an unequal comparison. In this event the host should send a Reset command and repeat the check process.

Worked Examples

The following worked examples are provided to assist with the setup and calculations associated with various functions.

Voltage Reference Check Calculation

TABLE 51. EXAMPLE REGISTER DATA

R/W	PAGE	ADDRESS	PARAMETER	VALUE (HEX)	DECIMAL
0	001	010000	IC Temperature	14'h2425	9253
0	001	010101	Reference Voltage	14'h20A7	8359
0	010	111000	Coefficient C	14'h00A4	164
0	010	111001	Coefficient B	14'h3FCD	-51
0	010	111010	Coefficient A	9'h006	6

Coefficients A, B, and C are two's complement numbers. B and C have a range +8191 to -8192. A has a range +255 to -256.

Coefficient B above is a negative number (Hex value > 1FFF). The value for B is 14'h3FCD - 14h3FFF- 1 or (16333_{10} - 16383_{10} - 1) = -51.

Coefficient A occupies the upper nine bits of register 6'b111010 (6'h3A). One way to extract the coefficient data from this register is to divide the complete register value by 32 and round the result down to the nearest integer. With 9'h006 in the upper nine bits, and assuming the lower five bits are 0, the complete register value will be 14'h0C0 = 192 decimal. Divide this by 32 to obtain 6.

Coefficients A, B, and C are used with the IC temperature reading to calibrate the Reference Voltage reading. The calibration is applied by subtracting an adjustment of the form from the reference voltage reading:

$$\text{Adjustment} = \frac{A}{256 \times 8192} \times dT^2 + \frac{B}{8192} \times dT + C \quad \text{(EQ. 5)}$$

An example calculation using the data of Table 51 is given in Equation 6.

$$dT = \frac{9253 - 9180}{2} = 36.5 \quad \text{(EQ. 6)}$$

where 9180 is the internal temperature monitor reading at +25°C (see the ""MEASUREMENT SPECIFICATIONS" on page 8).

$$\text{Adjustment} = \frac{6}{256 \times 8192} \times (36.5)^2 - \frac{51}{8192} \times 36.5 + 164 = 163.8 \quad \text{(EQ. 7)}$$

$$\text{Corrected } V_{REF} = 8359 - 163.8 = 8195.2 \quad \text{(EQ. 8)}$$

$$V_{REF} \text{ value} = \frac{8195.2}{16384} \times 5 = 2.5010 \quad \text{(EQ. 9)}$$

Cell Balancing – Manual Mode

Refer to "Manual Balance Mode" on page 46.

EXAMPLE: ACTIVATE BALANCING ON CELLS 1, 5, 7 AND 11

Step 1. Write the Balance Setup register: Set Manual Balance mode, Balance Status pointer, and turn off balance.

BMD = 01 (Manual Balance mode)
BWT = XXX
BSP = 0000 (Balance Status Pointer location 0)
BEN = 0 (Balancing disabled)

Note: Blue text indicates a register change.

TABLE 52. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX00 000X XX01

"X" values can be set to any number.

Step 2. Write the Balance Status register: Set Bits 0, 4, 6, and 10.

BAL12:1 = 0100 0101 0001

TABLE 53. BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 0100 0101 0001

Step 3. Enable balancing using the Balance Enable command.

TABLE 54. BALANCE ENABLE COMMAND

R/W	PAGE	ADDRESS	DATA
0	011	010000	00 0000

or enable balancing by setting BEN directly in the Balance Setup register:

BEN = 1

TABLE 55. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX1X XXXX XXXX

The balance FETs attached to Cells 1, 5, 7, and 11 turn on.

Turn balancing off by resetting BEN or by sending the Balance Inhibit command (Page 3, address 6'h11).

Cell Balancing – Timed Mode

Refer to "Timed Balance Mode" on page 47.

EXAMPLE: ACTIVATE BALANCING ON CELLS 2 AND 8 FOR 1 MINUTE.

Step 1. Write the Balance Setup register: Set Timed Balance mode, Balance Status pointer, and turn off balance.

BMD = 10 (Timed Balance mode)
BWT = XXX
BSP = 0000 (Balance Status Pointer location 0)
BEN = 0 (BALANCING disabled)

TABLE 56. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX00 000X XX10

"X" values can be set to any number.

Step 2. Write the Balance Status register: Set Bits 1 and 7.

BAL12:1 = 0000 1000 0010

TABLE 57. BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 0000 1000 0010

Step 3. Write the balance timeout setting to the Watchdog/Balance Time register (Page 2, address 6'h15, Bits [13:7]).

BTM6:1 = 0000011 (1 minute)

TABLE 58. WATCHDOG/BALANCE TIME REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010101	00 0001 1XXX XXXX

"X" values can be set to any number – the lower bits are the watchdog timeout value and should be set to a time longer than the balance time. A value of 111 1111 is suggested.

Step 4. Enable balancing using the Balance Enable command.

TABLE 59. BALANCE ENABLE COMMAND

R/W	PAGE	ADDRESS	DATA
0	011	010000	00 0000

or enable balancing by setting BEN directly in the Balance Setup register:

BEN = 1

TABLE 60. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX1X XXXX XXXX

The balance FETs attached to Cells 2 and 8 turn on. The FETs turn off after 1 minute. Balancing can be stopped by resetting BEN or by sending the Balance Inhibit command.

Cell Balancing – Auto Mode

Refer to "Auto Balance Mode" on page 47.

BALANCE VALUE CALCULATION EXAMPLE

This example is based on a cell State of Charge (SOC) of 9360 coulombs, a target SOC of 8890 coulombs, a balancing leg impedance of 31Ω (30Ω resistor plus 1Ω FET on resistance), and a sampling time interval of 5 minutes (300 seconds).

The Balance Value is calculated using Equation 10.

$$B = \frac{8191}{5} \times (9360 - 8890) \times \frac{31}{300} = 79562 = 28'h00136CA \quad \text{(EQ. 10)}$$

The value 8191/5 is the scaling factor of the cell voltage measurement.

The value of 28'h00136CA is loaded to the required Cell Balance Register and the value 7'b0001111 (5 minutes) is loaded to the Balance Time bits in the Watchdog/Balance time register.

In this example, the total coulomb difference to be balanced is: 470 coulomb (9360 - 8890). At 3.3V/31Ω * 300s = 31.9 coulomb per cycle, it takes about 15 cycles for the balancing to terminate.

AUTO BALANCE MODE CELL BALANCING EXAMPLE

The following describes a simple setup to demonstrate the Auto Balance mode cell balancing function of the ISL78610. Note that this balancing setup is not related to the balance value calculation in Equation 10.

Auto balance cells using the following criteria:

- Balance time = 20 seconds
- Balance wait time (dead time between balancing cycles) = 8 seconds
- Balancing disabled during cell measurements
- Balance Values: See Table 61

TABLE 61. CELL BALANCE VALUES (HEX) FOR EACH CELL

CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7	CELL 8	CELL 9	CELL 10	CELL 11	CELL 12
28'h 406A	28'h 3E4D	28'h 0	28'h 292F	28'h 3E00	28'h 0	28'h 2903	28'h 3D06	28'h 0	28'h 151E	28'h 502	28'h 6D6

- Balance Status Register: Set up balance:
  Cells 1, 4, 7, and 10 on first cycle
  Cells 3, 6, 9, and 12 on second cycle
  Cells 2, 5, 8, and 11 on third cycle
  (See Table 62)

TABLE 62. BALANCE STATUS SETUP

BPS [3:0]	CELL 1	2	3	4	5	6	7	8	9	10	11	12
0000	Reserved for Manual Balance mode and Timed Balance mode											
0001	1	0	0	1	0	0	1	0	0	1	0	0
0010	0	0	1	0	0	1	0	0	1	0	0	1
0011	0	1	0	0	1	0	0	1	0	0	1	0

Step 1. Write the Balance Value registers .

TABLE 63. BALANCE VALUE REGISTERS

R/W	PAGE	ADDRESS	DATA (HEX)	CELL
1	010	100000	14'h006A	1
1	010	100001	14'h0001	
1	010	100010	14'h3E4D	2
1	010	100011	14'h0000	
1	010	100100	14'h0000	3
1	010	100101	14'h0000	
1	010	100110	14'h292F	4
1	010	100111	14'h0000	
1	010	101000	14'h3E00	5
1	010	101001	14'h0000	
1	010	101010	14'h0000	6
1	010	101011	14'h0000	
1	010	101100	14'h2903	7
1	010	101101	14'h0000	
1	010	101110	14'h3D06	8
1	010	101111	14'h0000	
1	010	110000	14'h0000	9
1	010	110001	14'h0000	
1	010	110010	14'h151E	10
1	010	110011	14'h0000	
1	010	110100	14'h0502	11
1	010	110101	14'h0000	
1	010	110110	14'h06D6	12
1	010	110111	14'h0000	

TABLE 64. BALANCE VALUE REGISTERS (CELL1) - VALUE 28'h406A

6'20	B0107	B0106	B0105	B0104	B0103	B0102	B0101	B0100
	0	1	1	0	1	0	1	0
			B0113	B0112	B1011	B0110	B0109	B0108
			0	0	0	0	0	0
6'21	B0121	B0120	B0119	B0118	B0117	B0116	B0115	B0114
	0	0	0	0	0	0	0	1
			B0127	B0126	B0125	B0124	B0123	B0122
			0	0	0	0	0	0

Step 2. Write the BDDS bit in Device Setup register (turn balancing functions off during measurement).

BDDS = 1

TABLE 65. DEVICE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	011001	XX XXXX 1XXX XXXX

X = don't care

Step 3. Write the balance timeout setting to the Watchdog/Balance Time register: Balance timeout code = 0000001 (20 seconds).

BTM6:0 = 000 0001

TABLE 66. BALANCE TIMEOUT REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010101	00 0000 1XXX XXXX

"X" values can be set to any number – the lower bits are the watchdog timeout value and should be set to a time longer than the balance time. A value 111 1111 is suggested.

Step 4. Set up the Balance Status register (from Table 62 on page 81).

Step 4A. Write the Balance Setup register: Set Auto Balance mode, set the 8 second Balance wait time, and set balance off:

BMD = 11 (Auto Balance mode)
BWT = 100 (8 seconds)
BEN = 0 (Balancing disabled)

TABLE 67. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX0X XXX1 0011

"X" values can be set to any number.

Step 4B. Write the Balance Setup register: Set Balance Status Pointer = 1.

BSP = 0001 (Balance status pointer = 1)

TABLE 68. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XXX0 001X XXXX

"X" values can be set to any number.

Step 4C. Write the Balance Status register: Set Bits 1, 4, 7, and 10.

BAL12:1 = 0010 0100 1001

TABLE 69. BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 0010 0100 1001

Step 4D. Write the Balance Setup register: Set the Balance Status Pointer = 2.

BSP = 0010 (Balance status pointer = 2)

TABLE 70. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XXX0 010X XXXX

"X" values can be set to any number

Step 4E. Write the Balance Status register: Set Bits 3, 6, 9, and 12.

BAL12:1 = 1001 0010 0100

TABLE 71. BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 1001 0010 0100

Step 4F. Write the Balance Setup register: Set Balance Status Pointer = 3.

BSP = 0011 (Balance status pointer = 3)

TABLE 72. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XXX0 011X XXXX

"X" values can be set to any number

Step 4G. Write the Balance Status register: Set Bits 2, 5, 8, and 11.

BAL12:1 = 0100 1001 0010

TABLE 73. BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 0100 1001 0010

Step 4H. Write the Balance Setup register: Set the Balance Status Pointer = 4.

BSP = 0100 (Balance status pointer = 4)

TABLE 74. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XXX0 100X XXXX

"X" values can be set to any number

Step 4I. Write the Balance Status register: Set bits to all zero to set the end point for the instances.

BAL12:1 = 0000 0000 0000

TABLE 75. BALANCE STATUS REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010100	XX 0000 0000 0000

Step 5. Enable balancing using the Balance Enable command.

TABLE 76. BALANCE ENABLE COMMAND

R/W	PAGE	ADDRESS	DATA
0	011	010000	00 0000

Or enable balancing by setting BEN directly in the Balance Setup register:

BEN = 1

TABLE 77. BALANCE SETUP REGISTER

R/W	PAGE	ADDRESS	DATA
1	010	010011	XX XX1X XXXX XXXX

The balance FETs cycle through each instance of the Balance Status register in a loop, interposing the balance wait time between each instance. The measured voltage of each cell being balanced is subtracted from the balance value for that cell at the end of each Balance Status instance. The process continues until the Balance Value register for each cell contains zero.

System Registers

System registers contain 14 bits each. All register locations are memory mapped using a 9-bit address. The MSBs of the address form a 3-bit page address. Page 1 (3'b001) registers are the measurement result registers for cell voltages and temperatures. Page 3 (3'b011) is used for commands. Pages 1 and 3 are not subject to the checksum calculations. Page addresses 4 and 5 (3'b100 and 3b'101), with the exception of the EEPROM checksum registers, are reserved for internal functions.

All Page 2 registers (device configuration registers) and EEPROM checksum registers are subject to a checksum calculation. The checksum is calculated in response to the Calculate Register Checksum command using a Multiple Input Shift Register (MISR) error detection technique. The checksum is tested in response to a Check Register Checksum command. The occurrence of a checksum error sets the PAR bit in the Fault Status register and causes a Fault response accordingly. The normal response to a PAR error is for the host microcontroller to rewrite the Page 2 register contents. A PAR fault also causes the device to cease any scanning or cell balancing activity.

A description of each register is included in "Register Descriptions" and includes a depiction of the register with bit names and initialization values at power up, when the EN pin is toggled and the device receives a Reset Command, or when the device is reset. Bits that reflect the state of external pins are notated "Pin" in the initialization space. Bits which reflect the state of nonvolatile memory bits (EEPROM) are notated "NV" in the initialization space. Initialization values are shown below each bit name.

Reserved bits (indicated by gray areas) should be ignored when reading and should be set to "0" when writing to them.

Register Descriptions

Cell Voltage Data

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b001	Read Only	6'h00 - 6'h0C and 6'h0F	**Measured cell voltage and pack voltage values.** Address 001111 accesses all cell and Pack Voltage data with one read operation. See Figure 71D on page 61. Cell values are output as 13-bit signed integers with the 14th bit (MSB) denoting the sign, (for example, positive full scale is 14'h1FFF, 8191 decimal, negative full scale is 14'h2000, 8192 decimal). V_{BAT} is a 14-bit unsigned integer.

ACCESS	PAGE ADDR	REGISTER ADDRESS		DESCRIPTION
Read Only	3'b001	6'h00	V_{BAT} Voltage	$VCx = \frac{(HEXvalue_{10} - 16384) \times 2 \times 2.5}{8192}$ if...$HEXvalue_{10} \geq 8191$ $VCx = \frac{HEXvalue_{10} \times 2 \times 2.5}{8192}$ if...$HEXvalue_{10} < 8191$ $VBAT = \frac{HEXvalue_{10} \times 15.9350784 \times 2.5}{8192}$ $HEXvalue_{10}$ = Hex to Decimal conversion of the register contents.
		6'h01	Cell 1 Voltage	
		6'h02	Cell 2 Voltage	
		6'h03	Cell 3 Voltage	
		6'h04	Cell 4 Voltage	
		6'h05	Cell 5 Voltage	
		6'h06	Cell 6 Voltage	
		6'h07	Cell 7 Voltage	
		6'h08	Cell 8 Voltage	
		6'h09	Cell 9 Voltage	
		6'h0A	Cell 10 Voltage	
		6'h0B	Cell 11 Voltage	
		6'h0C	Cell 12 Voltage	
		6'h0F	Read all cell voltages	

Temperature Data, Secondary Voltage Reference Data, Scan Count

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b001	See individual register	6'h10 - 6'h16 and 6'h1F	**Measured temperature, Secondary reference, Scan Count.** Address 011111 accesses all these data in a continuous read (see Figure 71D on page 61). Temperature and reference values are output as 14-bit unsigned integers, (for example, full scale is 14'h3FFF (16383 decimal).

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read Only	3'b001	6'h10	Internal temperature reading. $T_{INTERNAL}(°C) = \frac{HEXvalue_{10} - 9180}{31.9} + 25$ $HEXvalue_{10}$ = Hex to Decimal conversion of the register contents.
		6'h11	External temperature Input 1 reading. $V_{TEMP} = \frac{HEXvalue_{10} \times 2.5}{16384}$ $T_{EXTERNAL}(°C) = V_{TEMP} \times R_{DIVIDER}$ where $R_{DIVIDER}$ depends on the external resistor divider circuit that includes an NTC thermistor (see Figure 50 on page 29 for an example external circuit.)
		6'h12	External temperature Input 2 reading.
		6'h13	External temperature Input 3 reading.
		6'h14	External temperature Input 4 reading.
		6'h15	Reference voltage (raw ADC) value. Use to calculate the corrected reference value with reference coefficient data. See Page 2 data, address 6'h38 – 6'h3A.
Read/ Write	3'h001	6'h16	**Scan Count:** Current scan instruction count. Count is incremented each time a scan command is received and wraps to zero when overflowed. Register may be compared to previous value to confirm scan command receipt. Bit Designations:

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED										SCN3	SCN2	SCN1	SCN0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read Only	3'h001	6'h1F	Read all: Temperature Data, Secondary Voltage Reference Data, Scan Count (locations 6'h10 - 6'h16)

Fault Registers

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'h010	Read/ Write	6'h00 - 6'h05 and 6'h0F	**Fault registers.** Fault setup and status information. Address 6'h0F accesses all fault data in a continuous read (daisy chain configuration only). See Figure 71D on page 61.

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'h010	6'h00	**Overvoltage Fault:** Overvoltage fault on Cells 12 to 1 correspond with Bits OF12 to OF1, respectively. Default values are all zero. Bits are set to 1 when faults are detected. The contents of this register can be reset through a register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		OF12	OF11	OF10	OF9	OF8	OF7	OF6	OF5	OF4	OF3	OF2	OF1
0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read/ Write	3'h010	6'h01	**Undervoltage Fault:** Undervoltage fault on Cells 12 to 1 correspond with Bits UF12 to UF1, respectively. Default values are all zero. Bits are set to 1 when faults are detected. The contents of this register can be reset through a register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		UF12	UF11	UF10	UF9	UF8	UF7	UF6	UF5	UF4	UF3	UF2	UF1
0	0	0	0	0	0	0	0	0	0	0	0	0	0

<table>
<tr><th>ACCESS</th><th>PAGE ADDR</th><th>REGISTER ADDRESS</th><th>DESCRIPTION</th></tr>
<tr><td>Read/ Write</td><td>3’h010</td><td>6’h02</td><td>
Open-Wire Fault:
Open-Wire fault on Pins VC12 to VC0 correspond with Bits OC12 to OC0, respectively.
Default values are all zero.
Bits are set to 1 when faults are detected.
The contents of this register can be reset through a register write (14’h0000).
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>OC12</td><td>OC11</td><td>OC10</td><td>OC9</td><td>OC8</td><td>OC7</td><td>OC6</td><td>OC5</td><td>OC4</td><td>OC3</td><td>OC2</td><td>OC1</td><td>OC0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
</td></tr>
<tr><td>Read/ Write</td><td>3’h010</td><td>6’h03</td><td>
Fault Setup:
These bits control various Fault configurations.
Default values and descriptions of each bit are shown below.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td>TST4</td><td>TST3</td><td>TST2</td><td>TST1</td><td>TST0</td><td>TOT2</td><td>TOT1</td><td>TOT0</td><td>WSCN</td><td>SCN3</td><td>SCN2</td><td>SCN1</td><td>SCN0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>SCN0, 1, 2, 3</td><td>Scan interval code. Decoded to provide the scan interval setup for the auto scan function. Initialized to 0000 (16ms scan interval). See Table 14 on page 42.</td></tr>
<tr><td>WSCN</td><td>Scan wires timing control. Set to 1 for tracking of the temperature scan interval. Set to 0 for tracking of the cell voltage scan interval above 512ms. Interval is fixed at 512ms for faster cell scan rates. See Table 14 on page 42.</td></tr>
<tr><td>TOT0, 1, 2</td><td>Fault Totalizer code bits. Decoded to provide the required fault totalization. An unbroken sequence of positive fault results equal to the totalize amount is needed to verify a fault condition. Initialized to 011 (8 sample totalizing.) See Table 45 on page 73.
This register must be rewritten following an error detection resulting from totalizer overflow.</td></tr>
<tr><td>TST0</td><td>Controls temperature testing of internal IC temperature. Set this bit to 1 to enable internal temperature test. Set to 0 to disable (not recommended). Initialized to 1 (on).</td></tr>
<tr><td>TST1 to TST4</td><td>Controls temperature testing on the external temperature Inputs 1 to 4, respectively. Set this bit to 1 to enable the corresponding temperature test. Set to 0 to disable. Allows external inputs to be used for general voltage monitoring without imposing a limit value. TST1 to TST4 are initialized to 0 (off).</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>ACCESS</th><th>PAGE ADDR</th><th>REGISTER ADDRESS</th><th>DESCRIPTION</th></tr>
<tr><td>Read/ Write</td><td>3’h010</td><td>6’h04</td><td>Fault Status:
The $\overline{\text{FAULT}}$ logic output is an OR function of the bits in this register: the output will be asserted low if any bits in the Fault Status register are set.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>MUX</td><td>REG</td><td>REF</td><td>PAR</td><td>OVSS</td><td>OVBAT</td><td>OW</td><td>UV</td><td>OV</td><td>OT</td><td>WDGF</td><td>OSC</td><td colspan="2">RESERVED</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>OSC</td><td>Oscillator fault bit. Bit is set in response to a fault on either the 4MHz or 32kHz oscillators. Note that communications functions can be disrupted by a fault in the 4MHz oscillator.</td></tr>
<tr><td>WDGF</td><td>Watchdog timeout fault. Bit is set in response to a watchdog timeout.</td></tr>
<tr><td>OT</td><td>Over-temperature fault. ‘OR’ of over-temperature fault bits: TFLT0 to TFLT4. This bit is latched. The bits in the Over-temperature Fault register must first be reset before this bit can be reset. Reset by writing 14’h0000 to this register.</td></tr>
<tr><td>OV</td><td>Overvoltage fault. ‘OR’ of Overvoltage fault bits: OF1 to OF12. This bit is latched. The bits in the Overvoltage Fault register must first be reset before this bit can be reset. Reset by writing 14’h0000 to this register.</td></tr>
<tr><td>UV</td><td>Undervoltage fault. ‘OR’ of Undervoltage fault bits: UF1 to UF12. This bit is latched. The bits in the Undervoltage Fault register must first be reset before this bit can be reset. Reset by writing 14’h0000 to this register.</td></tr>
<tr><td>OW</td><td>Open-Wire fault. ‘OR’ of open-wire fault bits: OC0 to OC12. This bit is latched. The bits in the Open-Wire Fault register must first be reset before this bit can be reset. Reset by writing 14’h0000 to this register.</td></tr>
<tr><td>OV_{BAT}</td><td>Open-wire fault on V_{BAT} connection. Bit set to 1 when a fault is detected. Can be reset through a register write (14’h0000).</td></tr>
<tr><td>OVSS</td><td>Open-wire fault on V_{SS} connection. Bit set to 1 when a fault is detected. Can be reset through a register write (14’h0000).</td></tr>
<tr><td>PAR</td><td>Register checksum (Parity) error. This bit is set in response to a register checksum error. The checksum is calculated and stored in response to a Calc Register Checksum command and acts on the contents of all Page 2 registers. The Check Register Checksum command is used to repeat the calculation and compare the results to the stored value. The PAR bit is then set if the two results are not equal. This bit is not set in response to a nonvolatile EEPROM memory checksum error. See Table 78 on page 94.</td></tr>
<tr><td>REF</td><td>Voltage reference fault. This bit is set if the voltage reference value is outside its “power-good” range.</td></tr>
<tr><td>REG</td><td>Voltage regulator fault. This bit is set if a voltage regulator value (V3P3, VCC or V2P5) is outside its “power-good” range.</td></tr>
<tr><td>MUX</td><td>Temperature multiplexer error. This bit is set if the VCC loopback check returns a fault. The VCC loopback check is performed at the end of each temperature scan.</td></tr>
</table></td></tr>
<tr><td>Read/ Write</td><td>3’h010</td><td>6’h05</td><td>Cell Setup:
Default values are shown below, as are descriptions of each bit.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>FFSN</td><td>FFSP</td><td>C12</td><td>C11</td><td>C10</td><td>C9</td><td>C8</td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>
<table>
<tr><td>C1 to C12</td><td>Enable/disable cell overvoltage, undervoltage and open-wire detection on Cells 1 to 12, respectively. Set to 1 to disable OV/UV and open-wire tests.</td></tr>
<tr><td>FFSP</td><td>Force ADC input to Full Scale Positive. All cell scan readings forced to 14'h1FFF. All temperature scan readings forced to 14'h3FFF.</td></tr>
<tr><td>FFSN</td><td>Force ADC input to Full Scale Negative. All cell scan readings forced to 14'h2000. All temperature scan readings forced to 14'h0000.</td></tr>
<tr><td colspan="2">NOTE: The ADC input functions normally if both FFSN and FFSP are set to '1' but this setting is not supported.</td></tr>
</table></td></tr>
</table>

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'h010	6'h06	**Over-Temperature Fault:** Over-temperature fault on Cells 12 to 1 correspond with bits OF12 to OF1, respectively. Default values are all zero. Bits are set to 1 when fault are detected. The contents of this register can be reset through a register write (14'h0000).

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED									TFLT4	TFLT3	TFLT2	TFLT1	TFLT0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

TFLT0	Internal over-temperature fault. Bit set to 1 when a fault is detected. Can be reset through a register write (14'h0000).
TFLT1 - TFLT4	External over-temperature inputs 1 to 4 (respectively.) Bit set to 1 when a fault is detected. Can be reset through a register write (14'h0000).

Read Only	3'h010	6'h0F	Read all Fault and Cell Setup data from locations: 6'h00 - 6'h06. See Figure 71D on page 61.

Set-Up Registers

BASE ADDR (PAGE)	Access	ADDRESS RANGE	DESCRIPTION
3'b010		6'h10 - 6'h1D and 6'h1F	**Device Set-up registers.** All device setup data.

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'b010	6'h10	**Overvoltage Limit:** Overvoltage Limit Value Overvoltage limit is compared to the measured values for Cells 1 to 12 to test for an overvoltage condition at any of the cells. Bit 0 is the LSB, Bit 12 is the MSB. Bit 13 is not used and must be set to 0.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	OV12	OV11	OV10	OV9	OV8	OV7	OV6	OV5	OV4	OV3	OV2	OV1	OV0
0	1	1	1	1	1	1	1	1	1	1	1	1	1

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'b010	6'h11	**Undervoltage Limit:** Undervoltage Limit Value Undervoltage limit is compared to the measured values for Cells 1 to 12 to test for an undervoltage condition at any of the cells. Bit 0 is the LSB, Bit 12 is the MSB. Bit 13 is not used and must be set to 0.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	UV12	UV11	UV10	UV9	UV8	UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'b010	6'h12	**External Temperature Limit:** Over-temperature limit value Over-temperature limit is compared to the measured values for external temperatures 1 to 4 to test for an over-temperature condition at any input. The temperature limit assumes NTC temperature measurement devices (i.e., an over-temperature condition is indicated by a temperature reading below the limit value). Bit 0 is the LSB, Bit 13 is the MSB.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETL13	ETL12	ETL11	ETL10	ETL9	ETL8	ETL7	ETL6	ETL5	ETL4	ETL3	ETL2	ETL1	ETL0
0	0	0	0	0	0	0	0	0	0	0	0	0	0

<table>
<tr><th>ACCESS</th><th>PAGE ADDR</th><th>REGISTER ADDRESS</th><th>DESCRIPTION</th></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h13</td><td>
Balance Setup:
Default values are shown below, as are descriptions of each bit.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td>BEN</td><td>BSP3</td><td>BSP2</td><td>BSP1</td><td>BSP0</td><td>BWT2</td><td>BWT1</td><td>BWT0</td><td>BMD1</td><td>BMD0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="4">BMD0, 1</td><td colspan="10">Balance mode. These bits set balance mode.
<table>
<tr><th>BMD1</th><th>BMD0</th><th>MODE</th></tr>
<tr><td>0</td><td>0</td><td>OFF</td></tr>
<tr><td>0</td><td>1</td><td>Manual</td></tr>
<tr><td>1</td><td>0</td><td>Timed</td></tr>
<tr><td>1</td><td>1</td><td>Auto</td></tr>
</table></td></tr>
<tr><td colspan="4">BWT0, 1, 2</td><td colspan="10">Balance wait time. Register contents are decoded to provide the required wait time between device balancing. This assists with thermal management and is used with Auto Balance mode. See Table 19 on page 46.</td></tr>
<tr><td colspan="4">BSP0, 1, 2, 3</td><td colspan="10">Balance Status register pointer. Points to one of the 13 incidents of the Balance Status register. Balance Status register 0 is used for Manual Balance mode and Timed Balance mode. Balance status registers 1 to 12 are used for Auto Balance mode. Reads and writes to the Balance Status register are accomplished by first configuring the Balance Status register pointer (for example, to read (write) Balance Status register 5, load 0101 to the Balance Status register pointer, then read (write) to the Balance Status register). See Table 19 on page 46.</td></tr>
<tr><td colspan="4">BEN</td><td colspan="10">Balance enable. Set to ‘1’ to enable balancing. ‘0’ inhibits balancing. Setting or clearing this bit does not affect any other register contents. Balance Enable and Balance Inhibit commands are provided to allow control of this function without requiring a register write. These commands have the same effect as setting this bit directly. This bit is cleared automatically when balancing is complete and the EOB bit (see “6’h19” on page 90) is set.</td></tr>
</table>
</td></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h14</td><td>
Balance Status
The Balance Status register is a multiple incidence register controlled by the BSP0-4 bits in the Balance setup register. See Table 19 on page 46.
Bit 0 is the LSB, Bit 11 is the MSB.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>BAL 12</td><td>BAL 11</td><td>BAL 10</td><td>BAL 8</td><td>BAL 8</td><td>BAL 7</td><td>BAL 6</td><td>BAL 5</td><td>BAL 4</td><td>BAL 3</td><td>BAL 2</td><td>BAL 1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td colspan="3">BAL1 to BAL12</td><td colspan="11">Cell 1 to Cell 12 balance control, respectively. A bit set to 1 enables balance control (turns FET on) of the corresponding cell. Writing this bit enables balance output for the current incidence of the Balance Status register for the cells corresponding to the particular bits, depending on the condition of BEN in the Balance Setup register. Read this bit to determine the current status of each cell’s balance control.</td></tr>
</table>
</td></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h15</td><td>
Watchdog/Balance Time
Defaults are shown below:
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>BTM6</td><td>BTM5</td><td>BTM4</td><td>BTM3</td><td>BTM2</td><td>BTM1</td><td>BTM0</td><td>WDG6</td><td>WDG5</td><td>WDG4</td><td>WDG3</td><td>WDG2</td><td>WDG1</td><td>WDG0</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td colspan="3">WDG0 to WDG6</td><td colspan="11">Watchdog timeout setting. Decoded to provide the time out value for the watchdog function. See “Watchdog Function” on page 76 for details. The watchdog may only be disabled (set to 7’h00) if the watchdog password is set. The watchdog setting can be changed to a nonzero value without writing to the watchdog password. Initialized to 7’h7F (128 minutes).</td></tr>
<tr><td colspan="3">BTM0 to BTM6</td><td colspan="11">Balance timeout setting. Decoded to provide the time out value for Timed Balance mode and Auto Balance mode. Initialized to 7’00 (Disabled). See Table 21 on page 47.</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>ACCESS</th><th>PAGE ADDR</th><th>REGISTER ADDRESS</th><th>DESCRIPTION</th></tr>
<tr><td>Read/ Write</td><td>3’b010</td><td>6’h16
6’h17</td><td>User Register
28 bits of register space arranged as 2 x 14 bits available for user data. These registers have no effect on the operation of the ISL78610. These registers are included in the register checksum function.</td></tr>
<tr><td rowspan="7">Read Only</td><td rowspan="7">3’b010</td><td rowspan="7">6’h18</td><td>Comms Setup
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">RESERVED</td><td>CRAT1</td><td>CRAT0</td><td>CSEL 2</td><td>CSEL 1</td><td>SIZE 3</td><td>SIZE 2</td><td>SIZE 1</td><td>SIZE 0</td><td>ADDR 3</td><td>ADDR 2</td><td>ADDR 1</td><td>ADDR 0</td></tr>
<tr><td>0</td><td>0</td><td>COMS RATE1 pin</td><td>COMS RATE0 pin</td><td>COMS SEL2 pin</td><td>COMS SEL1 pin</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>ADDR0-3</td><td>Device stack address. The stack address (device position in the stack) is determined automatically by the device in response to an “Identify” command. The resulting address is stored in ADDR0-3 and is used internally for communications pairing and sequencing. The stack address can be read by the user but not written to.</td></tr>
<tr><td>SIZE0-3</td><td>Device stack size (top stack device address). Corresponds to the number of devices in the stack. The stack size is determined automatically by the stack devices in response to an “Identify” command. The resulting number is stored in SIZE0-3 and is used internally for communications pairing and sequencing. The stack size can be read by the user but not written to.</td></tr>
<tr><td>CSEL1, 2</td><td>Communications setup bits. These bits reflect the state of the COMMS SELECT 1,2 pins and determine the operating mode of the communications ports. See Table 6 on page 27.</td></tr>
<tr><td>CRAT0, 1</td><td>Communications rate bits. These bits reflect the state of the COMMS RATE 0,1 pins and determine the bit rate of the daisy chain communications system. See Table 7 on page 28.</td></tr>
<tr><td rowspan="8">Read/ Write</td><td rowspan="8">3’b010</td><td rowspan="8">6’h19</td><td>Device Setup
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>WP5</td><td>WP4</td><td>WP3</td><td>WP2</td><td>WP1</td><td>WP0</td><td>BDDS</td><td>RESERVED</td><td>ISCN</td><td>SCAN</td><td>EOB</td><td>RESERVED</td><td>PIN37</td><td>PIN39</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>Pin</td><td>Pin</td></tr>
</table></td></tr>
<tr><td>PIN37, PIN39</td><td>These bits indicate the signal level on Pin 37 and Pin 39 of the device.</td></tr>
<tr><td>EOB</td><td>End Of Balance. This bit is set by the device when balancing is complete. This function is used in the Timed Balance mode and Auto Balance mode. The BEN bit is cleared as a result of this bit being set. Initialized to 1.</td></tr>
<tr><td>SCAN</td><td>Scan Continuous mode. This bit is set in response to a Scan Continuous command and cleared by a Scan Inhibit command.</td></tr>
<tr><td>ISCN</td><td>Set wire scan current source/sink values. Set to 0 for 150µA. Set to 1 for 1mA.</td></tr>
<tr><td>BDDS</td><td>Balance condition during measurement. Controls the balance condition in Scan Continuous mode and Auto Balance mode. Set to 1 to turn balancing functions off 10ms before and during cell voltage measurement. Set to 0 for normal operation (balancing functions are not affected by measurement).</td></tr>
<tr><td>WP5:0</td><td>Watchdog disable password. These bits must be set to 6’h3A (111010) before the watchdog can be disabled. Disable the watchdog by writing 7’h00 to the watchdog bits.</td></tr>
<tr><td rowspan="3">Read Only Value set in EEPROM</td><td rowspan="3">3’b010</td><td rowspan="3">6’h1A</td><td>Internal Temperature Limit
Bit 0 is the LSB, Bit 13 is the MSB.
<table>
<tr><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>ITL 13</td><td>ITL 12</td><td>ITL 11</td><td>ITL 10</td><td>ITL 8</td><td>ITL 8</td><td>ITL 7</td><td>ITL 6</td><td>ITL 5</td><td>ITL 4</td><td>ITL 3</td><td>ITL 2</td><td>ITL 1</td><td>ITL 0</td></tr>
<tr><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td><td>NV</td></tr>
</table></td></tr>
<tr><td>ITL1 to ITL12</td><td>IC over-temperature limit value. The over-temperature limit is compared to the measured values for the internal IC temperature to test for an over-temperature condition. The internal temperature limit value is stored in nonvolatile memory during test and loaded to these register bits at power up. The register contents can be read by the user but not written to.</td></tr>
<tr><td>Read Only</td><td>3’b010</td><td>6’h1B
6’h1C</td><td>Serial Number
The 28b serial number programmed in nonvolatile memory during factory test is mirrored to these 2 x 14 bit registers. The serial number may be read at any time but may not be written.</td></tr>
</table>

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION													
Read Only Value set in EEPROM	3'b010	6'h1D	**Trim Voltages**													
			13	12	11	10	9	8	7	6	5	4	3	2	1	0
			TV5	TV4	TV3	TV2	TV1	TV0	RESERVED							
			NV	NV	NV	NV	NV	NV	Ignore the Contents of these bits							
			TV5:0			Trim voltage (VNOM). The nominal cell voltage is programmed to nonvolatile memory during test and loaded to the Trim Voltage register at power up. The VNOM value is a 7-bit representation of the 0V to 5V cell voltage input range with 50 (7'h32) representing 5V (for example, LSB = 0.1V). The parts are additionally marked with the trim voltage by the addition of a two digit code to the part number. For example, 3.3V is denoted by the code 33 (1 bit per 0.1V of trim voltage, so 0 to 50 decimal covers the full range).									
Read Only	3'h010	6'h1F	Read all Setup data from locations: 6'h10 - 6'h1D. See Figure 71D on page 61.													

Cell Balance Registers

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b010	Read/ Write	6'h20 - 6'h37	**Cell balance registers.** These registers are loaded with data related to change in SOC desired for each cell. This data is then used during Auto Balance mode. The data value is decremented with each successive ADC sample until a zero value is reached. The register space is arranged as 2 x 14-bit per cell for 24 x 14-bit total. The registers are cleared at device power up or by a Reset command. See "Auto Balance Mode" on page 47.

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read/ Write	3'b010	6'h20	Cell 1 balance value Bits 0 to 13.
		6'h21	Cell 1 balance value Bits 14 to 27.
		~	
		6'h36	Cell 12 balance value Bits 0 to 13.
		6'h37	Cell 12 balance value Bits 14 to 27.

Reference Coefficient Registers

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b010	Read Only	6'h38 - 6'h3A	**Reference Coefficients** Bit 13 is the MSB, Bit 0 is the LSB

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION													
Read Only Value set in EEPROM	3'b010	6'h38	**Reference Coefficient C** Reference calibration coefficient C LSB. Use with coefficients A and B and the measured reference value to obtain the compensated reference measurement. Compare this result to the limits in the "Electrical Specifications" table to check that the reference is within limits. The register contents may be read by the user but not written to.													
			13	12	11	10	9	8	7	6	5	4	3	2	1	0
			RCC 13	RCC 12	RCC 11	RCC 10	RCC 9	RCC 8	RCC 7	RCC 6	RCC 5	RCC 4	RCC 3	RCC 2	RCC 1	RCC 0
			NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read Only	3'b010	6'h39	**Reference Coefficient B** Reference calibration coefficient B LSB. Use with coefficients A and C and the measured reference value to obtain the compensated reference measurement. Compare this result to the limits in the "Electrical Specifications" table to check that the reference is within limits. The register contents may be read by the user but not written to.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCB 13	RCB 12	RCB 11	RCB 10	RCB 9	RCB 8	RCB 7	RCB 6	RCB 5	RCB 4	RCB 3	RCB 2	RCB 1	RCB 0
NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV	NV

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read Only	3'b010	6'h3A	**Reference Coefficient A** Reference calibration coefficient A LSB. Use with coefficients B and C and the measured reference value to obtain the compensated reference measurement. Compare this result to the limits in the "Electrical Specifications" table to check that the reference is within limits. The register contents may be read by the user but not written to.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RCA 8	RCA 7	RCA 6	RCA 5	RCA 4	RCA 3	RCA 2	RCA 1	RCA 0	RESERVED				
NV	NV	NV	NV	NV	NV	NV	NV	NV	Ignore the content of these bits				

Cells In Balance Register

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b010	Read Only	6'h3B	**Cells In Balance**

ACCESS	PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
Read Only	3'b010	6'h3B	**Cells Balance Enabled (Valid for non-daisy chain configuration only).** This register reports the current condition of the cell balance outputs. Bit 0 is the LSB, Bit 11 is the MSB.

13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED		CBEN 12	CBEN 11	CBEN 10	CBEN 8	CBEN 8	CBEN 7	CBEN 6	CBEN 5	CBEN 4	CBEN 3	CBEN 2	CBEN 1
0	0	0	0	0	0	0	0	0	0	0	0	0	0
BALI1 to BALI12		Indicates the current balancing status of Cell 1 to Cell 12 (respectively). "1" indicates balancing is enabled for this cell. "0" indicates that balancing is turned off.											

Device Commands

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
3'b011	Read Only	6'h01 - 6'h14	Device commands. Actions and communications administration. Not physical registers but memory mapped device commands. Commands from host and device responses are all configured as reads (BASE ADDR MSB = 0). Write operations break the communication rules and produce a NAK from the target device.

PAGE ADDR	REGISTER ADDRESS	DESCRIPTION
3'b011	6'h01	**Scan Voltages.** Device responds by scanning V_{BAT} and all 12-cell voltages and storing the results in local memory.
	6'h02	**Scan Temperatures.** Device responds by scanning external temperature inputs, internal temperature, and the secondary voltage reference, and storing the results in local memory.
	6'h03	**Scan Mixed.** Device responds by scanning V_{BAT}, cell, and ExT1 voltages and storing the results in local memory. The ExT1 measurement is performed in the middle of the cell voltage scans to minimize measurement latency between the cell voltages and the voltage on ExT1.
	6'h04	**Scan Wires.** Device responds by scanning for pin connection faults and storing the results in local memory.
	6'h05	**Scan All.** Device responds by performing the functions of the Scan Voltages, Scan temperatures, and Scan Wires commands in sequence. Results are stored in local memory.
	6'h06	**Scan Continuous.** Places the device in Scan Continuous mode by setting the Device Setup register SCAN bit.
	6'h07	**Scan Inhibit.** Stops Scan Continuous mode by clearing the Device Setup register SCAN bit.
	6'h08	**Measure.** Device responds by measuring a targeted single parameter (cell voltage/V_{BAT}/external or internal temperatures or secondary voltage reference).
	6'h09	**Identify.** Special mode function used to determine device stack position and address. Devices record their own stack address and the total number of devices in the stack. See "Identify Command" on page 49 for details.
	6'h0A	**Sleep.** Places the part in Sleep mode (wake up through daisy comms). See "Communication Timing" on page 61.
	6'h0B	**NAK.** Device response if communications is not recognized. The device responds NAK down the daisy chain to the host microcontroller. The host microcontroller typically retransmits after receiving a NAK.
	6'h0C	**ACK.** Used by host microcontroller to verify communications without changing anything. Devices respond with an ACK.
	6'h0E	**Comms Failure.** Used in daisy chain implementations to communicate comms failure. If a communication is not acknowledged by a stack device, the last stack device that did receive the communication responds with Comms Failure. This is part of the communications integrity checking. Devices downstream of a communications fault are alerted to the fault condition by the watchdog function.
	6'h0F	**Wake-up.** Used in daisy chain implementations to wake up a sleeping stack of devices. The Wake-up command is sent to the bottom stack device (master device) through SPI. The master device then wakes up the rest of the stack by transmitting a low frequency clock. The top stack device responds ACK once it is awake. See "Wake-Up Command" on page 44.
	6'h10	**Balance Enable.** Enables cell balancing by setting BEN. Can be used to enable cell balancing on all devices simultaneously using the address All Stack Address 1111.
	6'h11	**Balance Inhibit.** Disables cell balancing by clearing BEN. Can be used to disable cell balancing on all devices simultaneously using the address All Stack Address 1111.
	6'h12	**Reset.** Resets all digital registers to its power-up state (reloads the factory programmed configuration data from nonvolatile memory). Stops all scan and balancing activity. Daisy chain devices must be reset in sequence starting with the top stack device and proceeding down the stack to the bottom (master) device. The Reset command must be followed by an Identify command (daisy chain configuration) before volatile registers can be rewritten.
	6'h13	**Calculate register checksum.** Calculates the checksum value for the current Page 2 register contents (registers with base address 0010). See "System Hardware Connection" on page 22.
	6'h14	**Check register checksum.** Verifies the register contents are correct for the current checksum. An incorrect result sets the PAR bit in the Fault status register which starts a standard fault response. See "System Hardware Connection" on page 22.

Nonvolatile Memory (EEPROM) Checksum

A checksum is provided to verify the contents of EEPROM memory. Two registers are provided. The MISR register (Table 78) contains the correct checksum value, which is calculated during factory testing. The MISR Shadow register contains the checksum value that is calculated each time the nonvolatile memory is loaded to shadow registers, either after a power cycle or after a device reset. See "Fault Diagnostics" on page 77. for more information.

TABLE 78. MISR REGISTER

BASE ADDR (PAGE)	ACCESS	ADDRESS RANGE	DESCRIPTION
100	Read Only	6'h3F	Nonvolatile memory Multiple Input Shift Register (MISR) register. This is the checksum value for the nonvolatile memory contents. It is programmed during factory testing.
101	Read Only	6'h00	MISR shadow register checksum value. This value is calculated when shadow registers are loaded from nonvolatile memory either after a power cycle or a reset.

Register Map

R/$\overline{W}$ + PAGE				BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	WRITE	ADDRESS	REGISTER NAME			BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0001		000000	V_{BAT} Voltage	VB7	VB6	VB5	VB4	VB3	VB2	VB1	VB0
						VB13	VB12	VB11	VB10	VB9	VB8
0001		000001	Cell 1 Voltage	C1V7	C1V6	C1V5	C1V4	C1V3	C1V2	C1V1	C1V0
						C1V13	C1V12	C1V11	C1V10	C1V9	C1V8
0001		000010	Cell 2 Voltage	C2V7	C2V6	C2V5	C2V4	C2V3	C2V2	C2V1	C2V0
						C2V13	C2V12	C2V11	C2V10	C2V9	C2V8
0001		000011	Cell 3 Voltage	C3V7	C3V6	C3V5	C3V4	C3V3	C3V2	C3V1	C3V0
						C3V13	C3V12	C3V11	C3V10	C3V9	C3V8
0001		000100	Cell 4 Voltage	C4V7	C4V6	C4V5	C4V4	C4V3	C4V2	C4V1	C4V0
						C4V13	C4V12	C4V11	C4V10	C4V9	C4V8
0001		000101	Cell 5 Voltage	C5V7	C5V6	C5V5	C5V4	C5V3	C5V2	C5V1	C5V0
						C5V13	C5V12	C5V11	C5V10	C5V9	C5V8
0001		000110	Cell 6 Voltage	C6V7	C6V6	C6V5	C6V4	C6V3	C6V2	C6V1	C6V0
						C6V13	C6V12	C6V11	C6V10	C6V9	C6V8
0001		000111	Cell 7 Voltage	C7V7	C7V6	C7V5	C7V4	C7V3	C7V2	C7V1	C7V0
						C7V13	C7V12	C7V11	C7V10	C7V9	C7V8
0001		001000	Cell 8 Voltage	C8V7	C8V6	C8V5	C8V4	C8V3	C8V2	C8V1	C8V0
						C8V13	C8V12	C8V11	C8V10	C8V9	C8V8
0001		001001	Cell 9 Voltage	C9V7	C9V6	C9V5	C9V4	C9V3	C9V2	C9V1	C9V0
						C9V13	C9V12	C9V11	C9V10	C9V9	C9V8
0001		001010	Cell 10 Voltage	C10V7	C10V6	C10V5	C10V4	C10V3	C10V2	C10V1	C10V0
						C10V13	C10V12	C10V11	C10V10	C10V9	C10V8
0001		001011	Cell 11 Voltage	C11V7	C11V6	C11V5	C11V4	C11V3	C11V2	C11V1	C11V0
						C11V13	C11V12	C11V11	C11V10	C11V9	C11V8
0001		001100	Cell 12 Voltage	C12V7	C12V6	C12V5	C12V4	C12V3	C12V2	C12V1	C12V0
						C12V13	C12V12	C12V11	C12V10	C12V9	C12V8

Register Map (Continued)

R/W + PAGE		ADDRESS	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	WRITE					BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0001		001111	All Cell Voltage Data	Daisy chain configuration only. This command returns all Page 1 data from address 6'h00 through 6'h0C in a single data stream. See "Communication Sequences" on page 57 and "System Out of Limit Detection" on page 73. See example in Figure 71D on page 61.							
0001		010000	IC Temperature	ICT7	ICT6	ICT5	ICT4	ICT3	ICT2	ICT1	ICT0
						ICT13	ICT12	ICT11	ICT10	ICT9	ICT8
0001		010001	External Temperature Input 1 Voltage (ExT1 pin)	ET1V7	ET1V6	ET1V5	ET1V4	ET1V3	ET1V2	ET1V1	ET1V0
						ET1V13	ET1V12	ET1V11	ET1V10	ET1V9	ET1V8
0001		010010	External Temperature Input 2 Voltage (ExT2 pin)	ET2V7	ET2V6	ET2V5	ET2V4	ET2V3	ET2V2	ET2V1	ET2V0
						ET2V13	ET2V12	ET2V11	ET2V10	ET2V9	ET2V8
0001		010011	External Temperature Input 3 Voltage (ExT3 pin)	ET3V7	ET3V6	ET3V5	ET3V4	ET3V3	ET3V2	ET3V1	ET3V0
						ET3V13	ET3V12	ET3V11	ET3V10	ET3V9	ET3V8
0001		010100	External Temperature Input 4 Voltage (ExT4 pin)	ET4V7	ET4V6	ET4V5	ET4V4	ET4V3	ET4V2	ET4V1	ET4V0
						ET4V13	ET4V12	ET4V11	ET4V10	ET4V9	ET4V8
0001		010101	Secondary Reference Voltage	RV7	RV6	RV5	RV4	RV3	RV2	RV1	RV0
						RV13	RV12	RV11	RV10	RV9	RV8
0001		010110	Scan Count					SCN3	SCN2	SCN1	SCN0
0001		011111	All Temperature Data	Daisy chain configuration only. This command returns all Page 1 data from address 6'h10 through 6'h16 in a single data stream. See "Communication Sequences" on page 57 and "System Out of Limit Detection" on page 73.							
0010	1010	000000	Overvoltage Fault	OF8	OF7	OF6	OF5	OF4	OF3	OF2	OF1
								OF12	OF11	OF10	OF9
0010	1010	000001	Undervoltage Fault	UF8	UF7	UF6	UF5	UF4	UF3	UF2	UF1
								UF12	UF11	UF10	UF9
0010	1010	000010	Open-Wire Fault	OC7	OC6	OC5	OC4	OC3	OC2	OC1	OC0
							OC12	OC11	OC10	OC9	OC8
0010	1010	000011	Fault Setup	TOT2	TOT1	TOT0	WSCN	SCN3	SCN2	SCN1	SCN0
							TTST4	TTST3	TTST2	TTST1	TTST0
0010	1010	000100	Fault Status	OW	UV	OV	OT	WDGF	OSC	0	0
						MUX	REG	REF	PAR	OVSS	OV_{BAT}
0010	1010	000101	Cell Setup	C8	C7	C6	C5	C4	C3	C2	C1
						FFSN	FFSP	C12	C11	C10	C9
0010	1010	000110	Over-Temperature Fault				TFLT4	TFLT3	TFLT2	TFLT1	TFLT0
0010		001111	All Fault Data	Daisy chain configuration only. This command returns all Page 2 data from address 6'h00 through 6'h06 in a single data stream. See "Communication Sequences" on page 57 and "System Out of Limit Detection" on page 73.							
0010	1010	010000	Overvoltage Limit	OV7	OV6	OV5	OV4	OV3	OV2	OV1	OV0
						OV13	OV12	OV11	OV10	OV9	OV8

Register Map (Continued)

R/W + PAGE		ADDRESS	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	WRITE					BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0010	1010	010001	Undervoltage Limit	UV7	UV6	UV5	UV4	UV3	UV2	UV1	UV0
						UV13	UV12	UV11	UV10	UV9	UV8
0010	1010	010010	External Temp Limit	ETL7	ETL6	ETL5	ETL4	ETL3	ETL2	ETL1	ETL0
						ETL13	ETL12	ETL11	ETL10	ETL9	ETL8
0010	1010	010011	Balance Setup	BSP2	BSP1	BSP0	BWT2	BWT1	BWT0	BMD1	BMD0
										BEN	BSP3
0010	1010	010100	Balance Status (Cells to Balance)	BAL8	BAL7	BAL6	BAL5	BAL4	BAL3	BAL2	BAL1
								BAL12	BAL11	BAL10	BAL9
0010	1010	010101	Watchdog/Balance Time	BTM0	WDG6	WDG5	WDG4	WDG3	WDG2	WDG1	WDG0
						BTM6	BTM5	BTM4	BTM3	BTM2	BTM1
0010	1010	010110	User Register	UR7	UR6	UR5	UR4	UR3	UR2	UR1	UR0
						UR13	UR12	UR11	UR10	UR9	UR8
0010	1010	010111	User Register	UR21	UR20	UR19	UR18	UR17	UR16	UR15	UR14
						UR27	UR26	UR25	UR24	UR23	UR22
0010		011000	Comms Setup	SIZE3	SIZE2	SIZE1	SIZE0	ADDR3	ADDR2	ADDR1	ADDR0
								CRAT1	CRAT0	CSEL2	CSEL1
0010	1010	011001	Device Setup	BDDS	0	ISCN	SCAN	EOB	0	Pin 37	Pin 39
						WP5	WP4	WP3	WP2	WP1	WP0
0010		011010	Internal Temp Limit	ITL7	ITL6	ITL5	ITL4	ITL3	ITL2	ITL1	ITL0
						ITL13	ITL12	ITL11	ITL10	ITL9	ITL8
0010		011011	Serial Number 0	SN7	SN6	SN5	SN4	SN3	SN2	SN1	SN0
						SN13	SN12	SN11	SN10	SN9	SN8
0010		011100	Serial Number 1	SN21	SN20	SN19	SN18	SN17	SN16	SN15	SN14
						SN27	SN26	SN25	SN24	SN23	SN22
0010		011101	Trim Voltage	RESERVED							
						TV5	TV4	TV3	TV2	TV1	TV0
0010		011111	All Setup Data	Daisy chain configuration only. This command returns all Page 2 data from address 6'h10 through 6'h1D in a single data stream. See "Communication Sequences" on page 57 and "System Out of Limit Detection" on page 73.							
0010	1010	100000	Cell 1 Balance Value 0	B0107	B0106	B0105	B0104	B0103	B0102	B0101	B0100
						B0113	B0112	B1011	B0110	B0109	B0108
0010	1010	100001	Cell 1 Balance Value 1	B0121	B0120	B0119	B0118	B0117	B0116	B0115	B0114
						B0127	B0126	B0125	B0124	B0123	B0122
0010	1010	100010	Cell 2 Balance Value 0	B0207	B0206	B0205	B0204	B0203	B0202	B0201	B0200
						B0213	B0212	B1011	B0210	B0209	B0208
0010	1010	100011	Cell 2 Balance Value 1	B0221	B0220	B0219	B0218	B0217	B0216	B0215	B0214
						B0227	B0226	B0225	B0224	B0223	B0222
		~	~	~							

Register Map (Continued)

R/W + PAGE		ADDRESS	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
READ	WRITE					BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
0010	1010	110111	Cell 12 Balance Value 1	B1221	B1220	B1219	B1218	B1217	B1216	B1215	B1214
						B1227	B1226	B1225	B1224	B1223	B1222
0010		111000	Reference Coefficient C	RCC7	RCC6	RCC5	RCC4	RCC3	RCC2	RCC1	RCC0
						RCC13	RCC12	RCC11	RCC10	RCC9	RCC8
0010		111001	Reference Coefficient B	RCB7	RCB6	RCB5	RCB4	RCB3	RCB2	RCB1	RCB0
						RCB13	RCB12	RCB11	RCB10	RCB9	RCB8
0010		111010	Reference Coefficient A	RCA2	RCA1	RCA0	RESERVED				
						RCA8	RCA7	RCA6	RCA5	RCA4	RCA3
0010		111011	Cells Balance Enabled (Valid in Stand-Alone only. Register read responds NAK otherwise).	CBEN8	CBEN7	CBEN6	CBEN5	CBEN4	CBEN3	BAL2	CBEN1
								CBEN12	CBEN11	CBEN10	CBEN9
0011		000001	Scan Voltages								
0011		000010	Scan Temperatures								
0011		000011	Scan Mixed								
0011		000100	Scan Wires								
0011		000101	Scan All								
0011		000110	Scan Continuous								
0011		000111	Scan Inhibit								
0011		001000	Measure								
0011		001001	Identify								
0011		001010	Sleep								
0011		001011	NAK								
0011		001100	ACK								
0011		001110	Comms Failure								
0011		001111	Wake-up								
0011		010000	Balance Enable								
0011		010001	Balance Inhibit								
0011		010010	Reset								
0011		010011	Calc Register Checksum								
0011		010100	Check Register Checksum								
0100		111111	EEPROM MISR Data Register	14-bit MISR EEPROM checksum value. Programmed during test.							
0101		000000	MISR Calculated Checksum	14-bit shadow register MISR checksum value. Calculated when shadow registers are loaded from nonvolatile memory.							

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
May 10, 2018	FN8830.3	Updated the Ordering Information table (removed Note 4, added tape and reel quantity column, added ISL78610EVKIT1Z, and updated Note 1). Removed Note 15 in Figure 63. Added Section “Daisy Chain Receive Buffer” on page 57. Added Figure 66 on page 57 and text to clarify Buffer over-flow. In Figures 61 to 63 and Figure 69, removed a 30us time reference between CS and first SPI clock. Changed the following abs Max values from 4.1V to 5.5V (BASE, DIN, SCLK, $\overline{CS}$, DOUT, $\overline{DATA\ READY}$, COMMS SELECT n, TEMPREG, REF, V3P3, VCC, $\overline{FAULT}$, COMMS RATE n, EN, VDDEXT). Updated Figure 41 and Figure 42 on page 24, Figure 43 and Figure 44 on page 25, Figure 51 on page 31, Figure 55 on page 35, and Figure 56 on page 36 to reflect new recommended input filter circuits. Added Table 2 on page 24 and Table 3 on page 25 and updated Table 11 on page 38. Added a paragraph in Section, “Daisy Chain Circuits,” on page 28 that discusses board capacitance effect on capacitor selection and changed Table 8 on page 28 and Table 9 on page 29 to match. Updated Figure 45 and added Table 5 (No actual changes to content). Updated Figure 48 and Table 8 (No actual changes to content). Updated Figure 49 and Table 9 (No actual changes to content). Updated Figure 50 and Table 10 (No actual changes to content). Removed About Intersil section and added new disclaimer.
Dec 21, 2016	FN8830.2	Clarified that “Cells in Balance” register is available only during Stand-Alone operation (page 49, page 92, page 97). Clarified that Scan Continuous functions during Manual, Timed, and Auto Balance Modes (page 42 and page 49). Clarified that the “BDDS” bit function in Timed and Auto Balance modes (page 49). Clarified the calculation of internal and external temperature values (page 84). Updated POD Q64.10x10D from rev 2 to rev 3. Changes: Added land pattern back in (as in rev 1), but removed the exposed pad.
Jun 16, 2016	FN8830.1	Updated ESD specification references to AEC on page 8. On page 15 in the “Performance Characteristics” tables updated the following MIN/MAX values: Initial Cell Reading Error -Minimum from “-3” to “-3.2” Maximum from “3” to “3.2” Initial VBAT Reading Error -Minimum from “-105” to “-175” Maximum from “105” to “175” -Minimum from “-175” to “-300” Maximum from “175” to “300” Initial Cell Monitor Voltage Error -Minimum from “-15” to “-12” Maximum from “-15” to “12” Initial VBAT Reading Error -Minimum from “-155” to “-250” Maximum from “155” to “250” -Minimum from “-285” to “-425” Maximum from “285” to “425” Replaced Figures 5 through 13 based on new bench board characterization.
Apr 12, 2016	FN8830.0	Initial Release

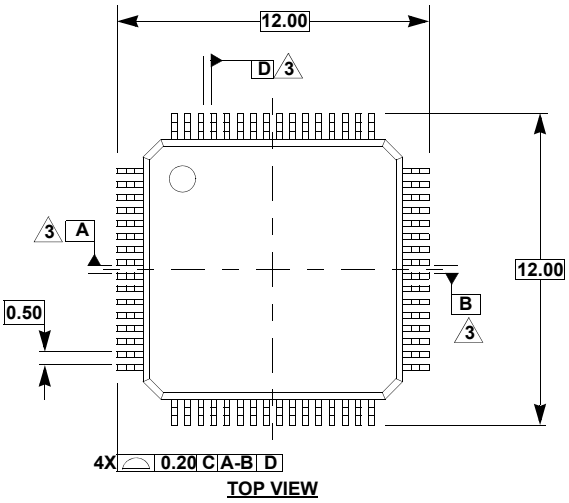
Package Outline Drawing

For the most recent package outline drawing, see Q64.10x10D.

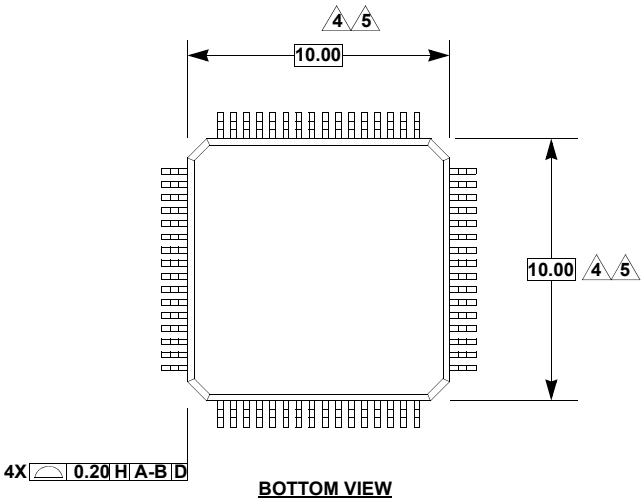
Q64.10x10D

64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

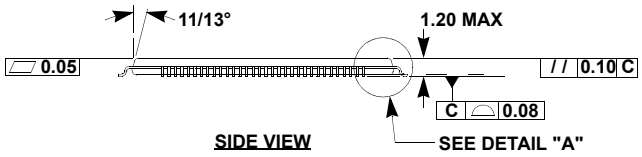
Rev 3, 11/16



TOP VIEW

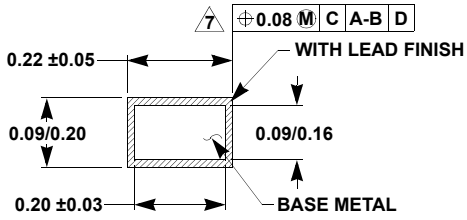


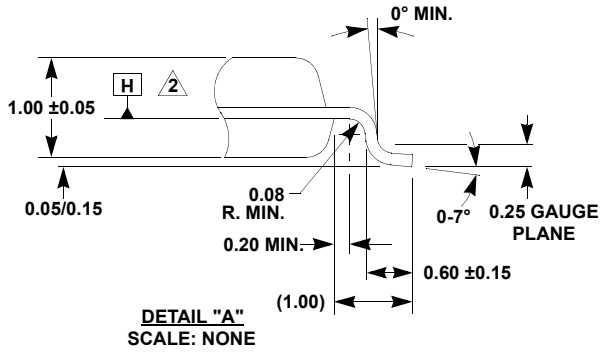
BOTTOM VIEW



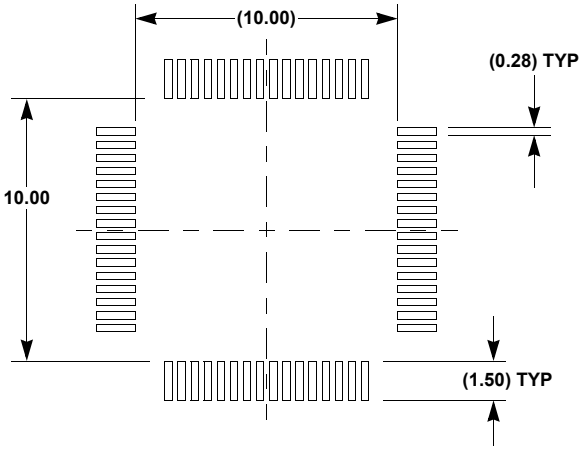
SIDE VIEW

SEE DETAIL "A"





DETAIL "A"
SCALE: NONE



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. All dimensioning and tolerancing conform to ANSI Y14.5-1982.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at centerline between leads where leads exit plastic body at datum plane H.
4. Dimensions do not include mold protrusion. Allowable mold protrusion is 0.254mm.
5. These dimensions to be determined at datum plane H.
6. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
7. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total at maximum material condition. Dambar cannot be located on the lower radius or the foot.
8. Controlling dimension: millimeter.
9. This outline conforms to JEDEC publication 95 registration MS-026, variation ACD.
10. Dimensions in ( ) are for reference only.

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