11.1Gb/s Driver

ISL35111

The ISL35111 is a de-emphasis driver with extended functionality for advanced protocols operating with line rates up to 11.1Gbps such as 10G Ethernet. The ISL35111 is a high-speed driver/limiting amplifier with built-in de-emphasis to drive twin-axial copper cables and compensate for the frequency dependent attenuation of PCB traces such as the SFI channel in the 10G SFP+ specification (SFF-8431).

Used in conjunction with Intersil's ISL36111 receive-side equalizer, ISL35111 enables active copper cable assemblies that support 10G serial data transmission over >15m of twin-axial copper cables.

Operating on a single 1.2V power supply, the ISL35111 enables channel throughputs of 10Gbps to 11.1Gbps while supporting lower data rates including 8.5, 6.25, 5, 4.25, 3.125, and 2.5Gb/s. The QL111VTx uses current mode logic (CML) input/output and is packaged in a 3mmx3mm 16 lead QFN.

Features

- Supports data rates up to 11.1Gbps
- Low power (85mW typical)
- Low latency (<500ps)
- Adjustable output de-emphasis
- Single channel driver in a 3mmx3mm QFN package for straight route-through architecture and simplified routing
- Supports 64b/66b encoded data – long run lengths
- Line silence preservation
- 1.2V supply voltage
- TX_Disable and TX_LOS

Applications

- Active copper cable modules (SFP+, QSFP, CXP, etc)
- Optical transceiver modules (SFP+, QSFP, CXP, etc)
- 10G Ethernet
- 40G/100G Ethernet
- Fibre Channel
- High-speed active cable assemblies
- High-speed printed circuit board (PCB) traces

Benefits

- Thinner gauge cable
- Extends cable reach greater than 3x
- Improved BER

Typical Application Diagram

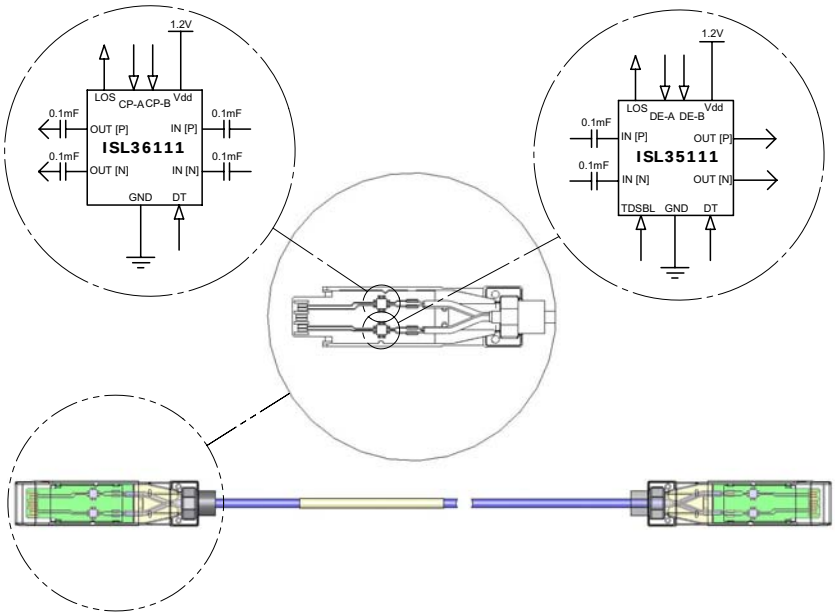


FIGURE 1. TYPICAL CABLE APPLICATION DIAGRAM

Ordering Information

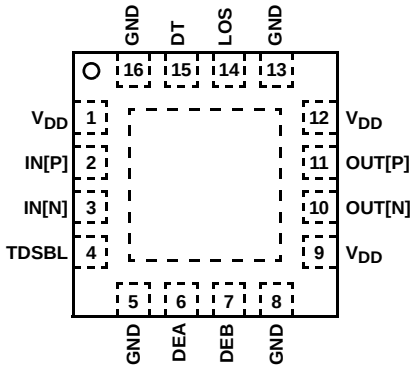
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL35111DRZ-TS	5111	0 to +85	16 Ld QFN (7'' 100 pcs.)	L16.3x3B
ISL35111DRZ-T7	5111	0 to +85	16 Ld QFN (7" 1k pcs.)	L16.3x3B

NOTES:

1. "-TS" and "-T7" suffix is for Tape and Reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL35111. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL35111
(16 LD QFN)
TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
V_{DD}	1, 9, 12	Power supply. 1.2V supply voltage. The use of parallel 100pF and 47nF decoupling capacitors to ground is recommended for each of these pins for broad high-frequency noise suppression.
IN[P,N]	2, 3	Driver differential input, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
TDSBL	4	Transmit Disable pin. Disables the IC and enters a low power mode when pulled HIGH. Must be externally pulled LOW for normal operation.
GND	5, 8, 13, 16	These pins must be grounded.
DE[A,B]	6, 7	Control pins for setting de-emphasis. CMOS logic inputs. Pins are read as a 2-digit number to set the de-emphasis level. A is the MSB, and B is the LSB. Pins are internally pulled up and down through 23kΩ resistors.
OUT[N,P]	10, 11	Driver differential output, CML. The use of 100nF low ESL/ESR MLCC capacitor with at least 6GHz frequency response is recommended.
LOS	14	LOS indicator. High output when Input signal is below DT threshold.
DT	15	Detection Threshold. Reference DC voltage threshold for input signal power detection. Data output OUT[P,N] is muted when the power of the input signal IN[P,N] falls below the threshold. Tie to ground to disable electrical idle preservation and always enable the output driver.
Exposed Pad	-	Exposed pad. For proper electrical and thermal performance, this pad should be connected to the PCB ground plane.

Absolute Maximum Ratings

Supply Voltage (V_{DD} to GND) . . . . . -0.3V to 1.5V
Voltage at All Input Pins . . . . . -0.3V to 1.5V
ESD Rating
High-Speed Pins . . . . . 1.5kV (HBM)
All Other Pins . . . . . 2kV (HBM)

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld QFN Package (Notes 4, 5) . .	56	10

Operating Ambient Temperature Range . . . . . 0°C to +85°C
Storage Ambient Temperature Range . . . . -55°C to +150°C
Maximum Junction Temperature . . . . . +125°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Operating Conditions

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		1.1	1.2	1.3	V
Operating Ambient Temperature	T_A		0	25	85	°C
Bit Rate		NRZ data applied to any channel		10	11.1	Gbps

Control Pin Characteristics

V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Input LOW Logic Level	V_{IL}	TDSBL	0	0	350	mV
Input HIGH Logic Level	V_{IH}	TDSBL	750		V_{DD}	mV
Output LOW Logic Level	V_{OL}	LOS	0	0	250	mV
Output HIGH Logic Level	V_{OH}	LOS	1000		V_{DD}	mV
Input Current		Current draw on DC control pin, i.e., DE[A,B]		30	100	µA

Electrical Characteristics

V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{DD}	De-Emphasis Disabled		65		mA	
		De-Emphasis Enabled		75		mA	
		Transmit Disable Mode		1.4		mA	
Input Amplitude Range	V_{IN}	Measured differentially at data source	120		1600	mV_{P-P}	
DC Differential Input Resistance		Measured on input channel IN[P,N]	80	100	120	Ω	
DC Single-Ended Input Resistance		Measured on input channel IN[P] or IN[N], with respect to V_{DD}.	40	50	60	Ω	
Input Return Loss Limit (Differential)	$S_{DD}11$	100MHz to 4.1GHz		See 6		dB	6
		4.1GHz to 11.1GHz		See 7		dB	7
Input Return Loss Limit (Diff. to Comm. Conversion)	$S_{CD}11$	100MHz to 11.1GHz		-10		dB	8
Output Amplitude Range	V_{OUT}	Measured differentially at OUT[P] and OUT[N] with 50Ω load on both output pins; de-emphasis disabled	450	700	820	mV_{P-P}	
Differential Output Impedance		Measured on OUT[k]	80	105	120	Ω	
Output Return Loss Limit (Differential)	$S_{DD}22$	100MHz to 4.1GHz		See 6		dB	6
		4.1GHz to 11.1GHz		See 7		dB	7

Electrical Characteristics V_{DD} = 1.2V, T_A = +25°C, and V_{IN} = 600mV_{P-P}, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Return Loss Limit (Common Mode)	$S_{CC}22$	100MHz to 2.5GHz		See 9		dB	9
		2.5GHz to 11.1GHz		-3		dB	8
Residual Deterministic Jitter		11.1Gbps; no channel attenuation; de-emphasis disabled		0.1		UI	10
Random Jitter				0.7		ps_{RMS}	
Output Transition Time	t_r, t_f	20% to 80%		35		ps	11
Minimum De-Emphasis Level				0		dB	
Maximum De-Emphasis Level				4		dB	
De-Emphasis Resolution				0.5		dB	

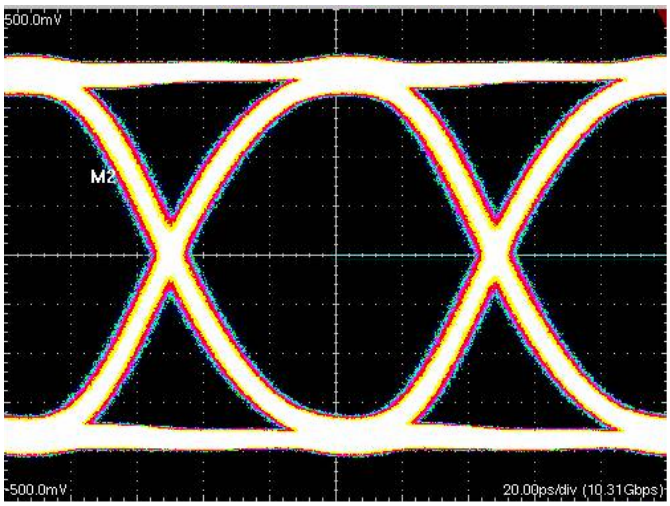
NOTES:

6. Maximum Reflection Coefficient given by equation SDDXX(dB)= -12 + 2*√(f), with f in GHz. Established by characterization and not production tested.
7. Maximum Reflection Coefficient given by equation SDDXX(dB)= -6.3 + 13Log10(f/5.5), with f in GHz. Established by characterization and not production tested.
8. Limits established by characterization and are not production tested.
9. Reflection Coefficient given by equation SCCXX(dB) < -7 + 1.6*f, with f in GHz. Established by characterization and not production tested.
10. Measured using a PRBS 2^{15}-1 pattern.
11. Rise and fall times measured using a 2GHz clock with a 20ps edge rate and with de-emphasis disabled.

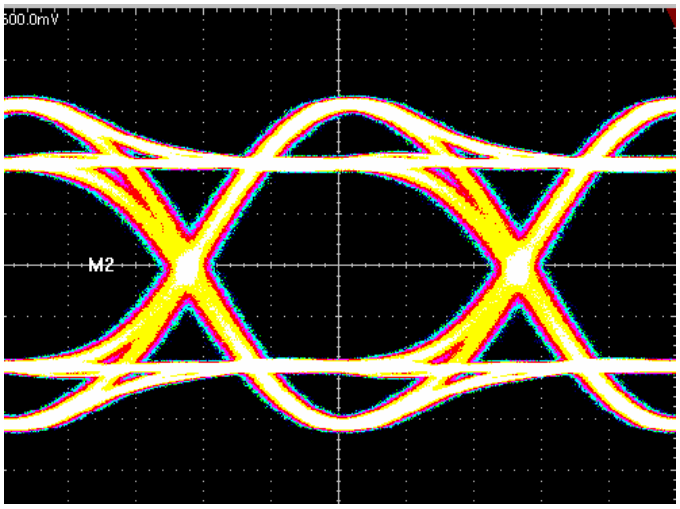
Typical Performance Characteristics

Performance is measured using the test setup illustrated in Figure 2. The signal from the pattern generator is launched into the chip evaluation board. The ISL35111 output signal is then visualized on a scope to determine signal integrity parameters such as jitter.

FIGURE 2. DEVICE CHARACTERIZATION TEST SETUP



3A. DE-EMPHASIS 0



3B. DE-EMPHASIS 6

FIGURE 3. ISL35111 10.3125Gbps OUTPUT; NO CHANNEL; PRBS-31

Typical Performance Characteristics (Continued)

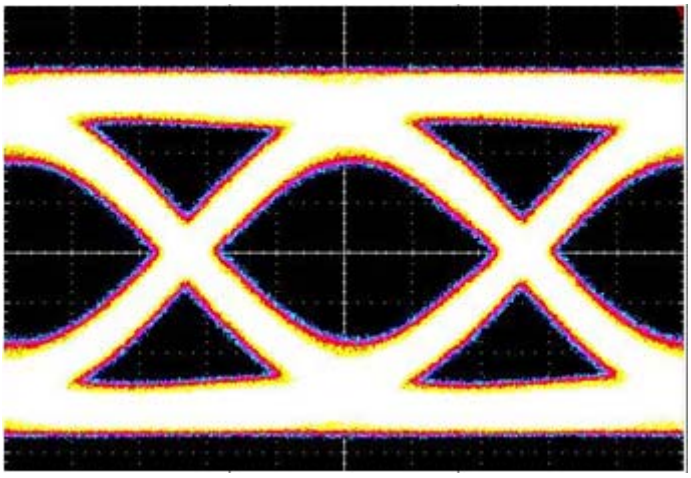


FIGURE 4. ISL35111 10.3125 GBPS OUTPUT AFTER A 22-INCH FR-408 TRACE, PRBS-31; DE-EMPHASIS 6

Operation

The ISL35111 is an advanced driver for high-speed interconnects. A functional diagram of ISL35111 is shown in Figure 5. In addition to a de-emphasis circuit to compensate for FR4 channel loss and restore signal fidelity, the ISL35111 contains unique integrated features to preserve special signaling protocols typically broken by other drivers. The signal detect function is used to mute the channel output when the input signal falls below the level determined by the Detection Threshold (DT) pin voltage. This function is intended to preserve periods of line silence.

As illustrated in Figure 5, the core of the high-speed signal path in the ISL35111 is a sophisticated driver followed by a de-emphasis circuit. The device applies pre-distortion to compensate for skin loss, dielectric loss, and impedance discontinuities in the transmission channel.

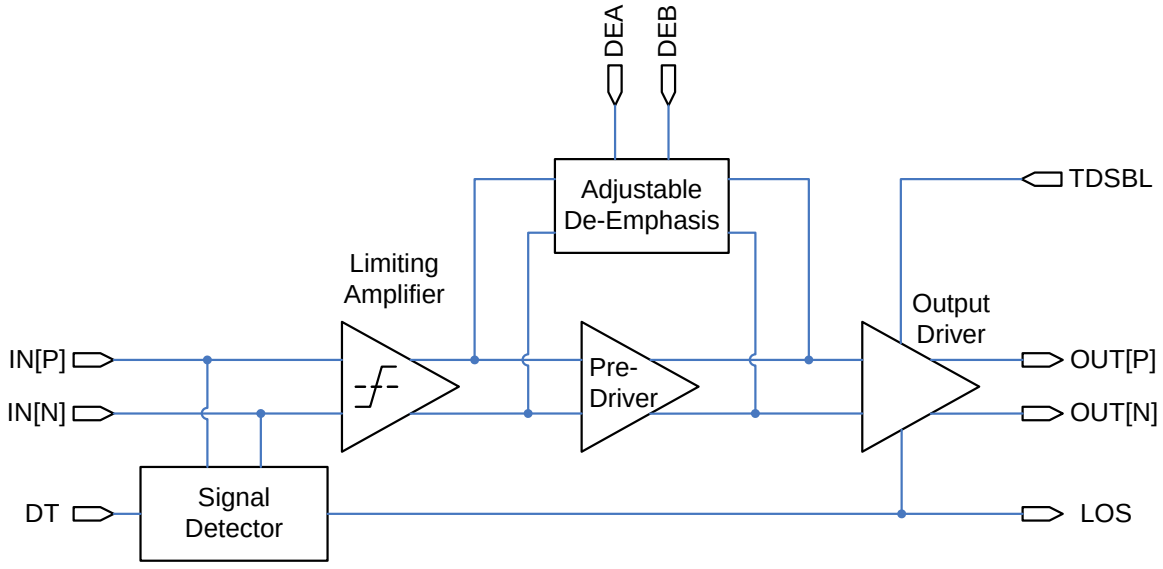


FIGURE 5. FUNCTIONAL BLOCK DIAGRAM OF THE ISL35111

CML Input and Output Buffers

The input and output buffers for the high-speed data channel in the ISL35111 are implemented using CML. Equivalent input and output circuits are shown in Figures 6 and 7.

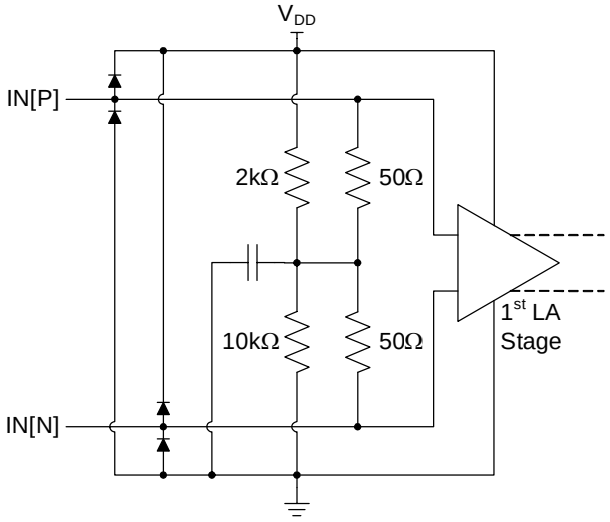


FIGURE 6. CML INPUT EQUIVALENT CIRCUIT FOR THE ISL35111

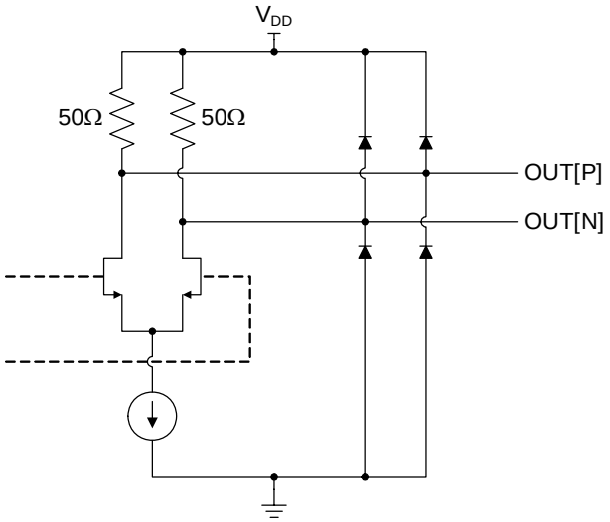


FIGURE 7. CML OUTPUT EQUIVALENT CIRCUIT FOR THE ISL35111

Adjustable De-Emphasis

ISL35111 features a settable de-emphasis driver for custom signal restoration.

The connectivity of the DE pins are used to determine the boost de-emphasis level of ISL35111. Table 1 defines the mapping from the 2-bit non-binary DE word to the 7 available output de-emphasis levels.

TABLE 1. MAPPING BETWEEN DE-EMPHASIS LEVEL AND DE-PIN CONNECTIVITY

DE PIN CONNECTION		NOMINAL DE-EMPHASIS LEVEL; 10.3125Gbps TO 11.1Gbps (dB)	DE-EMPHASIS SETTING
DE[A]	DE[B]		
Open	Open	0	0
Open	GND	0.6	1
Open	VDD	1.1	2
GND	Open	1.6	3
GND	GND	2.3	4
GND	VDD	3	5
VDD	Open	4	6

Disable Pin

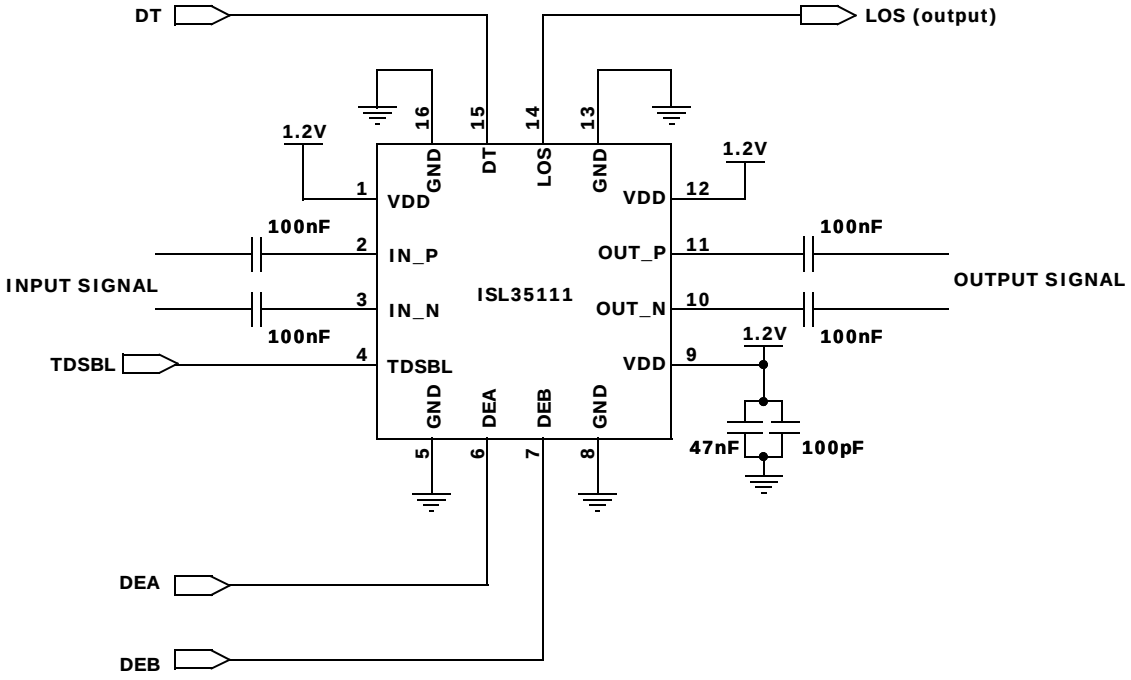
The disable (TDSBL) pin is used to disable the driver output in order to implement TX_Disable functions of such industry standards as SFP+ and QSFP. When this pin is pulled HIGH, the ISL35111 will enter a low-power standby mode. For active data transmission, this pin must be pulled LOW.

Line Silence / Quiescent Mode

The ISL35111 is capable of maintaining periods of line silence by monitoring its input pins for loss of signal (LOS) conditions and subsequently muting the output driver when such a condition is detected. A reference voltage applied to the detection threshold (DT) pin is used to set the LOS threshold of the internal signal detection circuitry. For most applications, it is recommended to leave the DT pin floating at its default internal bias. If the sensitivity of the detection threshold needs to be adjusted, the DT voltage can be adjusted with an external pull-up resistor. The resistor values should be validated on an application-specific basis. Connect the DT pin to ground in order to disable this feature and prevent the outputs from muting during line silence.

Application Information

Typical application schematic for ISL35111 is shown in Figure 8.



NOTES:

12. See “Adjustable De-Emphasis” on page 6 for information on how to connect the DE pins
13. See “Line Silence/Quiescent Mode” on page 6 for details on DT pin operation.
14. Although the filtering network is shown only for one V_{DD} pin for simplicity, all the V_{DD} pins need to be connected in this way.

FIGURE 8. TYPICAL APPLICATION REFERENCE SCHEMATIC FOR ISL35111

PCB Layout Considerations

Because of the high speed of the ISL35111 signals, careful PCB layout is critical to maximize performance. The following guidelines should be adhered to as closely as possible:

- All high speed differential pair traces should have a characteristic impedance of 50Ω with respect to ground plane and 100Ω with respect to each other.
- Avoid using vias for high speed traces as this will create discontinuity in the traces characteristic impedance.
- Input and output traces need to have DC blocking capacitors (100nF). Capacitors should be placed as close to the chip as possible.
- For each differential pair, the positive trace and the negative trace need to be of same length in order to avoid intra-pair skew. Serpentine technique may be used to match trace lengths.
- Maintain a constant solid ground plane underneath the high-speed differential traces
- Each V_{DD} pin should be connected to 1.2V and also bypassed to ground through a 47nF and a 100pF capacitor in parallel. Minimize the trace length and avoid vias between the V_{DD} pin and the bypass capacitors in order to maximize the power supply noise rejection.

About Q:ACTIVE®

Intersil has long realized that to enable the complex server clusters of next generation datacenters, it is critical to manage the signal integrity issues of electrical interconnects. To address this, Intersil has developed its groundbreaking Q:ACTIVE® product line. By integrating its analog ICs inside cabling interconnects, Intersil is able to achieve unsurpassed improvements in reach, power consumption, latency, and cable gauge size as well as increased airflow in tomorrow's datacenters. This new technology transforms passive cabling into intelligent "roadways" that yield lower operating expenses and capital expenditures for the expanding datacenter.

Intersil Lane Extenders allow greater reach over existing cabling while reducing the need for thicker cables. This significantly reduces cable weight and clutter, increases airflow, and improves power consumption.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
1/27/10	FN6975.1	1. Updated pin description for DE[A,B]. 2. Added Application Information, Figure 8, and PCB Layout section. 3. Changed VDD pin description to read "..and 47nF." 4. Replaced Figure 5. 5. Corrected pin description for DE pin to read "..as a 2-digit number.".
11/19/09	FN6975.0	Initial Release to web

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL35111

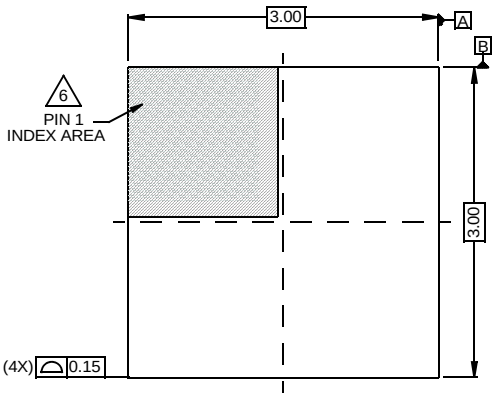
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

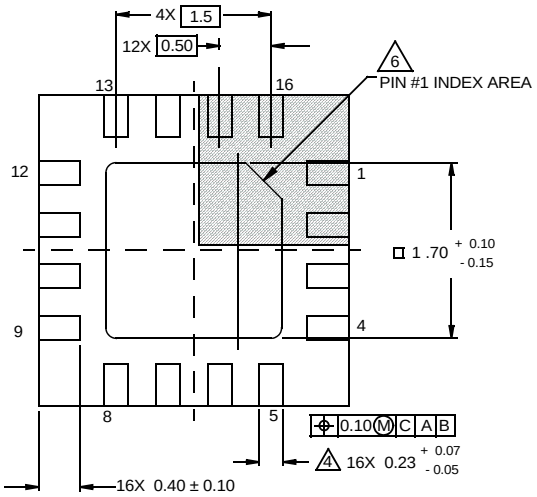
Package Outline Drawing

L16.3x3B

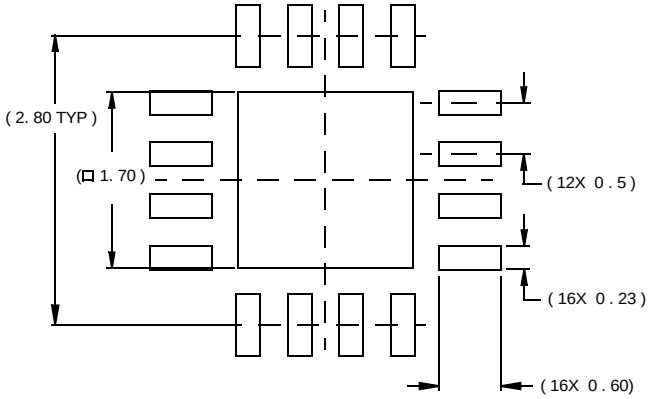
16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 4/07



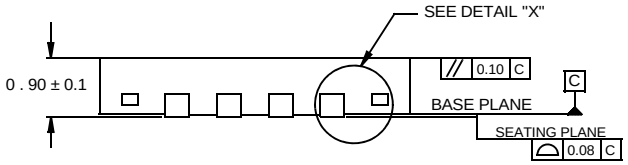
TOP VIEW



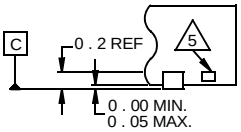
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.