

6-Channel SMBus/I²C or PWM Dimming LED Driver with Phase Shift Control

ISL97671A

The ISL97671A is a 6-Channel 45V dual dimming capable LED driver that can be used with either SMBus/I²C or PWM signal for dimming control. The ISL97671A can drive six channels of LEDs from input 4.5V~26.5V to output of up to 45V. It can also operate from input as low as 3V to output of up to 26.5V in bootstrap configuration (see Figure 40).

The ISL97671A features optional channel phase shift control to minimize the input, output ripple characteristics and load transients as well as spreading the light output to help reduce the video and audio interference from the backlight driver operation.

The device can also be configured in Direct PWM Dimming with minimum dimming duty cycle of 0.007% at 200Hz.

The ISL97671A can compensate for the non-uniformity of the forward voltage drops in the LED strings and its headroom control circuit monitors the highest LED forward voltage string for output regulation, to minimize the voltage headroom and power loss in a typical multi-string operation.

The ISL97671A is offered in compact and thermally efficient QFN-20 4mmx3mm package.

Features

- 6 x 50mA Channels
- 4.5V to 26.5V Input with Max 45V Output
- 3V (see Figure 40) to 21V Input with Max 26.5V Output
- PWM Dimming with Phase Shift Control
- SMBus/I²C controlled PWM or DC Dimming
- Direct PWM Dimming
- PWM Dimming Linearity
 - PWM Dimming with Adjustable Dimming Freq and Duty Cycle Linear from 0.4% to 100% <30kHz
 - Direct PWM Dimming Duty Cycle Linear from 0.007% to 100% at 200Hz
- Current Matching $\pm 0.7\%$
- 600kHz/1.2MHz selectable switching frequency
- Dynamic Headroom Control
- Fault Protection
 - String Open/Short Circuit, OVP, OTP, and Optional Output Short Circuit Fault Protection
- 20 Ld 4mmx3mm QFN Package

Applications

- Tablet PC to Notebook Displays LED Backlighting
- LCD Monitor LED Backlighting
- RGB LEDs or Field Sequential LED Backlighting

Typical Application Circuits

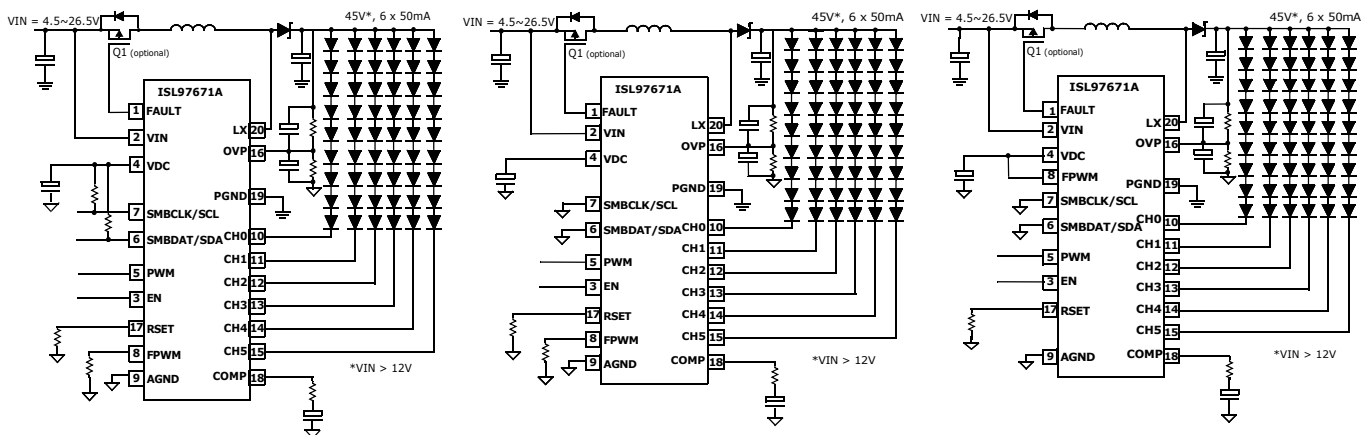


FIGURE 1A. SMBus/I²C CONTROLLED DIMMING

FIGURE 1B. PWM DIMMING WITH ADJUSTABLE DIMMING

FIGURE 1C. DIRECT PWM DIMMING

FIGURE 1. ISL97671A TYPICAL APPLICATION DIAGRAMS

ISL97671A

Block Diagram

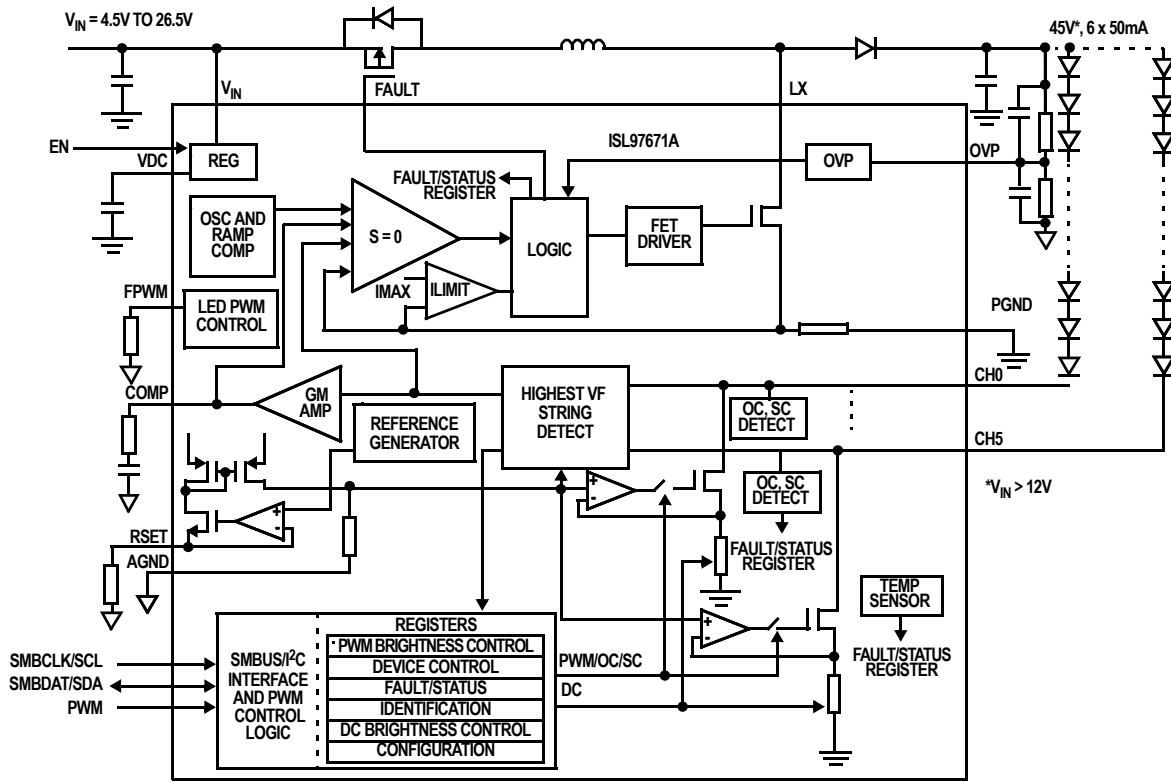


FIGURE 2. ISL97671A BLOCK DIAGRAM

ISL97671A

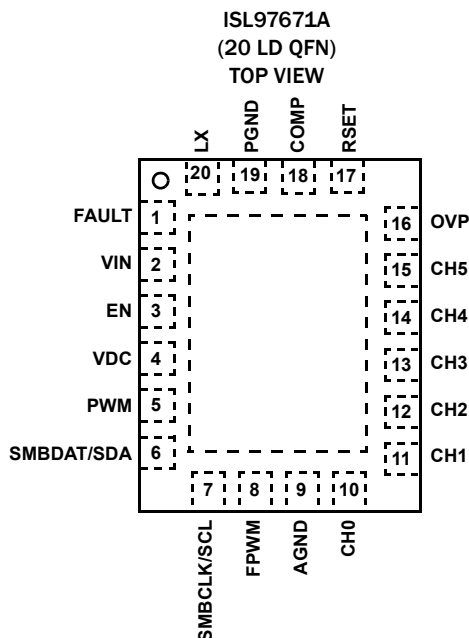
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL97671AIRZ	671A	20 Ld 3x4 QFN	L20.3x4
ISL97671AIRZ-EVALZ	Evaluation Board		

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL97671A](#). For more information on MSL please see techbrief [TB363](#).

Pin Configuration



Pin Descriptions (I = Input, O = Output, S = Supply, X = Don't Care)

PIN NAME	PIN #	TYPE	DESCRIPTION
FAULT	1	O	Fault Disconnect Switch Gate Control.
VIN	2	S	Input voltage for the device and LED power.
EN	3	I	The device needs 4ms for initial power-up enable. It will be disabled if it is not biased for longer than 28ms.
VDC	4	S	De-couple capacitor for internally generated supply rail.
PWM	5	I	PWM brightness control pin or DPST control input.
SMBDAT/SDA*	6	I/O	SMBus/I ² C serial data input and output. When pins 6 and 7 are grounded or in logic 0's for longer than 60ms, the drivers will be controlled by external PWM signal.
SMBCLK/SCL*	7	I	SMBus/I ² C serial clock input. When pins 6 and 7 are grounded or in logic 0's for longer than 60ms, the drivers will be controlled by external PWM signal.
FPWM	8	I	Set PWM dimming frequency, FPWM by connecting a resistor. When FPWM ties to VDC and SMBCLK/SMBDAT tie to ground, the device will be in Direct PWM Dimming where the output follows the input frequency and duty cycle without any digitization.
AGND	9	S	Analog Ground for precision circuits.
CH0, CH1, CH2, CH3, CH4, CH5	10, 11, 12, 13, 14, 15	I	Input 0, Input 1, Input 2, Input 3, Input 4, Input 5 to current source, FB, and monitoring.
OVP	16	I	Overvoltage protection input.
RSET	17	I	Resistor connection for setting LED current, (see Equation 2 for calculating the $I_{LED(peak)}$).
COMP	18	O	Boost compensation pin.
PGND	19	S	Power ground
LX	20	O	Input to boost switch.
EPAD			No electrical connection but should be used to connect PGND and AGND. For example uses top plane as PGND and bottom plane as AGND with vias on EPAD to allow heat dissipation and minimum noise coupling from PGND to AGND operation.

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Absolute Maximum Ratings (T_A = +25°C)

VIN, EN	-0.3V to 28V
FAULT	VIN - 8.5V to VIN + 0.3V
VDC, COMP, RSET	-0.3V to 5.5V
SMBCLK/SCL*, SMBDAT/SDA*, FPWM, PWM	-0.3V to 5.5V
EN, OVP	-0.3V to 5.5V
CHO - CH5, LX	-0.3V to 45V
PGND, AGND	-0.3V to +0.3V

Above voltage ratings are all with respect to AGND pin

ESD Rating

Human Body Model (Tested per JESD22-A114E)	3kV
Machine Model (Tested per JESD22-A115-A)	300V
Charged Device Model	1kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld QFN Package (Notes 4, 5, 7)	40	2.5
Thermal Characterization (Typical)	PSI _{JT} (°C/W)	
20 Ld QFN Package (Note 6)	1	
Maximum Continuous Junction Temperature	+125°C	
Storage Temperature	-65°C to +150°C	
Pb-Free Reflow Profile	see link below	

<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

Operating Conditions

Temperature Range -40°C to +85°C

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: T_J = T_C = T_A

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For θ_{JC} , the "case temp" location is the center of the exposed metal pad on the package underside.
- PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JA} thermal resistance ratings.
- Refer to JESD51-7 high effective thermal conductivity board layout for proper via and plane designs.

Electrical Specifications V_{IN} = 12V, EN = 5V, R_{SET} = 20.1k Ω , unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
GENERAL						
V _{IN} (Note 9)	Backlight Supply Voltage	≤13 LEDs per channel (3.2V/20mA type)	4.5		26.5	V
I _{VIN_STBY}	V _{IN} Shutdown Current	T _A = +25°C			5	μA
I _{VIN}	V _{IN} Active Current	EN = 5V		5		mA
V _{OUT}	Output Voltage	4.5V < V _{IN} ≤ 26V, F _{SW} = 600kHz			45	V
		8.55V < V _{IN} ≤ 26V, F _{SW} = 1.2MHz			45	V
		4.5V < V _{IN} ≤ 8.55V, F _{SW} = 1.2MHz			V_{IN}/0.19	V
V _{UVLO}	Undervoltage Lockout Threshold		2.1		2.6	V
V _{UVLO_HYS}	Undervoltage Lockout Hysteresis			200		mV
REGULATOR						
V _{DC}	LDO Output Voltage	V _{IN} ≥ 6V	4.55	4.8	5	V
I _{VDC_STBY}	Standby Current	EN = 0V			5	μA
V _{LDO}	VDC LDO Droop Voltage	V _{IN} > 5.5V, 20mA		20	200	mV
EN _{LOW}	Guaranteed Range for EN Input Low Voltage				0.5	V
EN _{HI}	Guaranteed Range for EN Input High Voltage		1.8			V
t _{ENLow}	EN Low Time Before Shut-down			30.5		ms
BOOST						
SW _I Limit	Boost FET Current Limit		1.5	2.0	2.7	A

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Electrical Specifications $V_{IN} = 12V$, $EN = 5V$, $R_{SET} = 20.1k\Omega$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40 °C to +85 °C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
$r_{DS(ON)}$	Internal Boost Switch ON-resistance	$T_A = +25^\circ C$		235	300	m Ω
SS	Soft-Start	100% LED Duty Cycle		7		ms
Eff_peak	Peak Efficiency	$V_{IN} = 12V$, 72 LEDs, 20mA each, L = 10 μ H with DCR 101m Ω , $T_A = +25^\circ C$		92.9		%
		$V_{IN} = 12V$, 60 LEDs, 20mA each, L = 10 μ H with DCR 101m Ω , $T_A = +25^\circ C$		90.8		%
$\Delta I_{OUT}/\Delta V_{IN}$	Line Regulation			0.1		%
D_{MAX}	Boost Maximum Duty Cycle	$F_{SW} = 1$, 600kHz	90			%
		$F_{SW} = 0$, 1.2MHz	81			
D_{MIN}	Boost Minimum Duty Cycle	$F_{SW} = 1$, 600kHz			9.5	%
		$F_{SW} = 0$, 1.2MHz			17	
f_{OSC_hi}	Lx Frequency High	$F_{SW} = 1$, 600kHz	475	600	640	kHz
f_{OSC_lo}	Lx Frequency Low	$F_{SW} = 0$, 1.2MHz	0.97	1.14	1.31	MHz
$I_{LX_leakage}$	LX Pin Leakage Current	LX = 45V, EN = 0V			10	μ A
REFERENCE						
FAULT DETECTION						
V_{SC}	Short Circuit Threshold Accuracy		7.5	8.2		V
Temp_shtdwn	Temperature Shutdown Threshold			150		$^\circ C$
Temp_Hyst	Temperature Shutdown Hysteresis			23		$^\circ C$
V_{OVPI0}	Overvoltage Limit on OVP Pin		1.19		1.25	V
CURRENT SOURCES						
I_{MATCH}	DC Channel-to-Channel Current Matching	$R_{SET} = 20.1k\Omega$, Reg0x00 = 0xFF, ($I_{OUT} = 20mA$)		± 0.7	± 1.0	%
I_{ACC}	Current Accuracy		-1.5		+1.5	%
$V_{HEADROOM}$	Dominant Channel Current Source Headroom at CH Pin	$I_{LED} = 20mA$ $T_A = +25^\circ C$		500		mV
V_{RSET}	Voltage at RSET Pin	$R_{SET} = 20.1k\Omega$	1.2	1.22	1.24	V
$I_{LED(max)}$	Maximum LED Current per Channel	$V_{IN} = 12V$, $V_{OUT} = 45V$, $F_{sw} = 1.2MHz$, $T_A = +25^\circ C$		50		mA
PWM GENERATOR						
V_{IL}	Guaranteed Range for PWM Input Low Voltage				0.8	V
V_{IH}	Guaranteed Range for PWM Input High Voltage		1.5		VDD	V
F_{PWMI}	PWM Input Frequency Range		200		30,000	Hz
PWMACC	PWM Dimming Accuracy (Except Direct PWM Dimming)			8		bits
$t_{DIRECTPWM}$	Direct PWM Minimum On Time	Direct PWM Mode	250		350	ns
F_{PWM}	PWM Dimming Frequency Range		100		30,000	Hz
FAULT PIN						
I_{FAULT}	Fault Pull-down Current	$V_{IN} = 12V$	12	21	30	μ A
V_{FAULT}	Fault Clamp Voltage with Respect to V_{IN}	$V_{IN} = 12$, $V_{IN} - V_{FAULT}$	6	7	8.3	V

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Electrical Specifications $V_{IN} = 12V$, $EN = 5V$, $R_{SET} = 20.1k\Omega$, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40 °C to +85 °C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
LXstart_thres	LX Start-up Threshold		0.9		1.2	V
ILXStart-up	LX Start-up Current		1	3.5	5	mA
SMBus/I²C INTERFACE						
V_{IL}	Guaranteed Range for Data, Clock Input Low Voltage				0.8	V
V_{IH}	Guaranteed Range for Data, Clock Input High Voltage		1.5		VDD	V
V_{OL}	SMBus/I ² C Data line Logic Low Voltage	$I_{PULLUP} = 4mA$			0.17	V
I_{LEAK}	Input Leakage On SMBData/SMBClk	Measured at 4.8V	-10		10	μA
SMBus/I²C TIMING SPECIFICATIONS						
t_{EN-SMB/I^2C}	Minimum Time Between EN high and SMBus/I ² C Enabled	1 μF capacitor on VDC	2			ms
PWS	Pulse Width Suppression on SMBCLK/SMBDAT		0.15		0.45	μs
f_{SMB}	SMBus/I ² C Clock Frequency				400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		1.3			μs
$t_{HD:STA}$	Hold Time After (Repeated) START Condition. After this Period, the First Clock is Generated		0.6			μs
$t_{SU:STA}$	Repeated Start Condition Setup Time		0.6			μs
$t_{SU:STO}$	Stop Condition Setup Time		0.6			μs
$t_{HD:DAT}$	Data Hold Time		300			ns
$t_{SU:DAT}$	Data Setup Time		100			ns
t_{LOW}	Clock Low Period		1.3			μs
t_{HIGH}	Clock High Period		0.6			μs
t_F	Clock/data Fall Time				300	ns
t_R	Clock/data Rise Time				300	ns

NOTES:

- Parameters with MIN and/or MAX limits are 100% tested at +25 °C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- At maximum V_{IN} of 26.5V, minimum V_{OUT} is limited 28V.

Typical Performance Curves

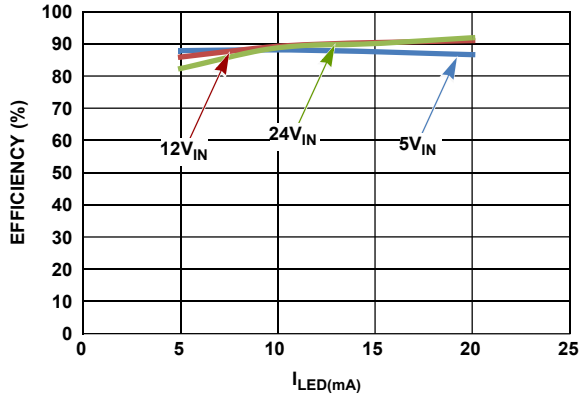


FIGURE 3. EFFICIENCY vs up to 20mA LED CURRENT (100% LED DUTY CYCLE) vs V_{IN}

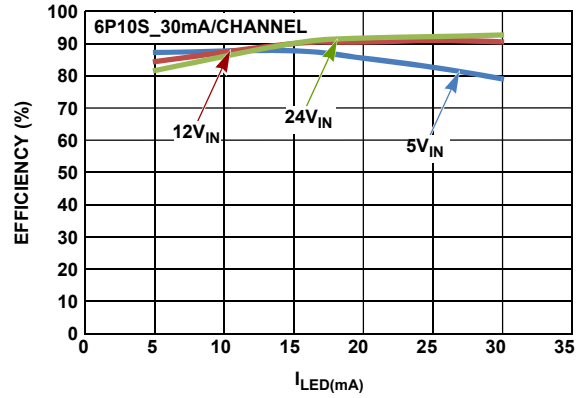


FIGURE 4. EFFICIENCY vs up to 30mA LED CURRENT (100% LED DUTY CYCLE) vs V_{IN}

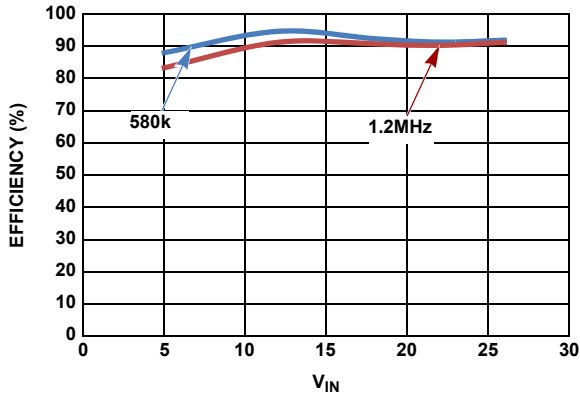


FIGURE 5. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 20mA (100% LED DUTY CYCLE)

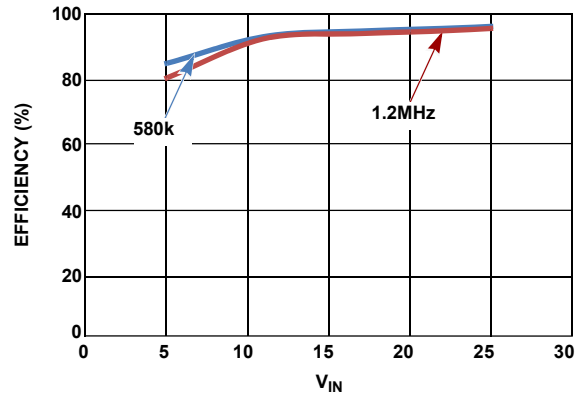


FIGURE 6. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 30mA (100% LED DUTY CYCLE)

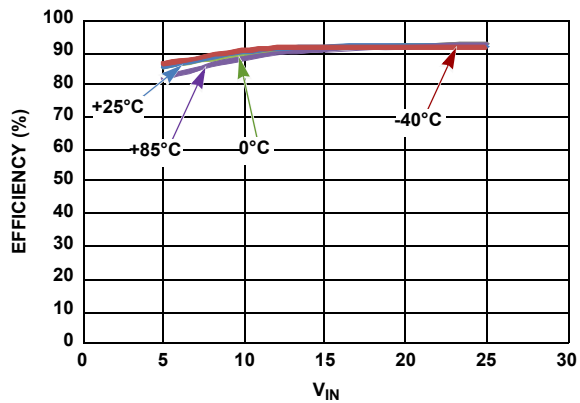


FIGURE 7. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 20mA (100% LED DUTY CYCLE)

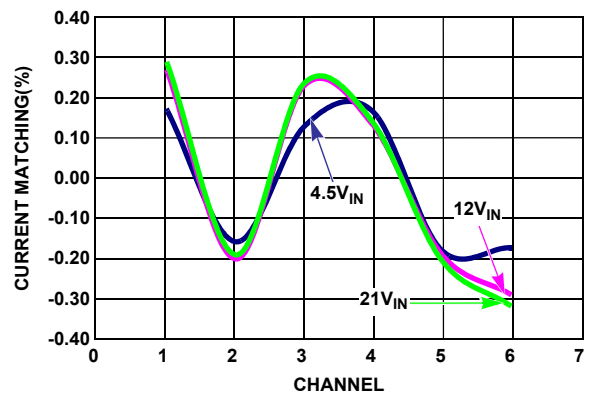


FIGURE 8. CHANNEL-TO-CHANNEL CURRENT MATCHING

Typical Performance Curves (Continued)

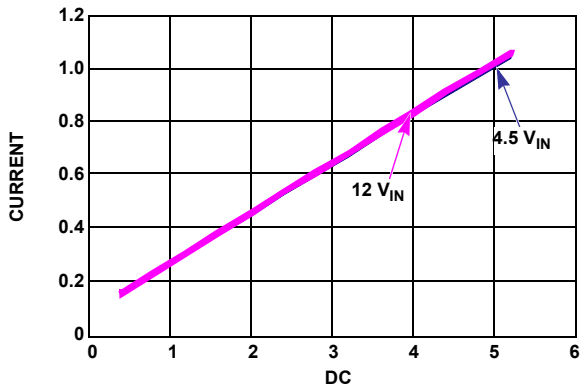


FIGURE 9. CURRENT LINEARITY vs LOW LEVEL PWM DIMMING DUTY CYCLE vs V_{IN}

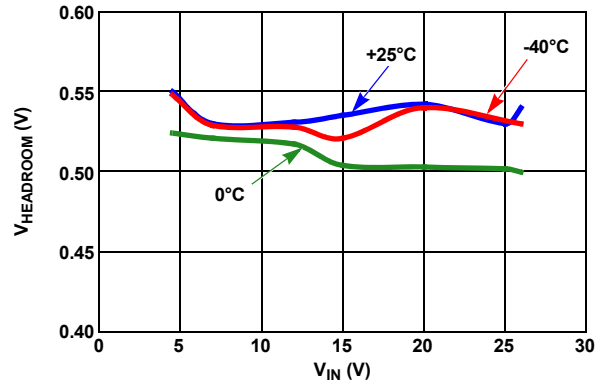


FIGURE 10. $V_{HEADROOM}$ vs V_{IN} AT 20mA

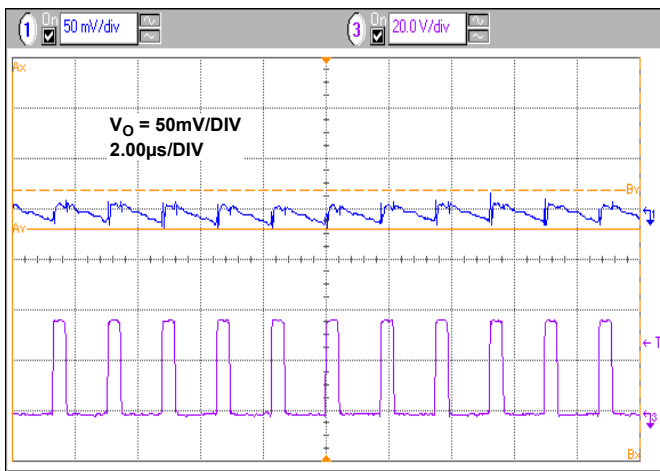


FIGURE 11. V_{OUT} RIPPLE VOLTAGE, $V_{IN} = 12V$, 6P12S AT 20mA/CHANNEL

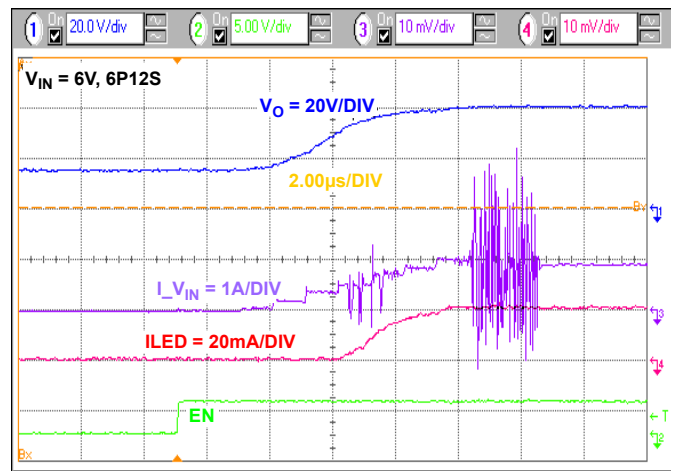


FIGURE 12. IN-RUSH and LED CURRENT AT $V_{IN} = 6V$ FOR 6P12S AT 20mA/CHANNEL

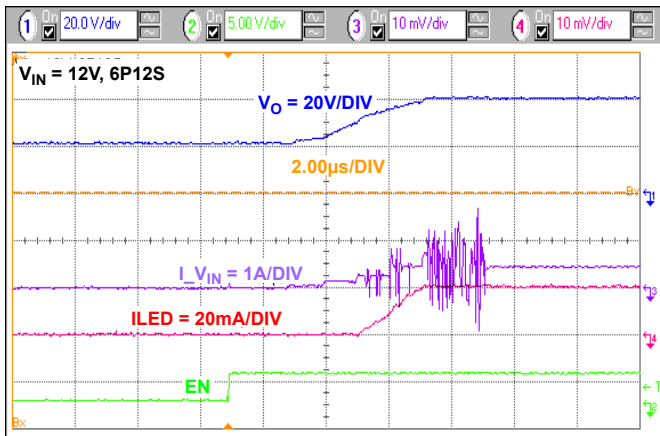


FIGURE 13. IN-RUSH and LED CURRENT AT $V_{IN} = 12V$ FOR 6P12S AT 20mA/CHANNEL

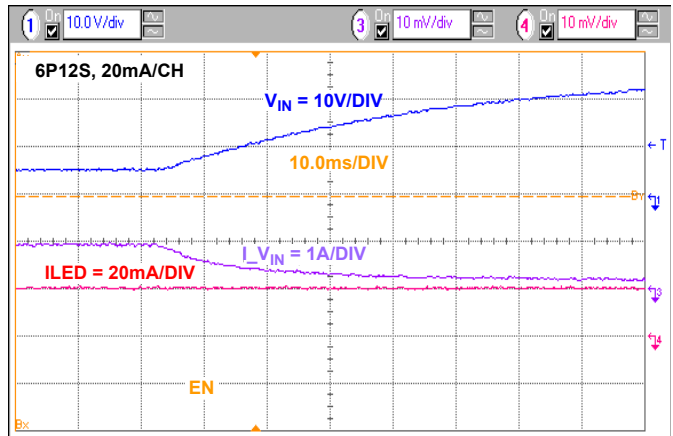


FIGURE 14. LINE REGULATION WITH V_{IN} CHANGE FROM 6V TO 26V, $V_{IN} = 12V$, 6P12S AT 20mA/CHANNEL

Typical Performance Curves (Continued)

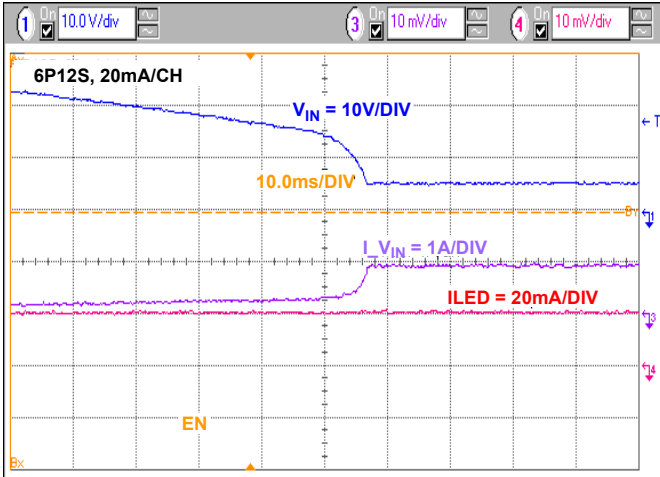


FIGURE 15. LINE REGULATION WITH V_{IN} CHANGE FROM 26V TO 6V FOR 6P12S AT 20mA/CHANNEL

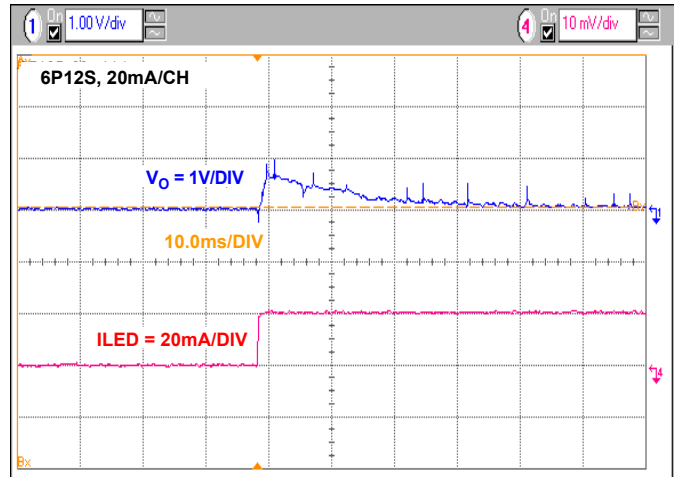


FIGURE 16. LOAD REGULATION WITH I_{LED} CHANGE FROM 0% TO 100% PWM DIMMING, $V_{IN} = 12V$, 6P12S AT 20mA/CHANNEL

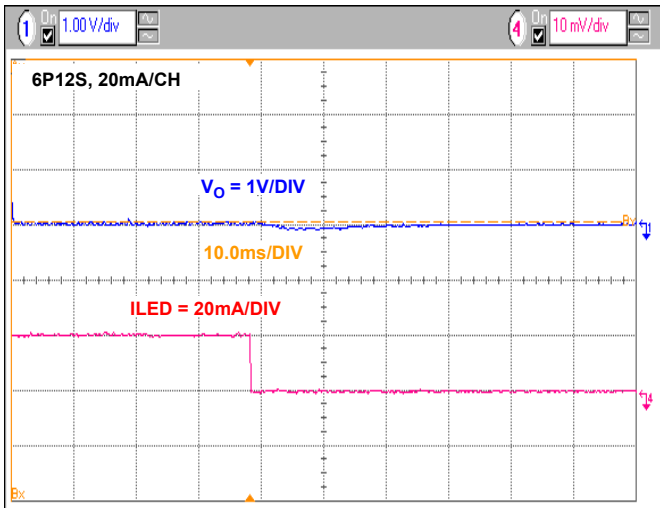


FIGURE 17. LOAD REGULATION WITH I_{LED} CHANGE FROM 100% TO 0% PWM DIMMING, $V_{IN} = 12V$, 6P12S AT 20mA/CHANNEL

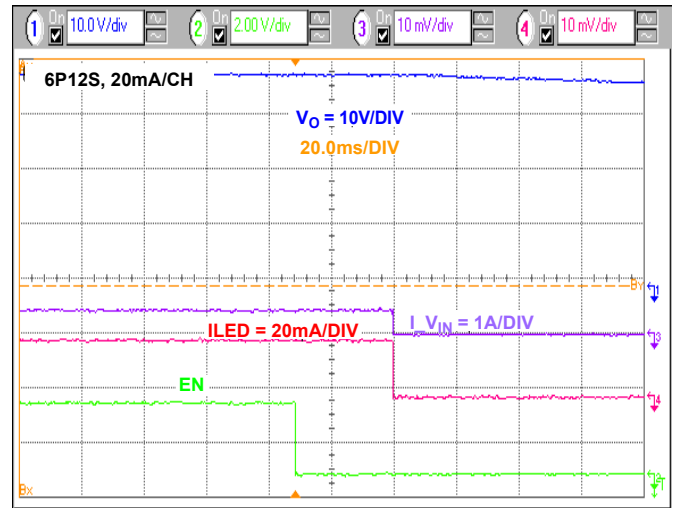


FIGURE 18. ISL97672A SHUTS DOWN AND STOPS SWITCHING ~30ms AFTER EN GOES LOW

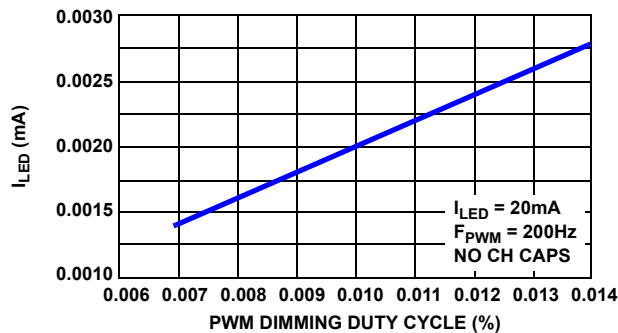


FIGURE 19. DIRECT PWM DIMMING MINIMUM DIMMING LINEARITY

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97671A employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for the notebook backlight application where the power can be a series of drained batteries or instantly change to an AC/DC adapter without rendering a noticeably visual nuisance. The number of LEDs that can be driven by ISL97671A depends on the type of LED chosen in the application. The ISL97671A is capable of boosting up to 45V and drive 6 channels of LEDs.

Enable

The EN pin is used to enable or disable the ISL97671A operation. It is a high voltage pin that can be tied directly to V_{IN} up to 26.5V if the system lacks of I/O for enable signal.

OVP and V_{OUT} Requirement

The Overvoltage Protection (OVP) pin has a function of setting the overvoltage trip level as well as limiting the V_{OUT} regulation range.

The ISL97671A OVP threshold is set by R_{UPPER} and R_{LOWER} as shown in Equation 1:

$$V_{OUT_OVP} = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad (EQ. 1)$$

V_{OUT} can only regulate between 64% and 100% of the V_{OUT_OVP} such that:

Allowable V_{OUT} = 64% to 100% of V_{OUT_OVP}

For example, if 10 LEDs are used with the worst case V_{OUT} of 35V. If R_1 and R_2 are chosen such that the OVP level is set at 40V, then the V_{OUT} is allowed to operate between 25.6V and 40V. If the requirement is changed to a 6 LEDs 21V V_{OUT} application, then the OVP level must be reduced and users should follow $V_{OUT} = (64\% \sim 100\%)$ OVP requirement. Otherwise, the headroom control will be disturbed such that the channel voltage can be much higher than expected and sometimes it can prevent the driver from operating properly.

The ratio of the OVP capacitors should be the inverse of the OVP resistors. For example, if $R_{UPPER} / R_{LOWER} = 33/1$, then $C_{UPPER} / C_{LOWER} = 1/33$ with $C_{UPPER} = 100pF$ and $C_{LOWER} = 3.3nF$.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 20.

The LED peak current is set by translating the R_{SET} current to the output with a scaling factor of $401.8/R_{SET}$. The source terminals of the current source MOSFETs are designed to run at 500mV to optimize power loss versus accuracy requirements. The sources of errors of the channel-to-channel current matching come from the op amps offset, internal layout, reference, and current source resistors. These parameters are optimized for current matching and absolute current accuracy. On the other hand, the absolute accuracy is additionally determined by the external R_{SET} , and therefore, additional

tolerance will be contributed by the current setting resistor. A 1% tolerance resistor is therefore recommended.

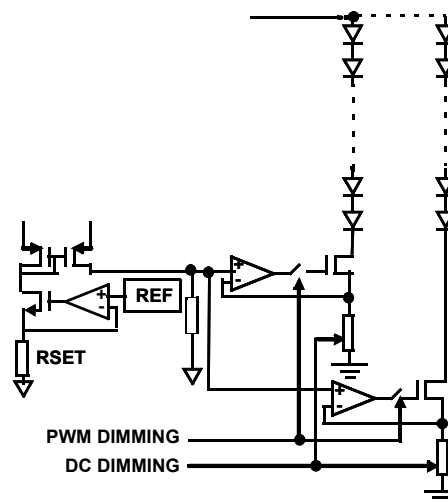


FIGURE 20. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97671A features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage from any of the CHO-CH5 pins. When this lowest channel voltage is lower than the short circuit threshold, V_{SC} , such voltage will be used as the feedback signal for the boost regulator. The boost makes the output to the correct level such that the lowest channel pin is at the target headroom voltage. Since all LED stacks are connected to the same output voltage, the other channel pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same programmed current. The output voltage will regulate cycle-by-cycle and is always referenced to the highest forward voltage string in the architecture.

Dimming Controls

The ISL97671A provides SMBus/I²C controlled PWM or DC dimming where the users need to turn the LEDs on through the SMBus/I²C communications (see the “SMBus/I²C Communications” on page 18). The ISL97671A also provides PWM dimming by external PWM signal where the SMBCLK and SMBDAT pins are grounded or pulled low and the dimming frequency can be adjusted. The ISL97671A also allows Direct PWM Dimming where the output duty cycle and dimming frequency follow the input PWM signal. The three dimming mode selection is summarized in Table 1.

TABLE 1. DIMMING MODE SELECTION

SMBCLK/SCL Pin SIGNAL	SMBDAT/SDA PIN SIGNAL	FPWM PIN	DIMMING MODE SELECTION
Low	Low	Resistor to ground	PWM Dimming with Adjustable Dimming Frequency, Phase Shift Enabled
Low	Low	Tie to VDC	Direct PWM Dimming
SMBus clock	SMBus data	Resistor to ground	SMBus Controlled Dimming
I ² C clock	I ² C data	Resistor to ground	I ² C Controlled Dimming

The ISL97671A allows two ways of controlling the LED current, and therefore, the brightness. They are:

1. DC current adjustment
2. PWM chopping of the LED current defined in Step 1.

There are various ways to achieve DC or PWM current control, described in the following.

MAXIMUM DC CURRENT SETTING

The initial brightness should be set by choosing an appropriate value for R_{SET} . This should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{401.8}{R_{SET}} \quad (EQ. 2)$$

Once R_{SET} is fixed, the LED DC current can be adjusted through Register 0x07 (BRTDC) as follows:

$$I_{LED} = 1.58 \times (BRTDC / R_{SET}) \quad (EQ. 3)$$

BRTDC can be programmed from 0 to 255 in decimal and defaults to 255 (0xFF). If left at the default value, LED current will be fixed at I_{LEDmax} . BRTDC can be adjusted dynamically on the fly during operation. BRTDC = 0 disconnects all channels.

For example, if the maximum required LED current ($I_{LED(max)}$) is 20mA, rearranging Equation 2 yields Equation 4:

$$R_{SET} = 401.8 / 0.02 = 20.1k\Omega \quad (EQ. 4)$$

If BRTDC is set to 200 then:

$$I_{LED} = 1.58 \cdot 200 / 20100 = 15.7mA \quad (EQ. 5)$$

PWM DIMMING CONTROL

The ISL97671A provides multiple PWM dimming methods, as described in the following. Each of these methods results in PWM chopping of the current in the LEDs for all 6 channels to provide an average LED current. During the On periods, the LED current will be defined by the value of R_{SET} and BRTDC, as described in Equations 2 and 3. The source of the PWM signal can be described as follows:

1. **Internally generated** 256 step duty cycle programmed through the SMBus/I²C.
2. **External** signal from PWM.
3. **DPST mode.** Internally generated signal with a duty cycle defined by the product of the external PWM and SMBus/I²C programmed PWM at the internal setting frequency.

The default PWM dimming is in DPST mode. In all of the methods, the average LED channel current is controlled by I_{LED} and the PWM duty cycle in percent, as shown in Equation 6:

$$I_{LED(ave)} = I_{LED} \times PWM \quad (EQ. 6)$$

Method 1 (Internal Mode, SMBus/I²C controlled PWM)

The average LED channel current is controlled by the internally generated PWM signal, as shown in Equation 7:

$$I_{LED(ave)} = I_{LED} \times (BRT / 255) \quad (EQ. 7)$$

where BRT is the PWM brightness level programmed in the Register 0x00. BRT ranges from 0 to 255 in decimal and defaults to 255 (0xFF). BRT = 0 disconnects all channels.

To use only the SMBus/I²C controlled PWM brightness control, users need to set Register 0x01 to 0x05.

The PWM dimming frequency is adjusted by a resistor at the FPWM pin.

Method 2 (External Mode)

The average LED channel current can also be controlled by an external PWM signal, as shown in Equation 8:

$$I_{LED(ave)} = I_{LED} \times PWMI \quad (EQ. 8)$$

The PWM dimming frequency can be set or applied up to 30kHz with duty cycles from 0.4% to 100%. The PWM dimming off time cannot be longer than 28ms or else the driver will enter shutdown.

To use externally applied PWM signal only for brightness control, users need to set Register 0x01 to 0x03.

Method 3 (DPST Mode)

The average LED channel current can also be controlled by the product of the SMBus/I²C controlled PWM and the external PWM signals as:

$$I_{LED(ave)} = I_{LED} \times PWM_{DPST} \quad (EQ. 9)$$

Where:

$$PWM_{DPST} = BRT / 255 \times PWMI \quad (EQ. 10)$$

Therefore:

$$I_{LED(ave)} = I_{LED} \times BRT / 255 \times PWMI \quad (EQ. 11)$$

Where BRT is the value held in Register 0x00 (default setting 0xFF) controlled by SMBus/I²C and PWM is the duty cycle of the incoming PWM signal. In this way, the users can change the PWM current in ratiometric manner to achieve DPST compliance backlight dimming.

To use the DPST mode, users need to set Register 0x01 to 0x01 with an external PWM signal.

The DPST mode PWM dimming frequency is adjusted by a resistor at the FPWM pin.

For example, if the SMBus/I²C controlled PWM duty is 80% dimming at 200Hz (see Equation 12) and the external PWM duty cycle is 60% dimming at 1kHz, the resultant PWM duty cycle is 48% dimming at 200Hz.

PWM Dimming Frequency Adjustment

The PWM dimming frequency is set by an external resistor at the FPWM pin as:

$$F_{PWM} = \frac{6.66 \times 10^7}{R_{FPWM}} \quad (EQ. 12)$$

where F_{PWM} is the desirable PWM dimming frequency and R_{FPWM} is the setting resistor.

The PWM dimming frequency can be set or applied up to 30kHz with duty cycle from 0.4% to 100%.

Direct PWM Dimming

When Direct PWM Dimming mode is selected where F_{PWM} is tied to V_{DC} and $SMBCLK/SMBDAT$ are grounded, 6 channels of PWM current will follow the incoming PWM signal's frequency and duty cycle. The change is analog fashion without any digitization that the minimum duty cycle can be as low as 0.007% at 200Hz (or equivalent pulse width of 350ns). To achieve this ultra low duty cycle dimming performance, any channel capacitor, either it is tied to V_{OUT} or ground, cannot be used. Also in Direct PWM Dimming mode the Phase Shift function will be disabled.

Phase Shift Control

The ISL97671A is capable of delaying the phase of each current source to minimize load transients. By default, phase shifting is disabled as shown in Figure 21 where the channels PWM currents are switching uniformly. The duty cycles can be controlled by the data in PWM Brightness Control Register via the SMBus/I²C interface, an external PWM signal with the frequency set by the R_{FPWM} , or by an external PWM signal with the frequency set by the incoming signal.

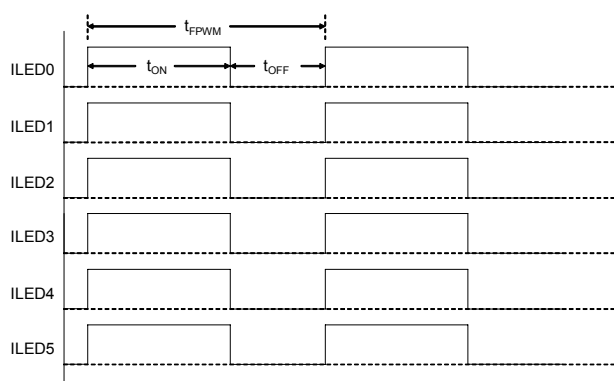


FIGURE 21. NO DELAY (DEFAULT PHASE SHIFT DISABLED)

When EqualPhase = 1, the phase shift evenly spreads the channels switching across the PWM cycle, depending on how many channels are enabled, as shown in Figures 22 and 23. Equal phase means there are fixed delays between channels and such delay can be calculated as Equations 13 and 14.

$$t_{D1} = \frac{t_{FPWM}}{255} \times \left(\frac{255}{N} \right) \quad (\text{EQ. 13})$$

$$t_{D2} = \frac{t_{FPWM}}{255} \times \left(255 - (N - 1) \left(\frac{255}{N} \right) \right) \quad (\text{EQ. 14})$$

where $(255/N)$ is rounded down to the nearest integer. For example, if $N = 6$, $(255/N) = 42$, that leads to:

$$t_{D1} = t_{FPWM} \times 42/255$$

$$t_{D2} = t_{FPWM} \times 45/255$$

where t_{FPWM} is the sum of t_{ON} and t_{OFF} . N is the number of LED channels. The ISL97671A will detect the numbers of operating channels automatically.

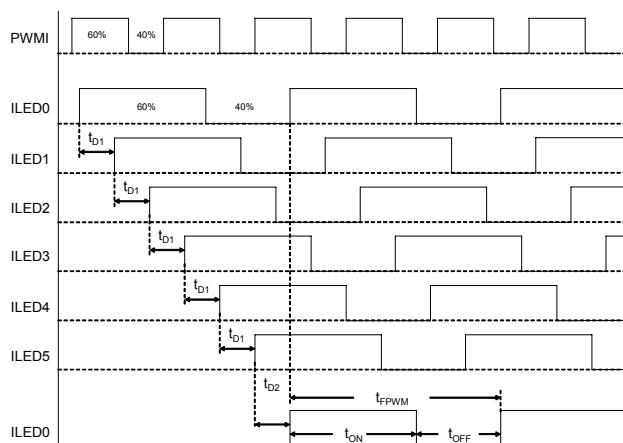
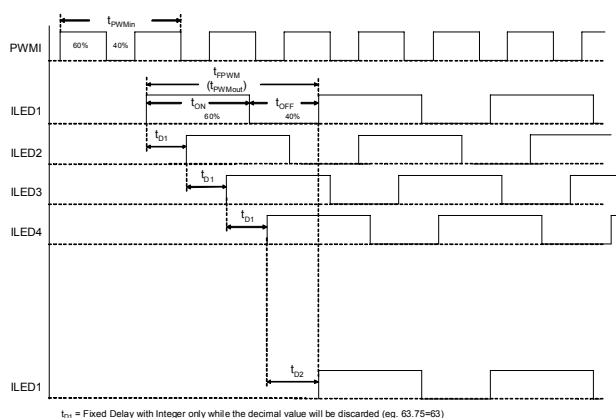


FIGURE 22. 6 EQUAL PHASE CHANNELS PHASE SHIFT ILLUSTRATION



t_{D1} = Fixed Delay with Integer only while the decimal value will be discarded (eg. 63.75=63)

FIGURE 23. 4 EQUAL PHASE CHANNELS PHASE SHIFT ILLUSTRATION

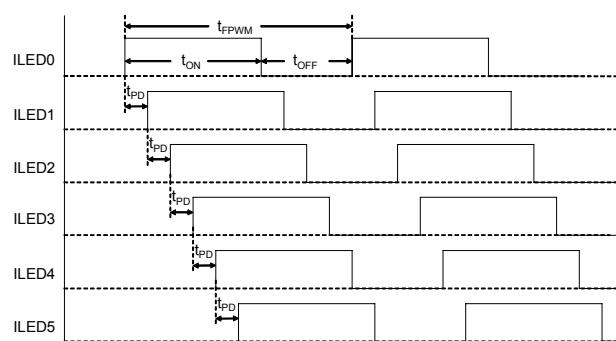


FIGURE 24. PHASE SHIFT WITH 7-BIT PROGRAMMABLE DELAY

The ISL97671A allows the user to program the amount of phase shift degree in 7-bit resolution, as shown in Figure 24. To enable programmable phase shifting, the user must write to the Phase Shift Control register with EqualPhase = 0 and the desirable phase shift value of PhaseShift[6:0]. The delay between CH5 and the repeated CH0 is the rest of the PWM cycle.

Switching Frequency

The default switching frequency is 600kHz but it can be selected to 600kHz or 1.2MHz if the SMBus/I²C communications is used. The switching frequency select bit is accessible in the SMBus/I²C Configuration Register 0x08 bit 2.

5V Low Dropout Regulator

A 5V LDO regulator is present at the VDC pin to develop the necessary low voltage supply, which is used by the chips internal control circuitry. Because VDC is an LDO pin, it requires a bypass capacitor of 1 μ F or more for the regulation. Low input voltage also allows only lower output voltage applications only with the maximum boost ratio defined in “Components Selections” on page 24. The VDC pin can be used as a coarse reference with a few mA sourcing capability.

Power-Up Sequencing, Soft-Start, and Fault Management

The ISL97671A includes circuits to manage input current draw during normal startup, to reduce inrush current as various bulk capacitors charge up. The ISL97671A also detects several external fault conditions, and acts to limit fault energy and prevent continued startup while detected faults exist. An external high-side PFET can optionally be fitted in series with VIN. The ISL97671A turns this fault protection PFET off in the event of a short fault to ground in the boost converter, avoiding damage to the system's main power supply in such an overload condition.

In-rush Control and Soft-start

The ISL97671A has separately built in independent in-rush control and soft-start functions. The in-rush control function is built around the short circuit protection FET, and is only available in applications, which include this device. At start-up, the fault protection FET is turned on slowly due to a 30 μ A pull-down current output from the FAULT pin. This discharges the fault FET's gate-source capacitance, turning on the FET in a controlled fashion. As this happens, the output capacitor is charged slowly through the weakly turned on FET before it becomes fully enhanced. This results in a low in-rush current. This current can be further reduced by adding a capacitor (in the 1nF to 5nF range) across the gate-source terminals of the FET.

Once the boost is enabled the current in the boost power switch is monitored and the switching is terminated in any cycle where the current exceeds the current limit. The ISL97671A includes a soft-start feature where this current limit starts at a low value (285mA). This is stepped up to the final 2.0A current limit in 7 further steps of 285mA. These steps will happen over at least 8ms, and will be extended at low LED PWM frequencies if the LED duty cycle is low. This allows the output capacitor to be charged to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

For systems with no master fault protection FET, the in-rush current will flow towards C_{OUT} when V_{IN} is applied and it is determined by the ramp rate of V_{IN} and the values of C_{OUT} and L.

Fault Protection and Monitoring

The ISL97671A features extensive protection functions to cover all the perceivable failure conditions. The failure mode of a LED can be either open circuit or as a short. The behavior of an open circuited LED can additionally take the form of either infinite resistance or, for some LEDs, a zener diode, which is integrated into the device in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes), an open circuit failure of an LED will only result in the loss of one channel

of LEDs without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels unless a similar fault is occurring. All LED faults are reported via the SMBus/I²C interface to Register 0x02 (Fault/Status register). The controller is able to determine which channels have failed via Register 0x09 (Output Masking register). The controller can also choose to use Register 0x09 to disable faulty channels at start-up, resulting in only further faulty channels being reported by Register 0x02.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97671A uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. See Table 2 on page 16 for more details.

A fault condition that results in an input current that exceeds the devices electrical limits will result in a shutdown of all output channels. The control device logic will remain functional such that the Fault/Status Register can be interrogated by the system. The root cause of the failure will be loaded to the volatile Fault/Status Register so that the host processor can interrogate the data for failure monitoring.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are detected above the programmed short circuit threshold. The short circuit threshold is 7.2V minimum. When an LED becomes shorted, the action taken is described in Table 2. The default short circuit threshold is 7.2V. The detection of this failure mode can be disabled via Register 0x08, see Table 3B for additional information.

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97671A monitors the current in each channel such that any string which reaches the intended output current is considered “good”. Should the current subsequently fall below the target, the channel will be considered an “open circuit”. Furthermore, should the boost output of the ISL97671A reaches the OVP limit or should the lower over-temperature threshold be reached, all channels which are not “good” will immediately be considered as “open circuit”. Detection of an “open circuit” channel will result in a time-out before disabling of the affected channel. This time-out is sped up when the device is above the lower over-temperature threshold in an attempt to prevent the upper over-temperature trip point from being reached.

Some users employ some special types of LEDs that have zener diode structure in parallel with the LED for ESD enhancement, thus enabling open circuit operation. When this type of LED goes open circuit, the effect is as if the LED forward voltage has increased, but no lighting. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, allowing all other LEDs in the string to remain functional. Care should be taken in this case that the boost OVP limit and SCP limit are set properly, so as to make sure that multiple failures on one string do not

cause all other good channels to be faulted out. This is due to the increased forward voltage of the faulty channel making all other channel look as if they have LED shorts. See Table 2 for details for responses to fault conditions.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the output voltage and keeps the voltage at a safe level. The OVP threshold is set as:

$$OVP = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad (EQ. 15)$$

These resistors should be large to minimize the power loss. For example, a $1M\Omega$ R_{UPPER} and $30k\Omega$ R_{LOWER} sets OVP to 41.2V. Large OVP resistors also allow C_{OUT} discharges slowly during the PWM Off time. Parallel capacitors should also be placed across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high value resistors.

Undervoltage Lock-out

If the input voltage falls below the UVLO level of 2.45V, the device will stop switching and be reset. Operation will restart only if the device is re-enabled through SMBus/I²C interface once the input voltage is back in the normal V_{IN} and operating range. In non-SMBus/I²C applications, the part will automatically restart once the input voltage clears the UVLO threshold with the part already enabled.

Input Overcurrent Protection

During normal switching operation, the current through the internal boost power FET is monitored. If the current exceeds the current limit, the internal switch will be turned off. This monitoring happens on a cycle by cycle basis in a self protecting way.

Additionally, the ISL97671A monitors the voltage at the LX and OVP pins. At start-up, a fixed current is injected out of the LX pins and into the output capacitor. The device will not start up unless the voltage at LX exceeds 1.2V. The OVP pin is also monitored such that if it rises above and subsequently falls below 20% of the target OVP level, the input protection FET will also be switched off.

Over-Temperature Protection (OTP)

The ISL97671A includes two over-temperature thresholds. The lower threshold is set to +130°C. When this threshold is reached, any channel which is outputting current at a level significantly below the regulation target will be treated as “open circuit” and disabled after a time-out period. This time-out period is also reduced to 800µs when it is above the lower threshold. The intention of the lower threshold is to allow bad channels to be isolated and disabled before they cause enough power dissipation (as a result of other channels having large voltages across them) to hit the upper temperature threshold.

The upper threshold is set to +150°C. Each time this is reached, the boost will stop switching and the output current sources will be switched off. Once the device has cooled to approximately +100°C, the device will restart with the DC LED current level reduced to 75% of the initial setting. If the dissipation problem persists, subsequent hitting of the limit will cause identical behavior, with the current reduced in steps to 50% and finally 25%. Hitting of the upper threshold will also set the thermal fault bit of the Fault/Status register 0x02. Unless disabled via the EN pin, the device stays in an active state throughout, allows the external processor to interrogate the fault condition.

For the extensive fault protection conditions, please refer to Figure 25 and Table 2 for details.

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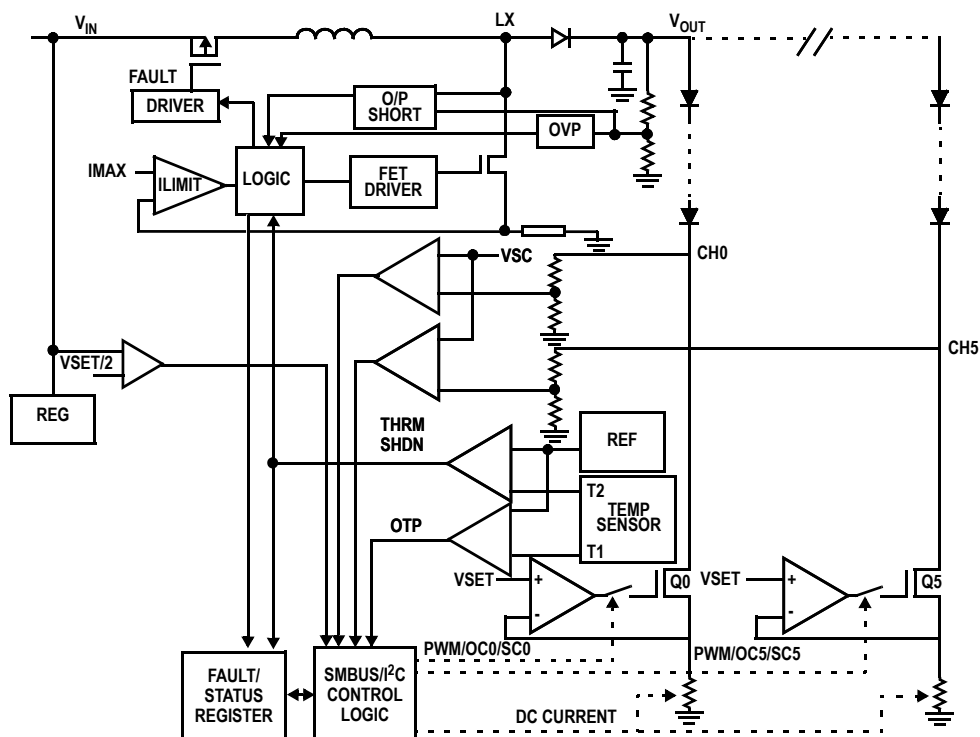


FIGURE 25. SIMPLIFIED FAULT PROTECTIONS

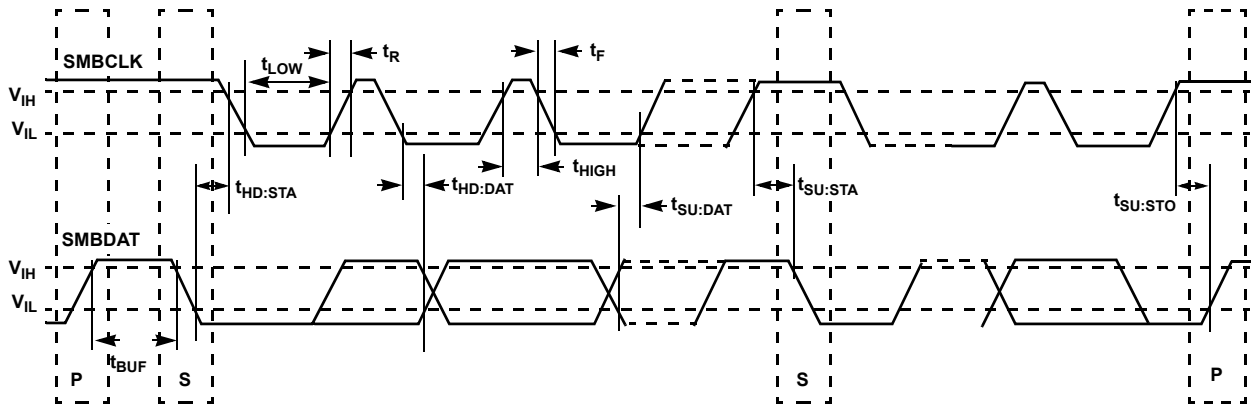
TABLE 2. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V _{OUT} REGULATED BY
1	CH0 Short Circuit	Upper Over-Temperature Protection limit (OTP) not triggered and CH0 < 7.5V	CH0 ON and burns power.	CH1 through CH5 Normal	Highest V _F of CH1 through CH5
2	CH0 Short Circuit	Upper OTP triggered but V _{CH0} < 7.5V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I _{OUT} further.	Same as CH0	Highest V _F of CH1 through CH5
3	CH0 Short Circuit	Upper OTP not triggered but CH0 > 7.5V	CH1 disabled after 6 PWM cycle time-out.	CH1 through CH5 Normal	Highest V _F of CH1 through CH5
4	CH0 Open Circuit with infinite resistance	Upper OTP not triggered and CH0 < 7.5V	V _{OUT} will ramp to OVP. CH1 will time-out after 6 PWM cycles and switch off. V _{OUT} will drop to normal level.	CH1 through CH5 Normal	Highest V _F of CH1 through CH5
5	CH0 LED Open Circuit but has paralleled Zener	Upper OTP not triggered and CH0 < 7.5V	CH1 remains ON and has highest V _F , thus V _{OUT} increases.	CH1 through CH5 ON, Q1 through Q5 burn power	V _F of CH0
6	CH0 LED Open Circuit but has paralleled Zener	Upper OTP triggered but CH0 < 7.5V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I _{OUT} further	Same as CH0	V _F of CH0
7	CH0 LED Open Circuit but has paralleled Zener	Upper OTP not triggered but CH _x > 7.5V	CH0 remains ON and has highest V _F , thus V _{OUT} increases.	V _{OUT} increases, then CH-X switches OFF after 6 PWM cycles. This is an unwanted shut off and can be prevented by setting OVP at an appropriate level.	V _F of CH0
8	Channel-to-Channel ΔV _F too high	Lower OTP triggered but CH _x < 7.5V	Any channel at below the target current will fault out after 6 PWM cycles. Remaining channels driven with normal current.		Highest V _F of CH0 through CH5

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TABLE 2. PROTECTIONS TABLE (Continued)

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V _{OUT} REGULATED BY
9	Channel-to-Channel ΔV_F too high	Upper OTP triggered but $CHx < 7.5V$	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I _{OUT} further		Highest V _F of CH0 through CH5
10	Output LED stack voltage too high	V _{OUT} > VOVP	Any channel that is below the target current will time-out after 6 PWM cycles, and V _{OUT} will return to the normal regulation voltage required for other channels.		Highest V _F of CH0 through CH5
11	V _{OUT} /LX shorted to GND at start-up or V _{OUT} shorted in operation	LX current and timing are monitored. OVP pins monitored for excursions below 20% of OVP threshold.	The chip is permanently shutdown 31mS after power-up if V _{OUT} /Lx is shorted to GND.		



NOTES:

SMBus/I²C Description

S = start condition

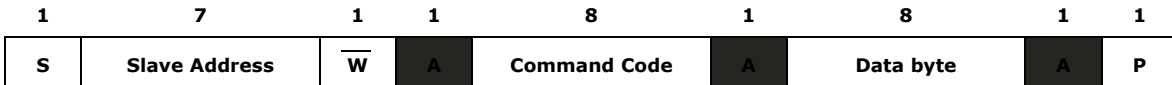
P = stop condition

A = acknowledge

\bar{A} = not acknowledge

R/ \bar{W} = read enable at high; write enable at low

FIGURE 26. SMBUS/I²C INTERFACE



Master to Slave

Slave to Master

FIGURE 27. WRITE BYTE PROTOCOL

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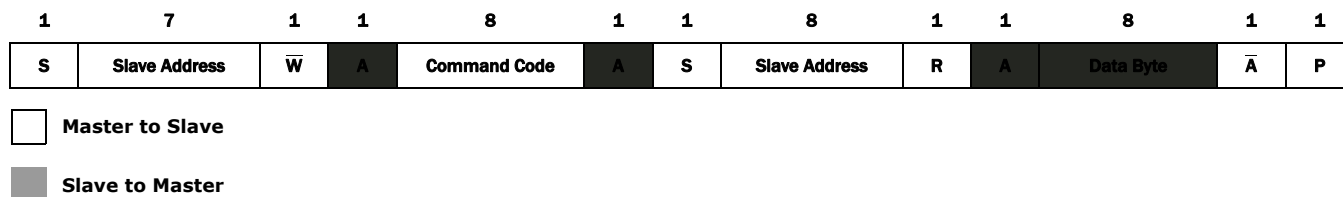


FIGURE 28. READ BYTE PROTOCOL

SMBus/I²C Communications

The ISL97671A can be controlled by SMBus/I²C for PWM or DC dimming. The LEDs driving is default to off and the users will need the SMBus/I²C interface to enable the driving and controlling of various parameters that will be described in this section. Please note that the ISL97671A can also be controlled by an external PWM signal for PWM dimming without any SMBus/I²C interface. To do so, the users need to pull the SMBCLK and SMBDAT pins to low or ground the pins permanently if SMBus/I²C control is not used. The switching frequency is fixed at 600kHz if SMBus/I²C is not used.

Write Byte

The Write Byte protocol is only three bytes long. The first byte starts with the slave address followed by the “command code,” which translates to the “register index” being written. The third byte contains the data byte that must be written into the register selected by the “command code.” A shaded label is used on cycles during which the slaved backlight controller “owns” or “drives” the Data line. All other cycles are driven by the “host master.”

Read Byte

Figure 28 shows the four byte long Read Byte protocol starts out with the slave address followed by the “command code” which translates to the “register index.” Subsequently, the bus direction turns around with the re-broadcast of the slave address with bit 0 indicating a read (“R”) cycle. The fourth byte contains the data being returned by the backlight controller. That byte value in the data byte reflects the value of the register being queried at the “command code” index. Note the bus directions, which are highlighted by the shaded label that is used on cycles during which the slaved backlight controller “owns” or “drives” the Data line. All other cycles are driven by the “host master.”

Slave Device Address

The slave address contains 7 MSB plus one LSB as R/W bit, but these 8 bits are usually called Slave Address bytes. Figure 29 shows the high nibble of the Slave Address byte is 0x5 or 0101b to denote the “backlight controller class.” Bit 3 in the lower nibble of the Slave Address byte is 1. Bit 0 is always the R/W bit, as specified by the SMBus/I²C protocol. Note: In this document, the device address will always be expressed as a full 8-bit address instead of the shorter 7-bit address typically used in other backlight controller specifications to avoid confusion. Therefore, if the device is in the write mode where bit 0 is 0, the slave address byte is 0x58 or 01011000b. If the device is in the read mode where bit 0 is 1, the slave address byte is 0x59 or 01011001b.

The backlight controller may sense the state of the pins at POR or during normal operation - the pins will not change state while the device is in operation.

SMBus/I²C Register Definitions

The backlight controller registers are Byte wide and accessible via the SMBus/I²C Read/Write Byte protocols. Their bit assignments are provided in the following sections with reserved bits containing a default value of “0”.

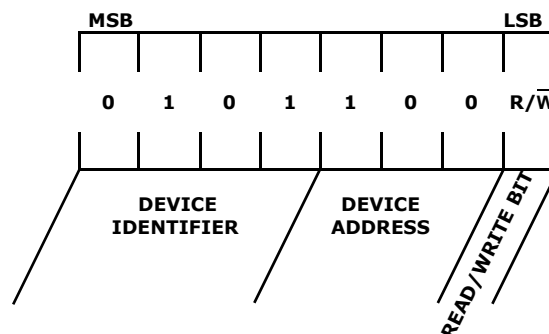


FIGURE 29. SLAVE ADDRESS BYTE DEFINITION

TABLE 3A. ISL97671A REGISTER LISTING

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT VALUE	SMBUS/I ² C PROTOCOL
0x00	PWM Brightness Control Register	BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0	0xFF	Read and Write
0x01	Device Control Register	Reserved	Reserved	Reserved	Reserved	Reserved	PWM_MD	PWM_SEL	BL_CTL	0x00	Read and Write
0x02	Fault/Status Register	Reserved	Reserved	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	FAULT	0x00	Read Only

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TABLE 3A. ISL97671A REGISTER LISTING (Continued)

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT VALUE	SMBUS/I ² C PROTOCOL
0x03	Identification Register	LED PANEL	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0	0xC8	Read Only
0x07	DC Brightness Control Register	BRTDC7	BRTDC6	BRTDC5	BRTDC4	BRTDC3	BRTDC2	BRTDC1	BRTDC0	0xFF	Read and Write
0x08	Configuration Register	Reserved	DirectPWM	0	1	1	FSW	Reserved	VSC	0x1F	Read and Write
0x09	Output Channel Register	Reserved	Reserved	CH5	CH4	CH3	CH2	CH1	CH0	0x3F	Read and Write
0x0A	Phase Shift Deg	Equal Phase	Phase Shift6	Phase Shift5	Phase Shift4	Phase Shift3	Phase Shift2	Phase Shift1	Phase Shift0	0x00	Read and Write

TABLE 3B. DATA BIT DESCRIPTIONS

ADDRESS	REGISTER	DATA BIT DESCRIPTIONS
0x00	PWM Brightness Control Register	BRT[7..0] = 256 steps of DPWM duty cycle brightness control
0x01	Device Control Register	PWM_MD = PWM mode select bit (1 = absolute brightness, 0 = % change), default = 0 PWM_SEL = Brightness control select bit (1 = control by PWMI, 0 = control by SMBus/I ² C), default = 0 BL_CTL = BL On/Off (1 = On, 0 = Off), default = 0
0x02	Fault/Status Register	2_CH_SD = Two LED output channels are shutdown (1 = shutdown, 0 = OK) 1_CH_SD = One LED output channel is shutdown (1 = shutdown, 0 = OK) BL_STAT = BL status (1 = BL On, 0 = BL Off) OV_CURR = Input overcurrent (1 = Overcurrent condition, 0 = Current OK) THRM_SHDN = Thermal Shutdown (1 = Thermal fault, 0 = Thermal OK) FAULT = Fault occurred (Logic "OR" of all of the fault conditions)
0x03	Identification Register	MFG[3..0] = Manufacturer ID (16 vendors available. Intersil is vendor ID 9) REV[2..0] = Silicon rev (Rev 0 through Rev 7 allowed for silicon spins)
0x07	DC Brightness Control Register	BRTDC[7..0] = 256 steps of DC brightness control
0x08	Configuration Register	DirectPWM = Forces the PWM input signal to directly control the current sources. Bits 3, 4, and 5 should be 1, 1, 0 FSW = Switching frequencies selection, FSW = 0 = 1.2MHz. FSW = 1 = 600kHz VSC[0] = Short circuit thresholds selection, 0 = disabled, 1 = 7.2V minimum
0x09	Output Channel Mask/Fault Readout Register	CH[5..0] = Output Channel Read and Write. In Write, 1 = Channel Enabled, 0 = Channel Disabled. In Read, 1 = Channel OK, 0 = Channel Not OK/Channel disabled
0x0A	Phase Shift Degree	EqualPhase = Controls phase shift mode - When 1, phase shift is 360/N (where N is the number of channels enabled). When 0, phase shift is defined by PhaseShift<6:0>. PS[6..0] = 7-bit Phase shift setting - phase shift between each channel is PhaseShift<6:0>/(255*PWMFreq). In direct PWM modes, phase shift between each channel is PhaseShift<6:0>/12.8MHz.

PWM Brightness Control Register (0x00)

The Brightness control resolution has 256 steps of PWM duty cycle adjustment. Figure 30 shows the bit assignment. All of the bits in this Brightness Control Register can be read or write. Step 0 corresponds to the minimum step where the current is less than 10µA. Steps 1 to 255 represent the linear steps between 0.39% and 100% duty cycle with approximately 0.39% duty cycle adjustment per step.

- An SMBus/I²C Write Byte cycle to Register 0x00 sets the PWM brightness level only if the backlight controller is in SMBus/I²C mode (see Table 4) Operating Modes selected by Device Control Register Bits 1 and 2).

- An SMBus/I²C Read Byte cycle to Register 0x00 returns the programmed PWM brightness level.
- An SMBus/I²C setting of 0xFF for Register 0x00 sets the backlight controller to the maximum brightness.
- An SMBus/I²C setting of 0x00 for Register 0x00 sets the backlight controller to the minimum brightness output.
- Default value for Register 0x00 is 0xFF.

REGISTER 0x00	PWM BRIGHTNESS CONTROL REGISTER
----------------------	--

BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
BRT[7..0]	= 256 steps of PWM brightness levels

FIGURE 30. DESCRIPTIONS OF BRIGHTNESS CONTROL REGISTER

REGISTER 0x01	DEVICE CONTROL REGISTER
----------------------	--------------------------------

RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWM_MD	PWM_SEL	BL_CTL
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

PWM_MD	PWM_SEL	BL_CTL	MODE
X	X	0	Backlight Off
0	0	1	SMBus/I ² C and PWM dimming (DPST)
0	1	1	PWMI controlled PWM dimming
1	0	1	SMBus/I ² C controlled PWM dimming
1	1	1	SMBus/I ² C controlled PWM dimming

FIGURE 31. DESCRIPTIONS OF DEVICE CONTROL REGISTER

Device Control Register (0x01)

This register has two bits that control either SMBus/I²C controlled or external PWM controlled PWM dimming and a single bit that controls the BL ON/OFF state. The remaining bits are reserved. The bit assignment is shown in Figure 31. All other bits in the Device Control Register will read as low unless otherwise written.

- All reserved bits have no functional effect when written.
- All defined control bits return their current, latched value when read.

A value of 1 written to BL_CTL turns on the BL in 4ms or less after the write cycle completes. The BL is

- deemed to be on when Bit 3 BL_STAT of Register 0x02 is 1 and Register 0x09 is not 0.
- A value of 0 written to BL_CTL immediately turns off the BL. The BL is deemed to be off when Bit 3 BL_STAT of Register 0x02 is 0 and Register 0x09 is 0.
- When SMBus/I²C mode with DPST is selected, Register 0x00 reflects the last value written to it from SMBus/I²C.

The default value for Register 0x01 is 0x00.

TABLE 4. OPERATING MODES SELECTED BY DEVICE CONTROL REGISTER BITS 1 AND 2

PWM_MD	PWM_SEL	MODE
X	1	PWM Mode
1	0	SMBus/I ² C Mode
0	0	SMBus/I ² C and PWM Mode with DPST

The PWM_SEL bit determines whether the SMBus/I²C or PWM input should drive the output brightness in terms of PWM dimming. When PWM_SEL bit is 1, the PWM drives the output brightness regardless of what the PWM_MD is.

When the PWM_SEL bit is 0, the PWM_MD bit selects the manner in which the PWM dimming is to be interpreted; when this bit is 1, the PWM dimming is based on the SMBus/I²C brightness setting. When this bit is 0, the PWM dimming reflects a percentage change in the current brightness programmed in the SMBus/I²C Register 0x00, i.e. DPST (Display Power Saving Technology) mode as:

$$\text{DSPT Brightness} = \text{Cbt} \times \text{PWM} \quad (\text{EQ. 16})$$

Where:

Cbt = Current brightness setting from SMBus/I²C Register 0x00 without influence from the PWM

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PWM = is the percent duty cycle of the PWM

For example, the Cbt = 50% duty cycle programmed in the SMBus/I²C Register 0x00 and the PWM frequency is tuned to be 200Hz with an appropriate capacitor at the FPWM pin. On the other hand, PWM is fed with a 1kHz 30% high PWM signal. When PWM_SEL = 0 and PWM_MD = 0, the device is in DPST operation where DPST brightness = 15% PWM dimming at 200Hz.

Fault/Status Register (0x02)

This register has 6 status bits that allow monitoring of the backlight controller's operating state. Bit 0 is a logical "OR" of all fault codes to simplify error detection. Not all of the bits in this register are fault related (Bit 3 is a simple BL status indicator). The remaining bits are reserved and return a "0" when read and ignore the bit value when written. All of the bits in this register are read-only, with the

exception of bit 0, which can be cleared by writing to it.

- A Read Byte cycle to Register 0x02 indicates the current BL on/off status in BL_STAT (1 if the BL is on, 0 if the BL is off).
- A Read Byte cycles to Register 0x2 also returns FAULT as the logical OR of THRM_SHDN, OV_CURR, 2_CH_SD, and 1_CH_SD should these events occur.
- 1_CH_SD returns a 1 if one or more channels have faulted out.
- 2_CH_SD returns a 1 if two or more channels have faulted out.
- A fault will not be reported in the event that the BL is commanded on and then immediately off by the system.
- When FAULT is set to 1, it will remain at 1 even if the signal which sets it goes away. FAULT will be cleared when the

REGISTER 0x02	FAULT/STATUS REGISTER
---------------	-----------------------

RESERVED	RESERVED	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	FAULT
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT	BIT ASSIGNMENT	BIT FIELD DEFINITIONS
Bit 5	2_CH_SD	= Two LED output channels are shutdown (1 = shutdown, 0 = OK)
Bit 4	1_CH_SD	= One LED output channel is shutdown (1 = shutdown, 0 = OK)
Bit 3	BL_STAT	= BL Status (1 = BL On, 0 = BL Off)
Bit 2	OV_CURR	= Input Overcurrent (1 = Overcurrent condition, 0 = Current OK)
Bit 1	THRM_SHDN	= Thermal Shutdown (1 = Thermal Fault, 0 = Thermal OK)
Bit 0	FAULT	= Fault occurred (Logic "OR" of all of the fault conditions)

FIGURE 32. DESCRIPTIONS OF FAULT/STATUS REGISTER

REGISTER 0x03	ID REGISTER
---------------	-------------

LED PANEL	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0
Bit 7 = 1	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
MFG[3..0]	= Manufacturer ID. See "Identification Register (0x03)" on page 21. data 0 to 8 in decimal correspond to other vendors data 9 in decimal represents Intersil ID data 10 to 14 in decimal are reserved data 15 in decimal Manufacturer ID is not implemented
REV[2..0]	= Silicon rev (Rev 0 through Rev 7 allowed for silicon spins)

FIGURE 33. DESCRIPTIONS OF ID REGISTER

REGISTER 0x07		DC BRIGHTNESS CONTROL REGISTER					
BRTDC7	BRTDC6	BRTDC5	BRTDC4	BRTDC3	BRTDC2	BRTDC1	BRTDC0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)
BIT ASSIGNMENT		BIT FIELD DEFINITIONS					
BRTDC[7..0]		= 256 steps of DC brightness levels					

FIGURE 34. DESCRIPTIONS OF DC BRIGHTNESS CONTROL REGISTER

DC Brightness Control Register (0x07)

The DC Brightness Control Register 0x07 allows users to have additional dimming flexibility by:

1. Effectively achieving 16-bits of dimming control when DC dimming is combined with PWM dimming
2. Achieving visual or audio noise free 8-bit DC dimming over potentially noisy PWM dimming.

The bit assignment is shown in Figure 34. All of the bits in this Register can be read or write. Steps 0 to 255 represent the linear steps of current adjustment in DC on-the-fly. It can also be considered as the peak current factory calibration feature to account for various LED production batch variations, but external EEPROM settings storing and restoring are required.

- An SMBus/I²C Write Byte cycle to Register 0x07 sets the brightness level in DC only.
- An SMBus/I²C Read Byte cycle to Register 0x07 returns the current DC brightness level.
- Default value for Register 0x07 is 0xFF.

Configuration Register (0x08)

The Configuration Register provides many extra functions that users can explore in order to optimize the driver performance at a given application.

A DirectPWM bit allows Direct PWM where the output current follows the same input PWM signal. The FSW bit allows users to set the boost conversion switching frequency between 1.2MHz and 600kHz. The VSC bits allow users to set LED string short circuit threshold Vsc to 7.2V or disable it.

The bit assignment is shown in Figure 35. The default value for Register 0x08 is 0x1F.

Output Channel Mask/Fault Readout Register (0x09)

This register can be read or write; the bit position corresponds to the channel. For example, Bit 0 corresponds to Ch0 and bit 5 corresponds to Ch5 and so on. Writing data to this register, it enables the channels of interest. When reading data from this register, any disabled channel and any faulted out channel will read as 0. This allows the user to determine which channel is

faulty and optionally not enabling it in order to allow the rest of the system to continue to function. Additionally, a faulted out channel can be disabled and re-enabled in order to allow a retry for any faulty channel without having to power-down the other channels.

The bit assignment is shown in Figure 36. The default for Register 0x09 is 0x3F.

REGISTER 0x08	CONFIGURATION REGISTER
----------------------	-------------------------------

RESERVED	RESERVED	BIT5	BIT4	BIT3	FSW	RESERVED	VSC
Bit 7 (R/W)	Bit 6 (R/W)	0 (W)	1(W)	1(W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
DirectPWM	Forces the PWM signal to directly control the current sources. Note that there is some synchronous delay between PWM and current sources.
BITS[5-3]	These bits should always be written as 011.
FSW	2 levels of Switching Frequencies (1 = 1,200kHz, 0 = 600kHz)
VSC[0]	2 levels of Short-Circuit Thresholds (0 = disabled, 1 = 7.5V minimum)

FIGURE 35. DESCRIPTIONS OF CONFIGURATION REGISTER

REGISTER 0x09	OUTPUT CHANNEL REGISTER
----------------------	--------------------------------

RESERVED	RESERVED	CH5	CH4	CH3	CH2	CH1	CH0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
CH[5..0]	CH5 = Channel 5, CH4 = Channel 4 and so on

FIGURE 36. OUTPUT CHANNEL REGISTER

REGISTER 0x0A		PHASE SHIFT CONTROL REGISTER					
EQUALPHASE	PHASESHIFT6	PHASESHIFT5	PHASESHIFT4	PHASESHIFT3	PHASESHIFT2	PHASESHIFT1	PHASESHIFT0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
EqualPhase	Controls phase shift mode - When 0, phase shift is defined by PhaseShift<6:0>. When 1, phase shift is 360/N (where N is the number of channels enabled).
PhaseShift[6..0]	7-bit Phase shift setting - phase shift between each channel is PhaseShift<6:0>/((255*PWMFreq) In direct PWM modes, phase shift between each channel is PhaseShift<6:0>/12.8MHz

FIGURE 37. DESCRIPTIONS OF PHASE SHIFT CONTROL REGISTER

Phase Shift Control Register (0x0A)

The Phase Shift Control register is used to set phase delay between each channels. When bit 7 is set high, the phase delay is set by the number of channels enabled and the PWM frequency. Refer to Figures 3 and 4, the delay time is defined by Equation 17:

$$t_{D1} = (t_{FPWM}/N) \quad (\text{EQ. 17})$$

where N is the number of channels enabled, and t_{FPWM} is the period of the PWM cycle. When bit 7 is set low, the phase delay is set by bits 6 to 0 and the PWM frequency. Referencing Figure 24, the programmable delay time is defined by Equation 18:

$$t_{PD} = (PS < 6, 0 > \times t_{FPWM} / (255)) \quad (\text{EQ. 18})$$

where PS is an integer from 0 to 127, and t_{FPWM} is the period of the PWM cycle. By default, all the register bits are set low, which sets zero delay between each channel. Note that the user should not program the register to give more than one period of the PWM cycle delay between the first and last enabled channels.

Components Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On time is equal to the change of inductor current during the switching regulator Off time. Since the voltage across an inductor is:

$$V_L = L \times \Delta I_L / \Delta t \quad (\text{EQ. 19})$$

and ΔI_L at On = ΔI_L at Off, therefore:

$$(V_1 - 0) / L \times D \times t_S = (V_0 - V_D - V_1) / L \times (1 - D) \times t_S \quad (\text{EQ. 20})$$

where D is the switching duty cycle defined by the turn-on time over the switching period. V_D is Schottky diode forward voltage that can be neglected for approximation.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle respectively as:

$$V_0 / V_1 = 1 / (1 - D) \quad (\text{EQ. 21})$$

$$D = (V_0 - V_1) / V_0 \quad (\text{EQ. 22})$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, thereby improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

In Boost mode, input current flows continuously into the inductor; AC ripple component is only proportional to the rate of the inductor charging, thus, smaller value input capacitors may be used. It is recommended that an input capacitor of at least 10 μ F be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

Inductor

The selection of the inductor should be based on its maximum current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance and stability.

The inductor's maximum current capability must be adequate enough to handle the peak current at the worst case condition. If an inductor core is chosen with too low a current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the Off period, as expressed in Equation 23:

$$I_{Lpk} = (V_O \times I_O) / (85\% \times V_I) + 1/2 [V_I \times (V_O - V_I) / (L \times V_O \times f_{SW})] \quad (\text{EQ. 23})$$

The choice of 85% is just an average term for the efficiency approximation. The first term is the average current, which is inversely proportional to the input voltage. The second term is the inductor current change, which is inversely proportional to L and f_{SW} . As a result, for a given switching frequency and minimum input voltage on which the system operates, the inductor I_{SAT} must be chosen carefully. At a given inductor size, usually the larger the inductance, the higher the series resistance because of the extra winding of the coil. Thus, the higher the inductance, the lower the peak current capability. The ISL97671A current limit should also have to be taken into account.

Output Capacitors

The output capacitor acts to smooth the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of the discharge of the output capacitor for I_{LPEAK} during FET On and the voltage drop due to flowing through the ESR of the output capacitor. The ripple voltage can be shown as:

$$\Delta V_{CO} = (I_O / C_O \times D / f_S) + (I_O \times \text{ESR}) \quad (\text{EQ. 24})$$

The conservation of charge principle in Equation 24 also brings up the fact that during the boost switch Off period, the output capacitor is charged with the inductor ripple current minus a relatively small output current in boost topology. As a result, the user needs to select an output capacitor with low ESR and enough input ripple current capability.

Output Ripple

ΔV_{CO} can be reduced by increasing C_O or f_{SW} , or using small ESR capacitors. In general, Ceramic capacitors are the best choice for output capacitors in small to medium sized LCD backlight applications due to their cost, form factor, and low ESR.

A larger output capacitor will also ease the driver response during PWM dimming Off period due to the longer sample and hold effect of the output drooping. The driver does not need to boost harder in the next On period that minimizes transient current. The output capacitor is also needed for compensation, and, in general $2 \times 4.7 \mu\text{F} / 50\text{V}$ ceramic capacitors are suitable for notebook display backlight applications.

Schottky Diode

A high speed rectifier diode is necessary to prevent excessive voltage overshoot, especially in the boost configuration. Low forward voltage and reverse leakage current will minimize losses, making Schottky diodes the preferred choice. Although the Schottky diode turns on only during the boost switch Off period, it carries the same peak current as the inductor, and therefore, a suitable current rated Schottky diode must be used.

Applications

High Current Applications

Each channel of the ISL97671A can support up to 50mA. For applications that need higher current, multiple channels can be grouped to achieve the desirable current. For example, the cathode of the last LED can be connected to CH0 to CH2, this configuration can be treated as a single string with 150mA current driving capability.

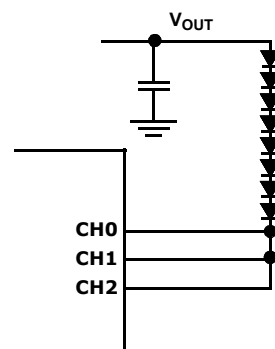


FIGURE 38. GANGING MULTIPLE CHANNELS FOR HIGH CURRENT APPLICATIONS

Multiple Drivers Operation

For large LCD panels where more than 6 channels of LEDs are needed, multiple ISL97671As with each driver having its own supporting components can be controlled together with the common SMBus/I²C. While the ISL97671A does not have extra pins strappable slave address feature, but a separate EN signal can be applied to each driver for asynchronous operation. A trade-off of such scheme is that an exact faulty channel cannot be identified since both controllers have the same I²C slave address.

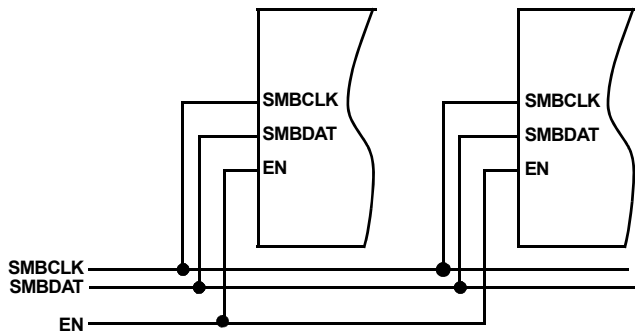


FIGURE 39. MULTIPLE DRIVERS OPERATION

Low Voltage Operations

The ISL97671A VIN pin can be separately biased from the LEDs power input to allow low voltage operation. For systems that have only single supply, V_{OUT} can be tied to the driver VIN pin to allow initial start-up, (see Figure 40). The circuit works as follows; when the input voltage is available and the device is not enable, the V_{OUT} follows V_{IN} with a Schottky diode voltage drop. The V_{OUT} bootstrapped to VIN pin allows an initial startup once the part is enable. Once the driver starts up with V_{OUT} regulating to the target, the VIN pin voltage also increases. As long as the V_{OUT} does not exceed 26.5V and the extra power loss on V_{IN} is acceptable, this configuration can be used for input voltage as low as 3.0V. The Fault Protection FET feature cannot be used in this configuration.

For systems that have dual supplies, VIN pin can be biased from 5V to 12V while input voltage can be as low as 2.7V, (see Figure 41). In this configuration V_{BIAS} is greater than or equal to V_{IN} for using the fault FET.

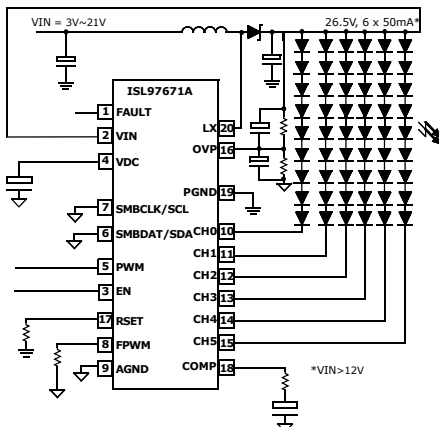


FIGURE 40. SINGLE SUPPLY 3V OPERATION

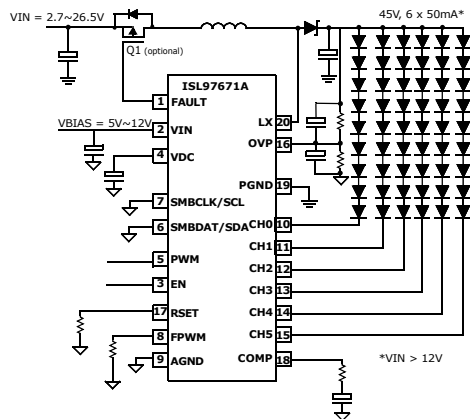


FIGURE 41. DUAL SUPPLIES 2.7V OPERATION

16-Bit Dimming

The SMBus/I²C controlled PWM and DC dimmings can be combined to effectively provide 16 bits of dimming capability, which can be valuable for automotive and avionics display applications.

RGB LEDs or Field Sequential LED Backlighting

The ISL97671A allows users to select the six channels of PWM dimming currents in any sequences and combinations that RGB LEDs or Field Sequential backlighting applications can be considered. On the other hand, the channel currents cannot be dimmed independently at the same time.

For example, an RGB LEDs application requires channels 0 and 1 for the red LEDs at 40mA peak with 25% dimming, channels 2 and 3 for green LEDs at 20mA peak with 50% dimming, and channels 4 and 5 for blue LEDs at 10mA peak with 100% dimming.

First the I_{LED} is set at 40mA with an appropriate R_{SET} , then the SMBus/I²C programming sequences are shown in the followings:

Register0x01 data 0x05 “turn BL on and select SMBus dimming”

Register0x09 data 0x03 “select ch 0 and 1”

Register0x07 data 0xFF “set 100% of 40mA in DC”

Register0x00 data 0x40 “apply 25% PWM dimming”

Register0x09 data 0x0C “select ch 2 and 3”

Register0x07 data 0x80 “set 50% of 40mA in DC”

Register0x00 data 0x80 “apply 50% PWM dimming”

Register0x09 data 0x30 “select ch 4 and 5”

Register0x07 data 0xFF “set 100% of 40mA in DC”

Register0x00 data 0xFF “apply 100% PWM dimming”

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Compensation

The ISL97671A has two main elements in the system; the Current Mode Boost Regulator and the op amp based multi-channel current sources. The ISL97671A incorporates a transconductance amplifier in its feedback path to allow the user some levels of adjustment on the transient response and better regulation. The ISL97671A uses current mode control architecture, which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation. The slow voltage loop must be

compensated for stable operation. The compensation network is a series Rc, Cc1 network from COMP pin to ground and an optional Cc2 capacitor connected to the COMP pin. The Rc sets the high frequency integrator gain for fast transient response and the Cc1 sets the integrator zero to ensure loop stability. For most applications, Rc is in the range of 15kΩ and Cc1 is in the range of 2.2nF. Depends on the PCB layout, a Cc2, in range of 47pF, may be needed to create a pole to cancel the output capacitor ESR's zero effect for stability.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
3/24/11	FN7709.1	Initial Release to web.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: [ISL97671A](http://www.intersil.com/products)

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: <http://rel.intersil.com/reports/search.php>

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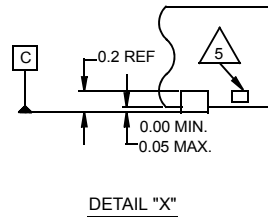
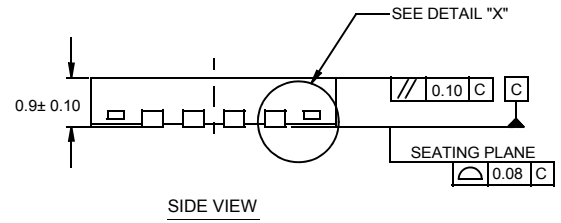
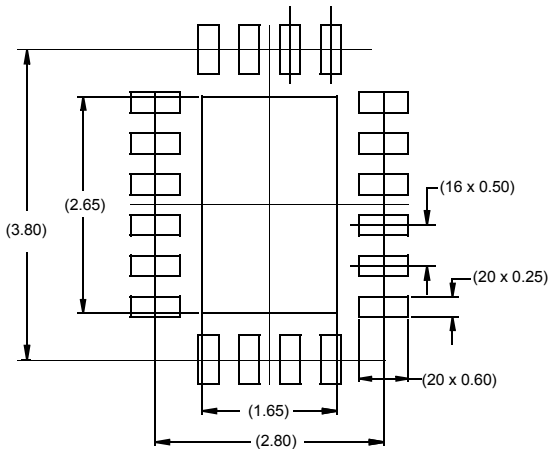
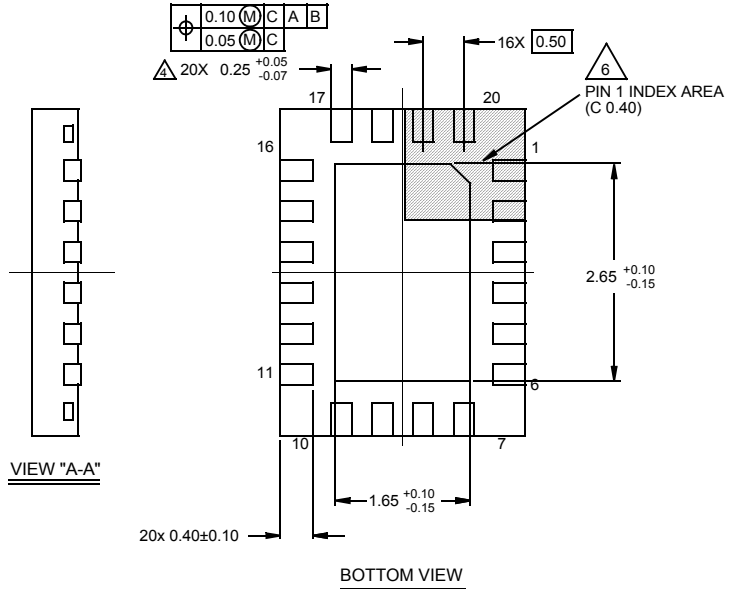
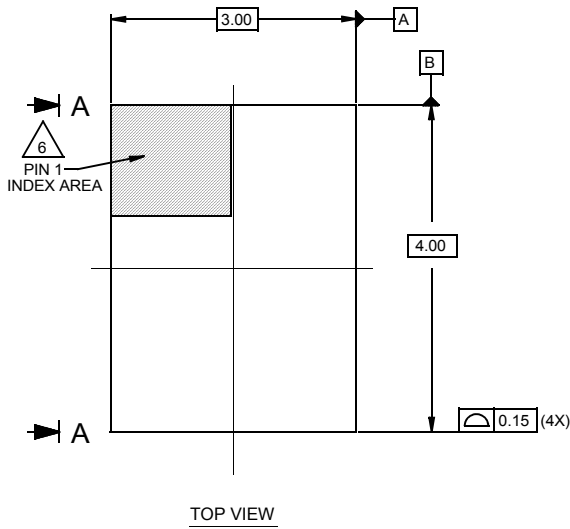
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Package Outline Drawing

L20.3x4

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 1, 3/10



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.