



NuMicro M051™ Series M052/M054 Product Brief

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1 DESCRIPTION

The NuMicro M051™ series are 32-bit microcontrollers with embedded ARM® Cortex™-M0 core for industrial control and applications which need rich communication interfaces. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller. The NuMicro M051™ series provide various options of products. M052/M054 is one of excellent products in NuMicro M051™ series.

M052/M054 can run up to 50MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. M052/M054 has 8K/16K-byte embedded flash, 4K-byte data flash, 4K-byte flash for the ISP, and 4K-byte embedded SRAM.

Many system level peripheral functions, such as I/O Ports, RAM, Timers, UART, SPI, I2C, PWM, ADC, Watchdog Timer and Brownout Detector, have been incorporated into M052/M054 in order to reduce component count, board space and system cost. These useful functions make M052/M054 powerful for a wide range of applications.

Additionally, M052/M054 is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
 - ARM® Cortex™ -M0 core runs up to 50 MHz.
 - One 24-bit system timer.
 - Supports low power sleep-mode.
 - Single-cycle 32-bit hardware multiplier.
 - NVIC for the 32 interrupt inputs, each with 4-levels of priority.
 - Serial Wire Debug (SWD) supports with 2 watchpoints/4 breakpoints.
- Memory
 - 8KB/16KB Flash memory for program memory (APROM)
 - 4KB Flash memory for data memory (DataFlash)
 - 4KB Flash memory for loader (LDRAM)
 - 4KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
 - Programmable system clock source
 - 22.1184MHz internal oscillator (trimmed to 1% accuracy)
 - 10kHz low-power oscillator for Watchdog Timer and wake-up in sleep mode
 - PLL allows CPU operation up to the maximum CPU rate
- I/O Port
 - Up to 40 general-purpose I/O (GPIO) pins for LQFP-48 package
 - Software-configured I/O type
 - ◆ Quasi-bidirectional input/output
 - ◆ Push-pull output
 - ◆ Open-drain output
 - ◆ Input-only
 - Optional Schmitt trigger input
- Timer
 - Four sets of 32-bit Timers
- Watchdog Timer
 - Programmable clock source and timeout period
 - Support wake-up function in power-down mode and power-sleep mode
 - Interrupt or reset selectable when timeout happens
- PWM
 - Built-in up to four 16-bit PWM generators provide eight PWM outputs or four complementary paired PWM outputs

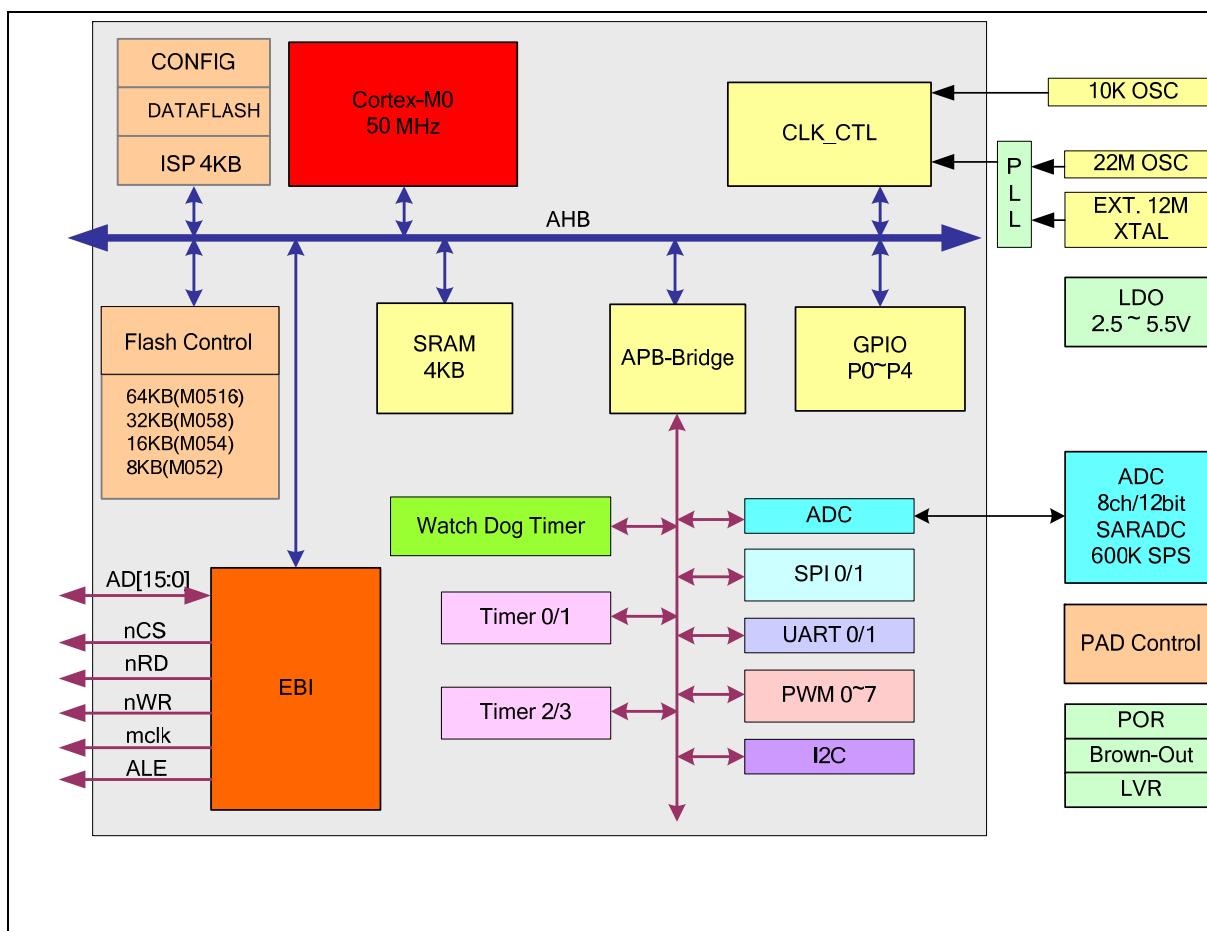


- Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
- PWM interrupt synchronized to PWM period
- 16-bit digital Capture timers (shared with PWM timers) with rising/falling capture inputs
- Support Capture interrupt
- UART
 - Up to two sets UART device.
 - Buffered receiver and transmitter, each with 15 bytes FIFO
 - Optional flow control function (CTS and RTS)
 - Support IrDA(SIR) function
 - Programmable baud-rate generator up to 1/16 system clock
 - Support RS485 function
- SPI
 - Up to two sets SPI device.
 - Master up to 16MHz, and Slave up to 10MHz
 - Support SPI master/slave mode
 - Full duplex synchronous serial data transfer
 - Variable length of transfer data from 1 to 32 bits
 - MSB or LSB first data transfer
 - Rx and Tx on both rising or falling edge of serial clock independently
 - Byte suspend mode in 32-bit transmission
- I2C
 - Master/Slave up to 1Mbit/s (Fast-mode Plus)
 - Bidirectional data transfer between masters and slaves
 - Multi-master bus (no central master).
 - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
 - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
 - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
 - Programmable clocks allow versatile rate control.
 - Support multiple address recognition (two slave address with mask option)

- ADC
 - 12-bit SAR ADC with 600k SPS
 - Up to 8-ch single-end input or 4-ch differential input
 - Single mode/burst mode/single cycle scan mode/continuous scan mode
 - Each channel with individual result register
 - Scan on enabled channels
 - Threshold voltage detection
 - Conversion started by S/W or external pin
- EBI (External Bus Interface) for external memory-mapped device access
- In-System Programming (ISP) & In-Circuit Programming (ICP)
- Brownout Detector
 - Programmable threshold levels: 4.5V/3.8V/2.7V/2.2V
 - Optional brownout interrupt or reset
- Built-in LDO for Wide Operating Voltage Range: 2.5V to 5.5V
- LVR (Low Voltage Reset)
- Operating Temperature: -40°C~85°C
- Packages:
 - Green package (RoHS)
 - 48-pin LQFP, 33-pin QFN

3 BLOCK DIAGRAM

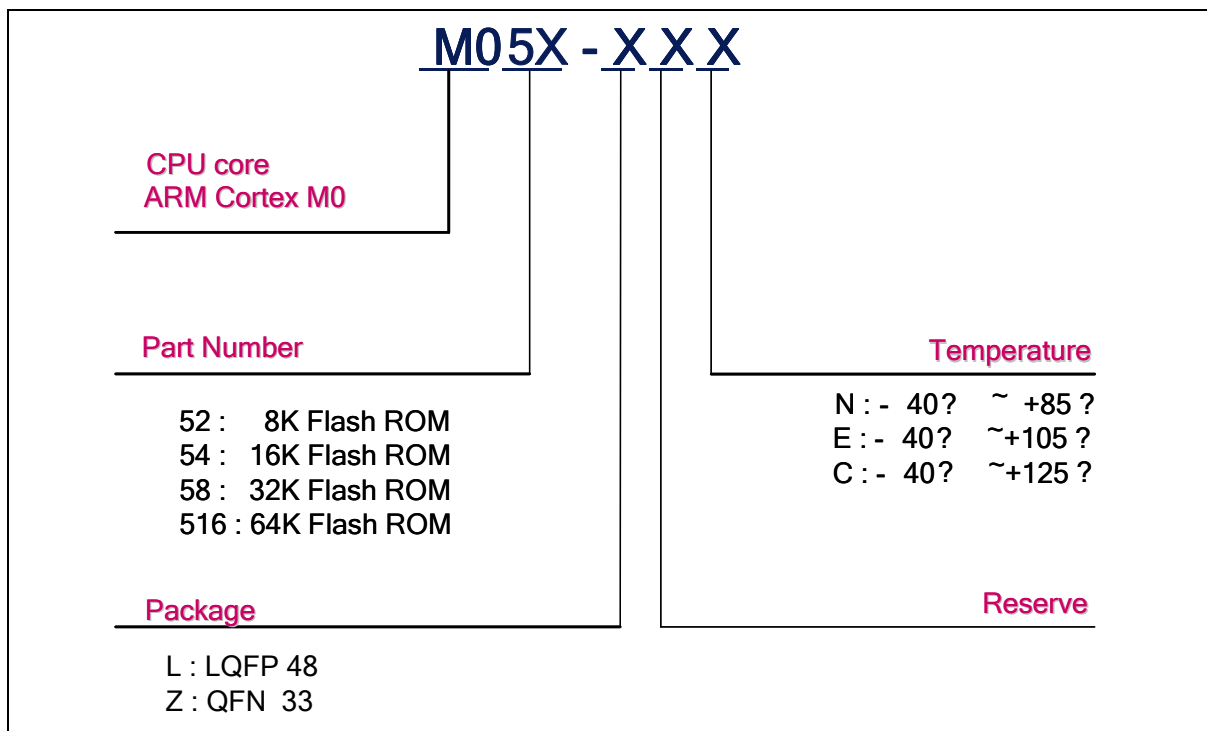
M052/M054 Block Diagram



4 SELECTION TABLE

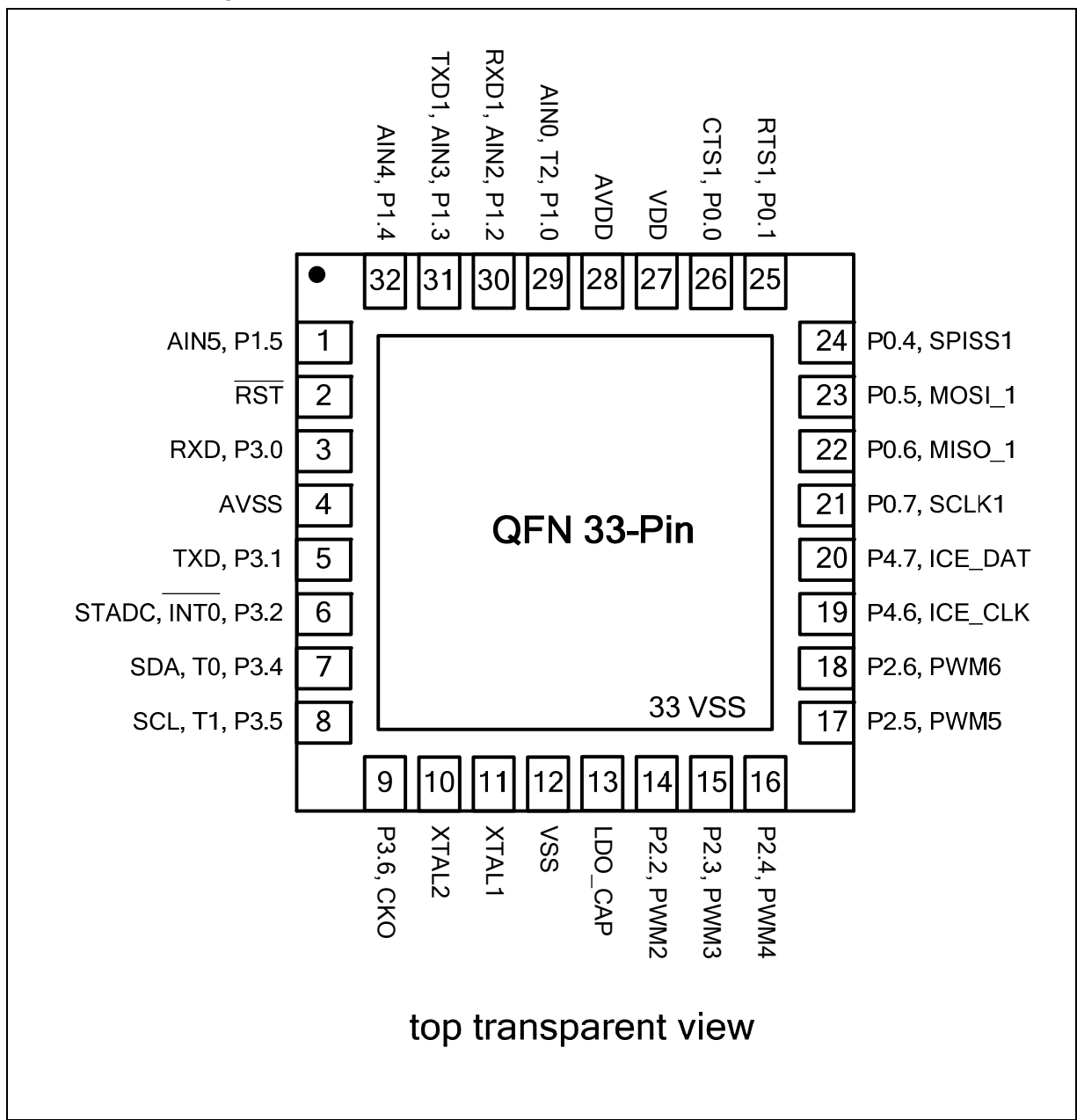
NuMicro M051™ Series Selection Guide

Part No.	APROM	RAM	Data Flash	LDROM	I/O	Timer	Connectivity			PWM	ADC	EBI	ISP ICP	Package
							UART	SPI	I2C					
M052LAN	8K	4K	4K	4K	40	4x32-bit	2	2	1	8	8x12-bit	v	v	LQFP48
M052ZAN	8K	4K	4K	4K	24	4x32-bit	2	1	1	5	5x12-bit		v	QFN33
M054LAN	16K	4K	4K	4K	40	4x32-bit	2	2	1	8	8x12-bit	v	v	LQFP48
M054ZAN	16K	4K	4K	4K	24	4x32-bit	2	1	1	5	5x12-bit		v	QFN33

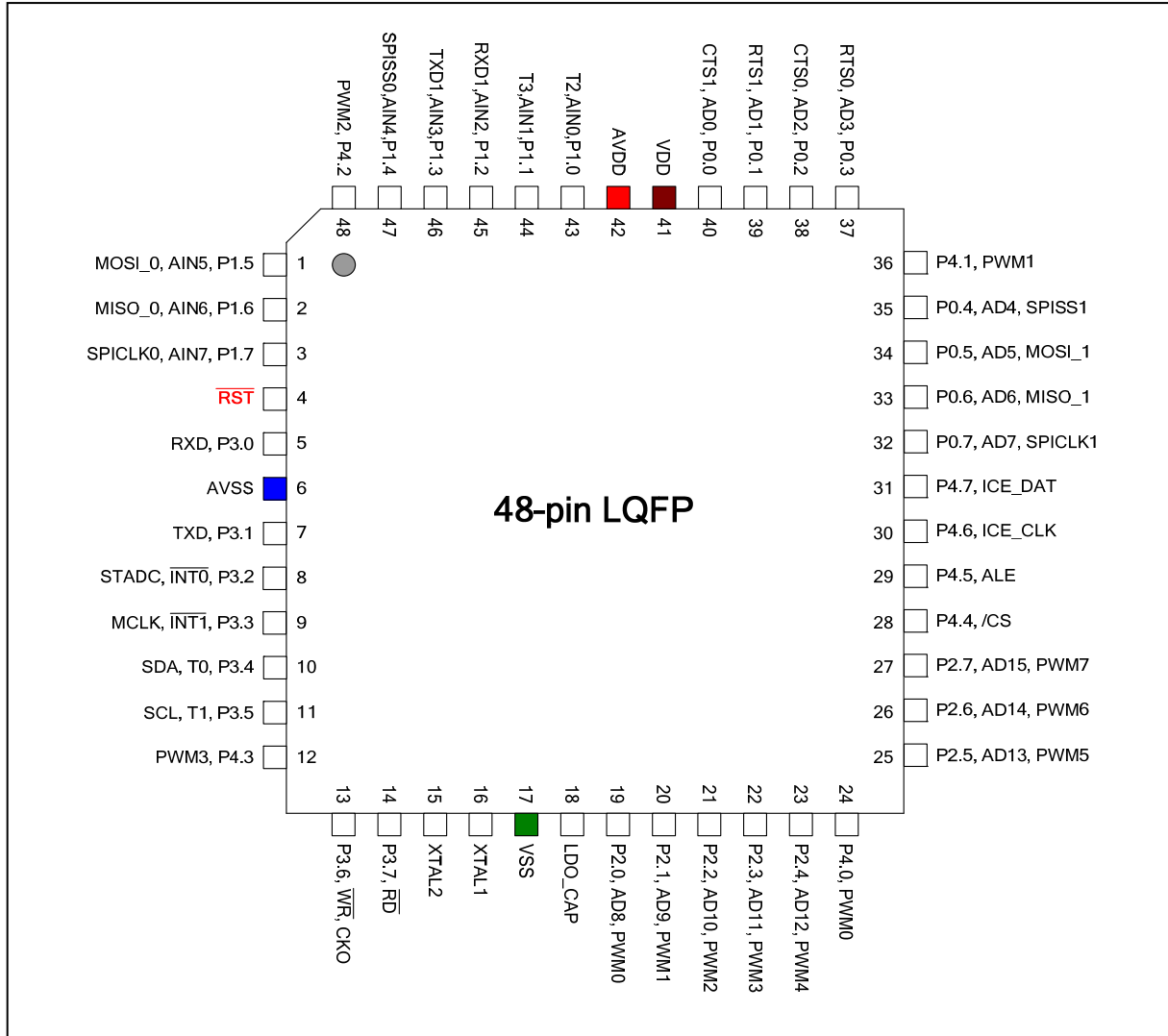


5 PIN CONFIGURATION

5.1 QFN 33 pin



5.2 LQFP 48 pin





5.3 Pin Description

Pin number		Symbol	Alternate Function		Type ^[1]	Description
QFN33	LQFP48		1	2		
11	16	XTAL1			I (ST)	CRYSTAL1: This is the input pin to the internal inverting amplifier. The system clock is from external crystal or resonator when FOSC[1:0] (CONFIG3[1:0]) are both logic 1 by default.
10	15	XTAL2			O	CRYSTAL2: This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
27	41	VDD			P	POWER SUPPLY: Supply voltage Digital V _{DD} for operation.
12	17	VSS			P	GROUND: Digital Ground potential.
33						
28	42	AVDD			P	POWER SUPPLY: Supply voltage Analog AV _{DD} for operation.
4	6	AVSS			P	GROUND: Analog Ground potential.
13	18	LDO_C AP			P	LDO: LDO output pin Note: It needs to be connected with a 10uF capacitor.
2	4	/RST			I (ST)	RESET: /RST pin is a Schmitt trigger input pin for hardware device reset. A "Low" on this pin for 768 clock counter of Internal RC 22M while the system clock is running will reset the device. /RST pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
26	40	P0.0	CTS1	AD0	D, I/O	PORT0: Port 0 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for CTS1, RTS1, CTS0, RTS0, SPISS1, MOSI_1, MISO_1, and SPICLK1. P0 has an alternative function as AD[7:0] while external memory accessing. During the external memory access, P0 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices. These pins which are SPISS1, MOSI_1, MISO_1, and SPICLK1 for the SPI function used. CTS0/1: Clear to Send input pin for UART0/1 RTS0/1: Request to Send output pin for UART0/1
25	39	P0.1	RTS1	AD1	D, I/O	
NC	38	P0.2	CTS0	AD2	D, I/O	
NC	37	P0.3	RTS0	AD3	D, I/O	
24	35	P0.4	SPISS1	AD4	D, I/O	
23	34	P0.5	MOSI_1	AD5	D, I/O	
22	33	P0.6	MISO_1	AD6	D, I/O	
21	32	P0.7	SPICLK1	AD7	D, I/O	
29	43	P1.0	T2	AIN0	I/O	PORT1: Port 1 is an 8-bit four mode output pin and two mode



Pin number		Symbol	Alternate Function		Type ^[1]	Description
QFN33	LQFP48		1	2		
NC	44	P1.1	T3	AIN1	I/O	input. Its multifunction pins are for T2, T3, RXD1, TXD1, SPISS0, MOSI_0, MISO_0, and SPICLK0.
30	45	P1.2	RXD1	AIN2	I/O	These pins which are SPISS0, MOSI_0, MISO_0, and SCLK0 for the SPI function used.
31	46	P1.3	TXD1	AIN3	I/O	These pins which are AIN0~AIN7 for the 12 bits ADC function used.
32	47	P1.4	SPISS0	AIN4	I/O	The RXD1/TXD1 pins are for UART1 function used.
1	1	P1.5	MOSI_0	AIN5	I/O	
NC	2	P1.6	MISO_0	AIN6	I/O	
NC	3	P1.7	SPICLK0	AIN7	I/O	
NC	19	P2.0	PWM0	AD8	D, I/O	PORT2: Port 2 is an 8-bit four mode output pin and two mode input. It has an alternative function
NC	20	P2.1	PWM1	AD9	D, I/O	P2 has an alternative function as AD[15:8] while external memory accessing. During the external memory access, P2 will output high will be internal strong pulled-up rather than weak pull-up in order to drive out high byte address for external devices.
14	21	P2.2	PWM2	AD10	D, I/O	
15	22	P2.3	PWM3	AD11	D, I/O	These pins which are PWM0~PWM7 for the PWM function used in the LQFP48 package.
16	23	P2.4	PWM4	AD12	D, I/O	
17	25	P2.5	PWM5	AD13	D, I/O	
18	26	P2.6	PWM6	AD14	D, I/O	
NC	27	P2.7	PWM7	AD15	D, I/O	
3	5	P3.0	RXD		I/O	PORT3: Port 3 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for RXD, TXD, $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, T0, T1, $\overline{\text{WR}}$, and $\overline{\text{RD}}$.
5	7	P3.1	TXD		I/O	
6	8	P3.2	$\overline{\text{INT0}}$	STADC	I/O	The RXD/TXD pins are for UART0 function used. The SDA/SCK pins are for I2C function used.
NC	9	P3.3	$\overline{\text{INT1}}$	MCLK	I/O	MCLK: EBI clock output pin. CKO: HCLK clock output
7	10	P3.4	T0	SDA	I/O	The STADC pin is for ADC external trigger input.
8	11	P3.5	T1	SCL	I/O	
9	13	P3.6	$\overline{\text{WR}}$	CKO	I/O	



Pin number		Symbol	Alternate Function		Type ^[1]	Description
QFN33	LQFP48		1	2		
NC	14	P3.7	$\overline{\text{RD}}$		I/O	
NC	24	P4.0	PWM0		I/O	PORT4: Port 4 is an 8-bit four mode output pin and two mode input. Its multifunction pins are for /CS, ALE, ICE_CLK and ICE_DAT. /CS for EBI (External Bus Interface) used. ALE (Address Latch Enable) is used to enable the address latch that separates the address from the data on Port 0 and Port 2. The ICE_CLK/ICE_DAT pins are for JTAG-ICE function used. PWM0-3 can be used from P4.0-P4.3 when EBI is active.
NC	36	P4.1	PWM1		I/O	
NC	48	P4.2	PWM2		I/O	
NC	12	P4.3	PWM3		I/O	
NC	28	P4.4	/CS		I/O	
NC	29	P4.5	ALE		I/O	
19	30	P4.6	ICE_CLK		I/O	
20	31	P4.7	ICE_DAT		I/O	

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger.

6 DC ELECTRICAL CHARACTERISTICS

(V_{DD}-V_{SS}=2.5~5.5V, T_A = 25°C, F_{OSC} = 50MHz unless otherwise specified.)

PARAMETER	SYM	SPECIFICATION				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operation voltage	V _{DD}	2.5		5.5	V	V _{DD} =2.5V~5.5V up to 50 MHz
Power Ground	V _{SS} AV _{SS}	-0.3			V	
LDO Output Voltage	V _{LDO}	-10%	2.45	+10%	V	V _{DD} > 2.7V
Band Gap Analog Input	V _{BG}	-5%	1.26	+5%	V	V _{DD} =2.5V ~ 5.5V
Analog Operating Voltage	AV _{DD}	3.0		V _{DD}	V	
Operating Current Normal Run Mode @ 50Mhz	I _{DD1}		32		mA	V _{DD} = 5.5V enable all IP and PLL , XTAL=12MHz
	I _{DD2}		24		mA	V _{DD} =5.5V disable all IP and enable PLL , XTAL=12MHz
	I _{DD3}		31		mA	V _{DD} = 3V enable all IP and PLL , XTAL=12MHz
	I _{DD4}		23		mA	V _{DD} = 3V disable all IP and enable PLL , XTAL=12MHz
Operating Current Normal Run Mode @ 12Mhz	I _{DD5}		17		mA	V _{DD} = 5.5V enable all IP and disable PLL , XTAL=12MHz
	I _{DD6}		14		mA	V _{DD} = 5.5V disable all IP and disable PLL , XTAL=12MHz
	I _{DD7}		16		mA	V _{DD} = 3V enable all IP and disable PLL , XTAL=12MHz
	I _{DD8}		13		mA	V _{DD} = 3V disable all IP and disable PLL , XTAL=12MHz



PARAMETER	SYM	SPECIFICATION				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operating Current Normal Run Mode @ 4Mhz	I _{DD9}		12		mA	V _{DD} = 5.5V enable all IP and disable PLL , XTAL=4MHz
	I _{DD10}		10		mA	V _{DD} = 5.5V disable all IP and disable PLL , XTAL=4MHz
	I _{DD11}		10		mA	V _{DD} = 3V enable all IP and disable PLL , XTAL=4MHz
	I _{DD12}		9		mA	V _{DD} = 3V disable all IP and disable PLL , XTAL=4MHz
Operating Current Idle Mode @ 50Mhz	I _{IDLE1}		19		mA	V _{DD} = 5.5V enable all IP and PLL , XTAL=12MHz
	I _{IDLE2}		11		mA	V _{DD} =5.5V disable all IP and enable PLL , XTAL=12MHz
	I _{IDLE3}		18		mA	V _{DD} = 3V enable all IP and PLL , XTAL=12MHz
	I _{IDLE4}		10		mA	V _{DD} = 3V disable all IP and enable PLL , XTAL=12MHz
Operating Current Idle Mode @ 12Mhz	I _{IDLE5}		10		mA	V _{DD} = 5.5V enable all IP and disable PLL , XTAL=12MHz
	I _{IDLE6}		7		mA	V _{DD} = 5.5V disable all IP and disable PLL , XTAL=12MHz
	I _{IDLE7}		9		mA	V _{DD} = 3V enable all IP and disable PLL , XTAL=12MHz
	I _{IDLE8}		6		mA	V _{DD} = 3V disable all IP and disable PLL , XTAL=12MHz
Operating Current Idle Mode @ 4Mhz	I _{IDLE9}		5		mA	V _{DD} = 5.5V enable all IP and disable PLL , XTAL=4MHz
	I _{IDLE10}		4		mA	V _{DD} = 5.5V disable all IP and disable PLL , XTAL=4MHz
	I _{IDLE11}		4		mA	V _{DD} = 3V enable all IP and disable PLL , XTAL=4MHz
	I _{IDLE12}		3		mA	V _{DD} = 3V disable all IP and disable PLL , XTAL=4MHz
Standby Current Power-down Mode (Deep Sleep Mode)	I _{PWD1}		15		μA	V _{DD} = 5.5V, No load @ Disable BOV function
	I _{PWD2}		11		μA	V _{DD} = 3.0V, No load @ Disable BOV function



PARAMETER	SYM	SPECIFICATION				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Input Current P0/1/2/3/4	I_{IN1}	-60	-	+15	μA	$V_{DD} = 5.5V, V_{IN} = 0V$ or $V_{IN} = V_{DD}$
Input Leakage Current P0/1/2/3/4	I_{LK}	-2	-	+2	μA	$V_{DD} = 5.5V, 0 < V_{IN} < V_{DD}$
Logic 1 to 0 Transition Current P0/1/2/3/4 (Quasi-bidirectional mode)	$I_{TL}^{[3]}$		-600	-200	μA	$V_{DD} = 5.5V, V_{IN} < 2.0V$
Input Low Voltage P0/1/2/3/4 (TTL input)	V_{IL1}	-0.3	-	0.8	V	$V_{DD} = 4.5V$
		-0.3	-	0.6		$V_{DD} = 2.5V$
Input High Voltage P0/1/2/3/4 (TTL input)	V_{IH1}	2.0	-	$V_{DD} + 0.2$	V	$V_{DD} = 5.5V$
		1.5	-	$V_{DD} + 0.2$		$V_{DD} = 3.0V$
Input Low Voltage XT1 ^[2]	V_{IL3}	0	-	0.8	V	$V_{DD} = 4.5V$
		0	-	0.4		$V_{DD} = 3.0V$
Input High Voltage XT1 ^[2]	V_{IH3}	3.5	-	$V_{DD} + 0.2$	V	$V_{DD} = 5.5V$
		2.4	-	$V_{DD} + 0.2$		$V_{DD} = 3.0V$
Negative going threshold (Schmitt input), /RST	V_{ILS}	-0.5	-	$0.3V_D$	V	
Positive going threshold (Schmitt input), /RST	V_{IHS}	$0.7V_D$	-	$V_{DD} + 0.5$	V	
Internal /RST pin pull up resistor	R_{RST}	40		150	K Ω	
Negative going threshold (Schmitt input), P0/1/2/3/4	V_{ILS}	-0.5	-	$0.2V_D$	V	
Positive going threshold (Schmitt input), P0/1/2/3/4	V_{IHS}	$0.4V_D$	-	$V_{DD} + 0.5$	V	
Source Current P0/1/2/3/4 (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	$V_{DD} = 4.5V, V_S = 2.4V$
	I_{SR12}	-50	-70	-90	μA	$V_{DD} = 2.7V, V_S = 2.2V$
	I_{SR12}	-40	-60	-80	μA	$V_{DD} = 2.5V, V_S = 2.0V$
Source Current P0/1/2/3/4 (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	$V_{DD} = 4.5V, V_S = 2.4V$
	I_{SR22}	-4	-6	-8	mA	$V_{DD} = 2.7V, V_S = 2.2V$
	I_{SR22}	-3	-5	-7	mA	$V_{DD} = 2.5V, V_S = 2.0V$
Sink Current P0/1/2/3/4 (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	$V_{DD} = 4.5V, V_S = 0.45V$
	I_{SK1}	7	10	13	mA	$V_{DD} = 2.7V, V_S = 0.45V$
	I_{SK1}	6	9	12	mA	$V_{DD} = 2.5V, V_S = 0.45V$

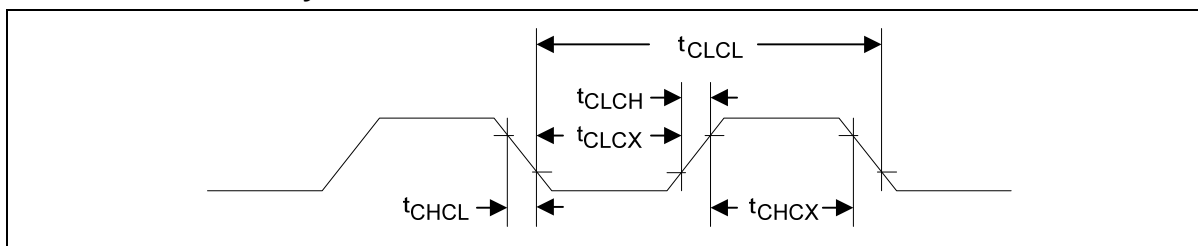
PARAMETER	SYM	SPECIFICATION				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Brownout voltage with BOV_VL [1:0] =00b	V _{BO2.2}	2.1	2.2	2.3	V	
Brownout voltage with BOV_VL [1:0] =01b	V _{BO2.7}	2.6	2.7	2.8	V	
Brownout voltage with BOV_VL [1:0] =10b	V _{BO3.8}	3.7	3.8	3.9	V	
Brownout voltage with BOV_VL [1:0] =11b	V _{BO4.5}	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V _{BH}	30	-	150	mV	V _{DD} = 2.5V~5.5V

Notes:

1. /RST pin is a Schmitt trigger input.
2. XTAL1 is a CMOS input.
3. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when V_{in} approximates to 2V.

7 AC ELECTRICAL CHARACTERISTICS

7.1 External Crystall



Note: Duty cycle is 50%.

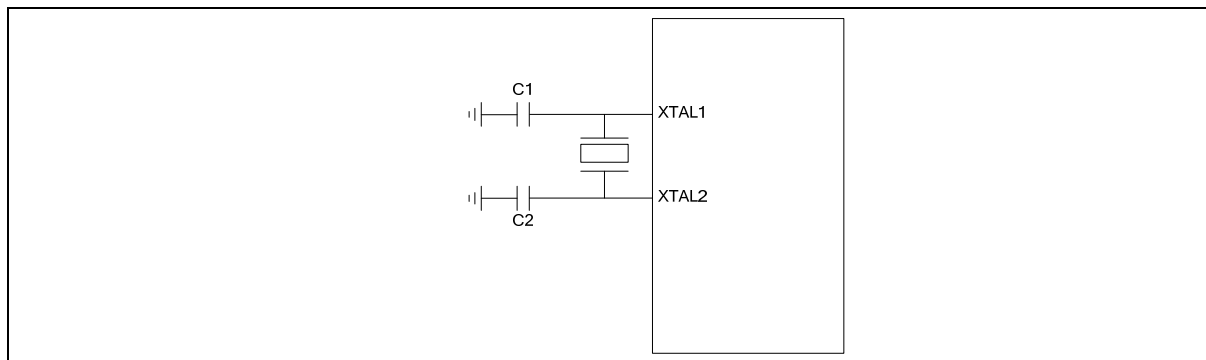
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	20	-	125	nS	
Clock Low Time	t_{CLCX}	20	-	125	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

7.2 External Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	°C
V_{DD}	-	2.5	5	5.5	V
Operating current	12MHz@ $V_{DD} = 5V$	-	5	-	mA

7.3 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4MHz ~ 24 MHz	Optional (Depend on crystal specification)	





7.4 Internal 22.1184MHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25°C; V _{DD} =5V	-1	-	+1	%
	-40°C~+85°C; V _{DD} =2.5V~5.5V	-3	-	+3	%
Accuracy of Un-calibrated Internal Oscillator Frequency	-40°C~+85°C; V _{DD} =2.5V~5.5V	-25	-	+25	%
Operating current	V _{DD} =5V	-	500	-	uA

7.5 Internal 10kHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage ^[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V _{DD} =5V	-30	-	+30	%
	-40°C~+85°C; V _{DD} =2.5V~5.5V	-50	-	+50	%
Operating current	V _{DD} =5V	-	5	-	uA

Notes:

1. Internal operation voltage comes from LDO.

7.6 Specification of 600k sps 12-bit SARADC

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	-	12	Bit
Differential nonlinearity error	DNL	-	±1.2	-	LSB
Integral nonlinearity error	INL	-	±1.5	-	LSB
Offset error	EO	-	+4	10	LSB
Gain error (Transfer gain)	EG	-	+7	1.005	-
Monotonic	-	-	Guaranteed		-
ADC clock frequency	FADC	-	-	20	MHz
Calibration time	TCAL	-	127	-	Clock
Sample time	TS	-	7	-	Clock
Conversion time	TADC	-	13	-	Clock
Sample rate	FS	-	-	600	k sps
Supply voltage	V _{LDO}	-	2.5	-	V
	V _{ADD}	3	-	5.5	V
Supply current (Avg.)	I _{DD}	-	0.5	-	mA
	I _{DDA}	-	1.5	-	mA
Input voltage range	V _{IN}	0	-	AVDD	V
Capacitance	C _{IN}	-	5	-	pF

7.7 Specification of LDO & Power management

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.7	5	5.5	V	V _{DD} input voltage
Output Voltage (bypass=0)	-10%	2.45	+10%	V	LDO output voltage
Output Voltage (bypass=1)	-10%	Input Voltage	+10%	V	Input Voltage < 2.7V
Quiescent Current (PD=0, bypass=0)	-	100	-	uA	
Quiescent Current (PD=1, bypass=0)	-	5	-	uA	
Quiescent Current (PD=1, bypass=1)	-	5	-	uA	
Iload (PD=0)	-	-	100	mA	
Iload (PD=1)	-	-	100	uA	
Cbp	-	1u	-	F	Resr=1ohm
Cload	-	250p	-	F	

Note:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.
2. For ensuring power stability, a 4.7uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise.

7.8 Specification of Low Voltage Reset

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	VDD5V=5.5V	-	-	5	uA
Threshold voltage	Temperature=25°C	-	2.0	-	V
	Temperature=-40°C	-	2.4	-	V
	Temperature=85°C	-	1.6	-	V
Hysteresis	-	0	0	0	V

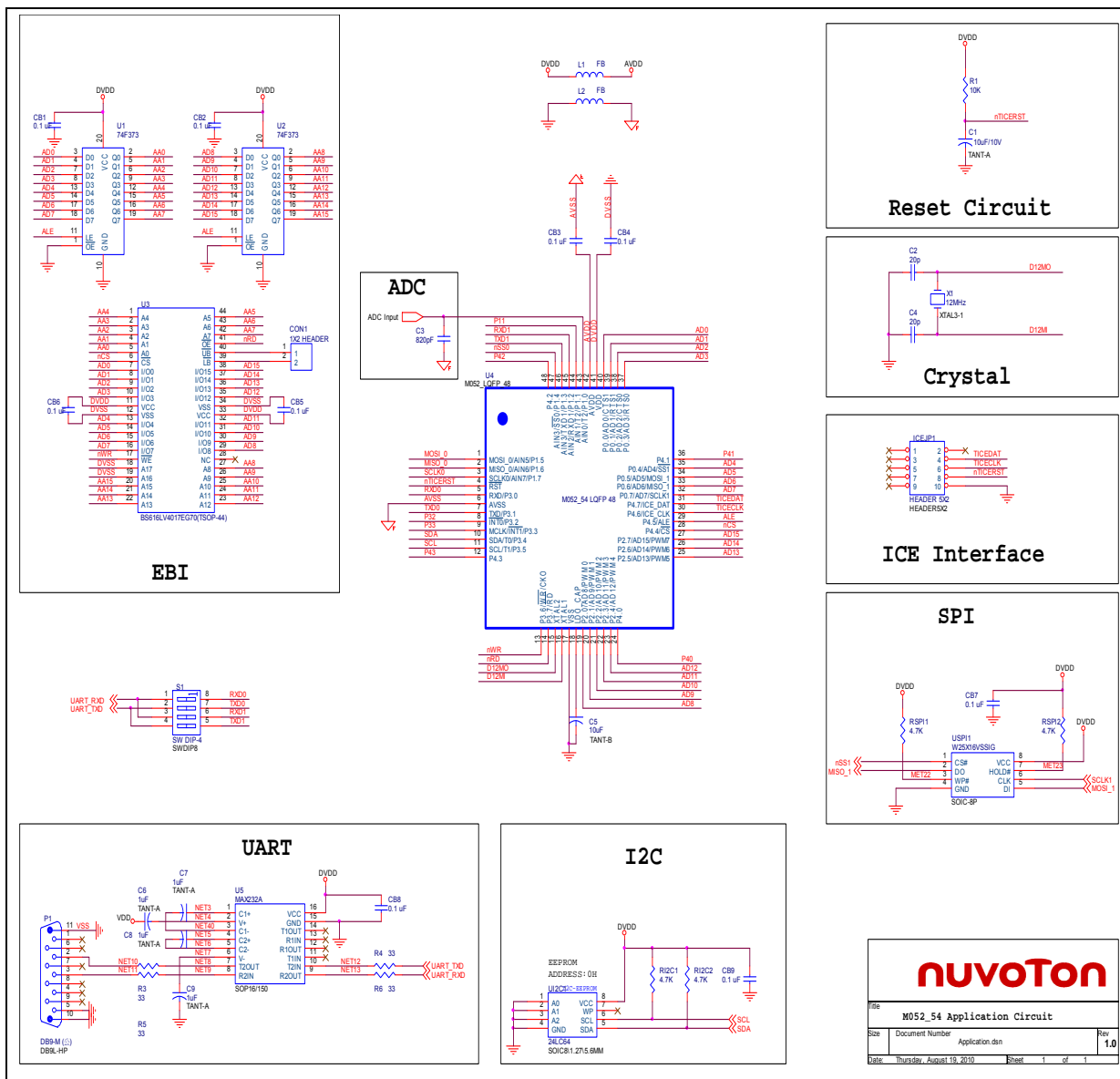
7.9 Specification of Brownout Detector

Parameter	Condition	Min.	Typ.	Max.	Unit
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AVDD=5.5V	-	-	125	μA
Brown-out voltage	BOV_VL[1:0]=11	4.4	4.5	4.6	V
	BOV_VL [1:0]=10	3.7	3.8	3.9	V
	BOV_VL [1:0]=01	2.6	2.7	2.8	V
	BOV_VL [1:0]=00	2.1	2.2	2.3	V
Hysteresis	-	30m	-	150m	V

7.10 Specification of Power-On Reset (5V)

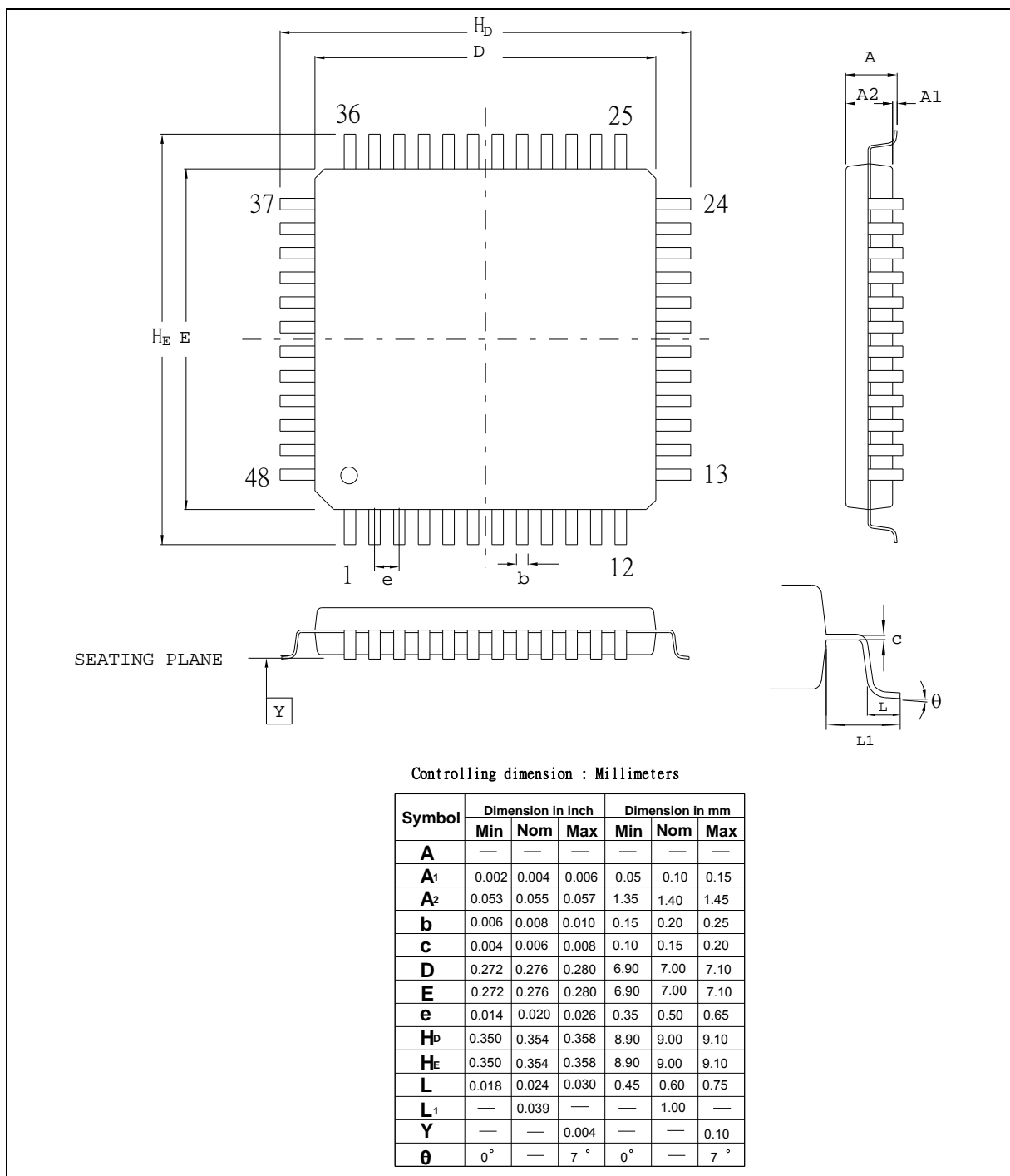
Parameter	Condition	Min.	Typ.	Max.	Unit
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

8 APPLICATION CIRCUIT

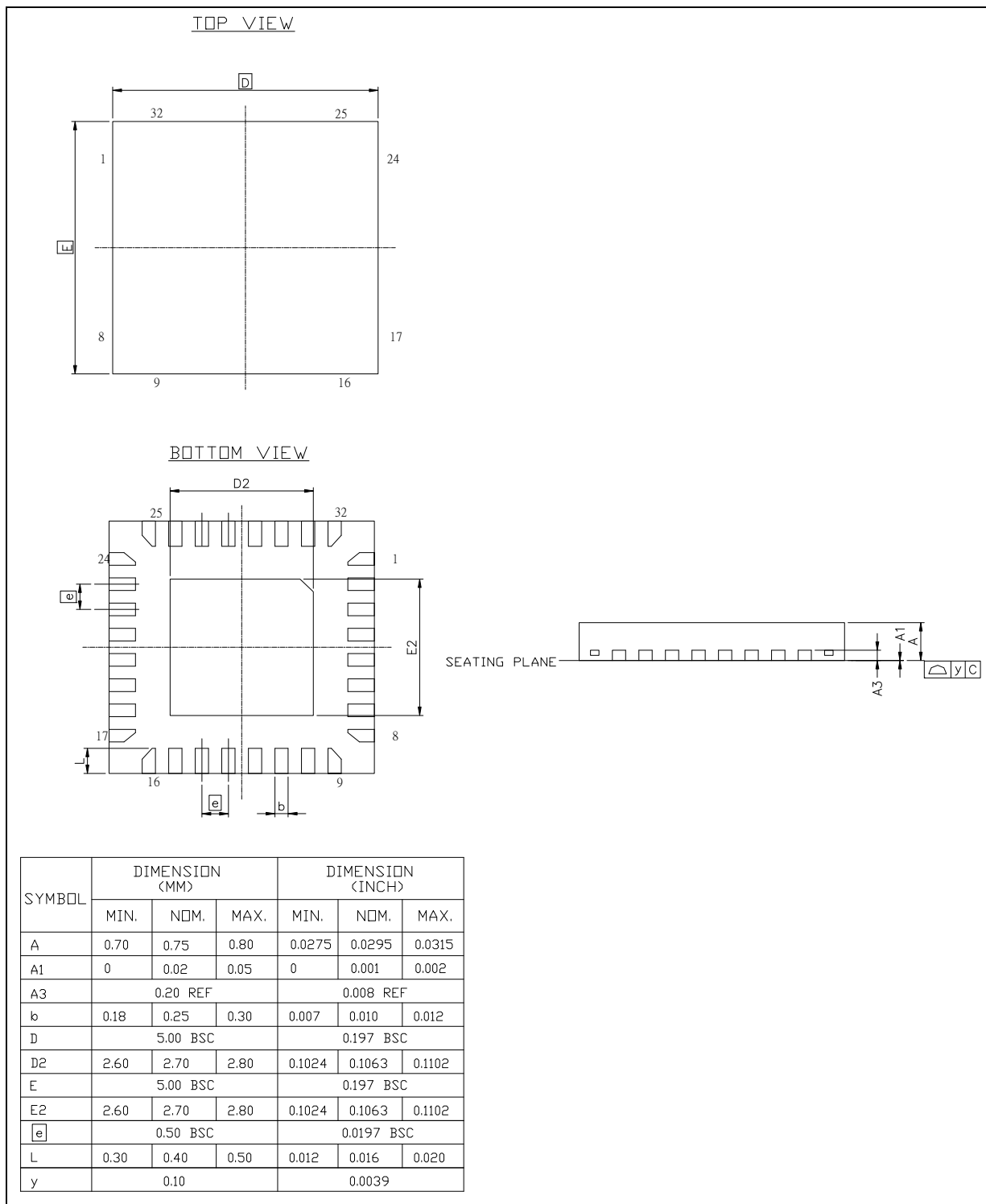


9 PACKAGE OUTLINE

9.1 48-Pin LQFP



9.2 33-Pin QFN





10 REVISION HISTORY

VERSION	DATE	PAGE/ CHAP.	DESCRIPTION
V1.0	Aug 19, 2010	-	Initial issued

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