ARM Cortex™-M0

32-BIT MICROCONTROLLER

NuMicro™ Family
Mini51 Series DataSheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

CONTENTS

List of Figures

List of Tables

1 GENERAL DESCRIPTION

The NuMicro Mini51™ series is a 32-bit microcontroller with embedded ARM® Cortex™-M0 core for industrial control and applications which need high performance, high-integration low-cost requirements. The Cortex™-M0 is the newest ARM embedded processor with 32-bit performance and at a cost equivalent to traditional 8-bit microcontroller.

The NuMicro Mini51™ series can run up to 24 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro Mini51™ series provides 4K/8K/16K-byte embedded program flash, configurable size data flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte embedded SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer and low voltage detector, have been incorporated into the NuMicro Mini51™ series in order to reduce component count, board space and system cost. These useful functions make the NuMicro Mini51™ series powerful for a wide range of applications.

Additionally, the NuMicro Mini51™ series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Core
  - ARM® Cortex™-M0 core runs up to 24 MHz
  - One 24-bit system timer
  - Supports low power Idle Mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Supports Serial Wire Debug (SWD) with 2 watchpoints/4 breakpoints
- Built-in LDO for Wide Operating Voltage Range: 2.5 V to 5.5 V
- Memory
  - 4KB/8KB/16KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2KB Flash memory for loader (LDROM)
  - 2KB SRAM for internal scratch-pad RAM (SRAM)
- In-System Programming (ISP) & In-Circuit Programming (ICP)
- Clock Control
  - Programmable system clock source
    - Switch clock sources on-the-fly
  - 4 ~ 24 MHz crystal oscillator (HXT)
  - 32.768K crystal oscillator (LXT) for idle wake-up and system operation clock
  - 22.1184 MHz internal oscillator (HIRC) (1% accuracy at 25^0C, 5V)
    - Dynamic calibrating the HIRC OSC to 22.0 MHz ±1% from -40^0C to 85^0C by external 32.768K crystal oscillator (LXT)
  - 10 KHz internal low-power oscillator (LIRC) for watchdog and idle wakeup
- I/O Port
  - Up to 30 General Purpose I/O (GPIO) pins for LQFP-48 package
  - Software-configured I/O type
    - Quasi-bidirectional input/output
    - Push-pull output
    - Open-drain output
    - Input-only with high impendence
  - Optional Schmitt trigger input
- Timer
  - Two 24-bit Timers with 8-bit pre-scaler
    - Support event counter mode

- Support toggle output mode
- Support external trigger in Pulse width measurement mode
  - Support external trigger in pulse width capture mode

- Watchdog Timer
  - Programmable clock source and timeout period
  - Support wake-up function in Power Down Mode and Idle Mode
  - Interrupt or reset selectable when timeout happens
- PWM
  - Built-in up to three 16-bit PWM generators provide six PWM outputs or three complementary paired PWM outputs
  - Support edge alignment or center alignment
  - Support fault detection
  - Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
  - PWM interrupt synchronized to PWM period
- UART
  - One UART device
  - Buffered receiver and transmitter with 16 bytes FIFO
  - Optional flow control function (CTSn and RTSn)
  - Support IrDA (SIR) function
  - Programmable baud-rate generator up to 1/16 system clock
  - Support RS-485 function
- SPI
  - One SPI device
  - Master up to 12 MHz, and Slave up to 4 MHz
  - Support SPI master/slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Byte suspend mode in 32-bit transmission
- I^2C
  - Master/Slave mode up to 1 Mbit/s (Fast-mode Plus)
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus

- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow versatile rate control
- Support multiple address recognition (four slave address with mask option)

- ADC
  - 10-bit SAR ADC with 150K SPS
  - Up to 8-ch single-end input and one internal input from band-gap
  - Conversion started by software or external pin
- Analog Comparator
  - Two analog comparators with programmable 16-level internal voltage reference
  - Build-in comparator reference voltage (CRV)
- BOD Reset
  - Programmable 3 threshold levels: 3.8V/2.7V/2.0V (default 2.0V)
  - Optional BOD interrupt or reset
- 96-bit unique ID
- Operating Temperature: -40℃~85℃
- Packages:
  - Green package (RoHS)
  - LQFP 48-pin (7x7), QFN 33-pin (5x5), QFN 33-pin (4x4)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro Mini51™ Series Product Selection Guide

Part number	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer	Connectivity			Comp.	PWM	ADC	ISP ICP	IRC 22.1184 MHz	Package
							UART	SPI	I^2C						
MINI51LAN	4 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI51ZAN	4 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI51TAN	4 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)
MINI52LAN	8 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI52ZAN	8 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI52TAN	8 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)
MINI54LAN	16 KB	2 KB	Configurable	2 KB	up to 30	2x32-bit	1	1	1	2	6	8x10-bit	v	v	LQFP48
MINI54ZAN	16 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(5x5)
MINI54TAN	16 KB	2 KB	Configurable	2 KB	up to 29	2x32-bit	1	1	1	2	6	8x10-bit	v	v	QFN33(4x4)

Figure 3.1-1 NuMicro Mini51™ Series Product Selection Guide

3.2 PIN CONFIGURATION

3.2.1 LQFP 48-pin

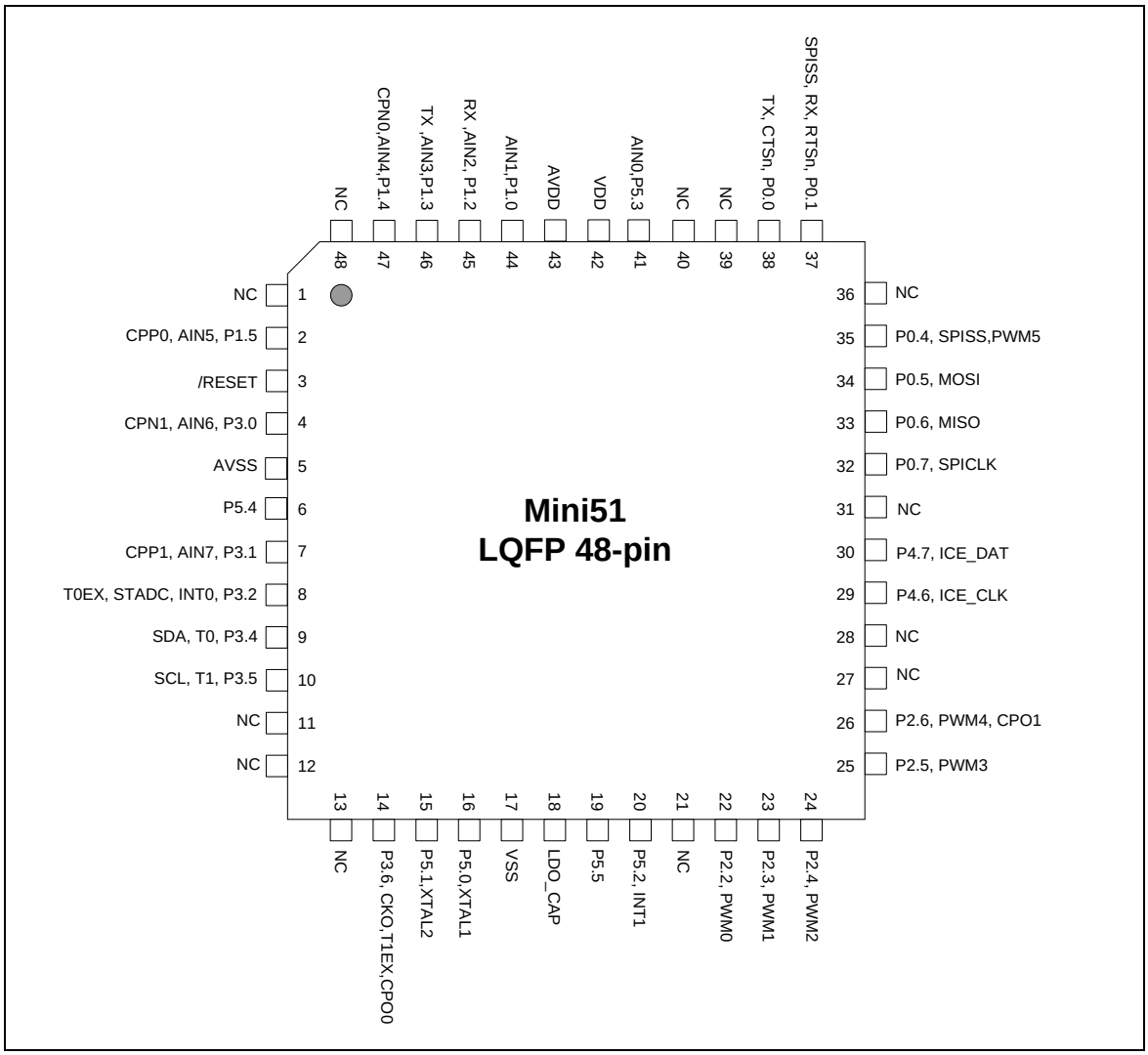


Figure 3.2-1 NuMicro Mini51™ Series LQFP 48-pin Diagram

3.2.2 QFN 33-pin

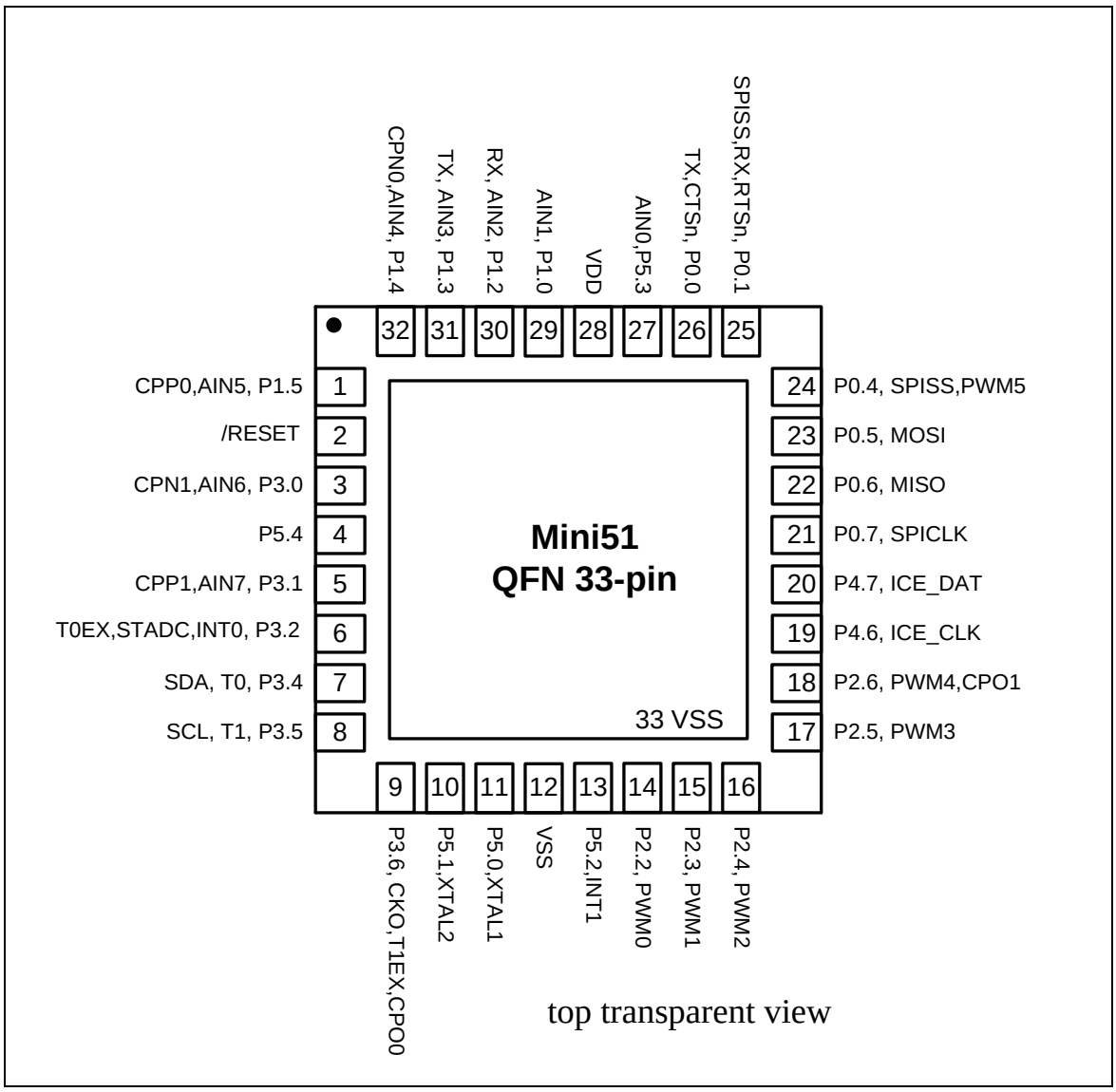


Figure 3.2-2 NuMicro Mini51™ Series QFN 33-pin Diagram

3.3 Pin Description

Pin Number		Pin Name	Pin Type	Description
LQFP 48	QFN 33			
1		NC		Not connected pin
2	1	P1.5	**I/O**	General purpose input/output digital pin
		AIN5	**AI**	ADC analog input pin
		CPP0	**AI**	Analog comparator Positive input pin
3	2	/RESET	**I(ST)**	This pin is a Schmitt trigger input pin for hardware device reset. A "**Low**" on this pin for 768 clock counter of Internal RC 22.1184 MHz while the system clock is running will reset the device. /RESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
4	3	P3.0	**I/O**	General purpose input/output digital pin
		AIN6	**AI**	ADC analog input pin
		CPN1	**AI**	Analog comparator negative input pin
5		AVSS	**AP**	Ground pin for analog circuit
6	4	P5.4	**I/O**	General purpose input/output digital pin
7	5	P3.1	**I/O**	General purpose input/output digital pin
		AIN7	**AI**	ADC analog input pin
		CPP1	**AI**	Analog comparator positive input pin
8	6	P3.2	**I/O**	General purpose input/output digital pin
		INT0	**I**	External interrupt 0 input pin
		STADC	**I**	ADC external trigger input pin
		T0EX	**I**	Timer 0 external capture/reset trigger input pin
9	7	P3.4	**I/O**	General purpose input/output digital pin
		T0	**I/O**	Timer 0 external event counter input pin
		SDA	**I/O**	I^2C data input/output pin
10	8	P3.5	**I/O**	General purpose input/output digital pin
		T1	**I/O**	Timer 1 external event counter input pin
		SCL	**I/O**	I^2C clock input/output pin
11		NC		Not connected pin
12		NC		Not connected pin

Pin Number		Pin Name	Pin Type	Description
LQFP 48	QFN 33			
13		NC		Not connected pin
14	9	P3.6	I/O	General purpose input/output digital pin
		CPO0	O	Analog comparator output pin
		CKO	O	Frequency Divider output pin
		T1EX	I	Timer 1 external capture/reset trigger input pin
15	10	P5.1	I/O	General purpose input/output digital pin
		XTAL2	O	This is the output pin from the internal inverting amplifier. It emits the inverted signal of XTAL1.
16	11	P5.0	I/O	General purpose input/output digital pin
		XTAL1	I	This is the input pin to the internal inverting amplifier. The system clock could be from external crystal or resonator.
17	12	VSS	P	Ground pin for digital circuit
	33			
18		LDO_CAP	P	LDO output pin
19		P5.5	I/O	General purpose input/output digital pin User program must enable pull-up resistor in QFN33 package.
20	13	P5.2	I/O	General purpose input/output digital pin
		INT1	I	External interrupt 1 input pin
21		NC		Not connected pin
22	14	P2.2	I/O	General purpose input/output digital pin
		PWM0	O	PWM0 output of PWM unit
23	15	P2.3	I/O	General purpose input/output digital pin
		PWM1	O	PWM1 output of PWM unit
24	16	P2.4	I/O	General purpose input/output digital pin
		PWM2	O	PWM2 output of PWM unit
25	17	P2.5	I/O	General purpose input/output digital pin
		PWM3	O	PWM3 output of PWM unit
26	18	P2.6	I/O	General purpose input/output digital pin
		PWM4	O	PWM4 output of PWM unit
		CPO1	O	Analog comparator output pin

Pin Number		Pin Name	Pin Type	Description
LQFP 48	QFN 33			
27		NC		Not connected pin
28		NC		Not connected pin
29	19	P4.6	I/O	General purpose input/output digital pin
		ICE_CLK	I	Serial wired debugger clock pin
30	20	P4.7	I/O	General purpose input/output digital pin
		ICE_DAT	I/O	Serial wired debugger data pin
31		NC		Not connected pin
32	21	P0.7	I/O	General purpose input/output digital pin
		SPICLK	I/O	SPI serial clock pin
33	22	P0.6	I/O	General purpose input/output digital pin
		MISO	I/O	SPI MISO (master in/slave out) pin
34	23	P0.5	I/O	General purpose input/output digital pin
		MOSI	O	SPI MOSI (master out/slave in) pin
35	24	P0.4	I/O	General purpose input/output digital pin
		SPISS	I/O	SPI slave select pin
		PWM5	O	PWM5 output of PWM unit
36		NC		Not connected pin
37	25	P0.1	I/O	General purpose input/output digital pin
		RTSn	O	UART RTS pin
		RX	I	UART data receiver input pin
		SPISS	I/O	SPI slave select pin
38	26	P0.0	I/O	General purpose input/output digital pin
		CTSn	I	UART CTS pin
		TX	O	UART transmitter output pin
39		NC		Not connected pin
40		NC		Not connected pin
41	27	P5.3	I/O	General purpose input/output digital pin
		AIN0	AI	ADC analog input pin
42	28	VDD	P	Power supply for digital circuit
43		AVDD	P	Power supply for analog circuit

Pin Number		Pin Name	Pin Type	Description
LQFP 48	QFN 33			
44	29	P1.0	**I/O**	General purpose input/output digital pin
		AIN1	**AI**	ADC analog input pin
45	30	P1.2	**I/O**	General purpose input/output digital pin
		AIN2	**AI**	ADC analog input pin
		RX	**I**	UART data receiver input pin
46	31	P1.3	**I/O**	General purpose input/output digital pin
		AIN3	**AI**	ADC analog input pin
		TX	**O**	UART transmitter output pin
47	32	P1.4	**I/O**	General purpose input/output digital pin
		AIN4	**I/O**	PWM5: PWM output/Capture input
		CPN0	**AI**	Analog comparator negative input pin
48		NC		Not connected pin

Table 3.3-1 NuMicro Mini51™ Series Pin Description

[1] I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

4 BLOCK DIAGRAM

4.1 NuMicro Mini51™ Block Diagram

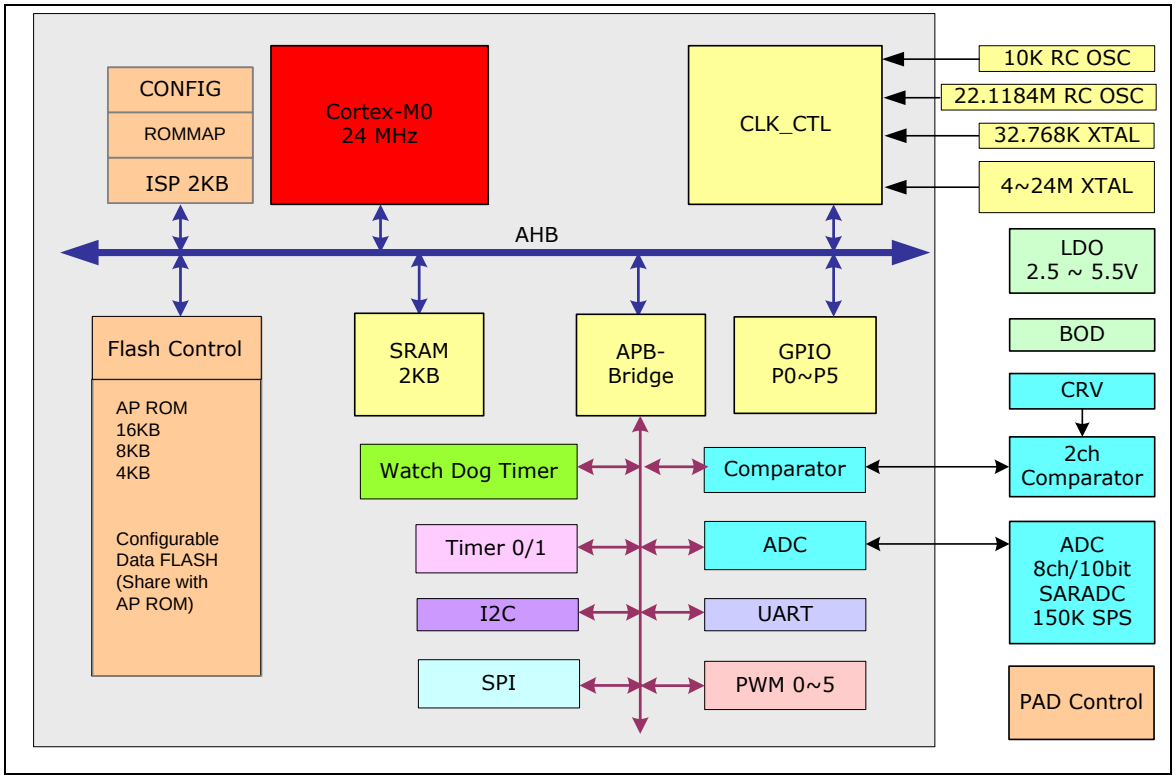


Figure 4.1-1 NuMicro Mini51™ Series Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 Memory Organization

5.1.1 Overview

NuMicro Mini51™ series provides a 4G-byte address space for programmers. The memory locations assigned to each on-chip modules are shown in Table 5.1-1. The detailed register and memory addressing and programming will be described in the following sections for individual on-chip modules. NuMicro Mini51™ series only supports little-endian data format.

5.1.2 System Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Address Space	Token	Controllers
Flash & SRAM Memory Space		
0x0000_0000 – 0x0000_3FFF	FLASH_BA	FLASH Memory Space (16KB)
0x2000_0000 – 0x2000_07FF	SRAM_BA	SRAM Memory Space (2KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GP_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4001_0000 – 0x4001_3FFF	TMR_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C_BA	I^2C Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI_BA	SPI Control Registers
0x4004_0000 – 0x4004_3FFF	PWM_BA	PWM Control Registers
0x4005_0000 – 0x4005_3FFF	UART_BA	UART Control Registers
0x400D_0000 – 0x400D_3FFF	CMP_BA	Analog Comparator Control Registers
0x400E_0000 – 0x400E_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
System Controllers Space (0xE000_E000 – 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	Nested Vectored Interrupt Control Registers
0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 5.1-1 Address Space Assignments for On-Chip Modules

5.2 Nested Vectored Interrupt Controller (NVIC)

5.2.1 Overview

Cortex™-M0 CPU provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features.

5.2.2 Feature

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.2.3 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro Mini51™ series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth

priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Exception Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 5.2-1 Exception Model

Exception Number	IRQ Number (Bit in Interrupt Registers)	Exception Name	Source IP	Exception description	Power Down wake-up
1 ~ 15	-	-	-	System exceptions	-
16	0	**BOD_OUT**	Brownout	Brownout low voltage detected interrupt	Yes
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt	Yes
18	2	**EINT0**	GPIO	External signal interrupt from P3.2 pin	Yes
19	3	**EINT1**	GPIO	External signal interrupt from P5.2 pin	Yes
20	4	**GP0/1_INT**	GPIO	External signal interrupt from GPIO group P0~P1	Yes
21	5	**GP2/3/4_INT**	GPIO	External signal interrupt from GPIO group P2~P4 except P3.2	Yes
22	6	**PWM_INT**	PWM	PWM interrupt	No
23	7	**BRAKE_INT**	PWM	PWM interrupt	No
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt	Yes
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt	Yes
26 ~ 27	10 ~ 11	-	-	-	
28	12	**UART_INT**	UART	UART interrupt	Yes

Exception Number	IRQ Number (Bit in Interrupt Registers)	Exception Name	Source IP	Exception description	Power Down wake-up
29	13	-	-	-	
30	14	**SPI_INT**	SPI	SPI interrupt	No
31	15	-	-	-	
32	16	**GP5_INT**	GPIO	External signal interrupt from GPIO group P5 except P5.2	Yes
33	17	**HFIRC_TRIM_INT**	HFIRC	HFIRC trim interrupt	No
34	18	**I2C_INT**	I^2C	I^2C interrupt	No
35 ~ 40	19 ~ 24	-	-	-	
41	25	**ACMP_INT**	ACMP	Analog Comparator 0 or 1 interrupt	Yes
42 ~ 43	26 ~ 27	-	-	-	
44	28	**PWRWU_INT**	CLKC	Clock controller interrupt for chip wake-up from power-down state	Yes
45	29	**ADC_INT**	ADC	ADC interrupt	No
46 ~ 47	30 ~ 31	-	-	-	

Table 5.2-2 System Interrupt Map

5.2.4 Vector Table

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARMv6-M, the vector table base address is fixed at 0x0000_0000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset (Bytes)	Description
0x00	Initial Stack Pointer value
Exception Number × 0x04	Exception Entry Pointer using that Exception Number

Table 5.2-3 Vector Table Format

5.2.5 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

5.3 System Manager

5.3.1 Overview

The following functions are included in system manager section

- System Memory Map
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System management registers for product ID
- System management registers for chip and module functional reset and multi-function pin control
- Brownout and chip miscellaneous Control Register
- Combined peripheral interrupt source identify

5.3.2 System Reset

The system reset includes one of the list below event occurs. For these reset event flags can be read by RSTSRC register.

- The Power-On Reset (POR)
- The low level on the /RESET pin
- Watchdog Time Out Reset (WDT)
- Brownout-Detected Reset (BOD)
- Cortex™-M0 CPU Reset
- Software one shot Reset

5.3.3 System Power Distribution

In this device, the power distribution is divided into three segments.

- Analog power from AVDD and AVSS provides the power for analog module operation
- Digital power from VDD and VSS supplies the power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins
- Build-in a capacitor for internal voltage regulator

The outputs of internal voltage regulator, which is LDO_CAP, require an external capacitor which should be located close to the corresponding pin. The Figure 5.3-1 shows the power architecture of this device.

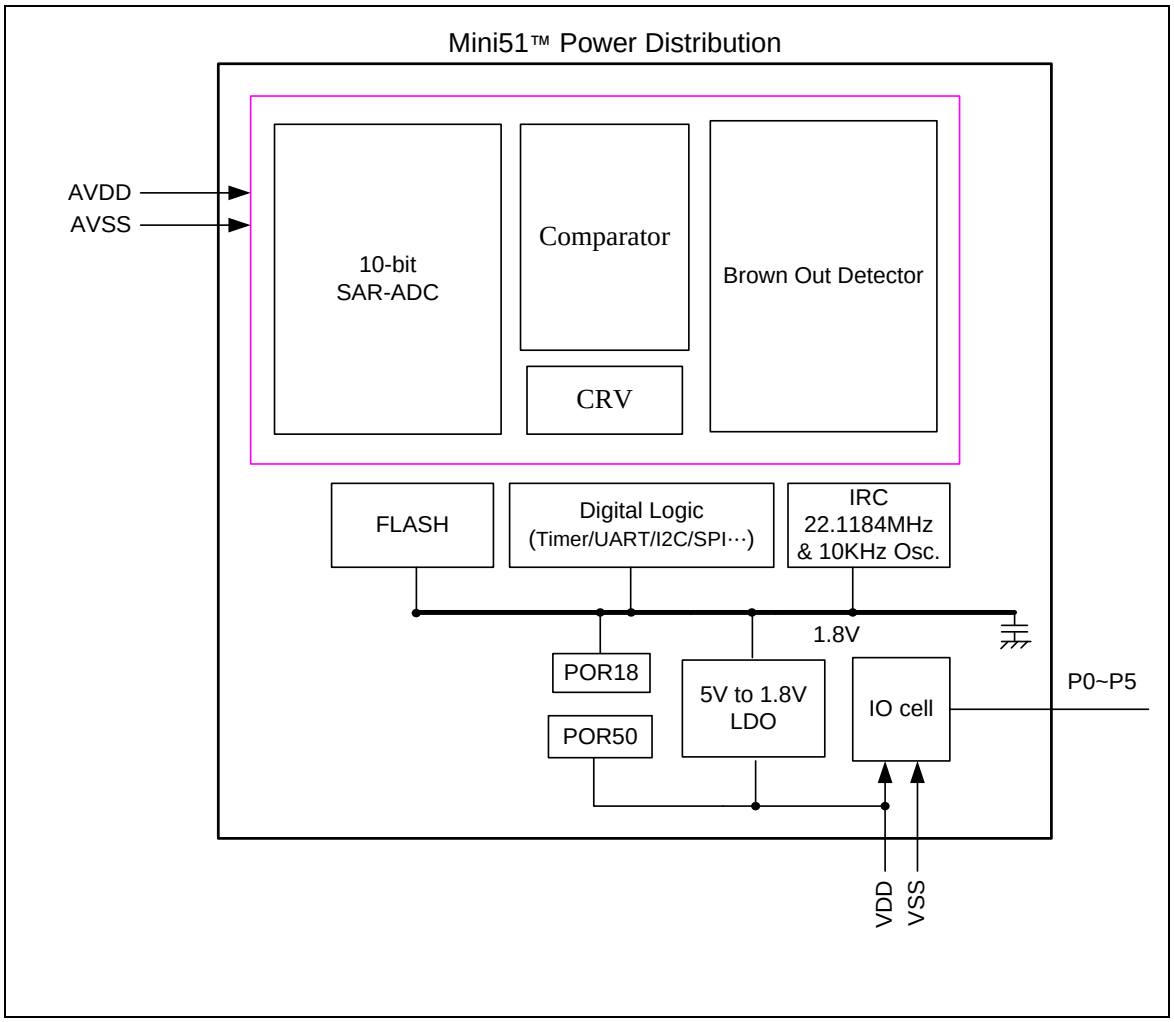


Figure 5.3-1 NuMicro Mini51™ Series Power Distribution Diagram

5.3.4 Memory mapping table

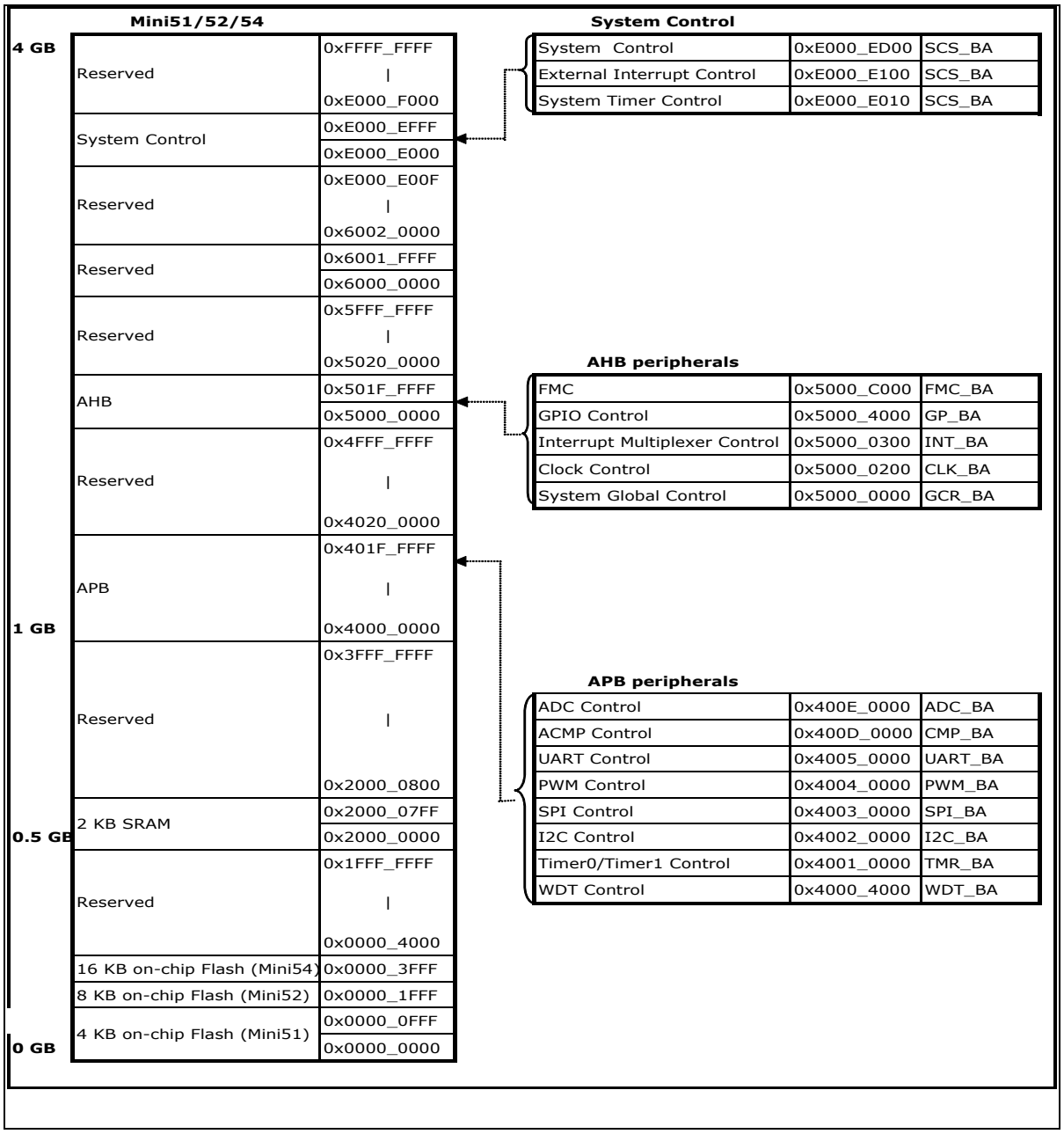


Table 5.3-1 Memory mapping table

5.4 Clock Controller

5.4.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a 4-bit clock divider. The chip will not enter power-down mode until CPU sets the power down enable bit (PWR_DOWN_EN) and Cortex-M0 core executes the WFI instruction. After that, chip enter power-down mode and wait for wake-up interrupt source triggered to leave power-down mode. In the power down mode, the clock controller turns off the external crystal and internal 22.1184 MHz oscillator to reduce the overall system power consumption.

5.4.2 Clock Generator

The clock generator consists of 3 sources which list below:

- One external 12 MHz (HXT) or 32 KHz (LXT) crystal
- One internal 22.1184 MHz RC oscillator (HIRC)
- One internal 10 KHz oscillator (LIRC)

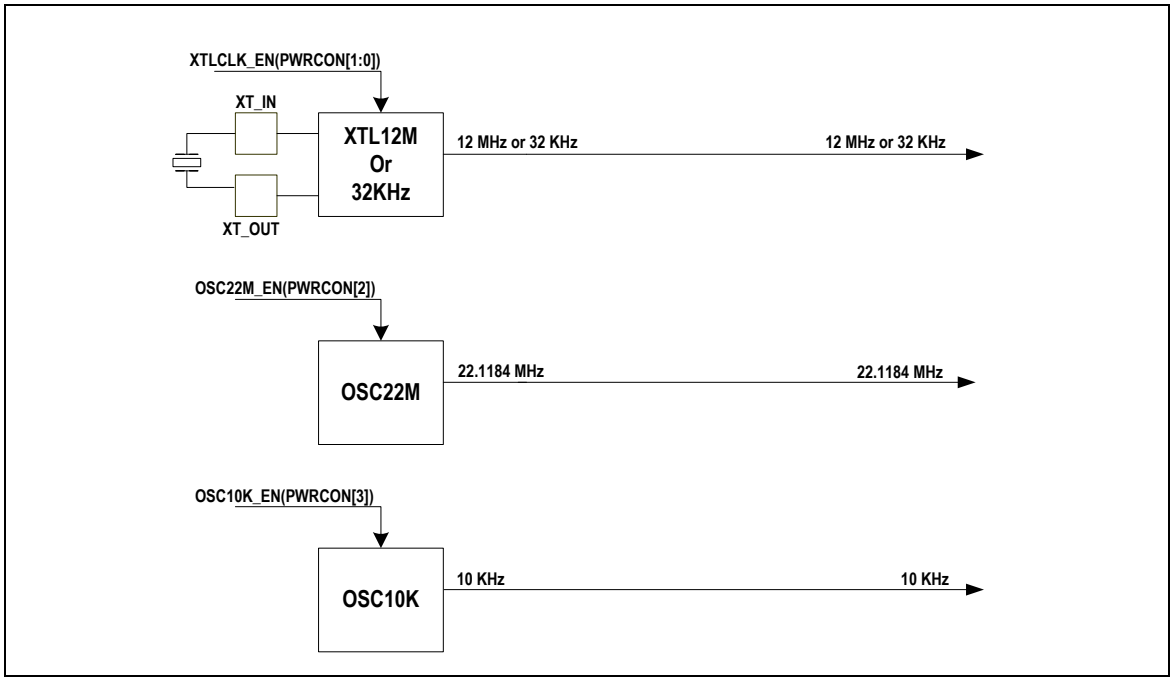


Figure 5.4-1 Clock generator block diagram

5.4.3 System Clock & SysTick Clock

The system clock has 3 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram lists below.

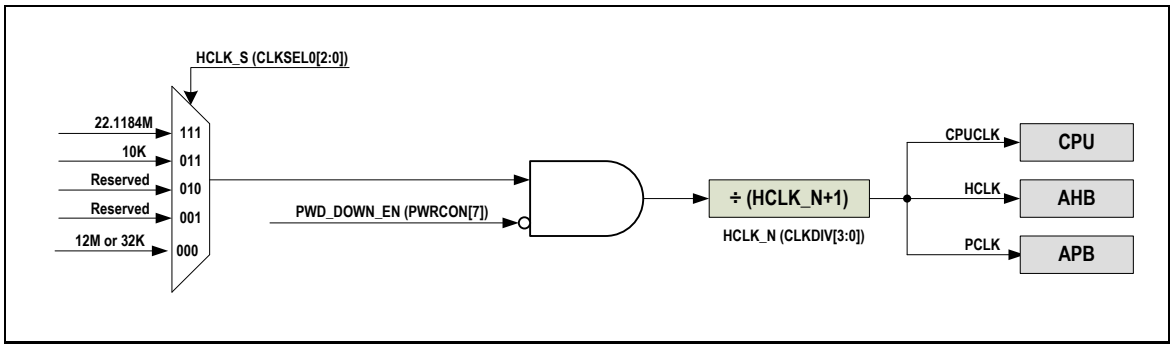


Figure 5.4-2 System Clock Block Diagram

The clock source of SysTick in Cortex-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 4 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]). The block diagram is shown in the Figure 5.4-3.

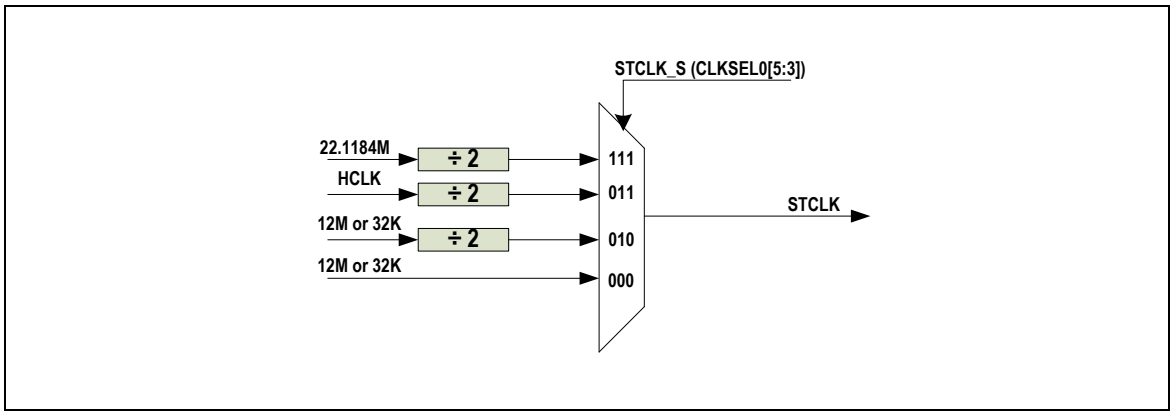


Figure 5.4-3 SysTick clock Control Block Diagram

5.4.4 AHB Clock Source Select

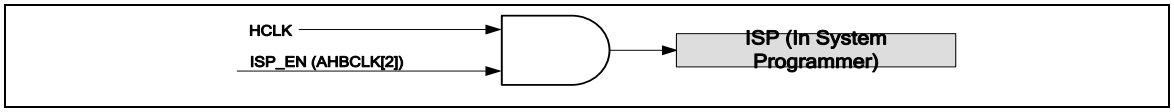


Figure 5.4-4 AHB Clock Source for HCLK

5.4.5 Peripherals Clock Source Select

The peripherals clock had different clock source switch setting which depends on the different peripheral. Please refer the CLKSEL1 & APBCLK register description in chapter **Error! Reference source not found.**.

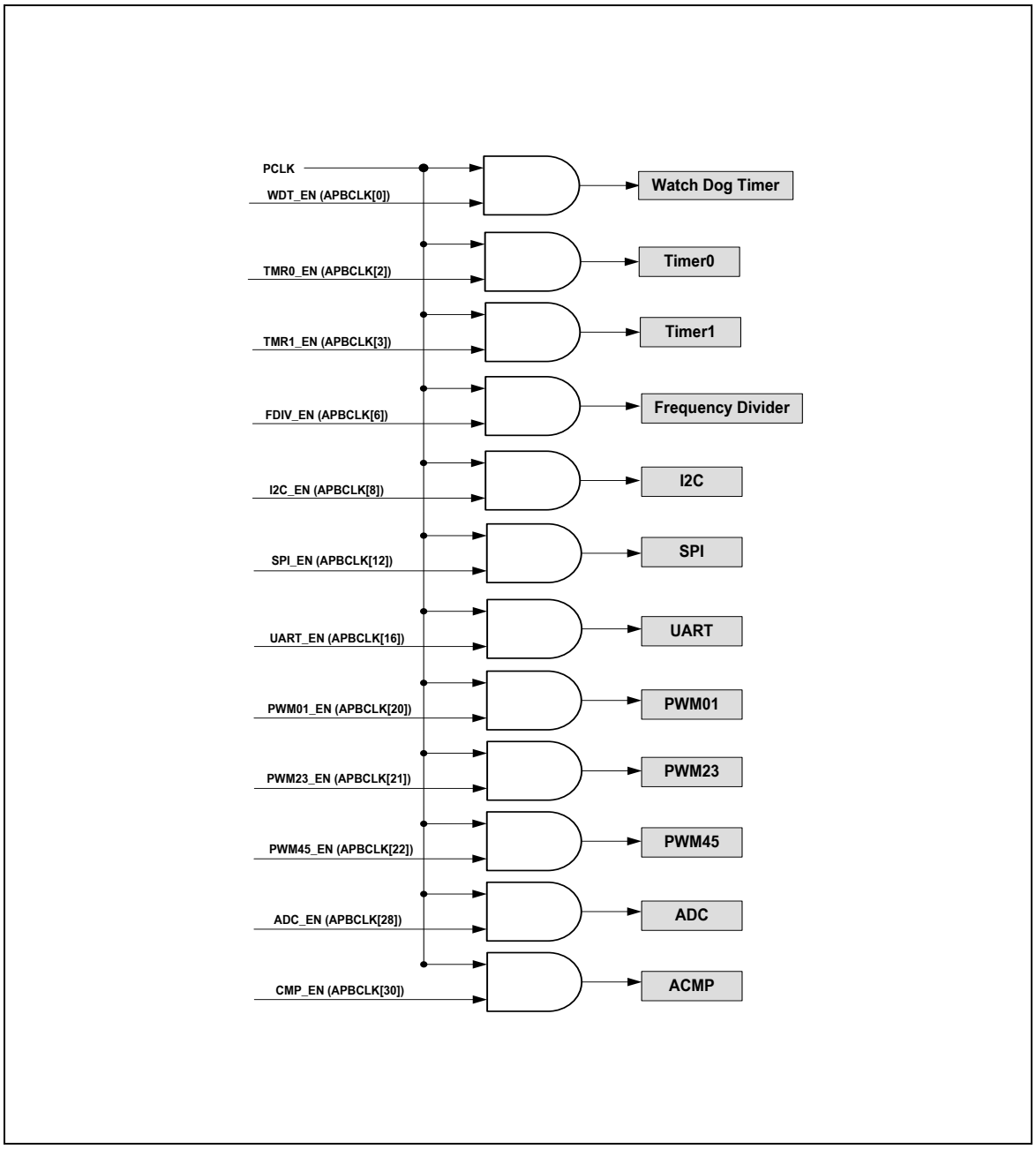


Figure 5.4-5 Peripherals Clock Source Select for PCLK

	Ext. CLK (12M or 32K)	IRC22.1184M	IRC10K	PCLK
WDT	Yes	No	Yes	Yes
Timer0	Yes	Yes	Yes	Yes
Timer1	Yes	Yes	Yes	Yes
I^2C	No	No	No	Yes
SPI	No	No	No	Yes
UART	Yes	Yes	No	No
PWM	No	No	No	Yes
ADC	Yes	Yes	No	Yes
ACMP	No	No	No	Yes

Table 5.4-1 Peripherals engine Clock Source Selection table

5.4.6 Power Down Mode Clock

When enter into Power Down Mode, some clock sources and peripherals clock and system clock will be disable. Some clock sources and peripherals clock are still active in power down mode.

For theses clocks which still keep active list below:

- Clock Generator
  - Internal 10 KHz RC oscillator (LIRC) clock
  - External 32.768 KHz crystal oscillator (LXT) clock (If PD_32K = "1" and XTLCLK_EN[1:0] = "10")
- Peripherals Clock (When these IP adopt 10 KHz as clock source)
  - Watchdog Clock
  - Timer 0/1 Clock

5.4.7 Frequency Divider Output

This device is equipped a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to P3.6. Therefore there are 16 options of power-of-2 divided clocks with the frequency from Fin/21 to Fin/217 where Fin is input clock frequency to the clock divider.

The output formula is Fout = Fin/2(N+1), where Fin is the input clock frequency, Fout is the clock divider output frequency and N is the 4-bit value in FREQDIV.FSEL[3:0].

When FREQDIV.FDIV_EN[4] is set to high, the rising transition will reset the chained counter and starts it counting. When FREQDIV.FDIV_EN[4] is written with a zero, the chained counter continuously runs till divided clock reaches low state and stay in low state.

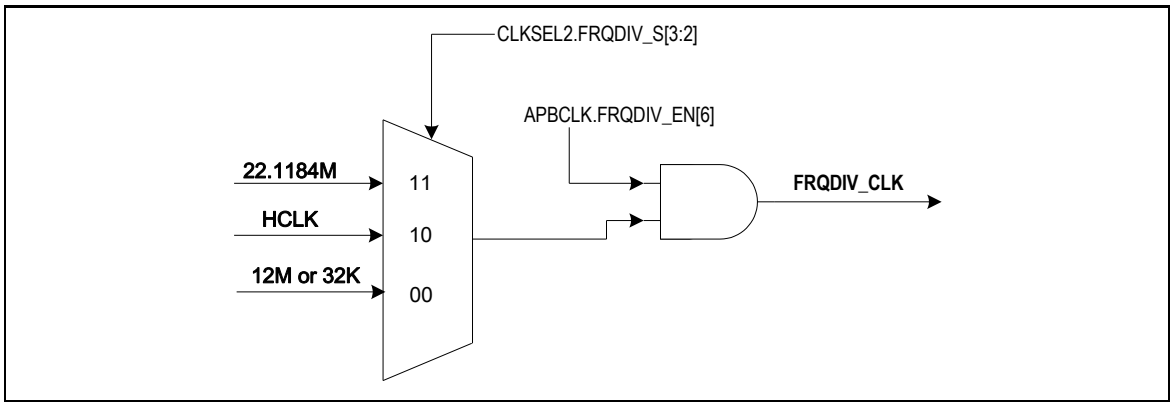


Figure 5.4-6 Clock Source of Frequency Divider

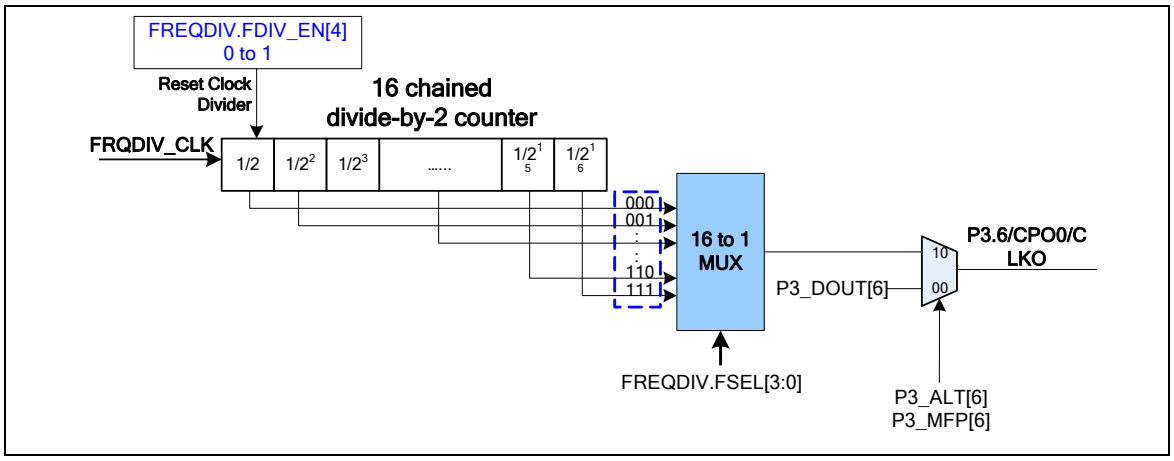


Figure 5.4-7 Block Diagram of Frequency Divider

5.5 Analog Comparator (CMP)

5.5.1 Overview

NuMicro Mini51™ Series contains two comparators. The comparators can be used in a number of different configurations. The comparator output is a logical one when positive input greater than negative input, otherwise the output is a zero. Each comparator can be configured to cause an interrupt when the comparator output value changes. The block diagram is shown in **Error! Reference source not found.**.

Note that the analog input port pins must be configured as input type before Analog Comparator function is enabled.

5.5.2 Features

- Analog input voltage range: 0 ~ 5.0 V
- Hysteresis function supported
- Two analog comparators with optional internal reference voltage input at negative end
- One comparator interrupt requested by either comparator

5.6 Analog-to-Digital Converter (ADC)

5.6.1 Overview

NuMicro Mini51™ series contain one 10-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 input channels. The A/D converters can be started by software and external STADC/P3.2 pin.

Note that the analog input pins must be configured as input type before ADC function is enabled.

5.6.2 Features

- Analog input voltage range: 0 ~ Vref (Max to 5.0 V)
- 10-bit resolution and 8-bit accuracy is guaranteed
- Up to 8 single-end analog input channels
- Maximum ADC clock frequency is 6 MHz
- Up to 150K SPS conversion rate
- A/D conversion is performed one time on a specified channel
- An A/D conversion can be started by
  - Software write “1” to ADST bit
  - External pin STADC
- Conversion results are held in data register with valid and overrun indicators
- Conversion result can be compared with specify value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting
- Channel 7 supports 2 input sources: external analog voltage and internal fixed band-gap voltage

5.7 FLASH Memory Controller (FMC)

5.7.1 Overview

NuMicro Mini51™ series equips with 4K/8K/16K bytes on chip embedded Flash EPROM for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip power on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, NuMicro Mini51™ series also provide DATA Flash Region, the data flash is shared with original program memory and its start address is configurable and defined by user in Config1. The data flash size is defined by user depends on her application request.

5.7.2 Features

- AHB interface compatible
- Run up to 24 MHz with zero wait state for discontinuous address read access
- 4K/8K/16KB application program memory (APROM)
- 2KB in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address and memory size with 512 bytes page erase unit
- In System Program (ISP) to update on chip Flash EPROM

5.8 General Purpose I/O

5.8.1 Overview

There are 30 General Purpose I/O pins shared with special feature functions in this MCU. The 30 pins are arranged in 6 ports named with P0, P1, P2, P3, P4 and P5. Each one of the 30 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be independently software configured as input, output, open-drain, or quasi-bidirectional mode. After reset, the I/O type of all pins stay in input mode and port data register Px_DOUT[n] resets to "1". For Quasi bi-direction mode, each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for VDD is from 5.0V to 2.5V.

5.8.2 Features

- Four I/O modes:
  - Quasi bi-direction
  - Push-Pull output
  - Open-Drain output
  - Input-only with high impendence
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- High driver and high sink IO mode support

5.9 I²C Serial Interface Controller (Master/Slave)

5.9.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. Serial, 8-bit oriented bi-directional data transfers can be made up 1.0 Mbps.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to the following figure for more detail I²C BUS Timing.

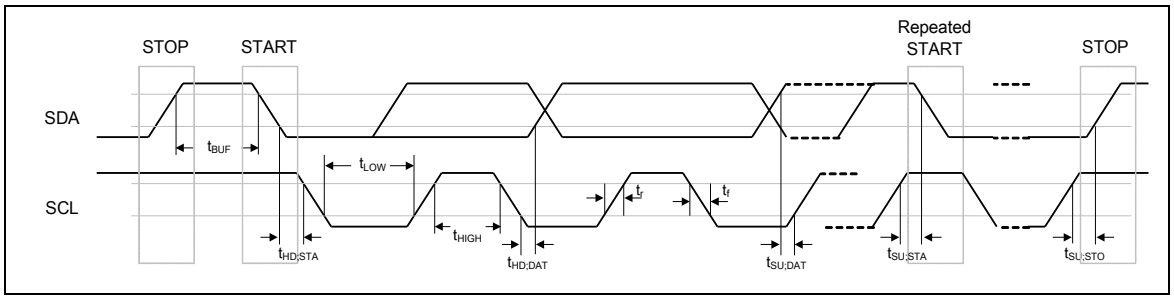


Figure 5.9-1 Bus Timing

The device's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. To enable this port, the bit ENSI in I2CON should be set to "1". The I²C H/W interfaces to the I²C bus via two pins: SDA (P3.4, serial data line) and SCL (P3.5, serial clock line). Pull-up resistor is needed for Pin P3.4 and P3.5 for I²C operation as these are open-drain pins. When the I/O pins are used as I²C port, user must set the pins function to I²C in advance.

5.9.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the bus are:

- Master/Slave mode up to 1 Mbit/s
- Bi-directional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer

- Built-in a 14-bit time-out counter will request the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
- External pull-up are needed for higher output pull-up speed
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- I^2C-bus controllers support multiple address recognition (four slave address with mask option)

5.10 Enhanced PWM Generator

5.10.1 Overview

NuMicro Mini51™ series has built-in one PWM unit which function is specially designed for motor driving control applications. The PWM unit supports 6 PWM Generators which can be configured as 6 independent PWM outputs, PWM0~PWM5, or as 3 complementary PWM pairs, (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5) with 3 programmable dead-zone generators.

Each PWM Generator share the 8-bit prescaler, clock divider providing 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16). Each PWM output has independent 16-bit counter for PWM period control, and 16-bit comparators for PWM duty control. The 6 PWM Generators provide six independent PWM interrupt flags which are set by hardware when the corresponding PWM period counter comparison matched. Each PWM interrupt source with its corresponding enable bit can cause to request PWM interrupt. The PWM Generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

5.10.2 Features

The PWM unit supports the following features:

- Six independent 16-bit PWM duty control units with maximum 6 port pins:
  - 6 independent PWM outputs – PWM0, PWM1, PWM2, PWM3, PWM4, and PWM5
  - 3 complementary PWM pairs, with each pin in a pair mutually complement to each other and capable of programmable dead-zone insertion – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
  - 3 synchronous PWM pairs, with each pin in a pair in-phase – (PWM0, PWM1), (PWM2, PWM3) and (PWM4, PWM5)
- Group control bit – PWM2 and PWM4 are synchronized with PWM0
- One-shot (only support edge alignment mode) or Auto-reload mode PWM
- Up to 16 bits resolution
- Support Edge aligned and Center aligned mode
- Programmable dead-zone insertion between complementary paired PWMs
- Each pin of PWM0 to PWM5 has independent polarity setting control
- Hardware fault brake protections
  - 2 Interrupt source types:
    - Interrupt is synchronously requested at PWM frequency when down counter comparison matched (edge and center aligned modes) or underflow (edge aligned mode)
    - Interrupt is requested when external fault brake asserted
      - BKP0: EINT0
      - BKP1: EINT1 or CPO0
- The PWM signals before polarity control stage are defined in the view of positive logic. The PWM ports is active high or active low are controlled by polarity control register.

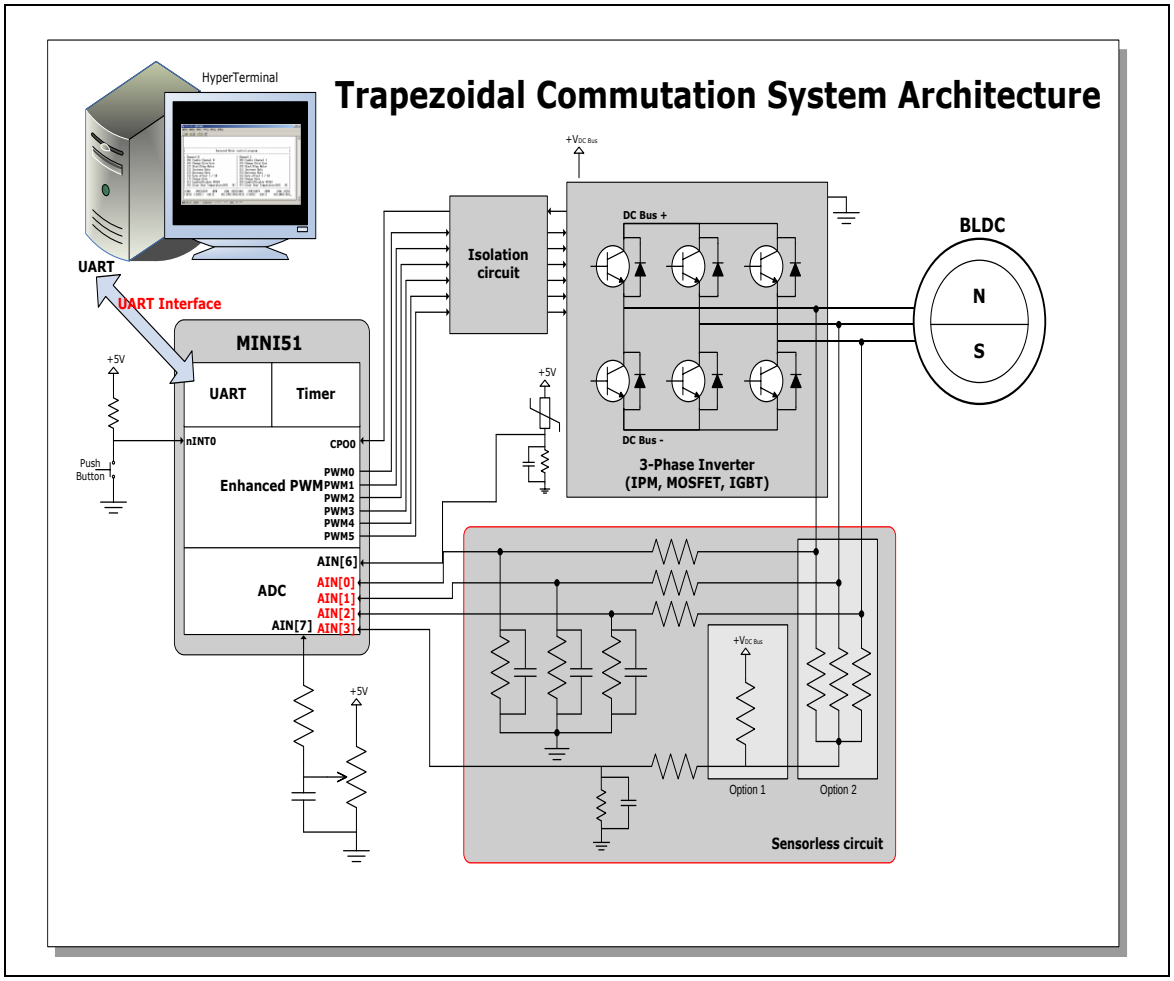


Figure 5.10-1 Application circuit diagram

5.11 Serial Peripheral Interface (SPI) CONTROLLER

5.11.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in master/slave mode with 4-wire bi-direction interface. NuMicro Mini51™ series contain one set of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. SPI controller can be set as a master; it also can be set as a slave controlled by an off-chip master device.

5.11.2 Features

- Support master or slave mode operation
- MSB or LSB first transfer
- Byte or word Suspend Mode
- Variable output serial clock frequency in master mode
- Support two programmable serial clock frequencies in master mode

5.12 Timer Controller

5.12.1 Overview

The timer module includes two channels, TIMER0~TIMER1, which allow user to easily implement a timer control for applications. The timer can perform functions like frequency measurement, interval measurement, clock generation, delay timing, and so on. The timer can generate an interrupt signal upon time-out, or provide the current value of count during operation.

5.12.2 Features

- 2 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each channel (TMR0_CLK, TMR1_CLK)
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time out period = (period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- Internal 24-bit up timer is readable through TDR (Timer Data Register)
- Support event counting function to count the event from external pin
- Support input capture function to capture or reset counter value

5.13 UART Interface Controller

NuMicro Mini51™ series provides one channel of Universal Asynchronous Receiver/Transmitters (UART). UART perform Normal Speed UART, and support flow control function.

5.13.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU. The UART controller also supports IrDA SIR Function, and RS-485 mode functions. Each UART channel supports six types of interrupts including transmitter FIFO empty interrupt (INT_THRE), receiver threshold level reaching interrupt (INT_RDA), line status interrupt (parity error or framing error or break interrupt) (INT_RLS), receiver buffer time out interrupt (INT_TOUT), MODEM/Wakeup status interrupt (INT_MODEM), and Buffer error interrupt (INT_BUF_ERR). Interrupt number 12 (vector number is 28) supports UART interrupt. Refer to Nested Vectored Interrupt Controller chapter for System Interrupt Map.

The UART is built-in with a 16-byte transmitter FIFO (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU and the CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data. The UART includes a programmable baud rate generator that is capable of dividing crystal clock input by divisors to produce the clock that transmitter and receiver need. The baud rate equation is Baud Rate = UART_CLK / M * [BRD + 2], where M and BRD are defined in Baud Rate Divider Register (UA_BAUD). Below table lists the equations in the various conditions and the UART baud rate setting table.

Table 5.13-1 UART Baud Rate Setting Table

Mode	DIV_X_EN	DIV_X_ONE	Divider X	BRD	Baud Rate Equation
0	0	0	B	A	UART_CLK / [16 * (A+2)]
1	1	0	B	A	UART_CLK / [(B+1) * (A+2)] , B must >= 8
2	1	1	Don't care	A	UART_CLK / (A+2), A must >=3

Table 5.13-2 UART Baud Rate Setting Table

System clock = 22.1184 MHz			
Baud rate	Mode0	Mode1	Mode2
921600	Not Support	A=0,B=11	A=22
460800	A=1	A=1,B=15 A=2,B=11	A=46
230400	A=4	A=4,B=15 A=6,B=11	A=94
115200	A=10	A=10,B=15	A=190

		A=14,B=11	
57600	A=22	A=22,B=15 A=30,B=11	A=382
38400	A=34	A=62,B=8 A=46,B=11 A=34,B=15	A=574
19200	A=70	A=126,B=8 A=94,B=11 A=70,B=15	A=1150
9600	A=142	A=254,B=8 A=190,B=11 A=142,B=15	A=2302
4800	A=286	A=510,B=8 A=382,B=11 A=286,B=15	A=4606

5.13.1.1 Auto-Flow Control

The UART controller support auto-flow control function that uses two low-level signals, CTSn (clear-to-send) and RTSn (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts RTSn to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR[19:16]), the RTSn is de-asserted. The UART sends data out when UART controller detects CTSn is asserted from external device. If a validly asserted CTSn is not detected the UART controller will not send data out.

5.13.1.2 IrDA Function Mode

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (User must set IrDA_EN (UA_FUN_SEL[1:0]) to enable IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception. This delay feature must be implemented by software.

5.13.1.3 RS-485 Function Mode

Another alternate function of UART controllers is RS-485 9 bit mode function, and direction control provided by RTSn pin or can program GPIO (P0.1 for RTSn) to implement the function by software. The RS-485 mode is selected by setting the UA_FUN_SEL register to select RS-485 function. The RS-485 driver control is implemented using the RTSn control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are same as UART.

5.13.2 Features

- Full duplex, asynchronous communications
- Separate receive / transmit 16 bytes entry FIFO for data payloads
- Support hardware auto flow control/flow control function (CTSn, RTSn) and programmable RTSn flow control trigger level
- Programmable receiver buffer trigger level
- Support programmable baud-rate generator for each channel individually
- Support CTSn wake-up function
- Support 7-bit receiver buffer time out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR[DLY] register
- Support break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5, 6, 7, 8 character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Support IrDA SIR function mode
  - Support for 3/16-bit duration for normal mode
- Support RS-485 function mode
  - Support RS-485 9-bit mode
  - Support hardware or software controls RTSn or software control GPIO to control transfer direction

5.14 Watchdog Timer

5.14.1 Overview

The purpose of Watchdog Timer is to perform a system reset after the software running into a problem. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports another function to wakeup CPU from power-down mode. The watchdog timer includes an 18-bit free running counter with programmable time-out intervals. Below table show the watchdog timeout interval selection and following figure shows the timing of watchdog interrupt signal and reset signal.

Setting WTE (WTCR[7]) enables the watchdog timer and the WDT counter starts counting up. When the counter reaches the selected time-out interval, Watchdog timer interrupt flag WTIF will be set immediately to request a WDT interrupt if the watchdog timer interrupt enable bit WTIE is set, in the meanwhile, a specified delay time (1024 * TWDT) follows the time-out event. User must set WTR (WTCR[0]) (Watchdog timer reset) high to reset the 18-bit WDT counter to avoid CPU from Watchdog timer reset before the delay time expires. WTR bit is cleared automatically by hardware after WDT counter is reset. There are eight time-out intervals with specific delay time which are selected by Watchdog timer interval select bits WTIS (WTCR[10:8]). If the WDT counter has not been cleared after the specific delay time expires, the watchdog timer will set Watchdog Timer Reset Flag (WTRF) high and reset CPU. This reset will last 63 WDT clocks (TRST) then CPU restarts executing program from reset vector (0x0000_0000). WTRF will not be cleared by Watchdog reset. User may poll WTRF by software to recognize the reset source. WDT also provides wakeup function. When chip is powered down and the Watchdog Timer Wakeup Function Enable bit (WTCR[4]) is set, if the WDT counter has not been cleared after the specific delay time expires, the chip will be waked up from power down state.

WTIS	WTR Timeout Interval T_{TIS}	Interrupt Period T_{INT}	WTR Timeout Interval (WDT_CLK = 10 KHz) T_{TIS}	WTR Reset Interval (WDT_CLK = 10 KHz) T_{WTR}
000	$2^4 * T_{WDT}$	$1024 * T_{WDT}$	1.6 ms	104 ms
001	$2^6 * T_{WDT}$	$1024 * T_{WDT}$	6.4 ms	108.8 ms
010	$2^8 * T_{WDT}$	$1024 * T_{WDT}$	25.6 ms	128 ms
011	$2^{10} * T_{WDT}$	$1024 * T_{WDT}$	102.4 ms	204.8 ms
100	$2^{12} * T_{WDT}$	$1024 * T_{WDT}$	407 ms	512 ms
101	$2^{14} * T_{WDT}$	$1024 * T_{WDT}$	1.638 s	1.741 s
110	$2^{16} * T_{WDT}$	$1024 * T_{WDT}$	6.553 s	6.6.656 s
111	$2^{18} * T_{WDT}$	$1024 * T_{WDT}$	26.214 s	26.316 s

Table 5.14-1 Watchdog Timeout Interval Selection

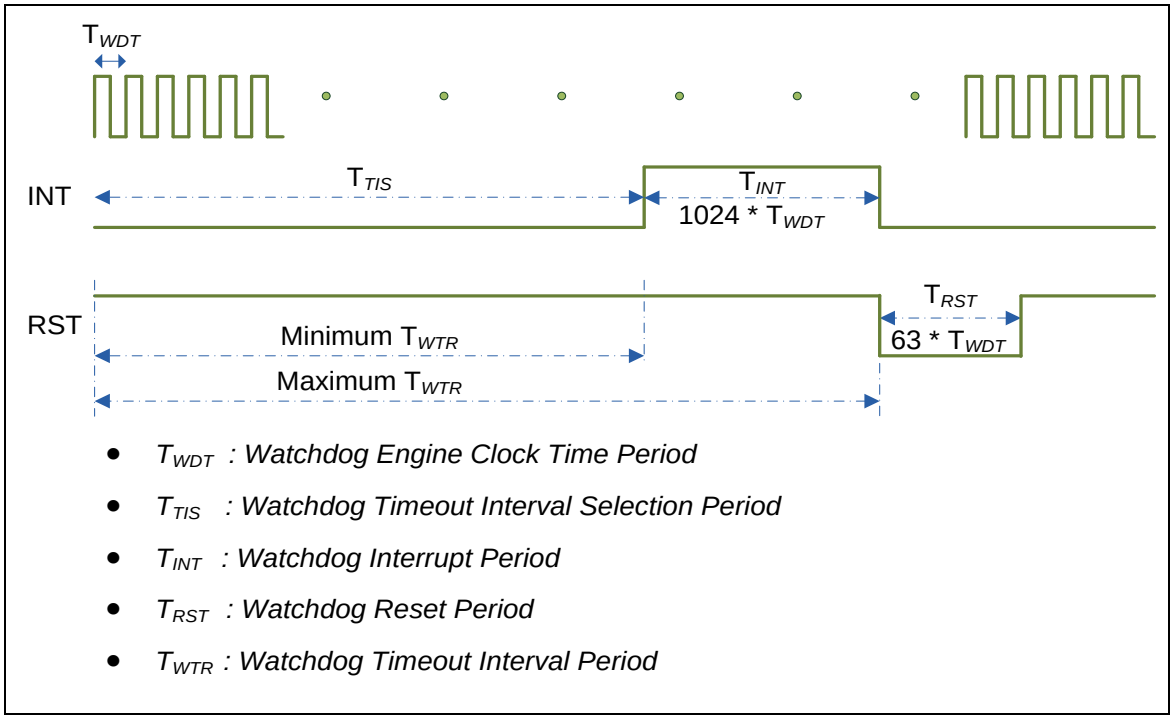


Figure 5.14-1 Timing of Interrupt and Reset Signal

5.14.2 Features

- 18-bit free running counter to avoid CPU from Watchdog timer reset before the delay time expires.
- Selectable time-out interval (24 ~ 218) and the time out interval is 104 ms ~ 26.3168 s (if WDT_CLK = 10 KHz).
- Reset period = (1 / 10 KHz) * 63, if WDT_CLK = 10 KHz.

6 ARM® CORTEX™-M0 CORE

6.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes - Thread and Handler modes. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional controller of processor.

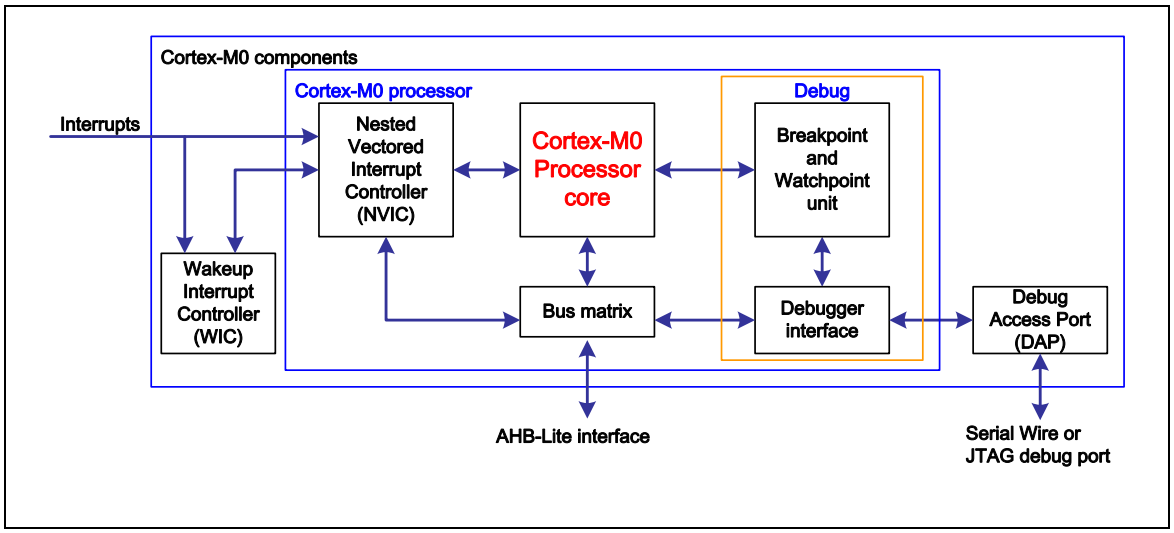


Figure 6.1-1 Functional Block Diagram

6.2 Feature

- A low gate count processor that features:
  - The ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - The system interface supports little-endian data accesses
  - The ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model

    This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power Idle Mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC that features:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated non-Maskable Interrupt (NMI) input
  - Support for both level-sensitive and pulse-sensitive interrupt lines
  - Wake-up Interrupt Controller (WIC), providing ultra-low power Idle Mode support
- Debug support
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.3 System Timer (SysTick)

The Cortex-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

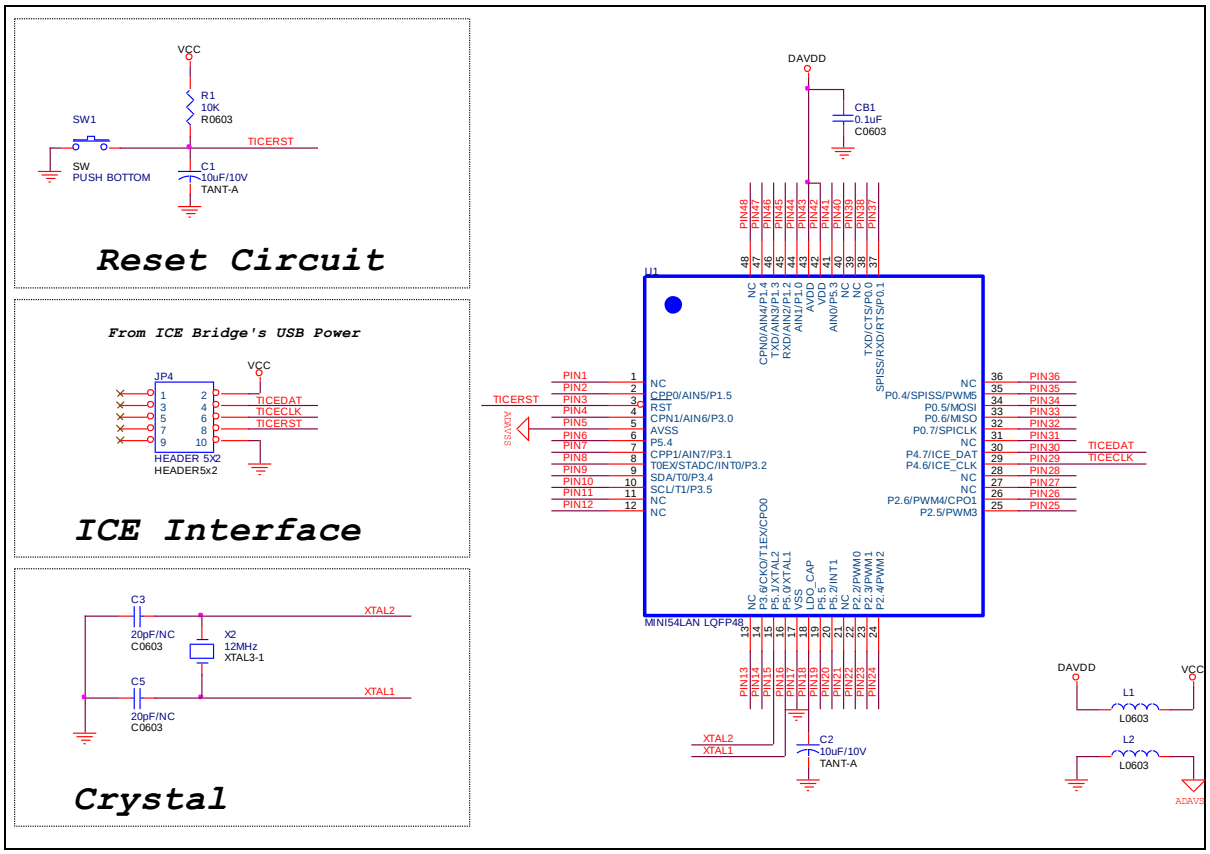
When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

7 APPLICATION CIRCUIT



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

8.2 DC Electrical Characteristics

(VDD-VSS=5.0 V, TA = 25°C, FOSC = 24 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5 V ~ 5.5 V up to 24 MHz
Power Ground	V_{SS} AV_{SS}	-0.3			V	
LDO Output Voltage	V_{LDO}	-10%	1.8	+10%	V	V_{DD} = 2.5V ~ 5.5V
Analog Operating Voltage	AV_{DD}	0		V_{DD}	V	
Operating Current Normal Run Mode @ 24 MHz	I_{DD1}		9.5		mA	V_{DD} = 5.5V@24 MHz, enable all IP
	I_{DD2}		7.5		mA	V_{DD} = 5.5V@24 MHz, disable all IP
	I_{DD3}		7.5		mA	V_{DD} = 3.3V@24 MHz, enable all IP
	I_{DD4}		6		mA	V_{DD} = 3.3V@24 MHz, disable all IP
Operating Current Normal Run Mode @ 12 MHz	I_{DD5}		5.5		mA	V_{DD} = 5.5V@12 MHz, enable all IP
	I_{DD6}		4.5		mA	V_{DD} = 5.5V@12 MHz, disable all IP
	I_{DD7}		4		mA	V_{DD} = 3.3V@12 MHz, enable all IP
	I_{DD8}		3		mA	V_{DD} = 3.3V@12 MHz, disable all IP
Operating Current Normal Run Mode @ 4 MHz	I_{DD9}		3.6		mA	V_{DD} = 5.5V@4 MHz, enable all IP
	I_{DD10}		3.3		mA	V_{DD} = 5.5V@4 MHz, disable all IP
	I_{DD11}		1.7		mA	V_{DD} = 3.3V@4 MHz, enable all IP
	I_{DD12}		1.4		mA	V_{DD} = 3.3V@4 MHz, disable all IP
Operating Current Normal Run Mode @ 22.1184 MHz IRC	I_{DD13}		6.6		mA	V_{DD} = 5.5V@22.1184 MHz, enable all IP
	I_{DD14}		5		mA	V_{DD} = 5.5V@22.1184 MHz, disable all IP
	I_{DD15}		6.6		mA	V_{DD} = 3.3V@22.1184 MHz, enable all IP
	I_{DD16}		5		mA	V_{DD} = 3.3V@22.1184 MHz, disable all IP

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Normal Run Mode @ 32.768 KHz crystal oscillator	I_{DD17}		116		μA	V_{DD} = 5.5V@32.768 KHz, enable all IP
	I_{DD18}		113		μA	V_{DD} = 5.5V@32.768 KHz, disable all IP
	I_{DD19}		112		μA	V_{DD} = 3.3V@32.768 KHz, enable all IP
	I_{DD20}		100		μA	V_{DD} = 3.3V@32.768 KHz, disable all IP
Operating Current Normal Run Mode @ 10 KHz IRC	I_{DD21}		109		μA	V_{DD} = 5.5V@10 KHz, enable all IP
	I_{DD22}		108		μA	V_{DD} = 5.5V@10 KHz, disable all IP
	I_{DD23}		100		μA	V_{DD} = 3.3V@10 KHz, enable all IP
	I_{DD24}		98		μA	V_{DD} = 3.3V@10 KHz, disable all IP
Operating Current Idle Mode @ 24 MHz	I_{IDLE1}		5.5		mA	V_{DD} = 5.5V@24 MHz, enable all IP
	I_{IDLE2}		3.5		mA	V_{DD} = 5.5V@24 MHz, disable all IP
	I_{IDLE3}		3.8		mA	V_{DD} = 3.3V@24 MHz, enable all IP
	I_{IDLE4}		1.8		mA	V_{DD} = 3.3V@24 MHz, disable all IP
Operating Current Idle Mode @ 12 MHz	I_{IDLE5}		3.3		mA	V_{DD} = 5.5V@12 MHz, enable all IP
	I_{IDLE6}		2.6		mA	V_{DD} = 5.5V@12 MHz, disable all IP
	I_{IDLE7}		2		mA	V_{DD} = 3.3V@12 MHz, enable all IP
	I_{IDLE8}		1		mA	V_{DD} = 3.3V@12 MHz, disable all IP
Operating Current Idle Mode @ 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5.5V@4 MHz, enable all IP
	I_{IDLE10}		2.3		mA	V_{DD} = 5.5V@4 MHz, disable all IP
	I_{IDLE11}		1		mA	V_{DD} = 3.3V@4 MHz, enable all IP
	I_{IDLE12}		0.7		mA	V_{DD} = 3.3V@4 MHz, disable all IP
Operating Current Idle Mode @ 22.1184 MHz IRC	I_{IDLE13}		3.0		mA	V_{DD} = 5.5V@22.1184 MHz, enable all IP
	I_{IDLE14}		1.2		mA	V_{DD} = 5.5V@22.1184 MHz, disable all IP
	I_{IDLE15}		3.0		mA	V_{DD} = 3.3V@22.1184 MHz, enable all IP

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{IDLE16}		1.2		mA	V_{DD} = 3.3V@22.1184 MHz, disable all IP
Operating Current Idle Mode @ 32.768 KHz crystal oscillator	I_{IDLE17}		110		μA	V_{DD} = 5.5V@32.768 KHz, enable all IP
	I_{IDLE18}		107		μA	V_{DD} = 5.5V@32.768 KHz, disable all IP
	I_{IDLE19}		105		μA	V_{DD} = 3.3V@32.768 KHz, enable all IP
	I_{IDLE20}		102		μA	V_{DD} = 3.3V@32.768 KHz, disable all IP
Operating Current Idle Mode @ 10 KHz IRC	I_{IDLE21}		103		μA	V_{DD} = 5.5V@10 KHz, enable all IP
	I_{IDLE22}		102		μA	V_{DD} = 5.5V@10 KHz, disable all IP
	I_{IDLE23}		96		μA	V_{DD} = 3.3V@10 KHz, enable all IP
	I_{IDLE24}		95		μA	V_{DD} = 3.3V@10 KHz, disable all IP
Standby Current Power Down Mode	I_{PWD1}		10		μA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF
	I_{PWD2}		5		μA	V_{DD} = 3.3V, CPU STOP All IP and Clock OFF
Standby Current Power Down Mode with 32.768 KHz crystal enable	I_{PWD3}		12		μA	V_{DD} = 5.0V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
	I_{PWD4}		7		μA	VDD = 3.3V, CPU STOP All IP and Clock OFF except 32.768KHz crystal oscillator
Input Current P0~P5 (Quasi-bidirectional mode)	I_{IN1}		-50	-60	μA	V_{DD} = 5.5 V, V_{IN} = 0 V or V_{IN}=V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3 V, V_{IN} = 0.45 V
Input Leakage Current PA, PB, PC, PD, PE	I_{LK}	-0.1	-	+0.1	μA	V_{DD} = 5.5 V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current PA~PE (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5 V, V_{IN}<2.0 V
Input Low Voltage P0~P5 (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input High Voltage P0~P5 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0 V
Input Low Voltage P0~P5, (Schmitt input)	V_{IL2}		0.4 V_{DD}		V	
Input High Voltage P0~P5, (Schmitt input)	V_{IH2}		0.6 V_{DD}		V	
Hysteresis voltage of P0~P5 (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 3.0 V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0 V
Internal /RESET pin pull up resistor	R_{RST}	40	-	100	KΩ	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.6 V_{DD}	-	V_{DD}+0.5	V	
Source Current P0~P5. (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	µA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR12}	-50	-70	-90	µA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR12}	-40	-60	-80	µA	V_{DD} = 2.5 V, V_S = 2.0 V
Source Current P0~P5, (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5 V, V_S = 2.0 V
Sink Current P0~P5, (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5 V, V_S = 0.45 V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7 V, V_S = 0.45 V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5 V, V_S = 0.45 V

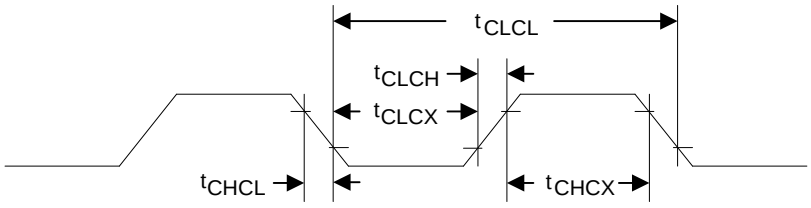
Note:

1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of P0~P5 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, the transition current reaches its maximum value when V_{IN} approximates to 2 V.

8.3 AC ELECTRICAL CHARACTERISTICS

8.3.1 External Input Clock

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	20			nS	
Clock Low Time	t_{CLCX}	20			nS	
Clock Rise Time	t_{CLCH}			10	nS	
Clock Fall Time	t_{CHCL}			10	nS	



Note: Duty cycle is 50%.

8.3.2 External 4~24 MHz XTAL Oscillator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{HXTAL}	4	12	24	MHz	VDD = 2.5V ~ 5.5V
Temperature	T_{HXTAL}	-40		+85	°C	
Operating current	I_{HXTAL}		TBD		mA	VDD = 5.0V

8.3.3 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	Optional (Depend on crystal specification)	

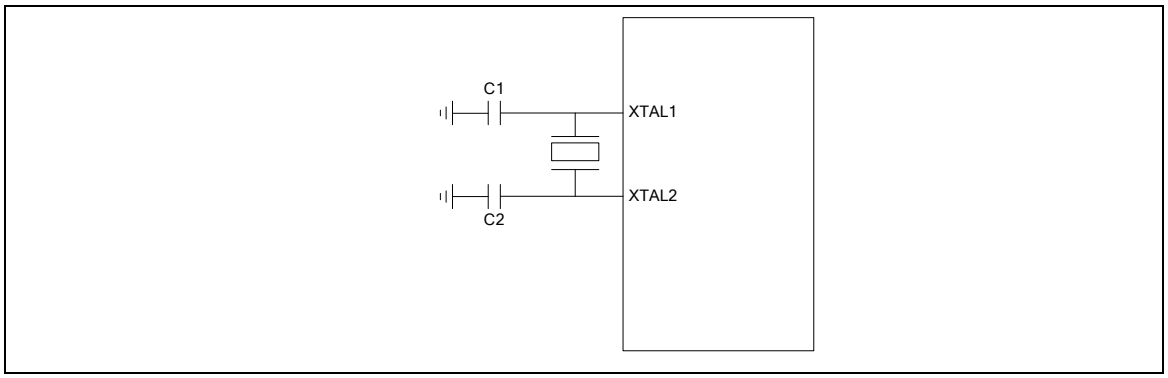


Figure 8.3-1 Typical Crystal Application Circuit

8.3.4 External 32.768 KHz XTAL Oscillator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	fL_{XTAL}		32.768		KHz	VDD = 2.5V ~ 5.5V
Temperature	TL_{XTAL}	-40		+85	°C	
Operating current	I_{HXTAL}		TBD		μA	VDD = 5.0V

8.3.5 Internal 22.1184 MHz RC Oscillator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{HRC}		1.8		V	
Center Frequency	F_{HRC}	21.89	22.1184	22.34	MHz	25°C, VDD = 5V
		20.57	22.1184	23.23	MHz	-40°C~+85 °C, VDD = 2.5V~5.5V
		21.78	22.0	22.22	MHz	-40°C~+85 °C, VDD = 2.5V~5.5V Enable 32.768K crystal oscillator and set TRIM_SEL = 1
Operating current	I_{HRC}		TBD		mA	

Note: Internal operation voltage comes from LDO

8.3.6 Internal 10 KHz RC Oscillator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{LRC}		1.8		V	
Center Frequency	F_{LRC}	7	10	13	KHz	25°C, VDD = 5V
		5	10	15	KHz	-40°C~+85 °C, VDD = 2.5V~5.5V
Operating current	I_{LRC}		TBD		μA	VDD = 5V

Note: Internal operation voltage comes from LDO

.

8.4 Analog Characteristics

(VDD-VSS=5.0 V, TA = 25°C, FOSC = 24 MHz unless otherwise specified.)

8.4.1 Specification of Brown-Out Reset (BOD)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{BOD}	2.0		5.5	V	
Operating current	I_{BOD}		5	15	μA	VDD = 5V Enable BOD27 and BOD38
BOD38 detection level	V_{B38dt}	3.6	3.8	4.0	V	25°C
BOD27 detection level	V_{B27dt}	2.6	2.7	2.8	V	25°C

8.4.2 Specification of Low Voltage Reset (LVR)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{BOD}	2.0		5.5	V	
Operating current	I_{BOD}		1	2	μA	
Detection level	V_{LVR}		2.0		V	25°C
LVR always enable		1.6	2.0	2.4	V	-40°C ~ +85°C

8.4.3 Specification of Analog Comparator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{BOD}	2.5	3.3	5.5	V	
Operating current	I_{CMP}		40	80	μA	
Input offset voltage	V_{OFFSET}		10	20	mV	
Output swing voltage	V_{swin}	0.2		V_{DD}-0.2	V	
Input common mode range (VCM)	V_{CM}	0.1		V_{DD}-0.1	V	
DC gain	G_{DC}		70		dB	
Propagation delay	T_{PDLY}		200		ns	VCM = 1.2V The difference voltage in CPPx and CPNx is 0.1V
Hysteresis	V_{HYS}		±10		mV	One bit control W/O & W. hysteresis @V_{CM}=0.2V ~ VDD-0.2V

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Stable time	T_{STBL}			2	μS	CPPx = 1.3V and CPNX = 1.2V

8.4.4 Analog Comparator Reference Voltage (CRV)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{BOD}	2.5		5.5	V	
CRV step size	V_{STEP}		V_{DD}/24		V	VDD = 5V Enable BOD27 and BOD38
CRV output voltage absolute accuracy	A_{CRV}	-5		+5	%	
Unit resistor value	R_{CRV}		2K		ohm	

8.4.5 Specification of 10-bit ADC

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	2.7		5.5	V	AV_{DD} = V_{DD}
Operating current	I_{ADC}			1	mA	AV_{DD} = V_{DD} = 5V, F_{SPS} = 150K
Resolution	R_{ADC}			10	Bit	
Reference voltage	V_{REF}		A_{VDD}		V	V_{REF} connect to A_{VDD} in chip
ADC input voltage	V_{IN}	0		V_{REF}	V	
Conversion time	T_{CONV}	6.7			μS	
Sampling Rate	F_{SPS}	150K			Hz	V_{DD} = 5V, ADC clock = 6MHz Free running conversion
Integral Non-Linearity Error (INL)	INL			±1	LSB	
Differential Non-Linearity (DNL)	DNL			±1	LSB	
Gain error	E_G			±2	LSB	
Offset error	E_{OFFSET}			3	LSB	
Absolute error	E_{ABS}			4	LSB	
ADC Clock frequency	F_{ADC}	100K		6M	Hz	

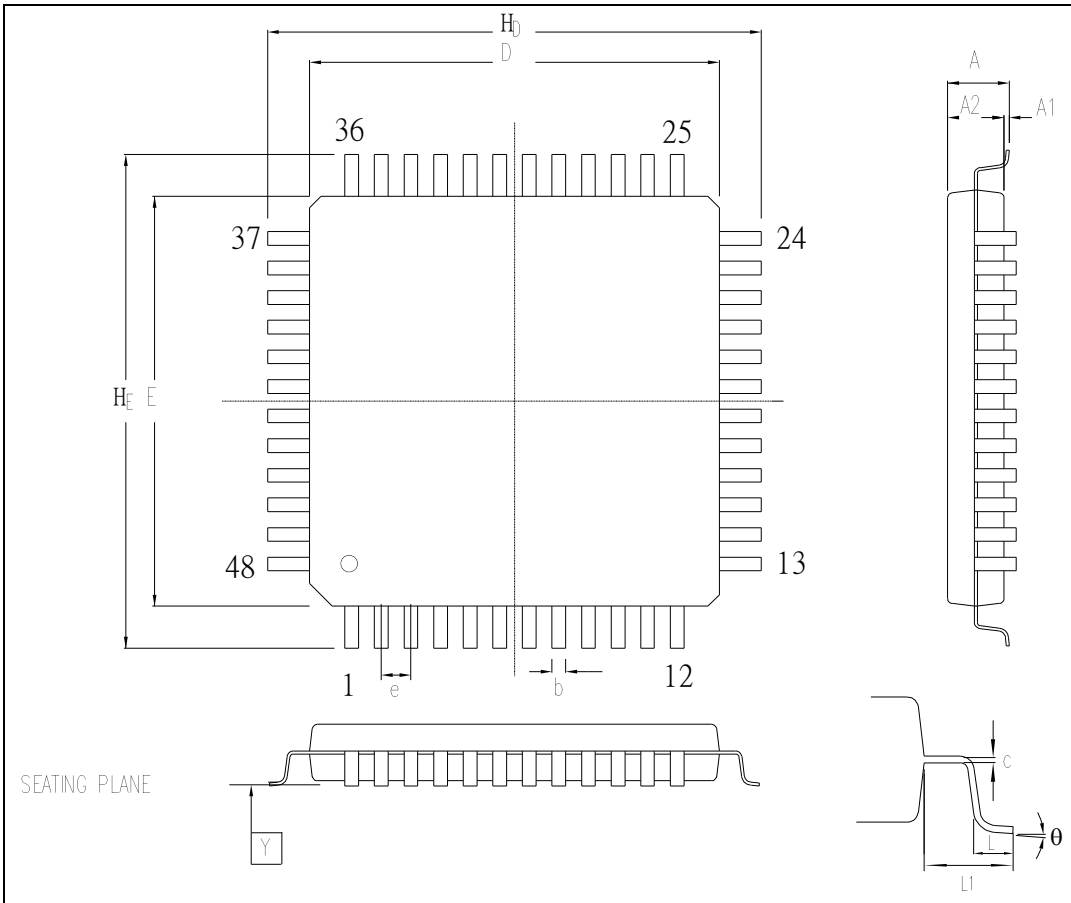
PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Clock cycle	AD_{CYC}	38			Cycle	
Bang-gap voltage	V_{BG}	1.28	1.35	1.42	V	-40°C ~ +85°C

8.4.6 Flash Memory Characteristics

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Cycling (erase / write) Program memory	N_{CYC}	100			K cycle	
Data retention	T_{RET}	10			years	T_A = +85°C
Erase time of ISP mode	T_{ERASE}	2.3	2.5	2.7	mS	Erase time for one page
Program time of ISP mode	T_{PROG}	57	62	67	μS	Programming time for one word
Program current	I_{PROG}		3.3		mA	V_{DD} = 5.5V

9 PACKAGE DIMENSION

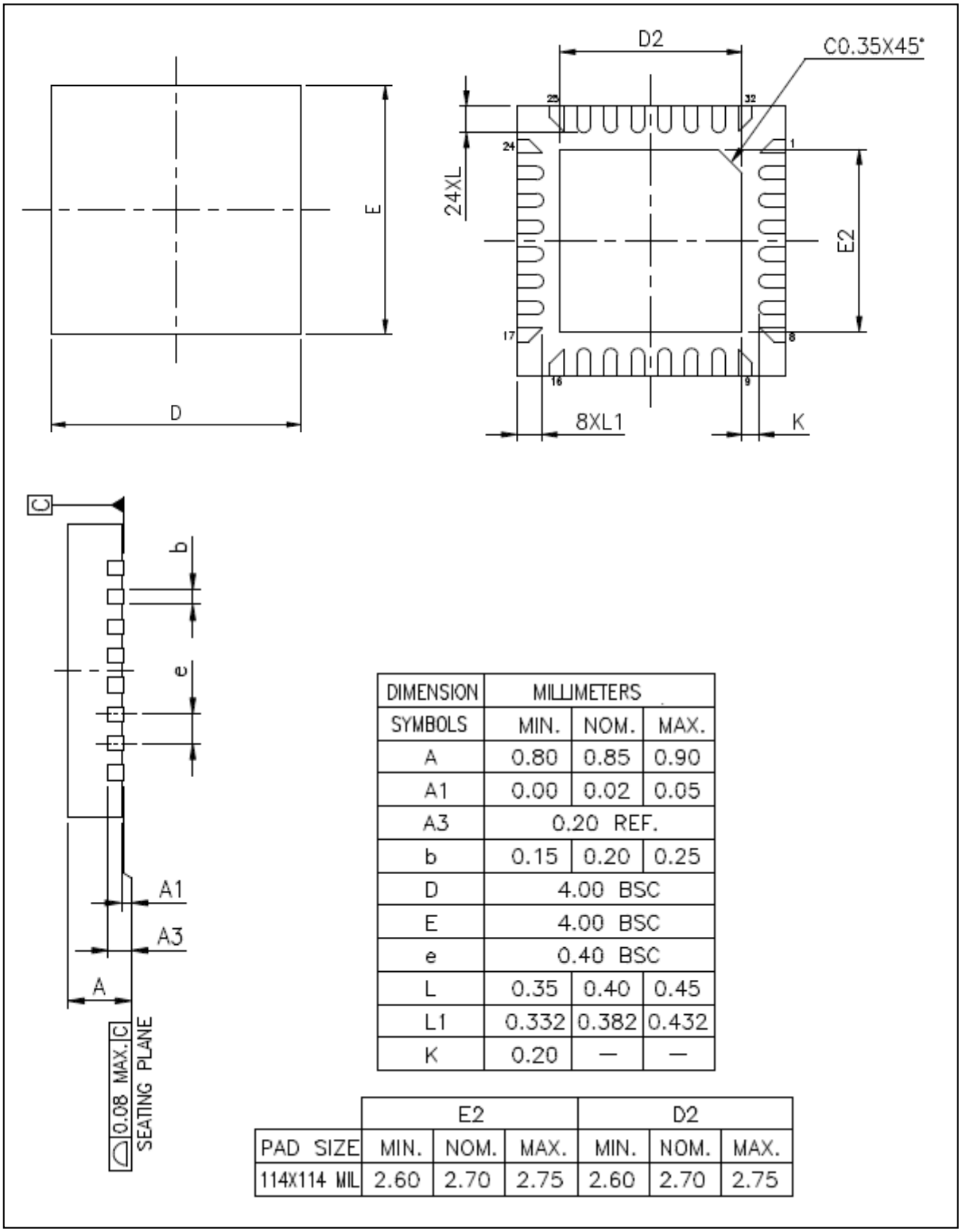
9.1 48-Pin LQFP



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0	—	7	0	—	7

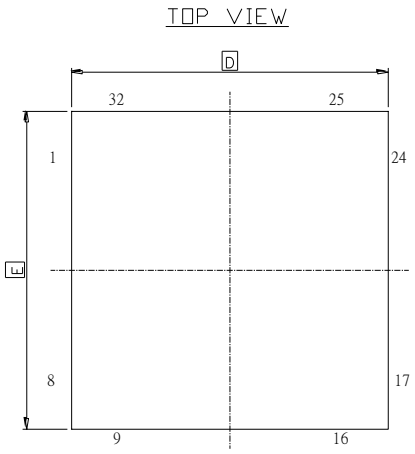
9.2 33-Pin QFN (4mm X 4mm)

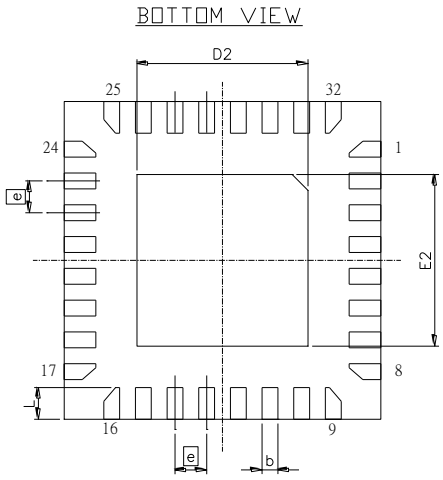


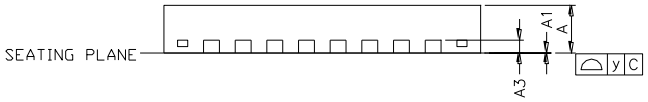
DIMENSION	MILLIMETERS		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
L	0.35	0.40	0.45
L1	0.332	0.382	0.432
K	0.20	—	—

	E2			D2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
114X114 MIL	2.60	2.70	2.75	2.60	2.70	2.75

9.3 33-Pin QFN (5mm X 5mm)







SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

SYMBOL	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
DIMENSION (MM)	3.4	3.5	3.6	3.4	3.5	3.6

10 REVISION HISTORY

Date	Revision	Changes
Sep 6, 2011	1.00	Initial release
Oct 20, 2011	1.01	1. Change electrical characteristics of comparator, 22MHZ RC oscillator, ADC and band-gap. 2. Add electrical characteristics of Flash memory 3. Change maximum SPI frequency as 12MHz 4. Fix some typos.
Dec 1, 2011	1.02	1. Fix electrical characteristics of 22MHZ RC oscillator 2. Modify all “1XX” description in registers and related figures. 3. Modify 33-pin QFN 5mmx5mm package outline specification. 4. Fix some typos.

Important Notice

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.

Please note that all data and specifications are subject to change without notice. All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.