

**Thyristors
logic level**

BT148W series

GENERAL DESCRIPTION

Glass passivated, sensitive gate thyristors in a plastic envelope suitable for surface mounting, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

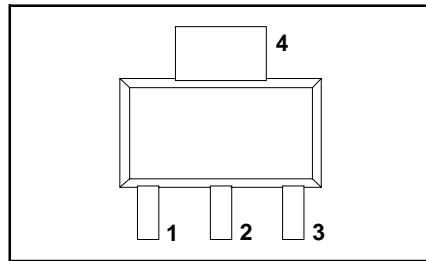
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
		400R	500R	600R	
V_{DRM} , V_{RRM}	Repetitive peak off-state voltages	400	500	600	V
$I_{T(AV)}$	Average on-state current	0.6	0.6	0.6	A
$I_{T(RMS)}$	RMS on-state current	1	1	1	A
I_{TSM}	Non-repetitive peak on-state current	10	10	10	A

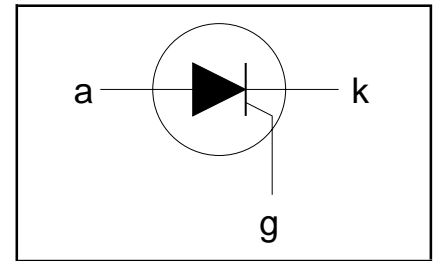
PINNING - SOT223

PIN	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-400R 400 ¹	-500R 500 ¹	-600R 600 ¹	
V_{DRM} , V_{RRM}	Repetitive peak off-state voltages		-				V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{sp} \leq 112\text{ }^\circ\text{C}$	-	0.6			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	1			A
I_{TSM}	Non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ }^\circ\text{C}$ prior to surge	-	10			A
I^2t	I^2t for fusing	$t = 10\text{ ms}$	-	11			A
dl_i/dt	Repetitive rate of rise of on-state current after triggering	$t = 10\text{ ms}$	-	0.5			A ² s
I_{GM}	Peak gate current	$I_{TM} = 4\text{ A}$; $I_G = 200\text{ mA}$; $dl_G/dt = 200\text{ mA}/\mu\text{s}$	-	50			A/ μs
V_{GM}	Peak gate voltage		-	1			A
V_{RGM}	Peak reverse gate voltage		-	5			V
P_{GM}	Peak gate power		-	5			V
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	1.2			W
T_{stg}	Storage temperature		-40	0.12			W
T_j	Operating junction temperature		-	150			$^\circ\text{C}$
				125 ²			$^\circ\text{C}$

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/ μs .

2 Note: Operation above 110 $^\circ\text{C}$ may require the use of a gate to cathode resistor of 1k Ω or less.

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THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-sp}$	Thermal resistance junction to solder point		-	-	15	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint pcb mounted, pad area as in fig:14	-	156 70	-	K/W K/W

STATIC CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise stated

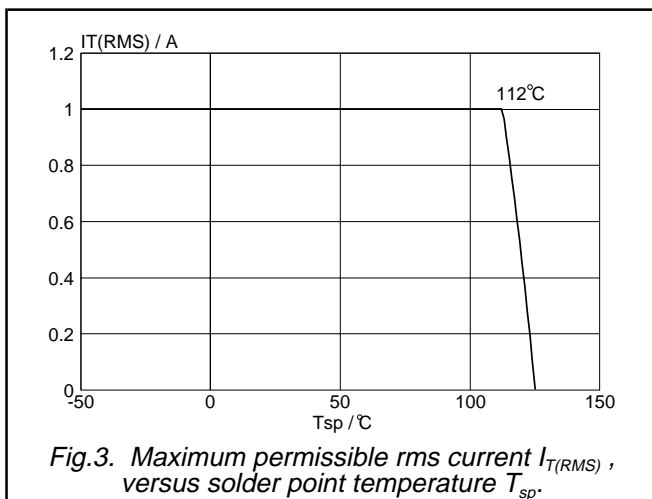
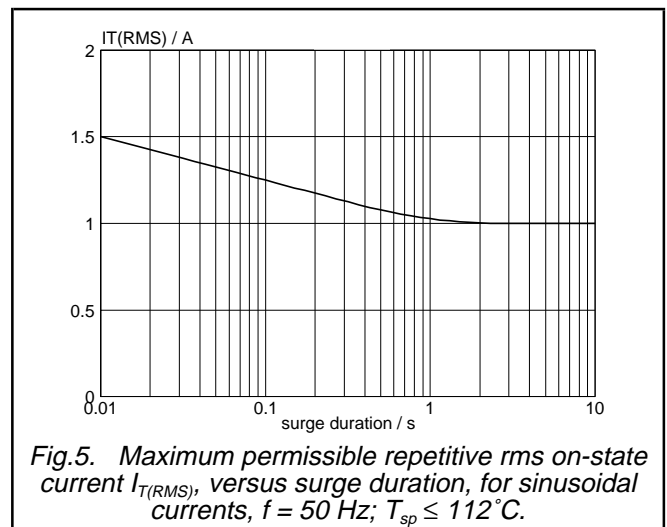
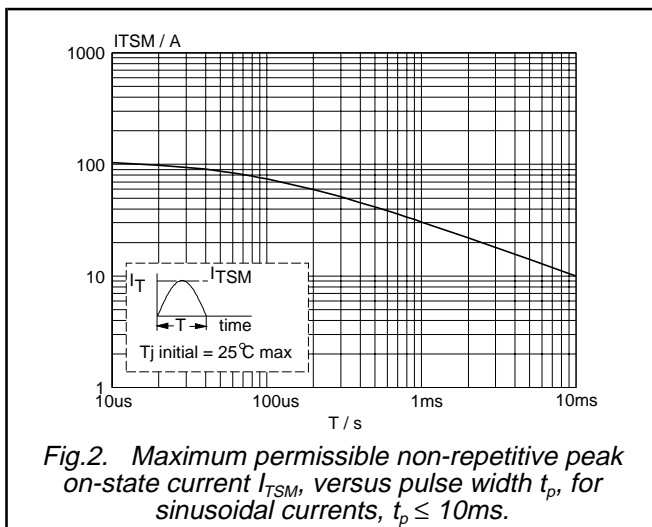
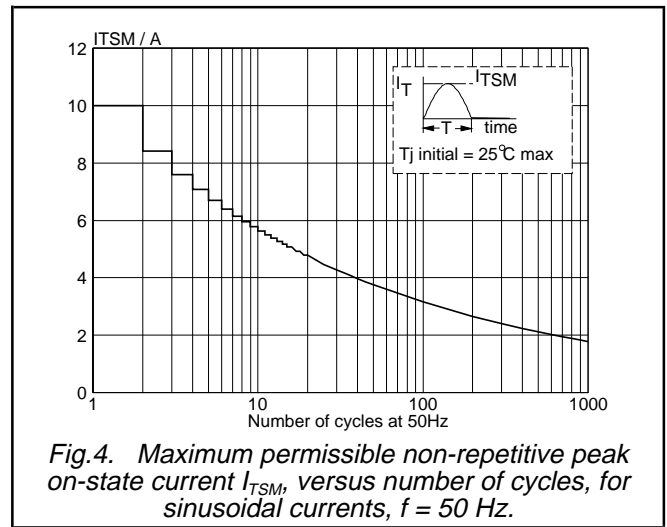
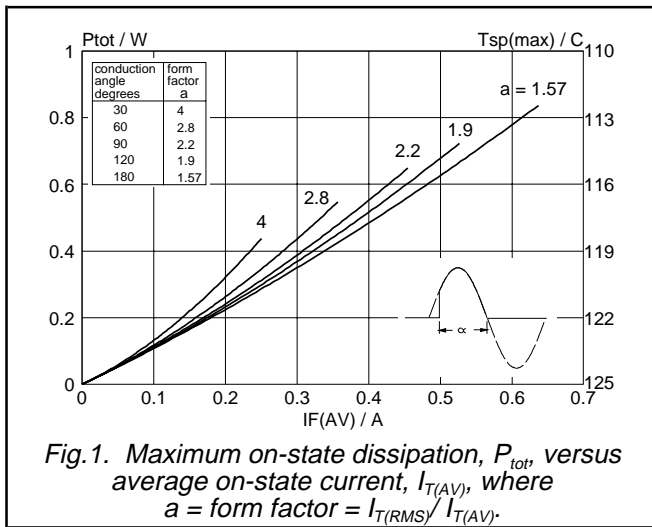
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	50	200	μA
I_L	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	0.17	10	mA
I_H	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	0.10	6	mA
V_T	On-state voltage	$I_T = 2\text{ A}$	-	1.3	1.5	V
V_{GT}	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.4	1.5	V
I_D, I_R	Off-state leakage current	$V_R = V_{RRM(max)}; I_T = 0.1\text{ A}; T_j = 110\text{ °C}$ $V_D = V_{DRM(max)}; V_R = V_{RRM(max)}; T_j = 125\text{ °C}$	0.1	0.2	-	V
			-	0.1	0.5	mA

DYNAMIC CHARACTERISTICS $T_j = 25\text{ °C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$ exponential waveform; $R_{GK} = 100\ \Omega$	-	50	-	V/ μs
t_{gt}	Gate controlled turn-on time	$I_{TM} = 4\text{ A}; V_D = V_{DRM(max)}; I_G = 5\text{ mA};$ $dl_G/dt = 0.2\text{ A}/\mu\text{s}$	-	2	-	μs
t_q	Circuit commutated turn-off time	$V_D = 67\% V_{DRM(max)}; T_j = 125\text{ °C}; I_{TM} = 2\text{ A};$ $V_R = 35\text{ V}; dl_{TM}/dt = 30\text{ A}/\mu\text{s};$ $dV_D/dt = 2\text{ V}/\mu\text{s}; R_{GK} = 1\text{ k}\Omega$	-	100	-	μs

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Fig. 7. Normalised gate trigger current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, versus junction temperature T_j .

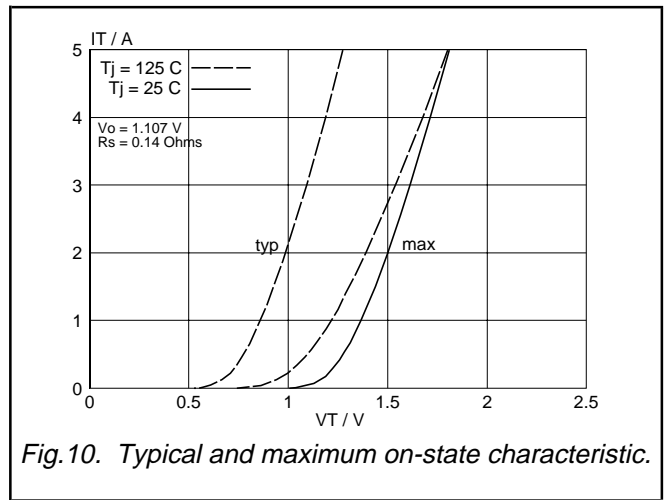


Fig. 10. Typical and maximum on-state characteristic.

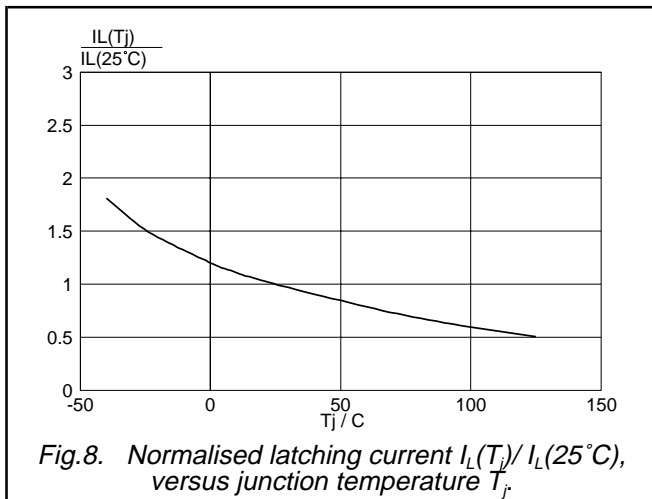


Fig. 8. Normalised latching current $I_L(T_j)/I_L(25^\circ\text{C})$, versus junction temperature T_j .

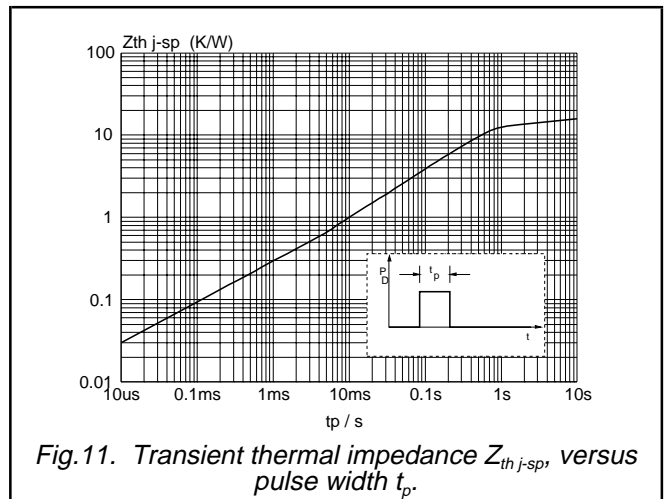


Fig. 11. Transient thermal impedance $Z_{th\ j-sp}$, versus pulse width t_p .

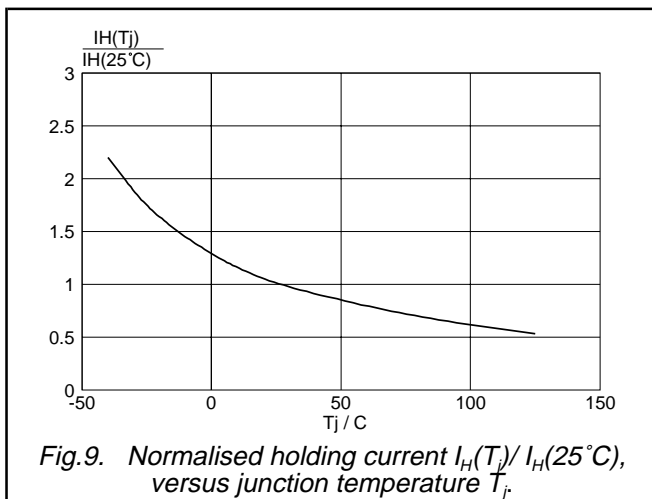


Fig. 9. Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, versus junction temperature T_j .

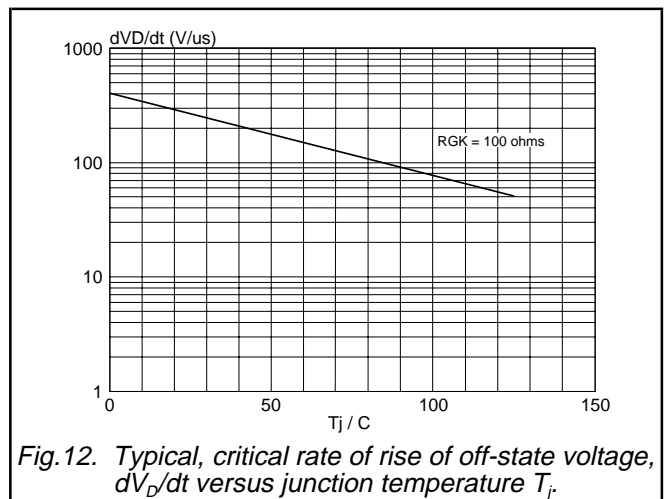


Fig. 12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j .

MOUNTING INSTRUCTIONS

Dimensions in mm.

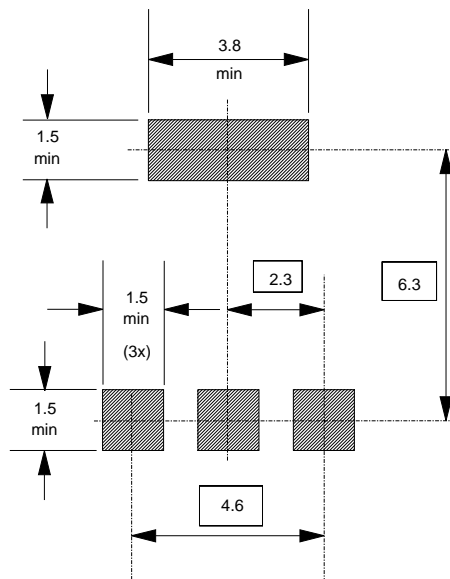
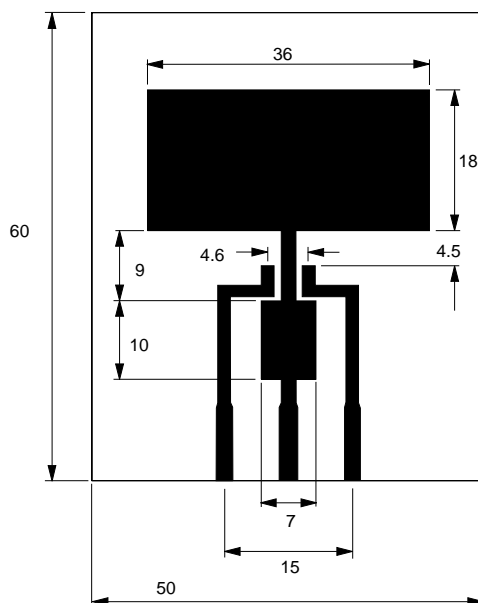


Fig.13. soldering pattern for surface mounting SOT223.

PRINTED CIRCUIT BOARD

Dimensions in mm.

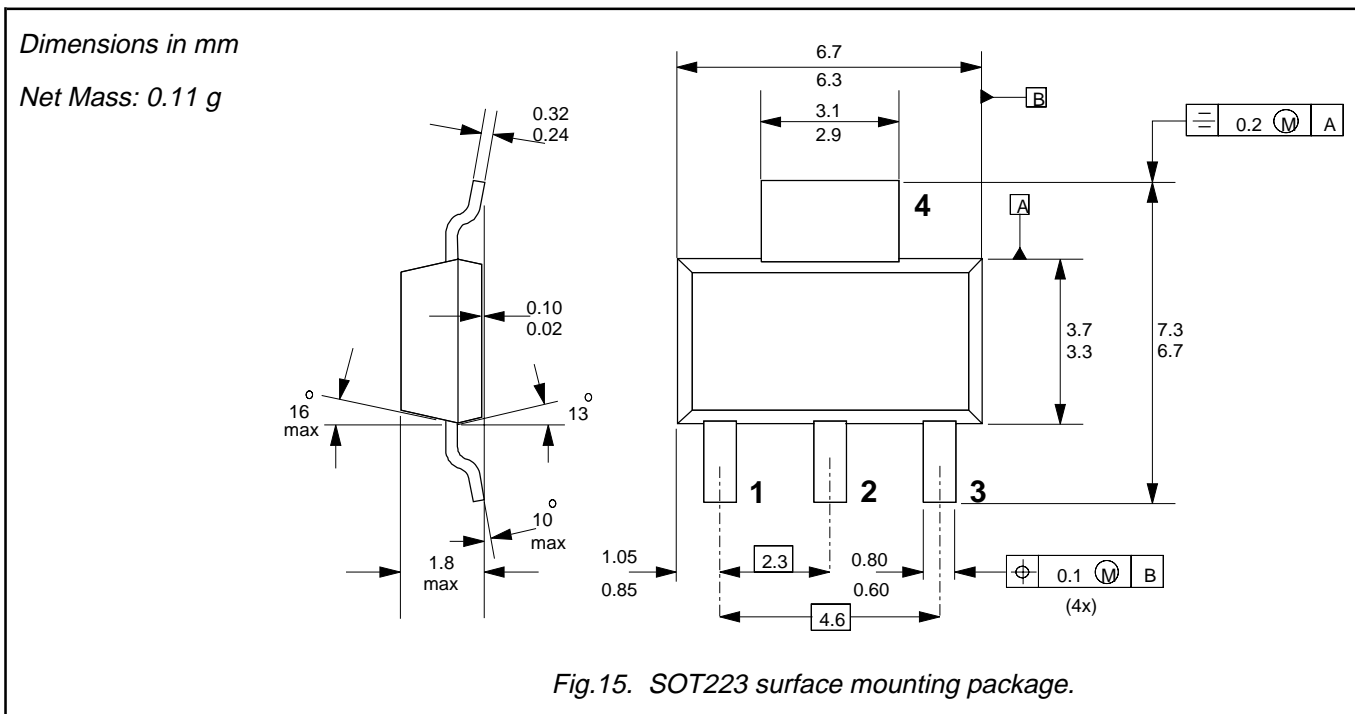


*Fig.14. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 μm thick).*

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MECHANICAL DATA



Notes

1. For further information, refer to Philips publication SC18 " SMD Footprint Design and Soldering Guidelines".
Order code: 9397 750 00505.
2. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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