DATA SHEET

O K I M I C R O C O N T R O L L E R P R O D U C T S

ML674000
CMOS 32-Bit ARM®-Based General-Purpose Microcontroller

July **2002**

Oki Semiconductor

Document Reference: PEDL674000-02

OKI Semiconductor

ML674000 Preliminary

CMOS 32-BitARM®-Based General-PurposeSingle-Chip Microcontroller

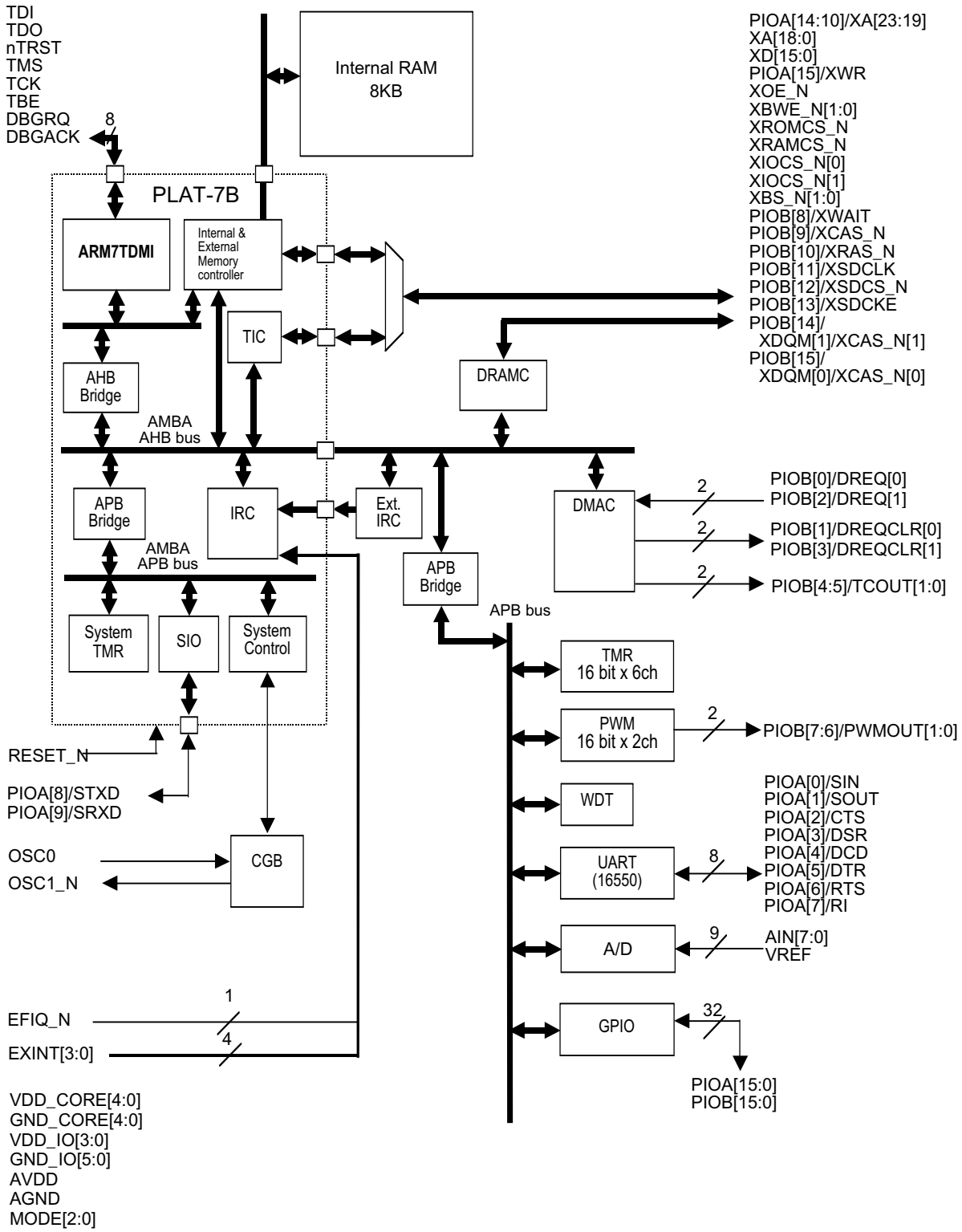
GENERAL DESCRIPTION

Oki's ML674000 LSI incorporates μPLAT™-7B, employing the CPU core ARM7TDMI®, as the CPU platform and operates at maximum 33 MHz. It contains built-in RAM and peripheral IOs such as Timer, WDT, GPIO, PWM, UART (16550 compatible), AD converter, DMA controller and DRAM controller, etc, and can be used as a microcontroller for configuring various systems.

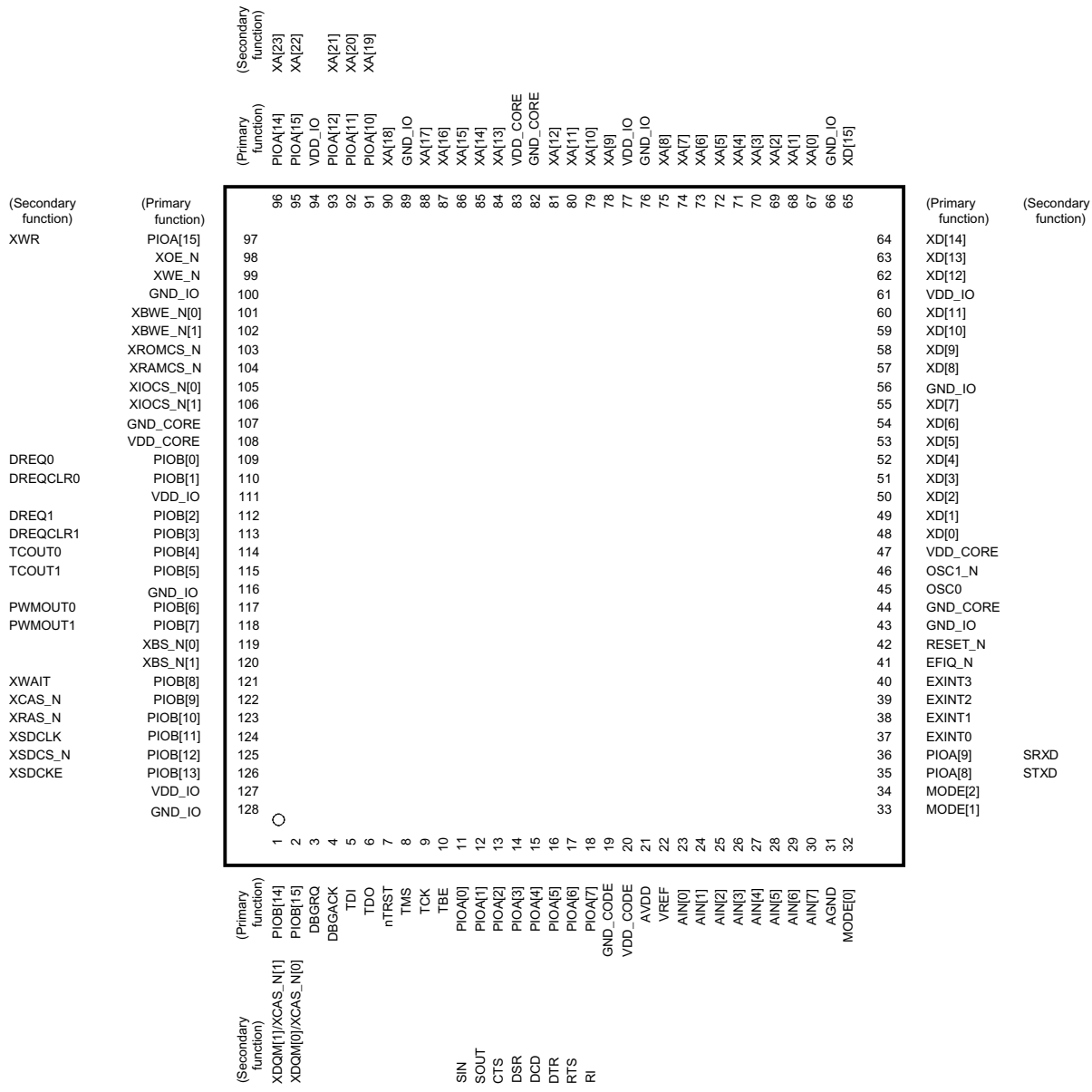
FEATURES

CPU	32-bit RISC CPU (ARM7TDMI) 32-bit instructions (ARM® Instrs) and 16-bit instructions (Thumb Instrs) mixed General purpose registers : 31 x 32 bits Barrel shifter and multiplier (32 bit x 8 bit, Modified Booth's Algorithm) Little endian Built-in debug function
Internal memory	RAM 8 KB (32-bit access)
External memory controller	ROM (FLASH): 16 MBytes SRAM: 16MBytes DRAM: 16Mbytes (SDRAM and EDO-DRAM support) External IO devices: 16Mbytes x 2 banks (with wait control by external signal) Programmable wait setting by each bank
Interrupt controller	23 sources: 18 internals and 5 externals (IRQ: 4, FIQ: 1)
DMA controller	2 channels: Dual address mode, cycle steal and burst tranfer mode maximum transfer count: 65536
Timer	1 channel: 16-bit auto reload for operating system 6 channels: 16-bit auto reload for application 1 channels: 16 bit watchdog timer
Serial interface	1 channels: asynchronous, Xon/Xoff interface 1 channels: asynchronous with 16-byte FIFO
Parallel I/O port	2 channels x 16 bits (bitwise input/output settings)
PWM	2 channels x 16 bits
AD converter	8 channels x 10 bits
Power down mechanism	Standby and Halt (clock stop by each function block) Clock gear (selectable 1/1, 1/2, 1/4, 1/8, 1/16 input clock frequency)
JTAG interface	Connectable to JTAG ICE (ex. ARM MutiICE)
Power supply voltage	Core section: 2.25 V to 2.75 V, IO section: 3.0 V to 3.6 V
Operating frequency	33 MHz (Max.)
Operating temperature (ambient temperature)	–40°C to +85°C
Package	128-pin plastic TQFP (TQFP128-P-1414-0.40-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



128-Pin Plastic TQFP

LIST OF PINS

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
1	PIOB[14]	I/O	General port (with interrupt function)	XDQM[1]/XCAS_N[1]	O	INPUT/OUTPUT mask/CAS (MSB)
2	PIOB[15]	I/O	General port (with interrupt function)	XDQM[0]/XCAS_N[0]	O	INPUT/OUTPUT mask/CAS (LSB)
3	DBGRQ	I	Input signal for debug	—		
4	DBGACK	O	Output signal for debug	—		
5	TDI	I	JTAG data input	—		
6	TDO	O	JTAG data output	—		
7	nTRST	I	JTAG reset	—		
8	TMS	I	JTAG mode selection	—		
9	TCK	I	JTAG clock	—		
10	TBE	I	Input signal for testing	—		
11	PIOA[0]	I/O	General port (with interrupt function)	SIN	I	UART Serial Data In
12	PIOA[1]	I/O	General port (with interrupt function)	SOUT	O	UART Serial Data Out
13	PIOA[2]	I/O	General port (with interrupt function)	CTS	I	UART Clear To Send
14	PIOA[3]	I/O	General port (with interrupt function)	DSR	I	UART Data Set Ready
15	PIOA[4]	I/O	General port (with interrupt function)	DCD	I	UART Data Carrier Detect
16	PIOA[5]	I/O	General port (with interrupt function)	DTR	O	UART Data Terminal Ready
17	PIOA[6]	I/O	General port (with interrupt function)	RTS	O	UART Request To Send
18	PIOA[7]	I/O	General port (with interrupt function)	RI	I	UART Ring Indicator
19	GND_CORE	GND	GND for CORE	—		
20	VDD_CORE	VDD	Power supply for CORE	—		
21	AVDD	VDD	Power supply for A/D converter	—		
22	VREF	I	Reference voltage for A/D converter	—		
23	AIN[0]	I	A/D converter analog input port	—		
24	AIN[1]	I	A/D converter analog input port	—		
25	AIN[2]	I	A/D converter analog input port	—		
26	AIN[3]	I	A/D converter analog input port	—		
27	AIN[4]	I	A/D converter analog input port	—		
28	AIN[5]	I	A/D converter analog input port	—		
29	AIN[6]	I	A/D converter analog input port	—		
30	AIN[7]	I	A/D converter analog input port	—		
31	AGND	GND	GND for A/D converter	—		
32	MODE[0]	I	Mode setting	—		
33	MODE[1]	I	Mode setting	—		
34	MODE[2]	I	Mode setting	—		
35	PIOA[8]	I/O	General port (with interrupt function)	STXD	O	SIO send data output
36	PIOA[9]	I/O	General port (with interrupt function)	SRXD	I	SIO receive data input
37	EXINT[0]	I	Interrupt input	—		
38	EXINT[1]	I	Interrupt input	—		

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
39	EXINT[2]	I	Interrupt input	–		
40	EXINT[3]	I	Interrupt input	–		
41	EFIQ_N	I	FIQ input	–		
42	RESET_N	I	Reset	–		
43	GND_IO	GND	GND for I/O	–		
44	GND_CORE	GND	GND for CORE	–		
45	OSC0	I	Oscillation input pin	–		
46	OSC1_N	O	Oscillation output pin	–		
47	VDD_CORE	VDD	Power supply for CORE	–		
48	XD[0]	I/O	External memory access data port	–		
49	XD[1]	I/O	External memory access data port	–		
50	XD[2]	I/O	External memory access data port	–		
51	XD[3]	I/O	External memory access data port	–		
52	XD[4]	I/O	External memory access data port	–		
53	XD[5]	I/O	External memory access data port	–		
54	XD[6]	I/O	External memory access data port	–		
55	XD[7]	I/O	External memory access data port	–		
56	GND_IO	GND	GND for I/O	–		
57	XD[8]	I/O	External memory access data port	–		
58	XD[9]	I/O	External memory access data port	–		
59	XD[10]	I/O	External memory access data port	–		
60	XD[11]	I/O	External memory access data port	–		
61	VDD_IO	VDD	Power supply for I/O	–		
62	XD[12]	I/O	External memory access data port	–		
63	XD[13]	I/O	External memory access data port	–		
64	XD[14]	I/O	External memory access data port	–		
65	XD[15]	I/O	External memory access data port	–		
66	GND_IO	GND	GND for I/O	–		
67	XA[0]	O	External memory access address output port	–		
68	XA[1]	O	External memory access address output port	–		
69	XA[2]	O	External memory access address output port	–		
70	XA[3]	O	External memory access address output port	–		
71	XA[4]	O	External memory access address output port	–		
72	XA[5]	O	External memory access address output port	–		
73	XA[6]	O	External memory access address output port	–		
74	XA[7]	O	External memory access address output port	–		
75	XA[8]	O	External memory access address output port	–		
76	GND_IO	GND	GND for I/O	–		
77	VDD_IO	VDD	Power supply for I/O	–		
78	XA[9]	O	External memory access address output port	–		
79	XA[10]	O	External memory access address output port	–		

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
80	XA[11]	O	External memory access address output port	–		
81	XA[12]	O	External memory access address output port	–		
82	GND_CORE	GND	GND for CORE	–		
83	VDD_CORE	VDD	Power supply for CORE	–		
84	XA[13]	O	External memory access address output port	–		
85	XA[14]	O	External memory access address output port	–		
86	XA[15]	O	External memory access address output port	–		
87	XA[16]	O	External memory access address output port	–		
88	XA[17]	O	External memory access address output port	–		
89	GND_IO	O	GND for I/O	–		
90	XA[18]	O	External memory access address output port	–		
91	PIOA[10]	I/O	General port (with interrupt function)	XA[19]	O	External memory access address output port
92	PIOA[11]	I/O	General port (with interrupt function)	XA[20]	O	External memory access address output port
93	PIOA[12]	I/O	General port (with interrupt function)	XA[21]	O	External memory access address output port
94	VDD_IO	VDD	Power supply for I/O			
95	PIOA[13]	I/O	General port (with interrupt function)	XA[22]	O	External memory access address output port
96	PIOA[14]	I/O	General port (with interrupt function)	XA[23]	O	External memory access address output port
97	PIOA[15]	I/O	General port (with interrupt function)	XWR	O	Transfer direction of external bus
98	XOE_N	O	Output enable (excluding SDRAM)	–		
99	XWE_N	O	Write enable	–		
100	GND_IO	GND	GND for I/O			
101	XBWE_N[0]	O	Byte write enable (LSB)	–		
102	XBWE_N[1]	O	Byte write enable (MSB)	–		
103	XROMCS_N	O	External ROM chip select	–		
104	XRAMCS_N	O	External RAM chip select	–		
105	XIOCS_N[0]	O	IO bank 0 chip select	–		
106	XIOCS_N[1]	O	IO bank 1 chip select	–		
107	GND_CORE	GND	GND for CORE	–		
108	VDD_CORE	VDD	Power supply for CORE	–		
109	PIOB[0]	I/O	General port (with interrupt function)	DREQ0	I	DMA request signal (CH0)
110	PIOB[1]	I/O	General port (with interrupt function)	DREQCLR0	O	DREQ clear signal (CH0)
111	VDD_IO	VDD	Power supply for I/O	–		
112	PIOB[2]	I/O	General port (with interrupt function)	DREQ1	I	DMA request signal (CH1)
113	PIOB[3]	I/O	General port (with interrupt function)	DREQCLR1	O	DREQ clear signal (CH1)
114	PIOB[4]	I/O	General port (with interrupt function)	TCOUT0	O	DMAC Terminal Count (CH0)
115	PIOB[5]	I/O	General port (with interrupt function)	TCOUT1	O	DMAC Terminal Count (CH1)
116	GND_IO	GND	GND for I/O	–		
117	PIOB[6]	I/O	General port (with interrupt function)	PWMOUT[0]	O	PWM output (CH0)
118	PIOB[7]	I/O	General port (with interrupt function)	PWMOUT[1]	O	PWM output (CH1)
119	XBS_N[0]	O	External bus byte select (LSB)	–		
120	XBS_N[1]	O	External bus byte select (MSB)	–		

Pin	Primary Function			Secondary Function		
	Symbol	Type	Description	Symbol	Type	Description
121	PIOB[8]	I/O	General port (with interrupt function)	XWAIT	O	
122	PIOB[9]	I/O	General port (with interrupt function)	XCAS_N	O	Column address strobe (SDRAM)
123	PIOB[10]	I/O	General port (with interrupt function)	XRAS_N	O	Row address strobe (SDRAM/EDO)
124	PIOB[11]	I/O	General port (with interrupt function)	XSDCLK	O	Clock for SDRAM
125	PIOB[12]	I/O	General port (with interrupt function)	XSDCS_N	O	SDRAM chip select
126	PIOB[13]	I/O	General port (with interrupt function)	XSDCKE	O	Clock enable (To SDRAM)
127	VDD_IO	VDD	Power supply for I/O	—		
128	GND_IO	GND	GND for I/O	—		

PIN DESCRIPTION

Pin Number	Pin Name	I/O	Description	Primary/ Secondary	Logic
System					
42	RESET_N	I	Reset input	—	Negative
45	OSC0	I	Crystal oscillator connection or external clock input. Connect a crystal oscillator (16 MHz to 33 MHz), if used, to OSC0 and OSC1_N.	—	
46	OSC1_N	O	Crystal oscillator connection. Leave this pin unconnected if using external clock input.	—	
10	TBE	I	Test pin. Connect to ground.	—	Negative
Debugging support. See Appendix A [pending] for specific uses.					
3	DBGRQ	I	Debugging pin. Normally connect to ground.	—	Positive
4	DBGACK	O	Debugging pin. Normally leave open.	—	Positive
9	TCK	I	Debugging pin. Normally connect to ground.	—	—
8	TMS	I	Debugging pin. Normally drive at High level.	—	Positive
7	nTRST	I	Debugging pin. Normally connect to ground.	—	Negative
5	TDI	I	Debugging pin. Normally drive at High level.	—	Positive
6	TDO	O	Debugging pin. Normally leave open.	—	Positive
General-purpose I/O ports					
11-18, 35-36, 91-93, 95-97	PIOA[15:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use.	Primary	Positive
109-110, 112-115, 117-118, 121-126 1-2	PIOB[15:0]	I/O	General-purpose port. Not available for use as port pins when secondary functions are in use. Note that enabling DRAM controller with MODE[2:0] inputs permanently configures PIOB[15:9] for their secondary functions, making them unavailable for use as port pins.	Primary	Positive
External Bus					
91-96	XA[23:19]	O	Address bus to external RAM, external ROM, external I/O banks, and external DRAM. After a reset, these pins are configured for their primary function (PIOA[14:10]).	Secondary	Positive
67-75, 78-81, 84-88	XA[18:0]	O	Address bus to external RAM, external ROM, external I/O banks, and external DRAM	—	Positive
48-55, 57-60, 62-65	XD[15:0]	I/O	Data bus to external RAM, external ROM, external I/O banks, and external DRAM	—	Positive

Pin Number	Pin Name	I/O	Description	Primary/ Secondary	Logic
External bus control signals					
103	XROMCS_N	O	ROM bank chip select	—	Negative
104	XRAMCS_N	O	SRAM bank chip select	—	Negative
105	XIOCS_N[0]	O	I/O bank 0 chip select	—	Negative
106	XIOCS_N[1]	O	I/O bank 1 chip select	—	Negative
98	XOE_N	O	Output enable/read enable	—	Negative
99	XWE_N	O	Write enable	—	Negative
119-120	XBS_N[1:0]	O	Byte select: XBS_N[1] for MSB; XBS_N[0] for LSB	—	Negative
101	XBWE_N[0]	O	LSB write enable	—	Negative
102	XBWE_N[1]	O	MSB write enable	—	Negative
97	XWR	O	Data transfer direction for external bus, used when connecting to Motorola I/O devices. This represents the secondary function of pin PIOA[15], produced by setting bit 7 in the port control (GPCTL) register to "1."	Secondary	—
121	XWAIT	I	External I/O bank 0 WAIT signal. This input permits access to devices slower than register settings.	Secondary	Positive
External bus control signals (DRAM)					
123	XRAS_N	O	Row address strobe. Used for both EDO DRAM and SDRAM.	Secondary	Negative
122	XCAS_N	O	Column address strobe signal (SDRAM)	Secondary	Negative
124	XSDCLK	O	SDRAM clock (same frequency as internal system clock)	Secondary	—
126	XSDCKE	O	Clock enable (SDRAM)	Secondary	—
125	XSDCS_N	O	Chip select (SDRAM)	Secondary	Negative
1	XDQM[1]/XCAS_N[1]	O	Connected to SDRAM: DQM (MSB) Connected to EDO DRAM: column address strobe signal (MSB)	Secondary	Positive
2	XDQM[0]/XCAS_N[0]	O	Connected to SDRAM: DQM (LSB) Connected to EDO DRAM: column address strobe signal (LSB)	Secondary	Positive
DMA control signals					
109	DREQ0	I	Ch 0 DMA request signal, used when DMA controller configured for DREQ type	Secondary	Positive
110	DREQCLR0	O	Ch 1 DREQ signal clear request. The DMA device responds to this output by negating DREQ.	Secondary	Positive
114	TCOUT0	O	Indicates to Ch 0 DMA device that last transfer has started	Secondary	Positive
112	DREQ1	I	Ch 1 DMA request signal, used when DMA controller configured for DREQ type	Secondary	Positive
113	DREQCLR1	O	Ch 1 DREQ signal clear request. The DMA device responds to this output by negating DREQ.	Secondary	Positive
115	TCOUT1	O	Indicates to Ch 1 DMA device that last transfer has started	Secondary	Positive

Pin Number	Pin Name	I/O	Description	Primary/ Secondary	Logic
SIO					
35	STXD	O	SIO transmit signal	Secondary	Positive
36	SRXD	I	SIO receive signal	Secondary	Positive
UART					
11	SIN	I	Serial data input	Secondary	Positive
12	SOUT	O	Serial data output	Secondary	Positive
13	CTS	I	Clear To Send. Indicates that modem or data set is ready to transfer data. Bit 4 in modem status register reflects this input.	Secondary	Negative
14	DSR	I	Data Set Ready. Indicates that modem or data set is ready to establish a communications link with UART. Bit 5 in modem status register reflects this input.	Secondary	Negative
15	DCD	I	Data Carrier Detect. Indicates that modem or data set has detected data carrier signal. Bit 7 in modem status register reflects this input.	Secondary	Negative
16	DTR	O	Data Terminal Ready. Indicates that UART is ready to establish a communications link with modem or data set. Bit 0 in modem control register controls this output.	Secondary	Negative
17	RTS	O	Request To Send. Indicates that UART is ready to transfer data to modem or data set. Bit 1 in modem control register controls this output.	Secondary	Negative
18	RI	O	Ring Indicator. Indicates that modem or data set has received telephone ring indicator. Bit 6 in modem status register reflects this input.	Secondary	Negative
PWM signals					
117	PWMOUT[0]	O	Ch 0 PWM output	Secondary	Positive
118	PWMOUT[1]	O	Ch 1 PWM output	Secondary	Positive
Analog-to-digital converter					
23	AIN[0]	I	Ch 0 analog input	—	
24	AIN[1]	I	Ch 1 analog input	—	
25	AIN[2]	I	Ch 2 analog input	—	
26	AIN[3]	I	Ch 3 analog input	—	
27	AIN[4]	I	Ch 4 analog input	—	
28	AIN[5]	I	Ch 5 analog input	—	
29	AIN[6]	I	Ch 6 analog input	—	
30	AIN[7]	I	Ch 7 analog input	—	
22	VREF	I	Analog-to-digital converter convert reference voltage	—	
21	AVDD		Analog-to-digital converter power supply	—	
31	AGND		Analog-to-digital converter ground	—	

Pin Number	Pin Name	I/O	Description	Primary/ Secondary	Logic
Interrupt signals					
37-40	EXINT[3:0]	I	External interrupt input signals	—	Positive/ Negative
41	EFIQ_N	I	External fast interrupt input signal. Interrupt controller connects this to CPU FIQ input.	—	Negative
MODE					
32-34	MODE[2:0]	I	Operating mode control signals	—	
Power supplies					
47, 83, 108	VDD_CORE		Core power supply	—	
61, 77, 94, 111, 127	VDD_IO		I/O power supply	—	
19, 44, 82, 107,	GND_CORE		Core ground	—	
43, 56, 66, 76, 89, 100, 116, 128	GND_IO		I/O ground	—	

DESCRIPTION OF FUNCTIONS

CPU

CPU core:	ARM7TDMI
Operating frequency:	1 MHz to 33 MHz
Instructions:	ARM instruction (32-bit length) and Thumb instruction (16-bit length) can be mixed.
General register bank:	31 x 32 bits
Built-in barrel shifter:	ALU and barrel shift operations can be executed by one instruction.
Multiplier:	32 bits x 8 bits (Modified Booth's Algorithm)
Built-in debug function:	JTAG interface, break point register

Built-in Memory

RAM:	8 KB (2K x 32 bits) Connected to processor bus (1 cycle access)

Interrupt Controller

Fast interrupt input (FIQ) and interrupt input (IRQ) are employed as interrupt input signals of ARM core. The interrupt controller controls these interrupt signals going to ARM core.

(1) Interrupt sources of ML674000
FIQ: 1 source, external source (external pin: EFIQ_N)
IRQ: 22 sources, internal sources : 18, external sources : 4 (external pins: EXINT [3 : 0])
(2) Interrupt priority level
Priority can be set in 8 levels for each source.
(3) External interrupt pin input
Level sense: Interrupt signal level is selected.
Edge sense: Rise or fall is selected.

Timer

7 channels of 16-bit reload timers are employed. Of these, 1 channel is used as system timer for OS.
The timers of other 6 channels are used in application software.

(1) System timer: 1 channel
16-bit auto reload timer: Used as system timer for OS
(This timer is incorporated in μPLAT-7B.)
(2) Application timer: 6 channels
16-bit auto reload timer
One shot, interval
Clock can be set for each channel

WDT

Possesses the function of interval timer mode in addition to the watch dog timer function.

(1) 16-bit timer
(2) Watch dog timer or interval timer mode can be selected
(3) Interrupt reset generation
(4) Maximum period: 200 msec or longer

PWM

This LSI contains two channels of PWM (Pulse Width Modulation) function which can change the duty in a certain fixed period. The PWM output resolution is 16 bits for each channel.

Serial Interface
This LSI contains two channels of serial interface.

(1) Start-stop synchronous serial interface without FIFO: 1 channel
This serial interface is incorporated in μPLAT-7B.
(2) Start-stop synchronous serial interface with 16-byte FIFO: 1 channel
This is ACE (Asynchronous Communication Element) equivalent in function to 16550A. It has 16-byte FIFO in both sending and receiving.

PIO
This LSI contains two channels 16-bit parallel port.

(1) Input or output can be selected for each bit.
(2) Interrupt can be used for all 16 bits of each channel and interrupt is possible for each channel.
(3) Interrupt mask and interrupt mode (level) can be set for all bits.
(4) Input state immediately after reset.

AD Converter
Successive approximation type AD converter.

(1) 10 bits x 8 channels
(2) Sample hold function
(3) Scan mode and select mode are supported
(4) Interrupt is generated after completion of conversion.
(5) Conversion time: shortest about 5 μs.

DMAC
Two channels of direct memory access controller which transfers data between memory and memory, between I/O and memory and between I/O and I/O.

(1) Number of channels: 2 channels
(2) Channel priority level: Fixed mode
Channel priority level is always fixed (channel 0 > 1).
Roundrobin
Priority level of the channel requested for transfer is kept lowest.
(3) Maximum number of transfers: 65,536 times (64K times)
(4) Data transfer size: Byte (8 bits), half-word (16 bits), word (32 bits)
(5) Bus request system: Cycle steal mode
Bus request signal is asserted for each DMA transfer cycle.
Burst mode:
Bus request signal is asserted until all transfers of transfer cycles are complete.
(6) DMA transfer request: Software request
By setting the software transfer request bit inside DMAC, the CPU starts DMA transfer.
External request
DMA transfer is started by external request allocated to each channel.
(7) Interrupt request: Interrupt request is generated in CPU after the end of DMA transfers for the set number of transfer cycles or after occurrence of error.
Interrupt request signal is output separately for each channel.
Interrupt request signal output can be masked for each channel.

External memory controller
Controls access of externally connected devices such as ROM (FLASH), SRAM, SDRAM (EDO DRAM) and IO devices.

(1) ROM (FLASH) access function
Supports 16-bit device
Supports FLASH memory: Byte write (can be written only by IF equivalent to SRAM).
Access timing setting
(2) SRAM access function
Supports 16-bit device
Supports asynchronous SRAM
Access timing setting
(3) DRAM access function
Supports 16-bit device
Supports EDO/SDRAM: Simultaneous connections to EDO-DRAM and SDRAM cannot be made.
Access timing setting
(4) External IO access function
Supports 8-bit/16-bit device
Supports 2 banks independently
Supports external wait input: XWAIT (IO bank 0 only)
Access timing setting (for each bank)

Power Management
HALT and STOP functions are supported as power save functions.

(1) HALT mode
HALT object
CPU, internal RAM, AHB bus control
HALT mode setting: Set by the system control register.
HALT mode cancelling: Reset, interrupt
(2) STOP mode
Stops the clock of entire LSI.
STOP mode setting: Specified by the system control register.
STOP mode cancelling: Reset, external interrupt (other than FIQ)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rated Value	Unit
Power Supply(CORE)	V_{DD_CORE}	GND = AGND = 0 V Ta = 25°C	–0.3 to +3.6	V
Power Supply(I/O)	V_{DD_IO}		–0.3 to +4.6	
Input Voltage	V_I		–0.3 to V_{DD_IO}+0.3	
Output Voltage	V_O		–0.3 to V_{DD_IO}+0.3	
Analog Power Supply	AV_{DD}		–0.3 to V_{DD_IO}+0.3	
Analog Reference Voltage	V_{REF}		–0.3 to V_{DD_IO}+0.3 and –0.3 to AV_{DD} +0.3	
Analog Input Voltage	V_{AI}		–0.3 to V_{REF}	
Power Dissipation	P_D	Ta=85°C	530	mW
Staorage Temperature	T_{STG}	—	–50 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply(CORE)	V_{DD_CORE}	—	2.25	2.5	2.75	V
Power Supply(I/O)	V_{DD_IO}		3.0	3.3	3.6	
Analog Power Supply	AV_{DD}	$A_{VDD} = V_{DD\_IO}$	3.0	3.3	3.6	
Analog reference Volatage	V_{REF}	$V_{REF} = A_{VDD} = V_{DD\_IO}$	3.0	3.3	3.6	
Operating Frequency	f_{OSC}	V_{DD_CORE} = 2.25 to 2.75 V_{DD_IO} = 3.0 to 3.6 (*1)	1	—	33	MHz
Ambient Temperature	Ta	—	–40	25	+85	°C

NOTES

(*1) On connecting a crystal oscillator, 16 MHz to 33 MHz
On connecting SDRAM, 2.56 MHz (Min)
On connecting EDO-DRAM, 6.4 MHz (Min)
On Using an AD Converter, 2 MHz (Min)

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD_CORE}=2.25 to 2.75V, V_{DD_IO}=3.0 to 3.6V,Ta =–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
H-Level Input Voltage	V_{IH}	—	2.0	—	V_{DD_IO}+0.3	V
L-Level Input Voltage	V_{IL}		–0.3	—	0.8	
Schmitt Positive Voltage	V_{T+}		—	1.6	2.1	
Schmitt Positive Voltage	V_{T-}		0.7	1.1	—	
Schmitt Histerisis	V_{HYS}		0.4	0.5	—	
H-Level Output Voltage	V_{OH}	I_{OH} = –100 mA	V_{DD}–0.2	—	—	
		I_{OH} = –4 mA	2.4	—	—	
L-Level Output Voltage	V_{OL}	I_{OL} = 100 mA	—	—	0.2	
L-Level Output Voltage 1		I_{OL} = 4 mA	—	—	0.4	
L-Level Output Voltage 2		I_{OL} = 6 mA	—	—	0.4	
Input Leakage Current 3	I_{IH} /I_{IL}	V_I = 0V / V_{DD_IO}	-10	—	10	μA
Input Leakage Current 4		V_I = 0V Pull-up resistor 50kΩ	10	66	200	
Output Leakage Current	I_{LO}	V_O = 0V / V_{DD_IO}	-10	—	10	
Input pin Capacitance	C_I	—	—	6	—	pF
Output pin Capacitance	C_O	—	—	9	—	
I/O pin Capacitance	C_{IO}	—	—	10	—	
Analog Reference Current	I_{REF}	AD Converter Operating	—	320	650	μA
		AD Converter Stopped	—	1	2	μA
Current Consumption(Standby Mode)	I_{DDS}	(*1)	—	3	50	μA
Current Consumption (HALT Mode)	I_{DDH}	f_{OSC} = 33 MHz No load	—	20	40	mA
Current Consumption (Operating)	I_{DD}		—	70	150	

NOTES
1. Not including XA[15:0]
2. XA[15:0]
3. Pins except RESET_N
4. RESET_N(with 50 kΩ pull up resistor)

(*1) Connecting input ports to either V_{DD_IO} or GND, and other pins not connect

AC Characteristics

Clock Timing

(V_{DD_CORE}=2.25 to 2.75V, V_{DD_IO}=3.0 to 3.6V, Ta =–40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Clock Frequency	f_C	—	1	—	33	MHz	
Clock Cycle Time	t_C		30	—	1000	ns	
Clock H-Level Pulse Width	t_{CH}		TBD	15	—		
Clock L-Level Pulse Width	t_{CL}		TBD	15	—		

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
nRESET Pulse Width (*1)	t_{RSTW1}	—	20 t_C	—	—	ns	
nRESET Pulse Width (*2)	t_{RSTW2}		Oscillator Stability Time	—	—	—	
nEFIQ Pulse Width	t_{EFIQW}		2 t_C	—	—	ns	
EXINT Pulse Width (*3)	$t_{EXINTW1}$		2 t_C	—	—		
EXINT Pulse Width (*4)	$t_{EXINTW2}$		t_C	—	—		
DREQCLR0/DREQCLR1 Delay Time	t_{DCLRD1}	CL = 5 pF	5 Tc + 9	—	—		
TCOUT0/TCOUT1 Delay Time	$t_{TCOUTD1}$		5 Tc + 9	—	—		
DREQCLR0/DREQCLR1 Delay Time	t_{DCLRD2}		2 Tc + 9	—	—		
TCOUT0/TCOUT1 Delay Time	$t_{TCOUTD2}$		2 Tc + 9	—	—		
DREQ0/DREQ1 Hold Time	t_{DREQH}	—	Tc	—	—		

NOTES
(*1) Not including when power is turned on and during halt/standby mode
(*2) When power is turned on and during halt/standby mode
(*3) Not including during standby mode
(*4) During standby mode

External Bus Timing

SDRAM							
Parameter	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
XSDCS_N Delay time(SDRAM)	t_{SDCSD}	CL =10 pF	0	—	3	ns	
XSDCKE Delay Time(SDRAM)	t_{SDCSD}		0	—	6		
DQM[0]/DQM[1] Delay Time(SDRAM)	t_{DQMD}		-3	—	3		
XRAS_N Delay Time(SDRAM)	t_{SDCASD}		0	—	3		
XCAS_N Delay Time(SDRAM)	t_{SDRASD}		0	—	3		
RASCAS Minimum Delay Time(SDRAM)	t_{SDRCD}	—	Tc	—	—		
RAS Active Time(SDRAM)	t_{SDRAS}		2 Tc	—	—		
RAS Precharge Time(SDRAM)	t_{SDRP}		Tc	—	—		
XWE_N Delay Time(SDRAM)	t_{SDWED}	CL = 5 pF	0	—	3		
XD[15:0] Input Setup Time(SDRAM)	t_{SDXDIS}	—	9	—	—		
XD[15:0] Input Hold Time(SDRAM)	t_{SDXDIH}		0	—	—		
XA[23:0] Delay Time(SDRAM)	t_{SDXAD}	CL = 25 pF	-3	—	6		
XD[15:0] Output Delay Time(SDRAM)	t_{SDXDOD}	CL = 20 pF	-3	—	3		
XD[15:0] Output Hold Time(SDRAM)	t_{SDXDOH}		-3	—			

EDO DRAM

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
RASCAS Delay Time (EDO-DRAM)	t_{EDRCD}	—	n_1 Tc	—	n_1 Tc + 3	ns	
CAS Pulse Width (EDO-DRAM)	t_{EDCAS}		n_2 Tc - 3	—	n_2 Tc		
RAS Pulse Width(EDO-DRAM)	t_{EDRAS}		5Tc - 3	—	—		n_1 = tRCD
RAS Precharge Time (EDO-DRAM)	t_{EDRP}		n_3 Tc	—	n_3 Tc + 3		n_2 = tCAS
CAS Precharge Time (EDO-DRAM)	t_{EDCP}		n_4 Tc	—	n_4 Tc + 3		n_3 = tRP
XRAS_N Delay Time (EDO-DRAM)	t_{EDRASD}	CL = 5 pF	Tc - 3	—	Tc + 3		n_4 = tCAC + 1 - tCAS
XOE_N Delay Time 1 (EDO-DRAM)	t_{EDOED1}		n_5 Tc - 6	—	n_5 Tc - 3		n_5 = tRAH
XOE_N Delay Time 2 (EDO-DRAM)	t_{EDOED2}		n_4 Tc - 3	—	n_4 Tc		n_6 = tRCD - tRAH
XWE_N Delay Time 1 (EDO-DRAM)	t_{EDWED1}		n_5 Tc - 3	—	n_5 Tc		n_7 = tCAC + 1
XWE_N Delay Time 2 (EDO-DRAM)	t_{EDWED2}		n_4 Tc	—	n_4 Tc + 3		
Row Address Hold Time (EDO-DRAM)	t_{EDRAH}	CL = 25 pF	n_5 Tc - 3	—	n_5 Tc + 3		
Column Address Hold Time (EDO-DRAM)	t_{EDCAD}		n_6 Tc - 3	—	n_6 Tc + 3		
Column Address Hold Time (EDO-DRAM)	t_{EDCAH}		n_2 Tc - 3	—	n_2 Tc + 3		
XD[15:0] Sampling Timing Delay Time (EDO-DRAM)	$t_{EDXDSMPLD}$	–	n_7Tc - 30	—	n_7Tc - 9		
XD[15:0] Input Setup Time (EDO-DRAM)	t_{EDXDIS}		-9	—	—		
XD[15:0] Input Hold Time (EDO-DRAM)	t_{EDXDIH}		6	—	—		
XD[15:0] Output Delay Time 1 (EDO-DRAM)	$t_{EDXDOD1}$	CL = 20 pF	-3	—	0		
XD[15:0] Output Delay Time 2 (EDO-DRAM)	$t_{EDXDOD2}$		-3	—	0		
XD[15:0] Output Hold Time (EDO-DRAM)	t_{EDXDOH}		Tc - 3	—	—		

NOTES

*The tRAS,tRAH,tCAC,tCAS,tRCD, and tRP for EDO-DRAM are parameters which can be set in DRPC register. Refer to the following Table in detail.

Table: Relation between DRPC Register settings and Parameters (tRAS, tRAH, tCAC, tCAS, tRCD, tRP) when using EDO-DRAM

	DRAMSPEC [3:0] Field	**tRAH tCAS**	**tRCD**	**tCAC tOEZ**	**tRP**	
	0000	1	2	1	1	Faster DRAM Lower Operating Frequency
	0001	1	2	1	2	^ ^
	0010	1	3	1	2	| |
	0011	1	3	1	3	| |
	0100	1	3	2	3	| |
	0101	1	4	2	4	| |
	0110	1	5	2	5	| |
	0111	2	4	2	4	| |
	1000	2	5	2	5	| |
	1001	2	6	2	6	v v
	1010	3	8	3	7	Slower DRAM Higher Operating Frequency
	1011	<Reserved>				Operation not guaranteed
	:	:				:
	1111	<Reserved>				Operation not guaranteed

SRAM/ROM

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
XOE_N Delay Time (SRAM/ROM)	t_{OED}	CL = 5 pF	-3		Tc	ns	n_8 = (OE/WE Pulse Width) n_9 = (Off Time)
XWE_N Delay Time (SRAM/ROM)	t_{WED}		0.5Tc		1.5Tc+ 3		
XBWE_N[1:0] Delay Time (SRAM/ROM)	t_{WELHD}		0.5Tc- 3		1.5Tc		
XBWE_N[1:0] Hold Time (SRAM/ROM)	t_{WELHH}		-3		0		
XOE_N, XWE_N Pulse Width (SRAM/ROM)	$t_{OE/WEW}$		n_8 Tc		n_8Tc + 3		
XBS_N[1:0] Delay Time (SRAM/ROM)	t_{BSBD}		0		3		
XBS_N[1:0] Output Hold Time 1 (SRAM/ROM)	t_{BSBH1}		-3				
XBS_N[1:0] Output Hold Time 2 (SRAM/ROM)	t_{BSBH2}		0.5Tc - 3				
XA[23:0] Delay Time (SRAM/ROM)	t_{XAD}	CL = 25 pF	-3		6		
XA[23:0] Output Hold Time 1 (SRAM/ROM)	t_{XAH1}		-3				
XA[23:0] Output Hold Time 2 (SRAM/ROM)	t_{XAH2}		0.5Tc - 3				
XD[15:0] Input Setup Time (SRAM/ROM)	t_{XDIS}		21				
XD[15:0] Input Hold Time (SRAM/ROM)	t_{XDIH}		n_9 Tc- 3				
XD[15:0] Output Delay Time (SRAM/ROM)	t_{XDOD}	CL = 20 pF	0		9		
XD[15:0] Output Hold Time (SRAM/ROM)	t_{XDOH}		0.5Tc - 3				
XROMCS_N,XRAMCS_N Output Hold Time 1 (SRAM/ROM)	t_{CSH1}	CL = 5 pF	-3				
XROMCS_N,XRAMCS_N Output Hold Time 2 (SRAM/ROM)	t_{CSH2}		0.5Tc -3				

NOTES

*The OE/WE Pulse Width and Off time for SRAM/ROM are parameters which can be set in RAMAC/ROMAC register. Refer to the following Table in detail.

Table: Relation between ROMAC register settings and Parameters (OE/WE Pulse Width and Off time)

ROMTYPE[2:0] Field	OE/WE Pulse Width	Off time	Note
000	1	0	
001	2	0	
010	3	2	
011	4	2	
100,101,110	-----	-----	Operation not guaranteed
111	8	4	

Table: Relation between RAMAC register settings and Parameters (OE/WE Pulse Width and Off time)

RAMTYPE[2:0] Field	OE/WE Pulse Width	Off time	Note
000	1	0	
001	2	0	
010	3	2	
011	4	2	
100,101,110	-----	-----	Operation not guaranteed
111	8	4	

IO0/IO1							
Parameter	**Symbol**	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**	**Note**
XWR Delay Time(IO0/IO1)	$t_{XIOXWRD}$	CL = 10 pF	0		3	ns	
XWAIT Sampling Timing Delay Time 1 (IO0/IO1)	$t_{XIOXWAITD1}$		n_{10}Tc- 24		n_{10}Tc- 9		n_{10} = (Address setup) + (OE/WE Pulse Width)
XWAIT Sampling Timing Delay Time 2 (IO0/IO1)	$t_{XIOXWAITD2}$		n_{11}Tc- 24		n_{11}Tc- 9		n_{11} = (Address setup) + 1 + (OE/WE Pulse Width)
XWAIT Setup Time (IO0/IO1)	$t_{XIOXWAITS}$		-9				
XWAIT Hold Time (IO0/IO1)	$t_{XIOXWAITH}$		6				
XOE_N Delay Time (IO0/IO1)	t_{XIOOED}	CL = 5 pF	n_{12} Tc		n_{12} Tc + 3		n_{12} = (Address setup)
XWE_N Delay Time (IO0/IO1)	t_{XIOWED}		n_{13} Tc		n_{13} Tc + 3		n_{13} = (Address setup)+ 1
XBWE_N[1:0] Delay Time (IO0/IO1)	$t_{XIOWELHD}$		n_{13} Tc		n_{13} Tc + 3		n_{14} = (OE/WE Pulse Width)
XOE_N,XWE_N Pulse Width (IO0/IO1)	$t_{XIOE/WEW}$		n_{14} Tc - 3		n_{14} Tc		$n_{1\_}$ = (Offtime)
XBWE_N[1:0] Hold Time (IO0/IO1)	$t_{XIOWELHH}$		-3		3		
XBS_N[1:0] Delay Time (IO0/IO1)	t_{XIOSBD}		0		3		
XBS_N[1:0] Output Hold Time (IO0/IO1)	t_{XIOSBH}		Tc				
XA[23:0] Delay Time (IO0/IO1)	t_{XIOXAD}	CL = 25 pF	-3		9		
XA[23:0] Output Hold Time 1 (IO0/IO1)	$t_{XIOXAH1}$		-3				
XA[23:0] Output Hold Time 2 (IO0/IO1)	$t_{XIOXAH2}$		Tc - 3				
XD[15:0] Input Setup Time (IO0/IO1)	t_{XIODIS}		18				
XD[15:0] Input Setup Time (IO0/IO1)	t_{XIODIH}		n_{15} Tc - 3				
XD[15:0] Output Delay Time (IO0/IO1)	t_{XIODOD}	CL = 20 pF	Tc - 3		Tc + 6		
XD[15:0] Output Hold Time (IO0/IO1)	t_{XIODOH}		Tc - 3				
XIOCS_N[0]/XIOCS_N[1] Output Hold Time (IO0/IO1)	t_{XIOCSH}	CL = 5 pF	Tc - 3				

NOTES

*The addess setup time, OE/WE Pulse Width and Off time for IO0/IO1 are parameters which can be set in IO0AC/IO1AC register. Refer to the following Table in detail.

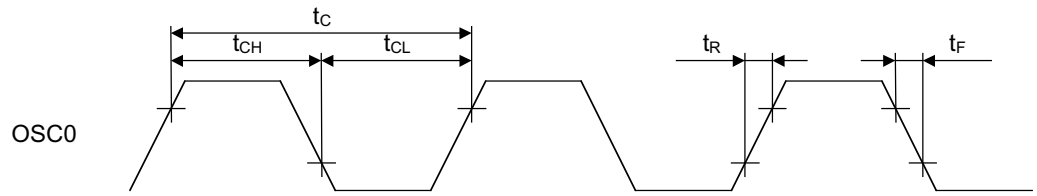
Table: Relation between IO0AC/IO1AC register settings and Parameters (Address setup time, OE/WE Pulse Width and Off time)

IOTYPE[2:0] Field	AS	R/W	OF	Note
000	1	1	1	
001	1	4	3	
010	-	-	-	Operation not guaranteed
011	2	8	5	
100	2	12	7	
101	2	16	8	
110	-	-	-	Operation not guaranteed
111	4	24	11	

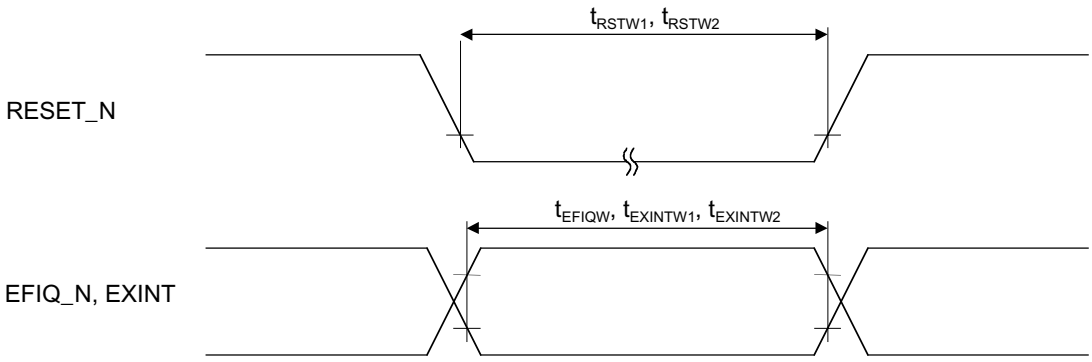
AS=address setup time, R/W=OE/WE Pulse Width, OF=Off time

TIMING DIAGRAMS

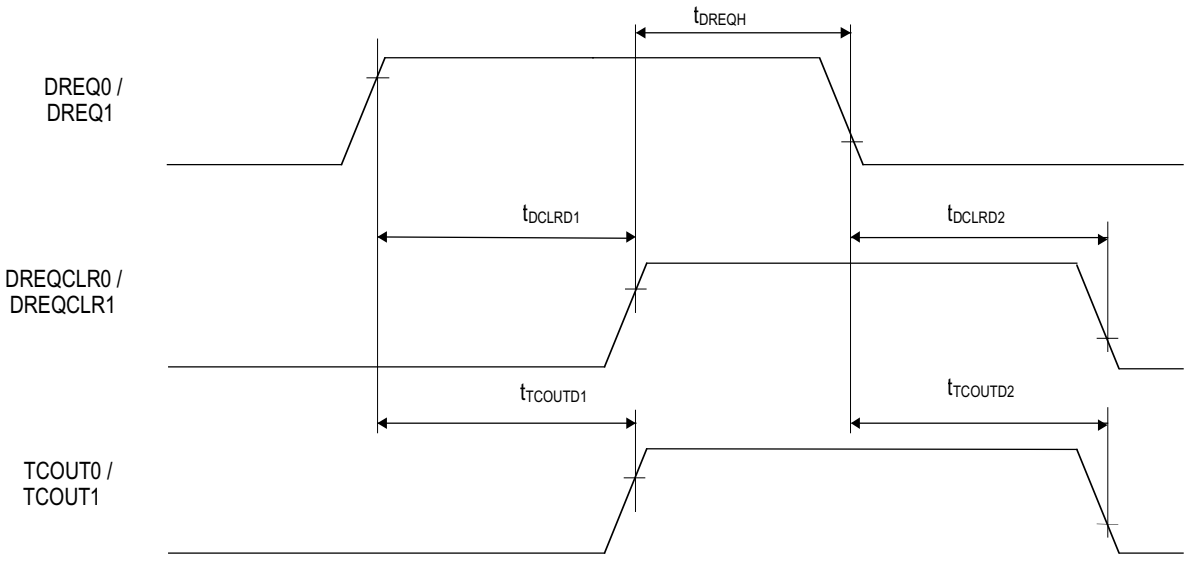
Clock Timing



Control Signal Timing

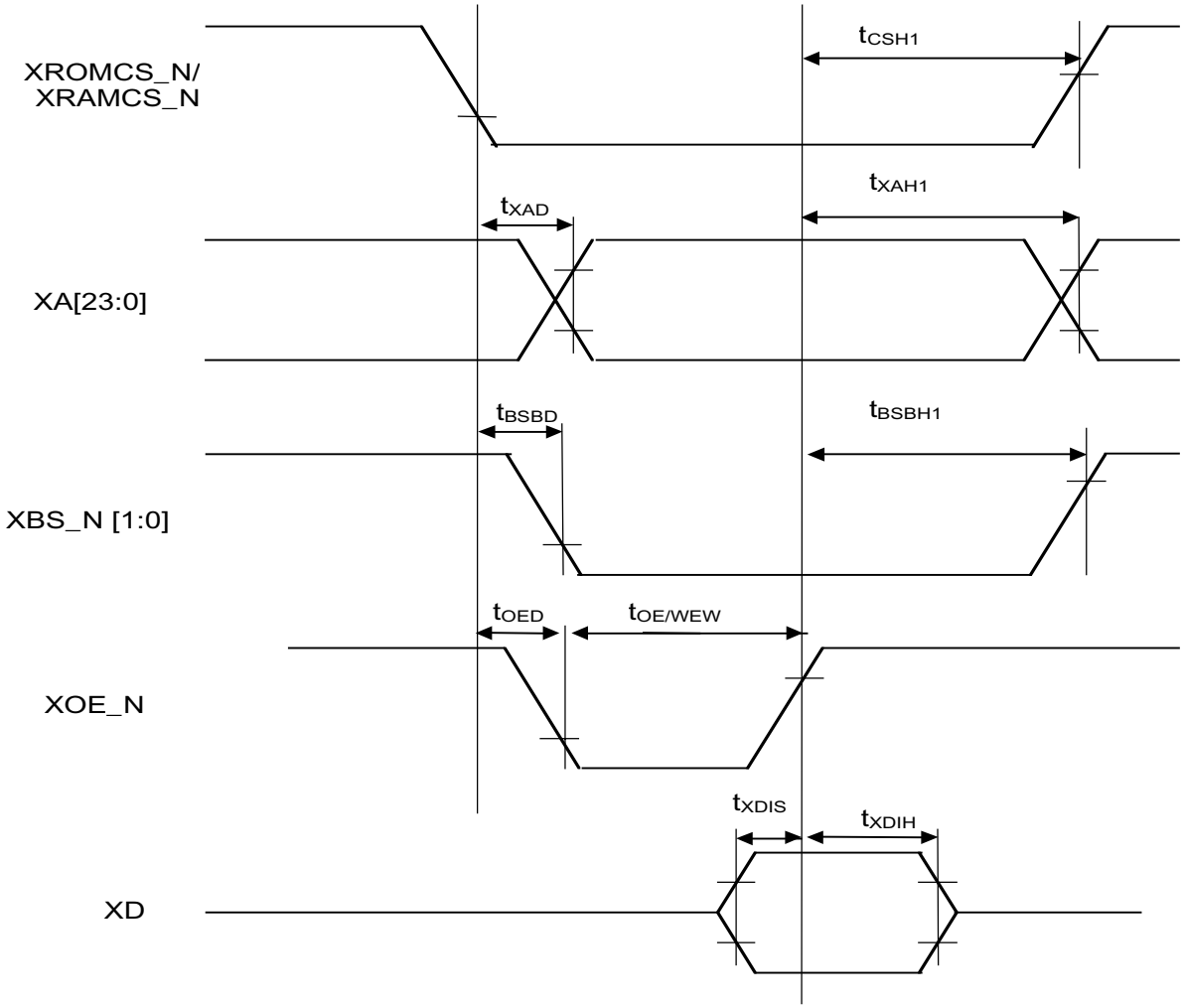


DMA Timing

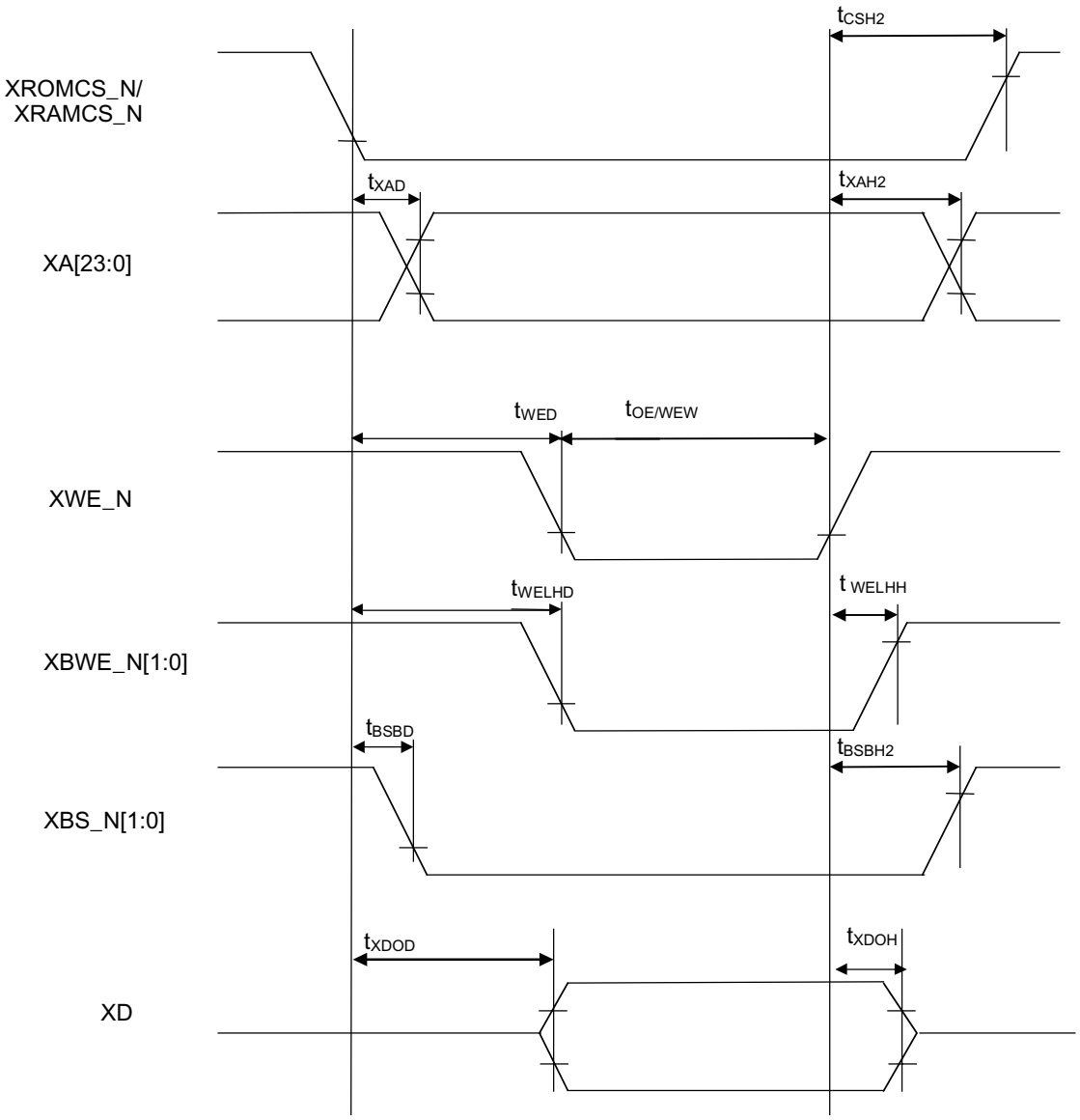

tDREQH
DREQ0 /
DREQ1
tDCLRD1
tDCLRD2
DREQCLR0 /
DREQCLR1
tTCOUTD1
tTCOUTD2
TCOUT0 /
TCOUT1

External Bus Timing

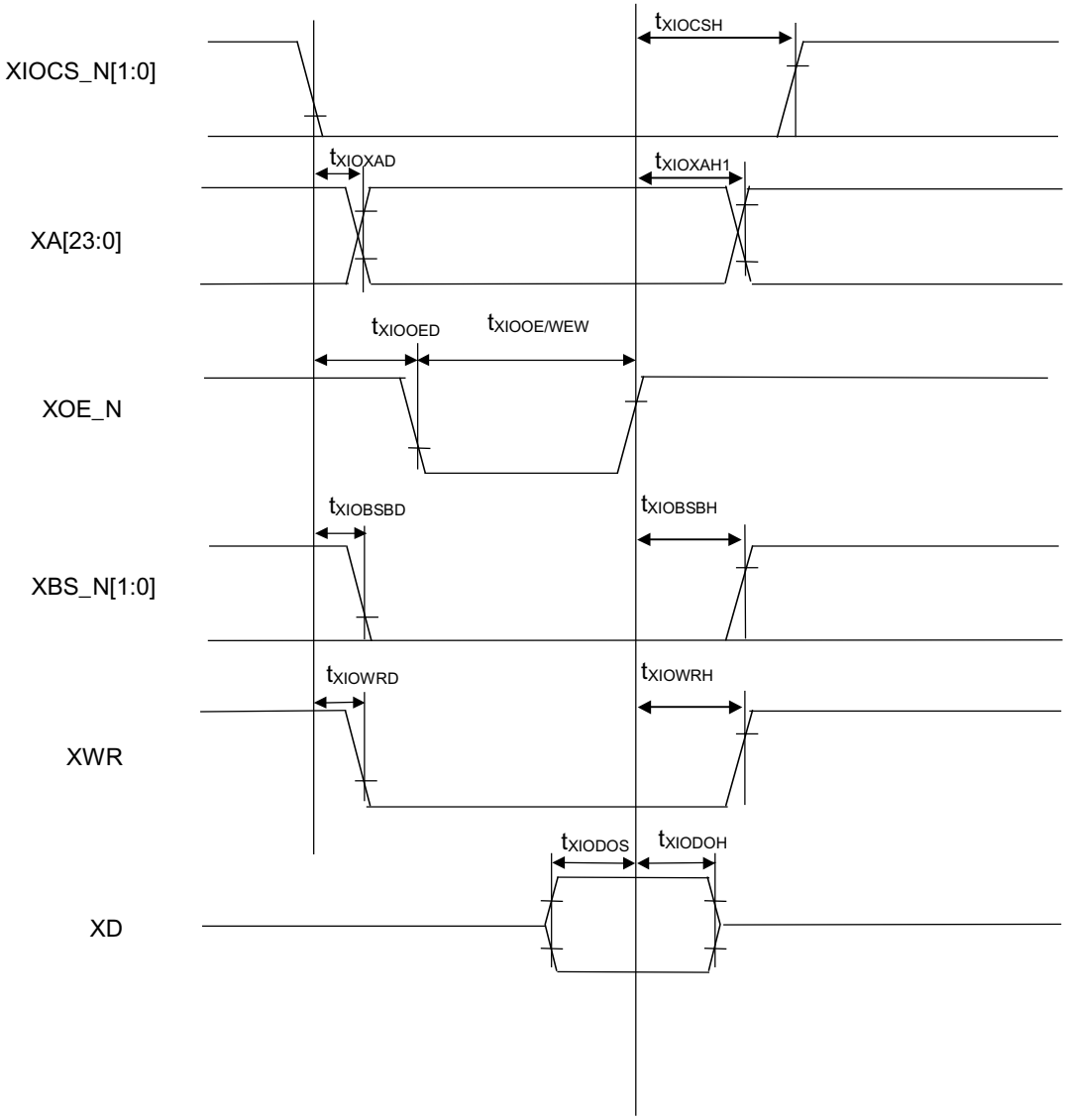
External ROM and External RAM Read Cycle



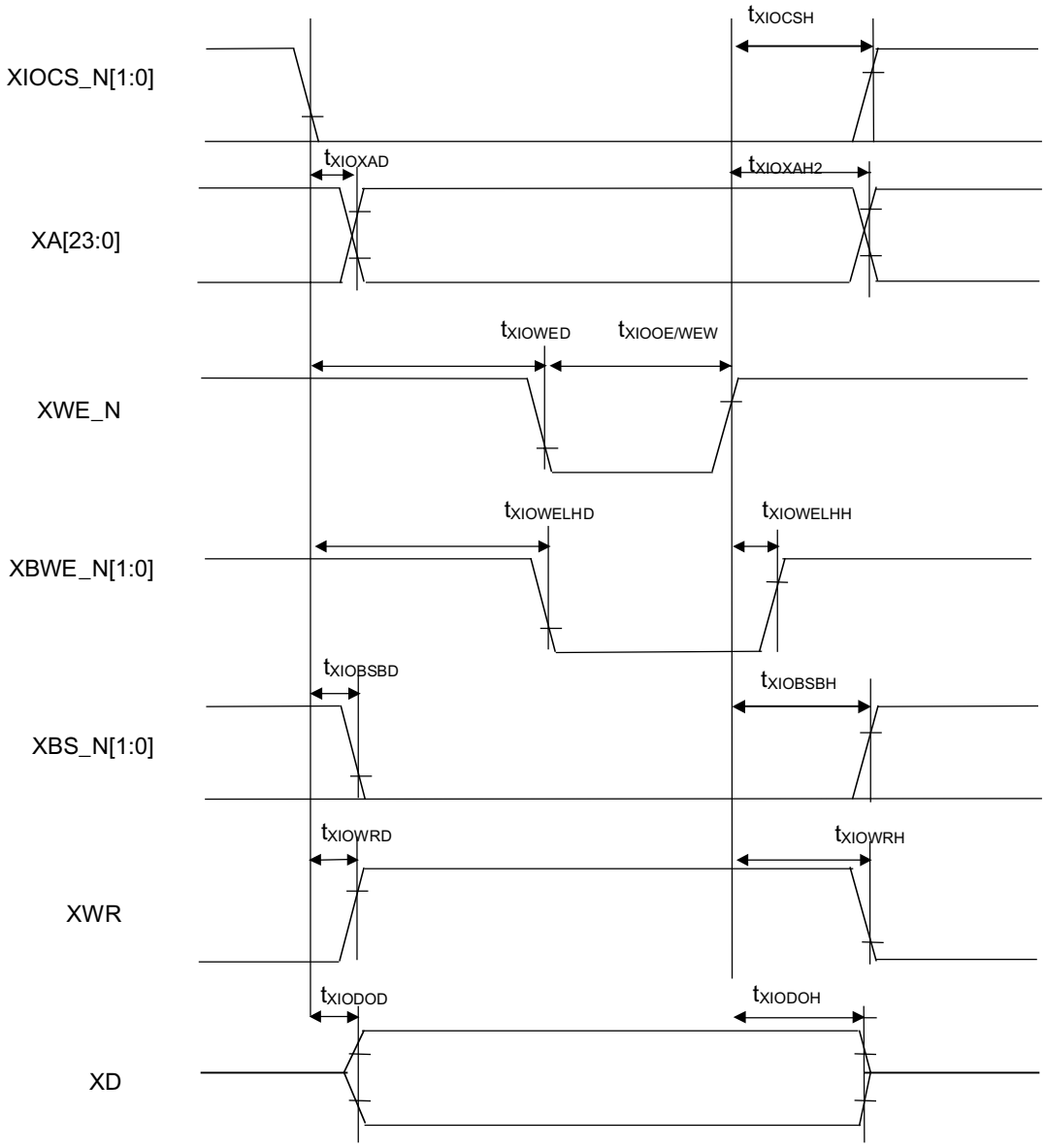
External ROM and External RAM Write Cycle



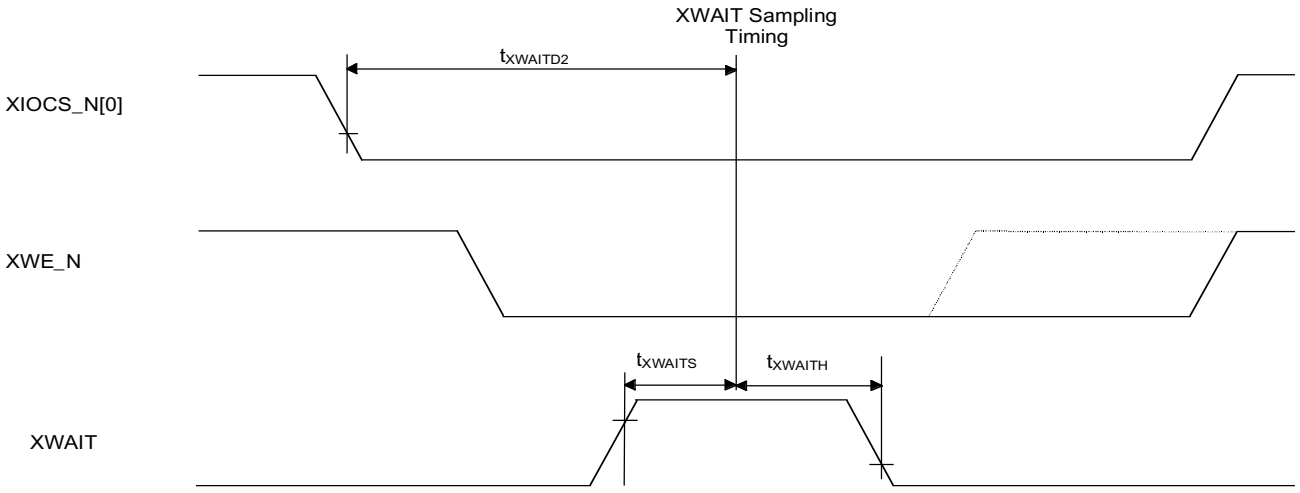
External IO0, 1 Read Cycle

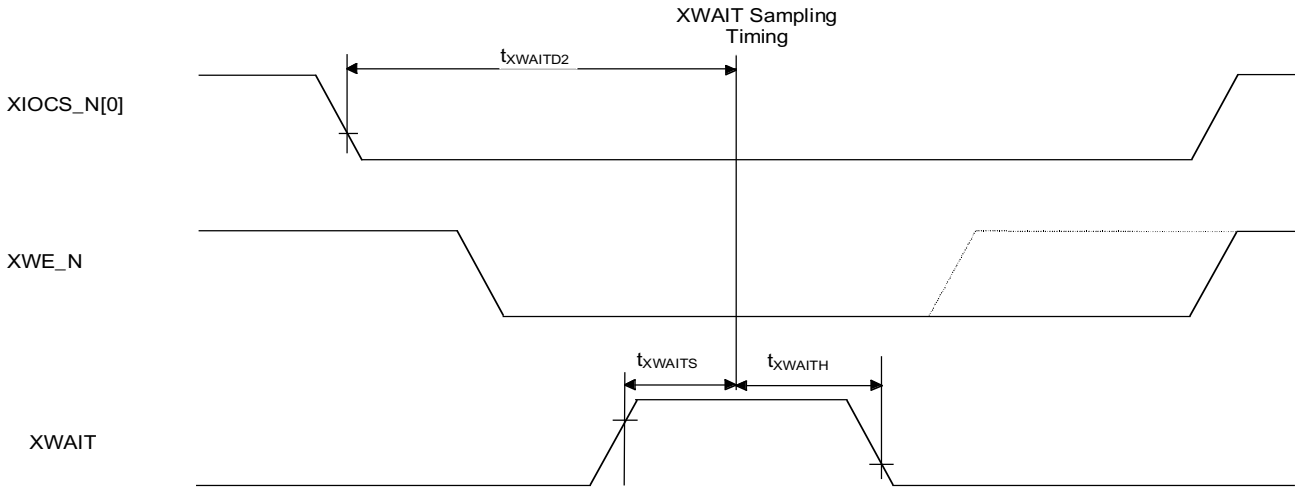


External IO0, 1 Write Cycle

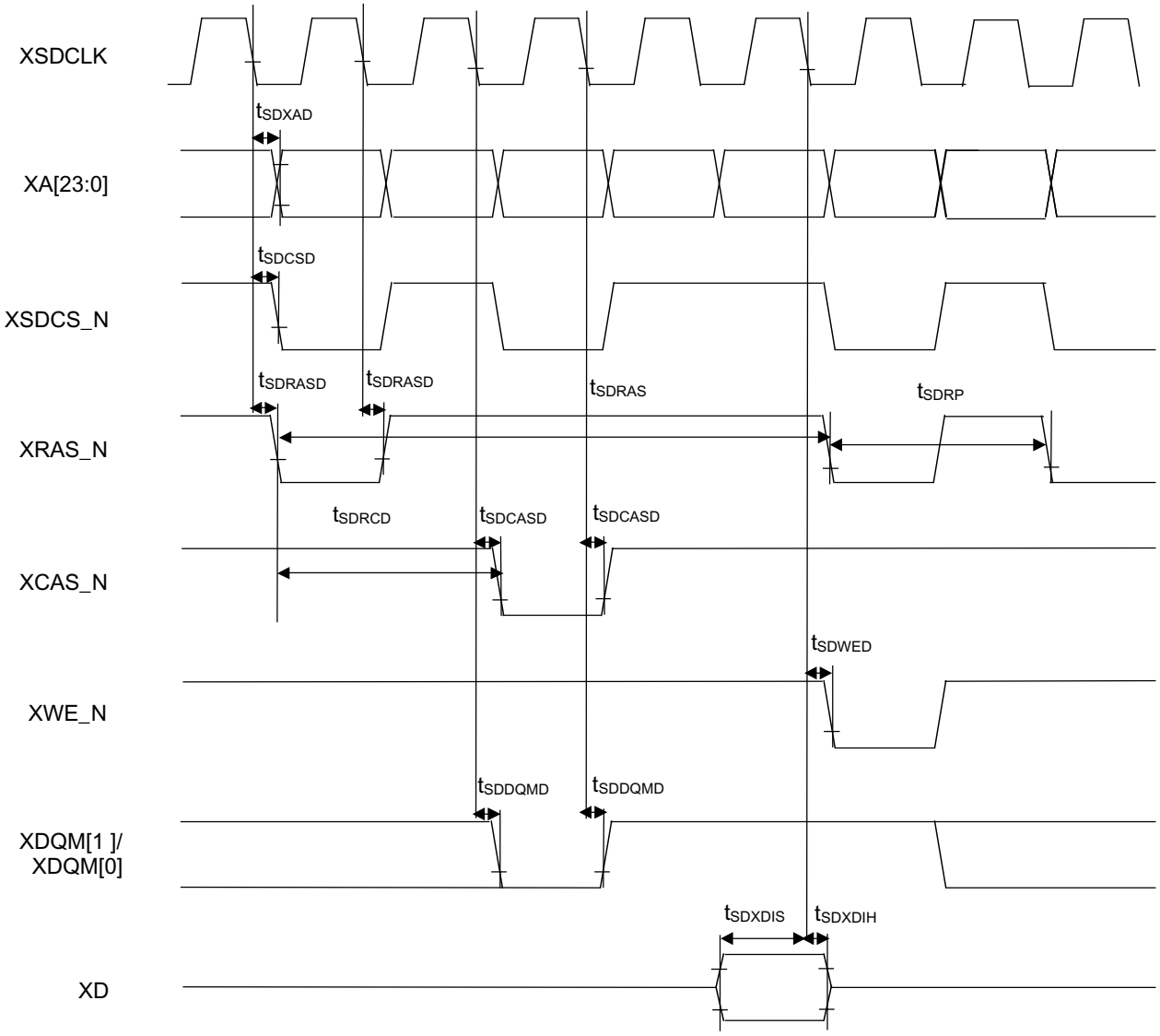


XWAIT Signal Input Timing

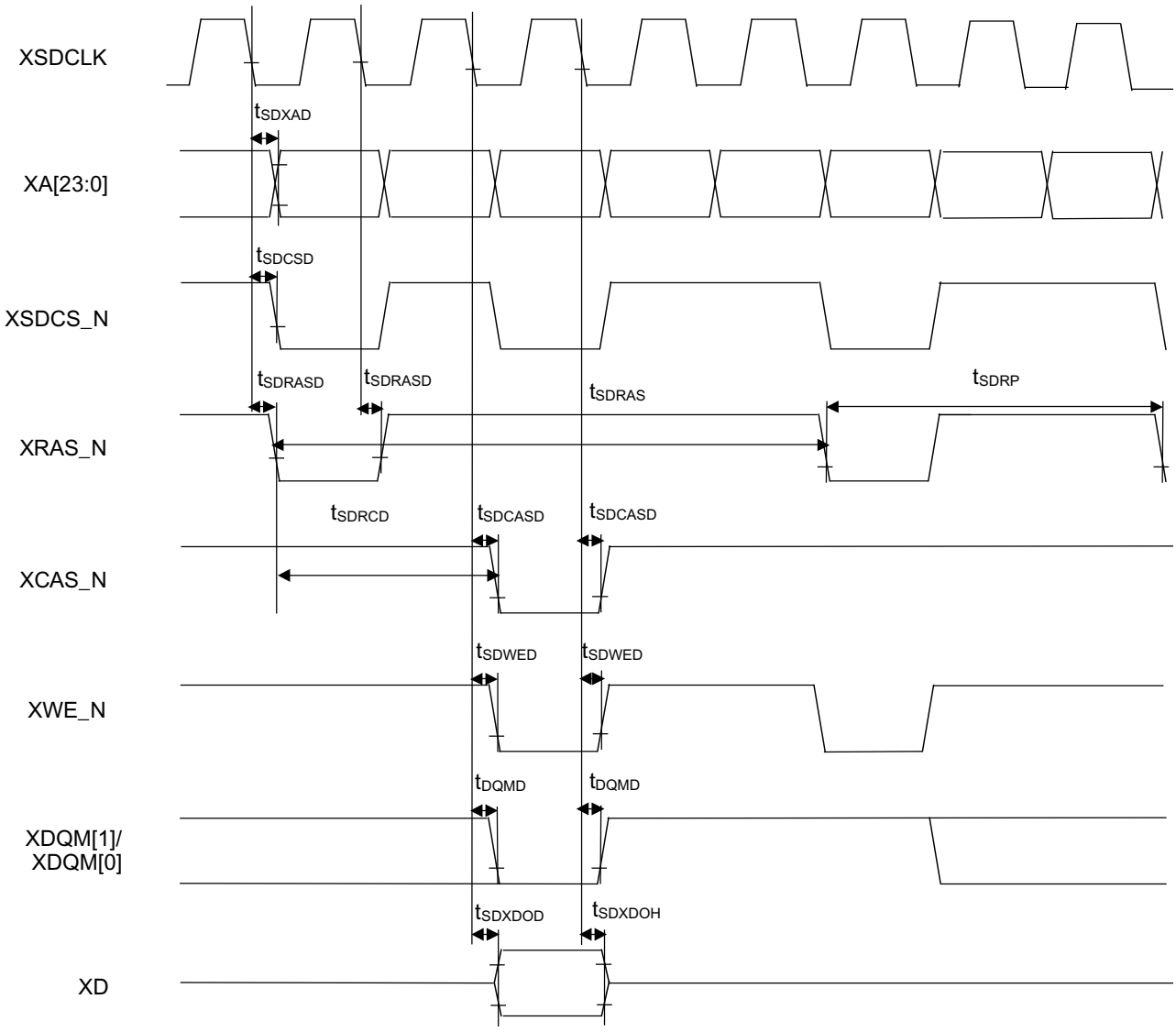




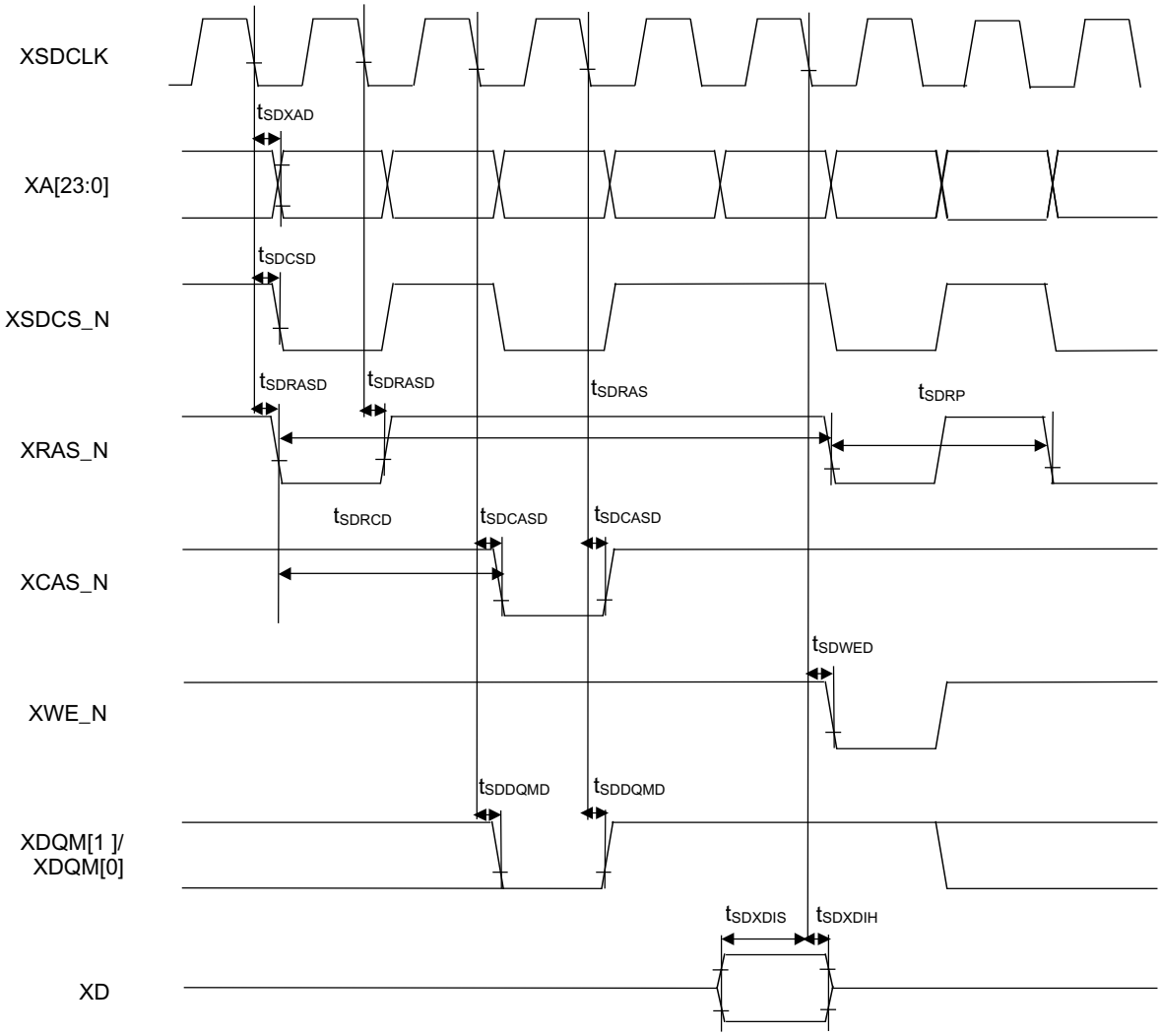
SDRAM Read Cycle



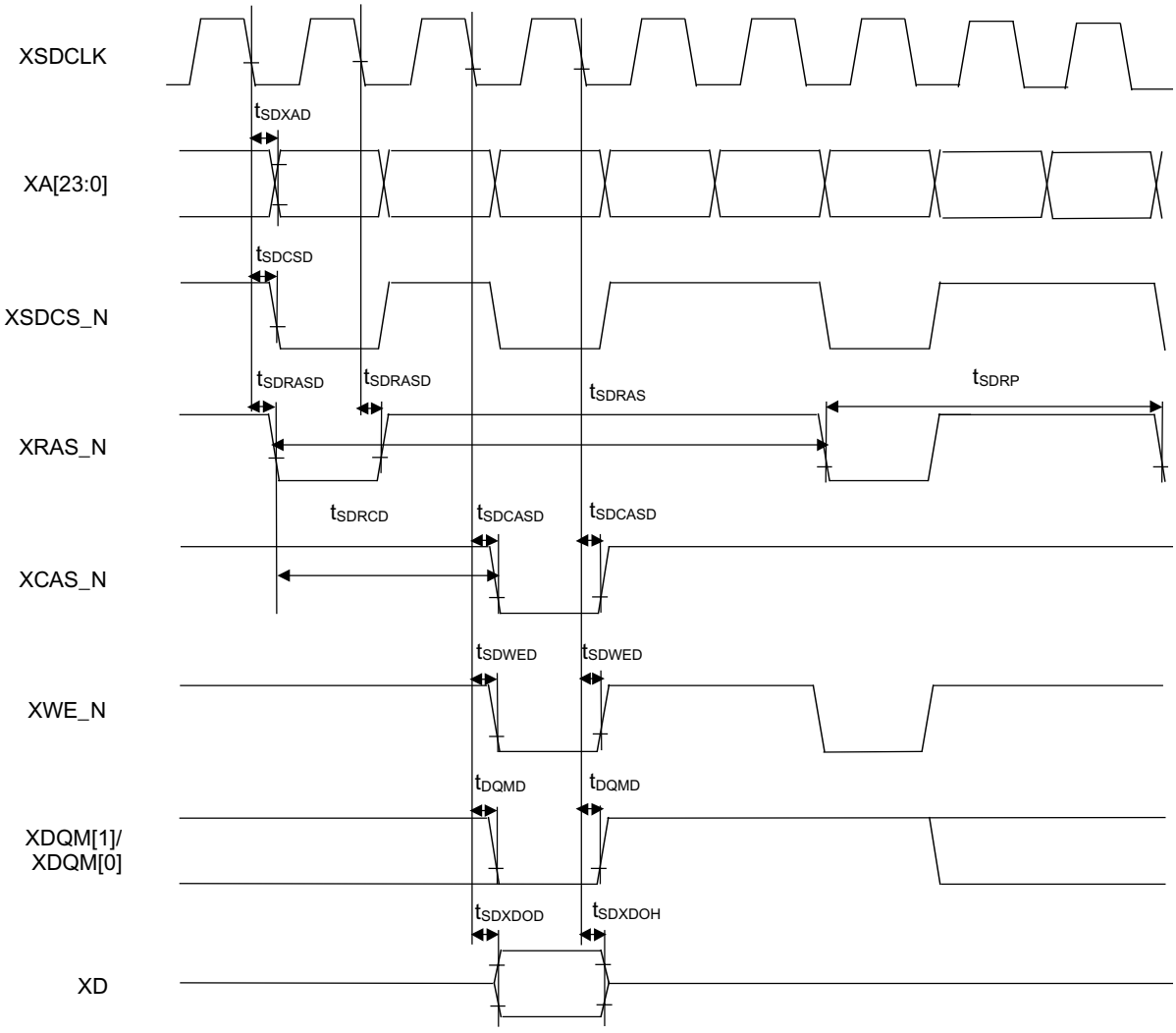
SDRAM Write Cycle



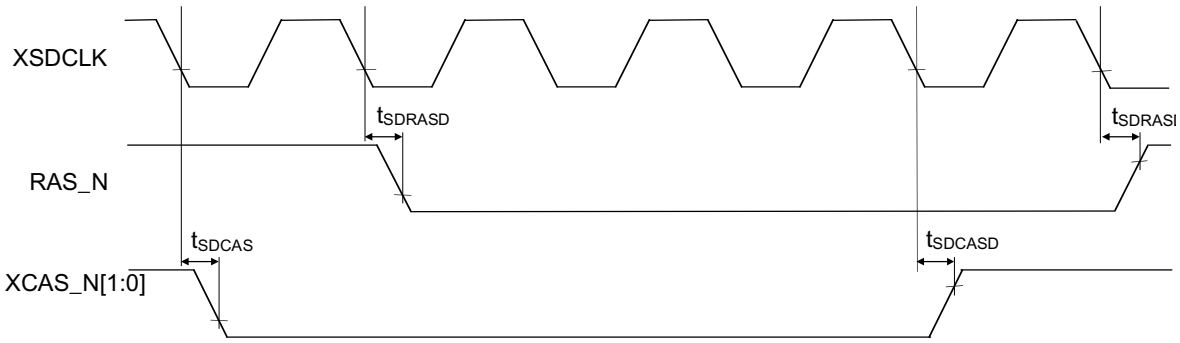
EDO-DRAM Read Cycle



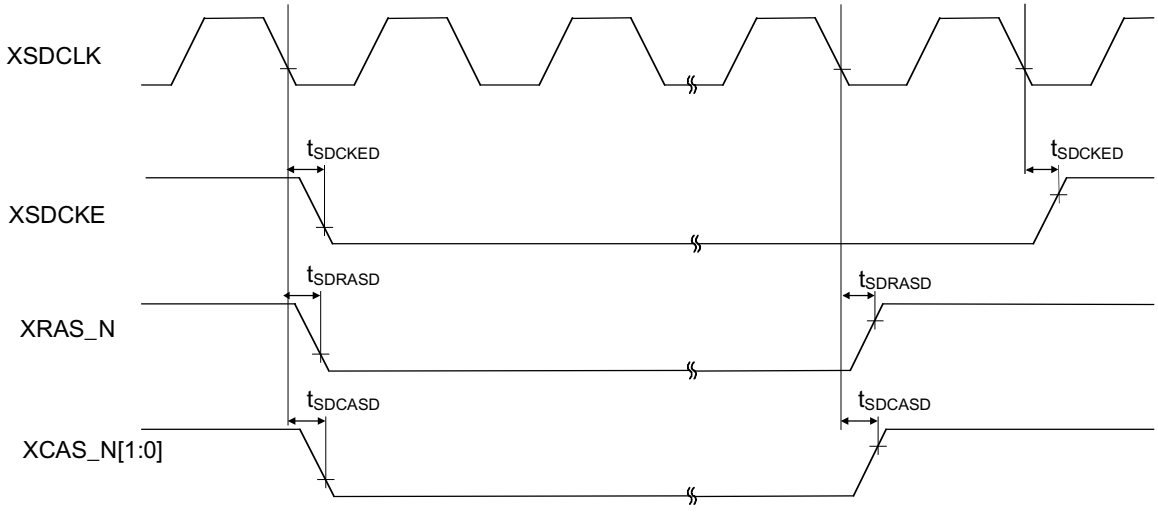
EDO-DRAM Write Cycle



CAS Before RAS Refresh (CBR)



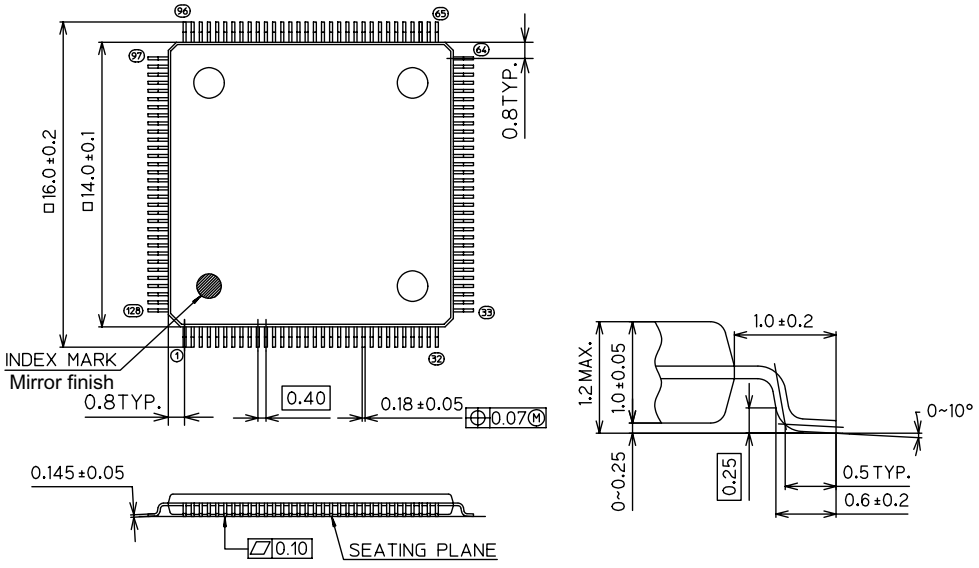
Self Refresh



PACKAGE DIMENSIONS

(Unit : mm)

TQFP128-P-1414-0.40-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥
Package weight (g)	0.55 TYP.

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.

Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL674000-01	Oct., 2001	—	—	Preliminary edition 1
PEDL674000-02	May 17, 2002	—	—	Preliminary edition 2
		1	1	Feature Table rewritten.
		2-13	2-12	Pin names are changed.
		14-16	13-15	Description rewritten.
		17	16-37	Electrical characteristics added.

The information contained herein can change without notice owing to product and/or technical improvements.

Please make sure before using the product that the information you are referring to is up-to-date.

The outline of action and examples of application circuits described herein have been chosen as an explanation of the standard action and performance of the product. When you actually plan to use the product, please ensure that the outside conditions are reflected in the actual circuit and assembly designs.

Oki assumes no responsibility or liability whatsoever for any failure or unusual or unexpected operation resulting from misuse, neglect, improper installation, repair, alteration or accident, improper handling, or unusual physical or electrical stress including, but not limited to, exposure to parameters outside the specified maximum ratings or operation outside the specified operating range.

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