NCP1421

600 mA Sync-Rect PFM Step-Up DC-DC Converter with True-Cutoff and Ring-Killer

NCP1421 is a monolithic micropower high-frequency step-up switching converter IC specially designed for battery-operated hand-held electronic products up to 600 mA loading. It integrates Sync-Rect to improve efficiency and to eliminate the external Schottky Diode. High switching frequency (up to 1.2 MHz) allows for a low profile, small-sized inductor and output capacitor to be used. When the device is disabled, the internal conduction path from LX or BAT to OUT is fully blocked and the OUT pin is isolated from the battery. This True-Cutoff function reduces the shutdown current to typically only 50 nA. Ring-Killer is also integrated to eliminate the high-frequency ringing in discontinuous conduction mode. In addition to the above, Low-Battery Detector, Logic-Controlled Shutdown, Cycle-by-Cycle Current Limit and Thermal Shutdown provide value-added features for various battery-operated applications. With all these functions ON, the quiescent supply current is typically only 8.5 μA. This device is available in the compact and low profile Micro8™ package.

Features

- High Efficiency: 94% for 3.3 V Output at 200 mA from 2.5 V Input
  88% for 3.3 V Output at 500 mA from 2.5 V Input
- High Switching Frequency, up to 1.2 MHz (not hitting current limit)
- Output Current up to 600 mA at V_{IN} = 2.5 V and V_{OUT} = 3.3 V
- True-Cutoff Function Reduces Device Shutdown Current to typically 50 nA
- Anti-Ringing Ring-Killer for Discontinuous Conduction Mode
- High Accuracy Reference Output, 1.20 V ±1.5%, can Supply 2.5 mA Loading Current when V_{OUT} > 3.3 V
- Low Quiescent Current of 8.5 μA
- Integrated Low-Battery Detector
- Open Drain Low-Battery Detector Output
- 1.0 V Startup at No Load Guaranteed
- Output Voltage from 1.5 V to 5.0 V Adjustable
- 1.5 A Cycle-by-Cycle Current Limit
- Multi-function Logic-Controlled Shutdown Pin
- On Chip Thermal Shutdown with Hysteresis
- Housed in Space-Saving and Low Profile Micro8 Package

Typical Applications

- Personal Digital Assistants (PDA)
- Handheld Digital Audio Products
- Camcorders and Digital Still Cameras
- Hand-held Instruments
- Conversion from one to two Alkaline, NiMH, NiCd Battery Cells to 3.0-5.0 V or one Lithium-ion cells to 5.0 V

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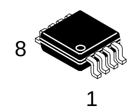
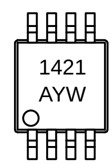


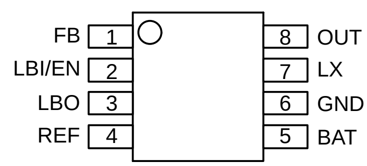
Micro8
DM SUFFIX
CASE 846A

MARKING DIAGRAM



1421	= Device Code
A	= Assembly Location
Y	= Year
W	= Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP1421DMR2	Micro8	4000 Tape & Reel

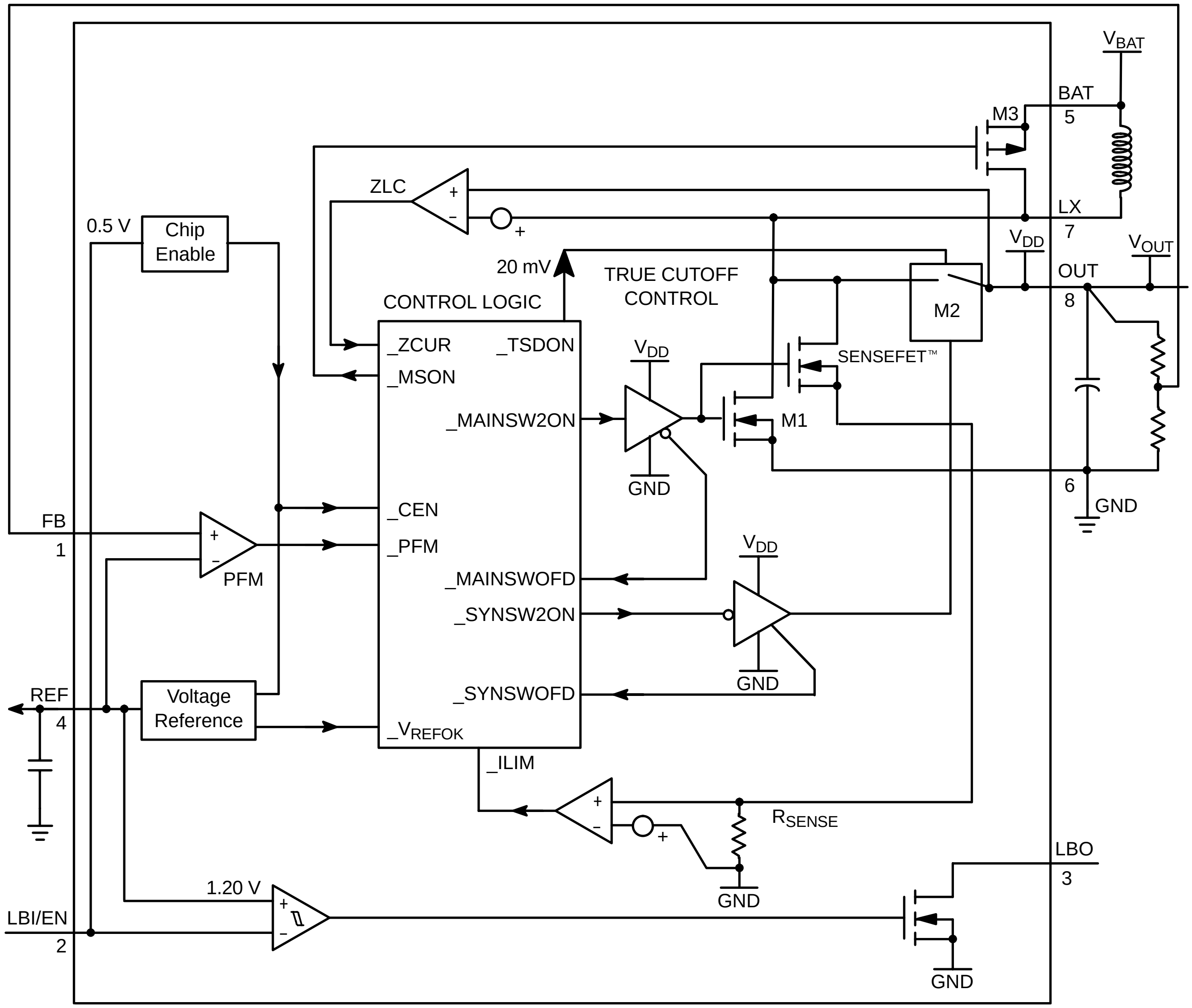


Figure 1. Detailed Block Diagram

PIN FUNCTION DESCRIPTIONS

Pin	Symbol	Description
1	FB	Output Voltage Feedback Input.
2	LBI/EN	Low-Battery Detector Input and IC Enable. With this pin pulled down below 0.5 V, the device is disabled and enters the shutdown mode.
3	LBO	Open-Drain Low-Battery Detector Output. Output is LOW when V_{LBI} is < 1.20 V. LBO is high impedance in shutdown mode.
4	REF	1.20 V Reference Voltage Output, bypass with 300 nF capacitor. If this pin is not loaded, bypass with 1.0 μF capacitor; this pin can be loaded up to 2.5 mA @ V_{OUT} = 3.3 V.
5	BAT	Battery input connection for internal ring-killer.
6	GND	Ground.
7	LX	N-Channel and P-Channel Power MOSFET drain connection.
8	OUT	Power Output. OUT also provides bootstrap power to the device.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply (Pin 8)	V_{OUT}	-0.3, 5.5	V
Input/Output Pins Pin 1-5, Pin 7	V_{IO}	-0.3, 5.5	V
Thermal Characteristics Micro8 Plastic Package Thermal Resistance Junction-to-Air	 P_D $R_{\theta JA}$	 520 240	 mW °C/W
Operating Junction Temperature Range	T_J	-40 to +150	°C
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

1. This device contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114. *Except OUT pin, which is 1k V.
   Machine Model (MM) ±200 V per JEDEC standard: JESD22-A115. *Except OUT pin, which is 100 V.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

3. Latch-up Current Maximum Rating: ±150 mA per JEDEC standard: JESD78.
4. Moisture Sensitivity Level: MSL 1 per IPC/JEDEC standard: J-STD-020A.

ELECTRICAL CHARACTERISTICS (V_{OUT} = 3.3 V, T_A = 25°C for typical value, -40°C ≤ T_A ≤ 85°C for min/max values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{IN}	1.0	-	5.0	V
Output Voltage Range	V_{OUT}	1.5	-	5.0	V
Reference Voltage (V_{OUT} = 3.3 V, I_{LOAD} = 0 μA, C_{REF} = 200 nF, T_A = 25°C)	V_{REF_NL}	1.183	1.200	1.217	V
Reference Voltage (V_{OUT} = 3.3 V, I_{LOAD} = 0 μA, C_{REF} = 200 nF, T_A = -40°C to 85°C)	V_{REF_NL}	1.174	-	1.220	V
Reference Voltage Temperature Coefficient	TC_{VREF}	-	0.03	-	mV/°C
Reference Voltage Load Current (V_{OUT} = 3.3 V, V_{REF} = V_{REF_NL} ±1.5% C_{REF} = 1.0 μF) (Note 5)	I_{REF}	-	2.5	-	mA
Reference Voltage Load Regulation (V_{OUT} = 3.3 V, I_{LOAD} = 0 to 100 μA, C_{REF} = 1.0 μF)	V_{REF_LOAD}	-	0.05	1.0	mV
Reference Voltage Line Regulation (V_{OUT} from 1.5 V to 5.0 V, C_{REF} = 1.0 μF)	V_{REF_LINE}	-	0.05	1.0	mV/V
FB Input Threshold (I_{LOAD} = 0 mA, T_A = 25°C)	V_{FB}	1.192	1.200	1.208	V
FB Input Threshold (I_{LOAD} = 0 mA, T_A = -40°C to 85°C)	V_{FB}	1.184	-	1.210	V
LBI Input Threshold (I_{LOAD} = 0 mA, T_A= -40°C to 85°C)	V_{LBI}	1.162		1.230	V
LBI Input Threshold (T_A = 25°C)	V_{LBI}	1.182	1.200	1.218	V
Internal NFET ON-Resistance	$R_{DS(ON)\_N}$	-	0.3	-	Ω
Internal PFET ON-Resistance	$R_{DS(ON)\_P}$	-	0.3	-	Ω
LX Switch Current Limit (N-FET) (Note 7)	I_{LIM}	-	1.5	-	A
Operating Current into BAT (V_{BAT} = 1.8 V, V_{FB} = 1.8 V, V_{LX} = 1.8 V, V_{OUT} = 3.3 V)	I_{QBAT}	-	1.3	3	μA
Operating Current into OUT (V_{FB} = 1.4 V, V_{OUT} = 3.3 V)	I_Q	-	8.5	14	μA
LX Switch MAX. ON-Time (V_{FB} = 1.0 V, V_{OUT} = 3.3 V, T_A = 25°C)	t_{ON}	0.46	0.72	1.15	μs
LX Switch MIN. OFF-Time (V_{FB} = 1.0 V, V_{OUT} = 3.3 V, T_A = 25°C)	t_{OFF}	-	0.12	0.22	μs
FB Input Current	I_{FB}	-	1.0	50	nA
True-Cutoff Current into BAT (LBI/EN = GND, V_{OUT} = 0, V_{IN} = 3.3 V, LX = 3.3 V)	I_{BAT}	-	50	-	nA
BAT-to-LX Resistance (V_{FB} = 1.4 V, V_{OUT} = 3.3 V) (Note 7)	R_{BAT_LX}	-	100	-	Ω
LBI/EN Input Current	I_{LBI}	-	1.5	50	nA

5. Loading capability increases with V_{OUT}.

ELECTRICAL CHARACTERISTICS (V_{OUT} = 3.3 V, T_A = 25°C for typical value, -40°C ≤ T_A ≤ 85°C for min/max values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
LBO Low Output Voltage (V_{LBI} = 0, I_{SINK} = 1.0 mA)	V_{LBO_L}	-	-	0.2	V
Soft Start Time (V_{IN} = 2.5 V, V_{OUT} = 5.0 V, C_{REF} = 200 nF) (Note 6)	T_{SS}	-	1.5	20	ms
EN Pin Shutdown Threshold (T_A = 25°C)	V_{SHDN}	0.35	0.5	0.67	V
Thermal Shutdown Temperature (Note 7)	T_{SHDN}	-	-	145	°C
Thermal Shutdown Hysteresis (Note 7)	T_{SDHYS}	-	30	-	°C

6. Design guarantee, value depends on voltage at V_{OUT}.
7. Values are design guaranteed.

TYPICAL OPERATING CHARACTERISTICS

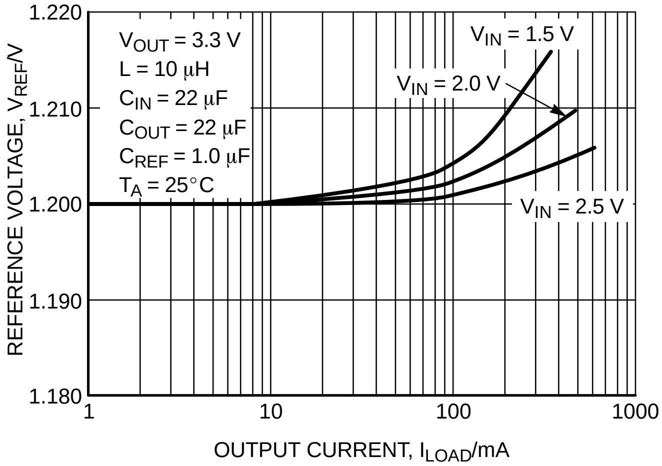


Figure 2. Reference Voltage vs. Output Current

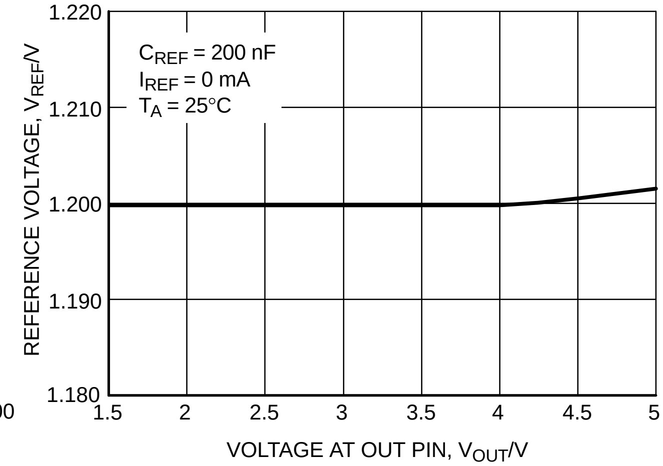


Figure 3. Reference Voltage vs. Voltage at OUT Pin

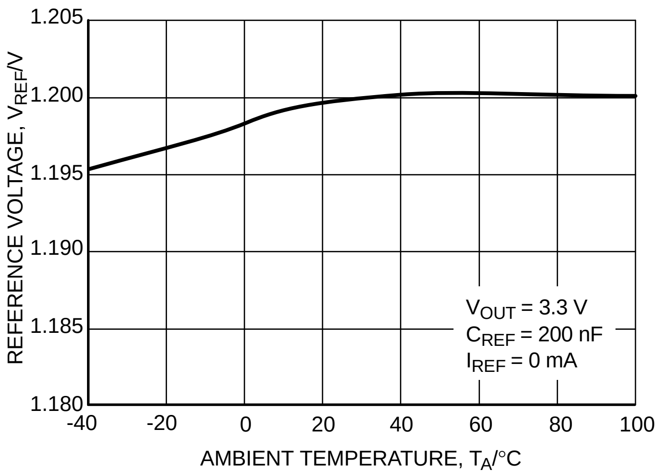


Figure 4. Reference Voltage vs. Temperature

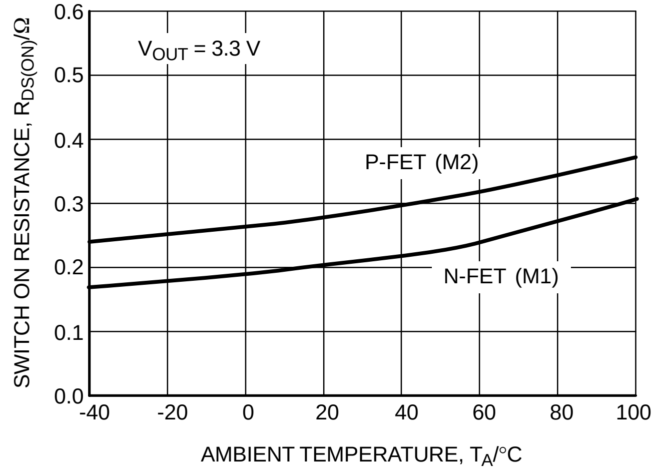


Figure 5. Switch ON Resistance vs. Temperature

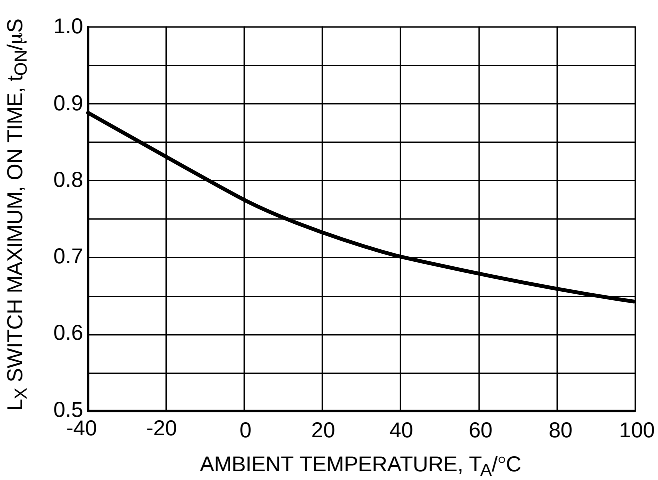


Figure 6. L_X Switch Max. ON Time vs. Temperature

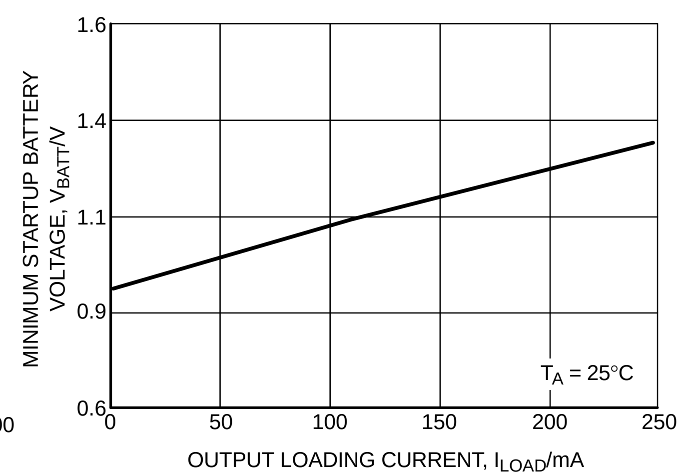


Figure 7. Minimum Startup Battery Voltage vs. Loading Current

TYPICAL OPERATING CHARACTERISTICS

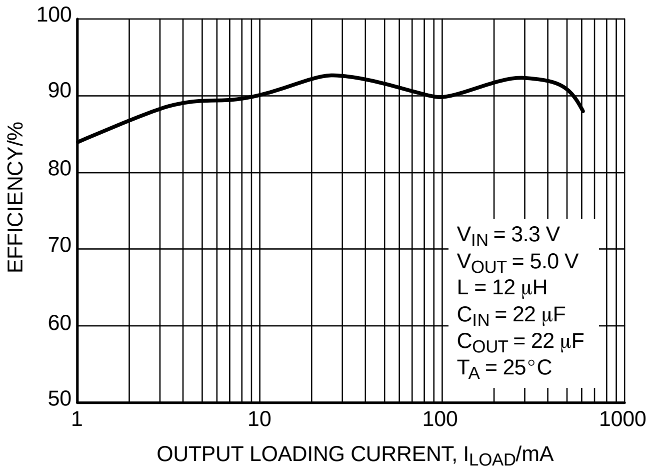


Figure 8. Efficiency vs. Load Current

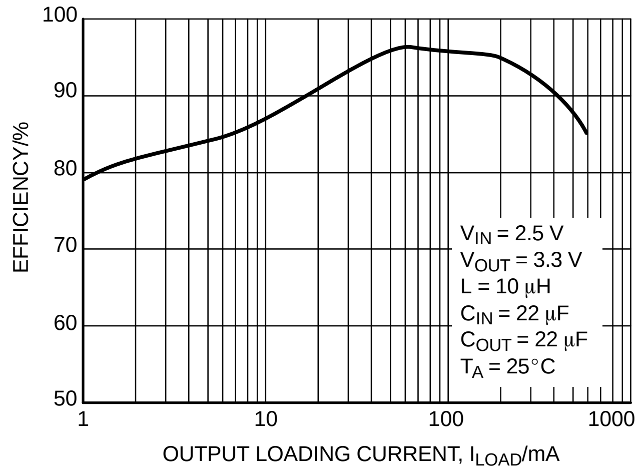


Figure 9. Efficiency vs. Load Current

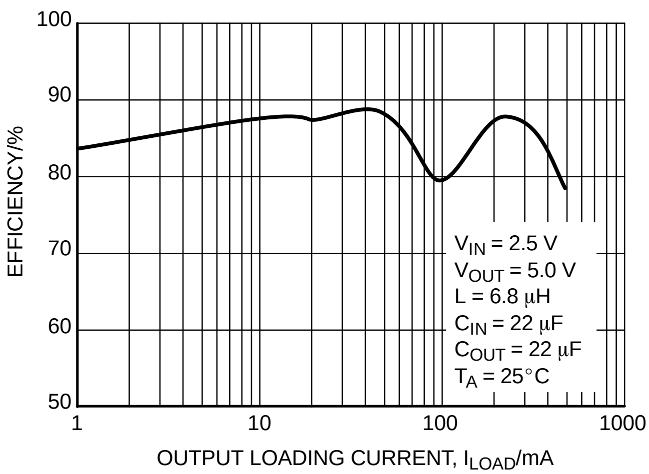


Figure 10. Efficiency vs. Load Current

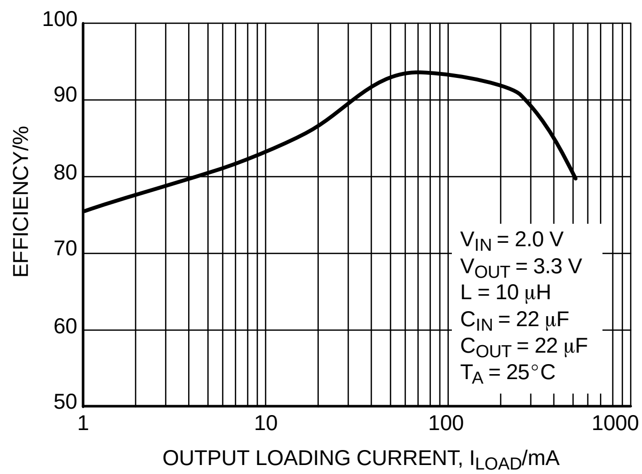


Figure 11. Efficiency vs. Load Current

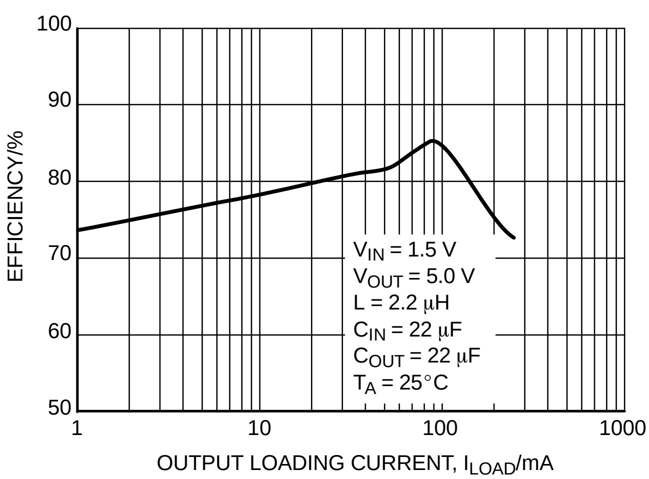


Figure 12. Efficiency vs. Load Current

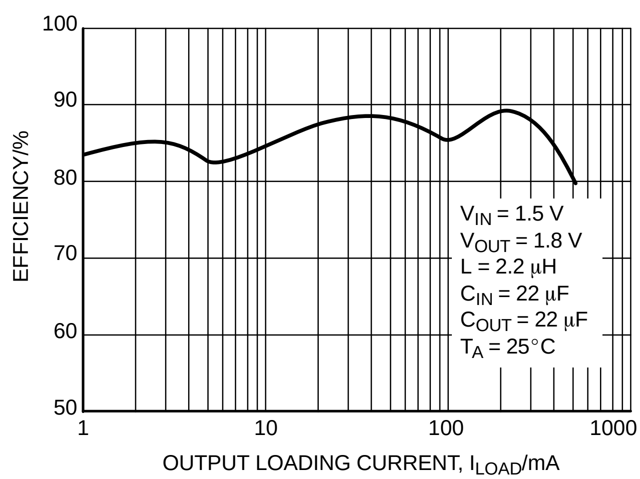


Figure 13. Efficiency vs. Load Current

TYPICAL OPERATING CHARACTERISTICS

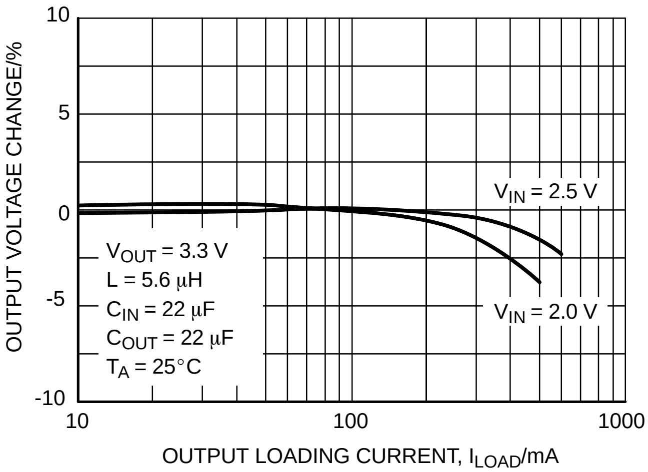


Figure 14. Output Voltage Change vs. Load Current

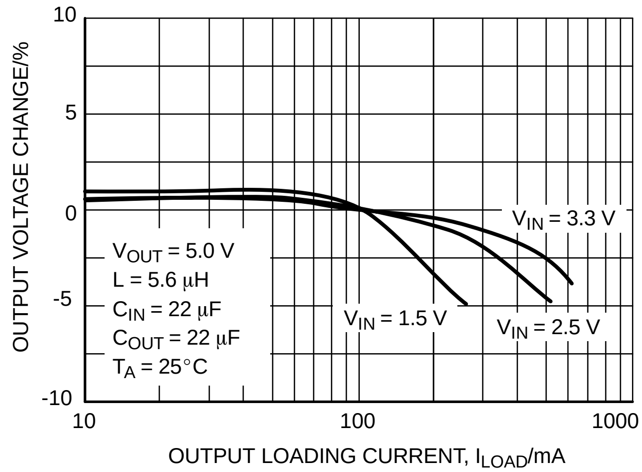


Figure 15. Output Voltage Change vs. Load Current

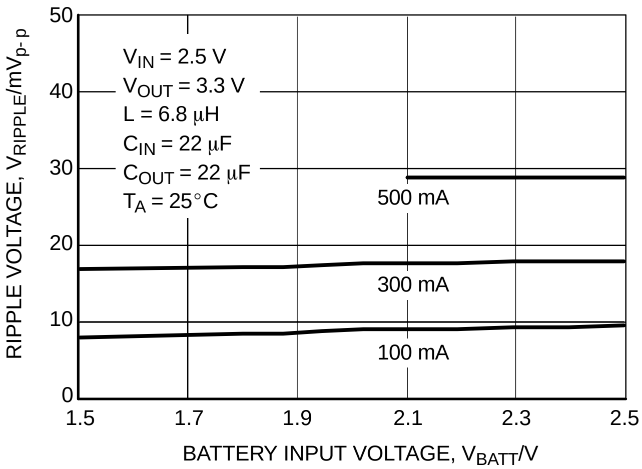
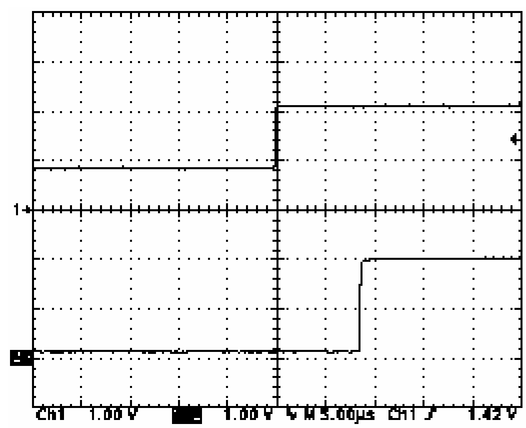


Figure 16. Battery Input Voltage vs. Output Ripple Voltage



Upper Trace: Voltage at LBI Pin, 1.0 V/Division
Lower Trace: Voltage at LBO Pin, 1.0 V/Division

Figure 17. Low Battery Detect

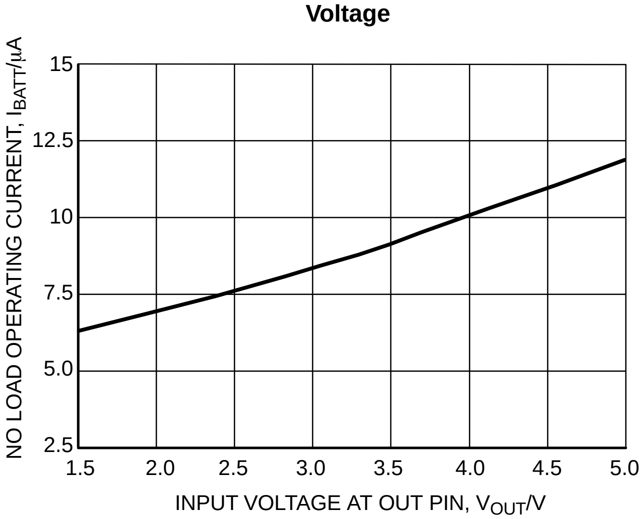
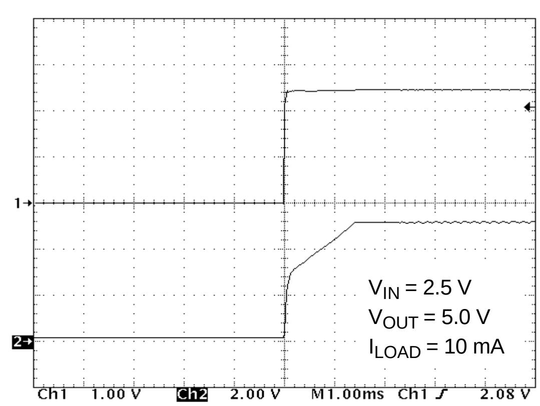


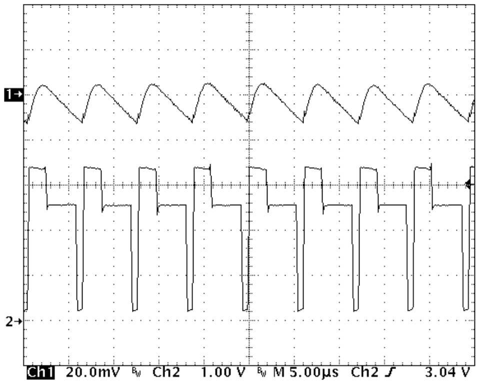
Figure 18. No Load Operating Current vs. Input Voltage at OUT Pin



Upper Trace: Input Voltage Waveform, 1.0 V/Division
Lower Trace: Output Voltage Waveform, 2.0 V/Division

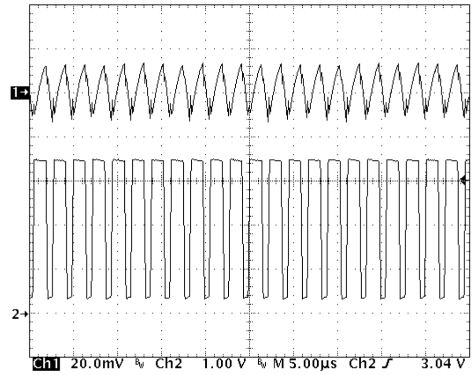
Figure 19. Startup Transient Response

TYPICAL OPERATING CHARACTERISTICS



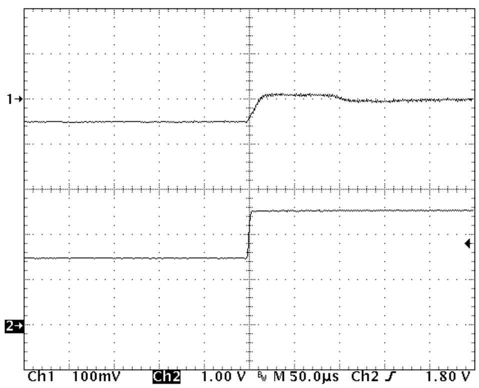
(V_{IN} = 2.5 V, V_{OUT} = 3.3 V, I_{LOAD} = 50 mA; L = 5.6 μH, C_{OUT} = 22 μF)
Upper Trace: Output Voltage Ripple, 20 mV/Division
Lower Trace: Voltage at Lx pin, 1.0 V/Division

Figure 20. Discontinuous Conduction Mode Switching Waveform



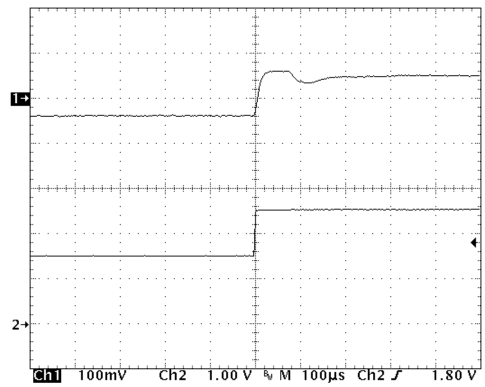
(V_{IN} = 2.5 V, V_{OUT} = 3.3 V, I_{LOAD} = 500 mA; L = 5.6 μH, C_{OUT} = 22μF)
Upper Trace: Output Voltage Ripple, 20 mV/Division
Lower Trace: Voltage at LX pin, 1.0 V/Division

Figure 21. Continuous Conduction Mode Switching Waveform



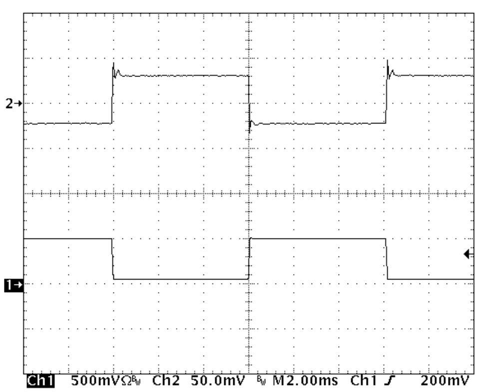
(V_{IN} = 1.5 V to 2.5 V; L = 5.6 μH, C_{OUT} = 22μF, I_{LOAD} = 100 mA)
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Battery Voltage, $V_{IN,}$ 1.0 V/Division

Figure 22. Line Transient Response for V_{OUT} = 3.3 V



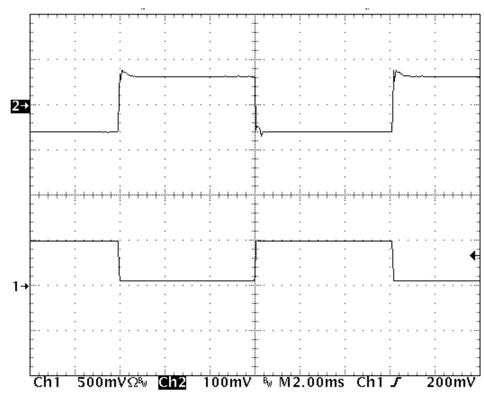
(V_{IN} = 1.5 V to 2.5 V; L = 5.6 μH, C_{OUT} = 22μF, I_{LOAD} = 100 mA)
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Battery Voltage, $V_{IN,}$ 1.0 V/Division

Figure 23. Line Transient Response For V_{OUT} = 5.0 V



(V_{OUT} = 3.3 V, I_{LOAD} = 50 mA to 500 mA; L = 5.6 μH, C_{OUT} = 22 μF)
Upper Trace: Output Voltage Ripple, 50 mV/Division
Lower Trace: Load Current, I_{LOAD}, 500 mA/Division

Figure 24. Load Transient Response For V_{IN} = 2.5 V



(V_{OUT} = 5.0 V, I_{LOAD} = 50 mA to 500 mA; L = 5.6 μH, C_{OUT} = 22 μF)
Upper Trace: Output Voltage Ripple, 100 mV/Division
Lower Trace: Load Current, I_{LOAD}, 500 mA/Division

Figure 25. Load Transient Response For V_{IN} = 3.0 V

DETAILED OPERATION DESCRIPTION

NCP1421 is a monolithic micropower high-frequency step-up voltage switching converter IC specially designed for battery operated hand-held electronic products up to 600 mA loading. It integrates a Synchronous Rectifier to improve efficiency as well as to eliminate the external Schottky diode. High switching frequency (up to 1.2 MHz) allows for a low profile inductor and output capacitor to be used. Low-Battery Detector, Logic-Controlled Shutdown, and Cycle-by-Cycle Current Limit provide value-added features for various battery-operated applications. With all these functions ON, the quiescent supply current is typically only 8.5 μA. This device is available in a compact Micro8 package.

PFM Regulation Scheme

From the simplified functional diagram (Figure 1), the output voltage is divided down and fed back to pin 1 (FB). This voltage goes to the non-inverting input of the PFM comparator whereas the comparator's inverting input is connected to the internal voltage reference, REF. A switching cycle is initiated by the falling edge of the comparator, at the moment the main switch (M1) is turned ON. After the maximum ON-time (typically 0.72 μS) elapses or the current limit is reached, M1 is turned OFF and the synchronous switch (M2) is turned ON. The M1 OFF time is not less than the minimum OFF-time (typically 0.12 μS), which ensures complete energy transfer from the inductor to the output capacitor. If the regulator is operating in continuous conduction mode (CCM), M2 is turned OFF just before M1 is supposed to be ON again. If the regulator is operating in discontinuous conduction mode (DCM), which means the coil current will decrease to zero before the new cycle starts, M1 is turned OFF as the coil current is almost reaching zero. The comparator (ZLC) with fixed offset is dedicated to sense the voltage drop across M2 as it is conducting; when the voltage drop is below the offset, the ZLC comparator output goes HIGH and M2 is turned OFF. Negative feedback of closed-loop operation regulates voltage at pin 1 (FB) equal to the internal reference voltage (1.20 V).

Synchronous Rectification

The Synchronous Rectifier is used to replace the Schottky Diode to reduce the conduction loss contributed by the forward voltage of the Schottky Diode. The Synchronous Rectifier is normally realized by powerFET with gate control circuitry that incorporates relatively complicated timing concerns.

As the main switch (M1) is being turned OFF and the synchronous switch M2 is just turned ON with M1 not being completely turned OFF, current is shunt from the output bulk capacitor through M2 and M1 to ground. This power loss lowers overall efficiency and possibly damages the switching FETs. As a general practice, a certain amount of dead time is introduced to make sure M1 is completely turned OFF before M2 is being turned ON.

The previously mentioned situation occurs when the regulator is operating in CCM, M2 is being turned OFF, M1 is just turned ON, and M2 is not being completely turned OFF. A dead time is also needed to make sure M2 is completely turned OFF before M1 is being turned ON.

As coil current is dropped to zero when the regulator is operating in DCM, M2 should be OFF. If this does not occur, the reverse current flows from the output bulk capacitor through M2 and the inductor to the battery input, causing damage to the battery. The ZLC comparator comes with fixed offset voltage to switch M2 OFF before any reverse current builds up. However, if M2 is switched OFF too early, large residue coil current flows through the body diode of M2 and increases conduction loss. Therefore, determination of the offset voltage is essential for optimum performance. With the implementation of the synchronous rectification scheme, efficiency can be as high as 94% with this device.

Cycle-by-Cycle Current Limit

In Figure 1, a SENSEFET is used to sample the coil current as M1 is ON. With that sample current flowing through a sense resistor, a sense-voltage is developed. The threshold detector (I_{LIM}) detects whether the sense-voltage is higher than the preset level. If the sense voltage is higher than the present level, the detector output notifies the Control Logic to switch OFF M1, and M1 can only be switched ON when the next cycle starts after the minimum OFF-time (typically 0.12 μS). With proper sizing of the SENSEFET and sense resistor, the peak coil current limit is typically set at 1.5 A.

Voltage Reference

The voltage at REF is typically set at 1.20 V and can output up to 2.5 mA with load regulation ±2% at V_{OUT} equal to 3.3 V. If V_{OUT} is increased, the REF load capability can also be increased. A bypass capacitor of 200 nF is required for proper operation when REF is not loaded. If REF is loaded, a 1.0 μF capacitor at the REF pin is needed.

True-Cutoff

The NCP1421 has a True-Cutoff function controlled by the multi-function pin LBI/EN (pin 2). Internal circuitry can isolate the current through the body diode of switch M2 to load. Thus, it can eliminate leakage current from the battery to load in shutdown mode and significantly reduce battery current consumption during shutdown. The shutdown function is controlled by the voltage at pin 2 (LBI/EN). When pin 2 is pulled to lower than 0.3 V, the controller enters shutdown mode. In shutdown mode, when switches M1 and M2 are both switched OFF, the internal reference voltage of the controller is disabled and the controller typically consumes only 50 nA of current. If the pin 2 voltage is raised to higher than 0.5 V (for example, by a resistor connected to V_{IN}), the IC is enabled again, and the internal circuit typically consumes 8.5 μA of current from the OUT pin during normal operation.

Low-Battery Detection

A comparator with 30 mV hysteresis is applied to perform the low-battery detection function. When pin 2 (LBI/EN) is at a voltage (defined by a resistor divider from the battery voltage) lower than the internal reference voltage of 1.20 V, the comparator output turns on a 50 Ω low side switch. It pulls down the voltage at pin 3 (LBO) which has hundreds of kΩ of pull-high resistance. If the pin 2 voltage is higher than 1.20 V + 30 mV, the comparator output turns off the 50 Ω low side switch. When this occurs, pin 3 becomes high impedance and its voltage is pulled high again.

APPLICATIONS INFORMATION

Output Voltage Setting

A typical application circuit is shown in Figure 26. The output voltage of the converter is determined by the external feedback network comprised of R1 and R2. The relationship is given by:

$$V_{OUT} = 1.20\ V \times \left(1 + \frac{R1}{R2}\right)$$

where R1 and R2 are the upper and lower feedback resistors, respectively.

Low Battery Detect Level Setting

The Low Battery Detect Voltage of the converter is determined by the external divider network that is comprised of R3 and R4. The relationship is given by:

$$V_{LB} = 1.20\ V \times \left(1 + \frac{R3}{R4}\right)$$

where R3 and R4 are the upper and lower divider resistors respectively.

Inductor Selection

The NCP1421 is tested to produce optimum performance with a 5.6 μH inductor at V_{IN} = 2.5 V and V_{OUT} = 3.3 V, supplying an output current up to 600 mA. For other input/output requirements, inductance in the range 3 μH to 10 μH can be used according to end application specifications. Selecting an inductor is a compromise between output current capability, inductor saturation limit, and tolerable output voltage ripple. Low inductance values can supply higher output current but also increase the ripple at output and reduce efficiency. On the other hand, high inductance values can improve output ripple and efficiency; however, it is also limited to the output current capability at the same time.

Another parameter of the inductor is its DC resistance. This resistance can introduce unwanted power loss and reduce overall efficiency. The basic rule is to select an inductor with the lowest DC resistance within the board space limitation of the end application. In order to help with the inductor selection, reference charts are shown in Figure 27 and 28.

Capacitors Selection

In all switching mode boost converter applications, both the input and output terminals see impulsive voltage/current waveforms. The currents flowing into and out of the capacitors multiply with the Equivalent Series Resistance (ESR) of the capacitor to produce ripple voltage at the terminals. During the Syn-Rect switch-off cycle, the charges stored in the output capacitor are used to sustain the output load current. Load current at this period and the ESR combine and reflect as ripple at the output terminals. For all cases, the lower the capacitor ESR, the lower the ripple voltage at output. As a general guideline, low ESR capacitors should be used. Ceramic capacitors have the lowest ESR, but low ESR tantalum capacitors can also be used as an alternative.

PCB Layout Recommendations

Good PCB layout plays an important role in switching mode power conversion. Careful PCB layout can help to minimize ground bounce, EMI noise, and unwanted feedback that can affect the performance of the converter. Hints suggested below can be used as a guideline in most situations.

Grounding

A star-ground connection should be used to connect the output power return ground, the input power return ground, and the device power ground together at one point. All high-current paths must be as short as possible and thick enough to allow current to flow through and produce insignificant voltage drop along the path. The feedback signal path must be separated from the main current path and sense directly at the anode of the output capacitor.

Components Placement

Power components (i.e., input capacitor, inductor and output capacitor) must be placed as close together as possible. All connecting traces must be short, direct, and thick. High current flowing and switching paths must be kept away from the feedback (FB, pin 1) terminal to avoid unwanted injection of noise into the feedback path.

Feedback Network

Feedback of the output voltage must be a separate trace detached from the power path. The external feedback network must be placed very close to the feedback (FB, pin 1) pin and sense the output voltage directly at the anode of the output capacitor.

TYPICAL APPLICATION CIRCUIT

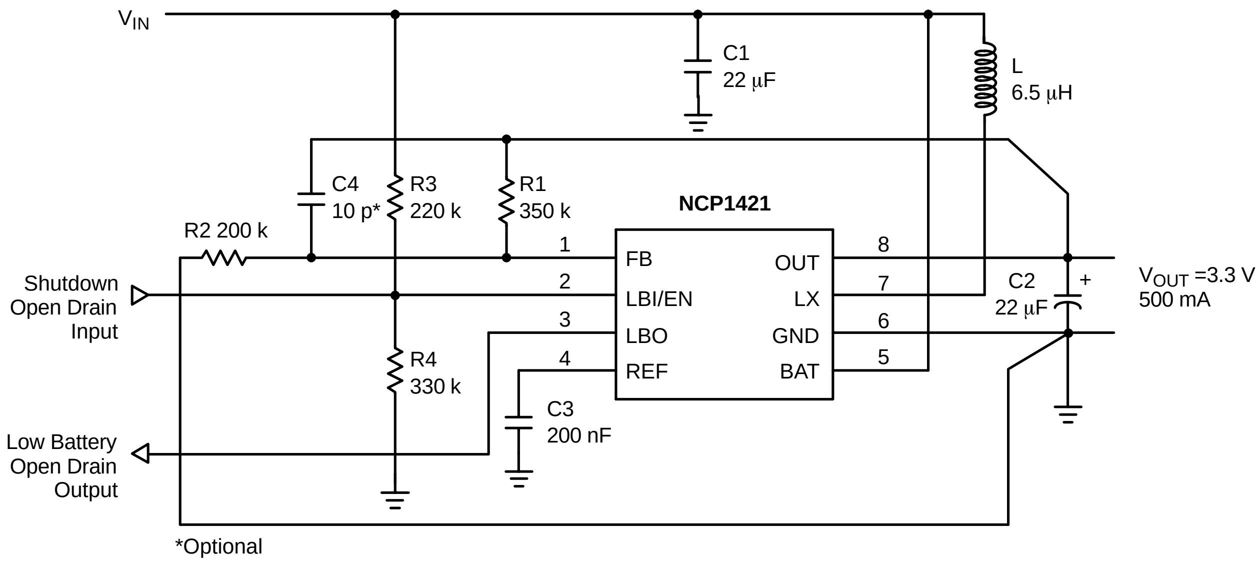


Figure 26. Typical Application Schematic for 2 Alkaline Cells Supply

GENERAL DESIGN PROCEDURES

Switching mode converter design is considered a complicated process. Selecting the right inductor and capacitor values can allow the converter to provide optimum performance. The following is a simple method based on the basic first-order equations to estimate the inductor and capacitor values for NCP1421 to operate in Continuous Conduction Mode (CCM). The set component values can be used as a starting point to fine tune the application circuit performance. Detailed bench testing is still necessary to get the best performance out of the circuit.

Design Parameters:

V_{IN} = 1.8 V to 3.0 V, Typical 2.4 V
V_{OUT} = 3.3 V
I_{OUT} = 500 mA (600 mA max)
V_{LB} = 2.0 V
$V_{OUT-RIPPLE}$ = 45 mV_{p-p} at I_{OUT} = 500 mA

Calculate the feedback network:

Select R2 = 200 k

$$R1 = R2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

$$R1 = 200\,k\left(\frac{3.3\,V}{1.20\,V} - 1\right) = 350\,k$$

Calculate the Low Battery Detect divider:

V_{LB} = 2.0 V
Select R4 = 330 k

$$R3 = R4\left(\frac{V_{LB}}{V_{REF}} - 1\right)$$

$$R3 = 300\,k\left(\frac{2.0\,V}{1.20\,V} - 1\right) = 220\,k$$

Determine the Steady State Duty Ratio, D, for typical V_{IN}. The operation is optimized around this point:

$$\frac{V_{OUT}}{V_{REF}} = \frac{1}{1 - D}$$

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{2.4\,V}{3.3\,V} - 1 = 0.273$$

Determine the average inductor current, I_{LAVG}, at maximum I_{OUT}:

$$I_{LAVG} = \frac{I_{OUT}}{1 - D} = \frac{500\,mA}{1 - 0.273} = 688\,mA$$

Determine the peak inductor ripple current, $I_{RIPPLE-P}$, and calculate the inductor value:

Assume $I_{RIPPLE-P}$ is 20% of I_{LAVG}. The inductance of the power inductor can be calculated as follows:

$$L = \frac{V_{IN} \times t_{ON}}{2\,I_{RIPPLE-P}} = \frac{2.4\,V \times 0.75\,\mu S}{2\,(137.6\,mA)} = 6.5\,\mu H$$

A standard value of 6.5 µH is selected for initial trial.

Determine the output voltage ripple, $V_{OUT-RIPPLE}$, and calculate the output capacitor value:

$V_{OUT-RIPPLE}$ = 40 mV_{P-P} at I_{OUT} = 500 mA

$$C_{OUT} > \frac{I_{OUT} \times t_{ON}}{V_{OUT-RIPPLE} - I_{OUT} \times ESR_{COUT}}$$

where t_{ON} = 0.75 uS and ESR_{COUT} = 0.05 Ω,

$$C_{OUT} > \frac{500\,mA \times 0.75\,\mu S}{45\,mV - 500\,mA \times 0.05\,\Omega} = 18.75\,\mu F$$

From the previous calculations, you need at least 18.75 µF in order to achieve the specified ripple level at the conditions stated. Practically, a capacitor that is one level larger is used to accommodate factors not taken into account in the calculations. Therefore, a capacitor value of 22 μF is selected. The NCP1421 is internally compensated for most applications, but in case additional compensation is required, the capacitor C4 can be used as external compensation adjustment to improve system dynamics.

In order to provide an easy way for customers to select external parts for NCP1421 in different input voltage and output current conditions, values of inductance and capacitance are suggested in Figure 27, 28 and 29.

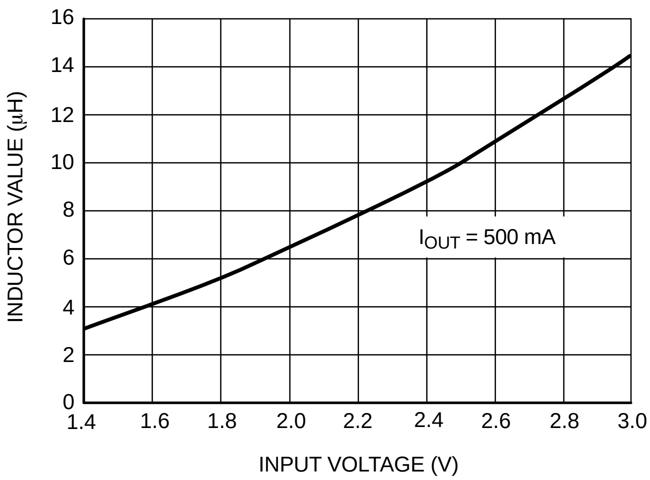


Figure 27. Suggested Inductance of V_{OUT} = 3.3 V

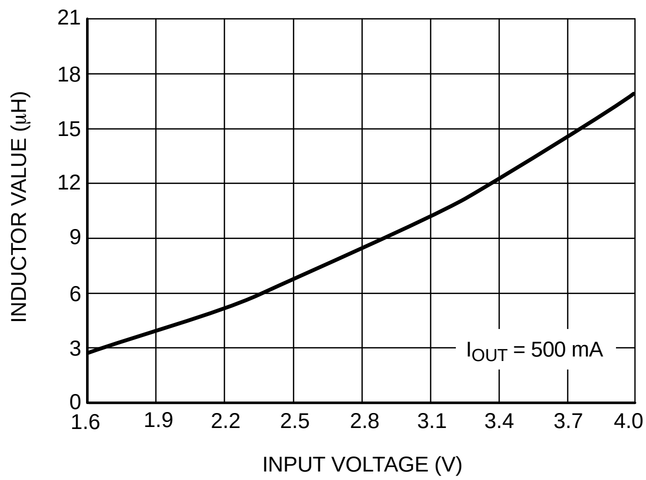


Figure 28. Suggested Inductance of V_{OUT} = 5.0 V

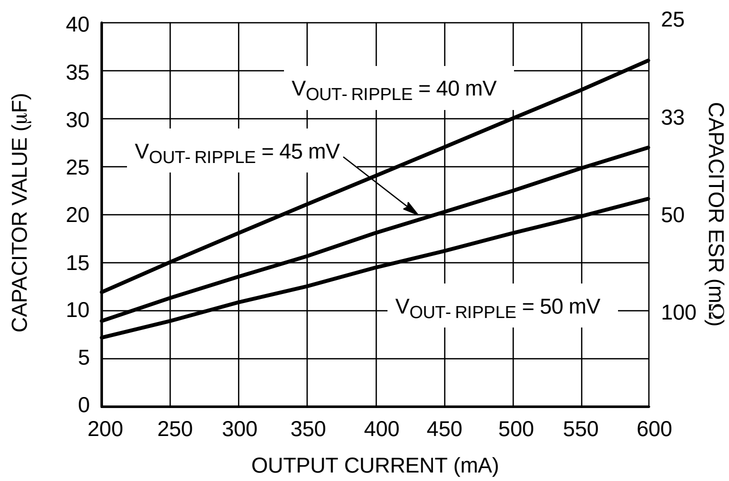


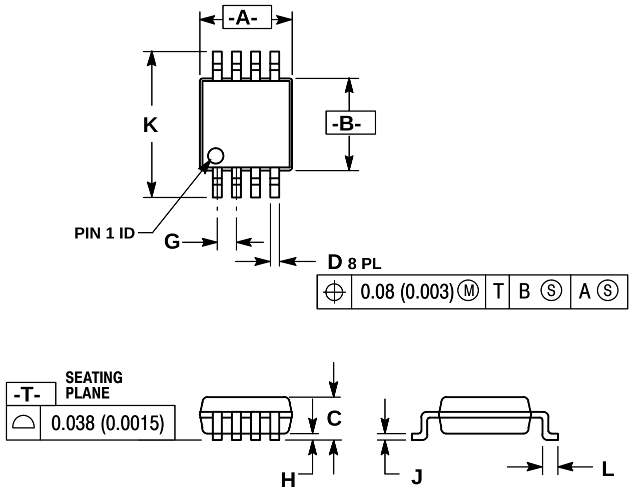
Figure 29. Suggested Capacitance for Output Capacitor

Table 1. Suggestions for Passive Components

Output Current	Inductors	Capacitors
500 mA	Sumida CR43, CR54,CDRH6D28 series	Panasonic ECJ series Kemet TL494 series
250 mA	Sumida CR32 series	Panasonic ECJ series Kemet TL494 series

PACKAGE DIMENSIONS

Micro8
DM SUFFIX
CASE 846A-02
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

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