

# PNP 2N5883, 2N5884\*, NPN 2N5885, 2N5886\*

Preferred Device

## Complementary Silicon High-Power Transistors

... designed for general-purpose power amplifier and switching applications.

- Low Collector-Emitter Saturation Voltage –  
 $V_{CE(sat)} = 1.0 \text{ Vdc}$ , (max) at  $I_C = 15 \text{ Adc}$
- Low Leakage Current  
 $I_{CEX} = 1.0 \text{ mAdc}$  (max) at Rated Voltage
- Excellent DC Current Gain –  
 $h_{FE} = 20$  (min) at  $I_C = 10 \text{ Adc}$
- High Current Gain Bandwidth Product –  
 $f_T = 4.0 \text{ MHz}$  (min) at  $I_C = 1.0 \text{ Adc}$

### MAXIMUM RATINGS (No

Rating	Symbol	2N5883 2N5885	2N5884 2N5886	Unit
Collector-Emitter Voltage	$V_{CEO}$	60	80	Vdc
Collector-Base Voltage	$V_{CB}$	60	80	Vdc
Emitter-Base Voltage	$V_{EB}$	5.0		Vdc
Collector Current – Continuous Peak	$I_C$	25 50		Adc
Base Current	$I_B$	7.5		Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.15		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200		$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$\theta_{JC}$	0.875	$^\circ\text{C}/\text{W}$

1. Indicates JEDEC registered data. Units and conditions differ on some parameters and re-registration reflecting these changes has been requested. All above values most or exceed present JEDEC registered data.

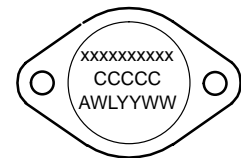
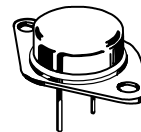


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## 25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60 – 80 V 200 W

### MARKING DIAGRAM



CASE 1-07  
TO-204AA  
(TO-3)

xx = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
CCCCC = Non USA Country Code

Preferred devices are recommended choices for future use and best overall value.

# PNP 2N5883, 2N5884\*, NPN 2N5885, 2N5886\*

**\*ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
Collector–Emitter Sustaining Voltage (Note 2) ( $I_C = 200\text{ mAdc}$ , $I_B = 0$ )	2N5883, 2N5885 2N5884, 2N5886	$V_{CEO(sus)}$	60 80	– –	Vdc
Collector Cutoff Current ( $V_{CE} = 30\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ )	2N5883, 2N5885 2N5984, 2N5886	$I_{CEO}$	– –	2.0 2.0	mAdc
Collector Cutoff Current ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{BE(off)} = 1.5\text{ Vdc}$ , $T_C = 150^\circ\text{C}$ )	2N5883, 2N5885 2N5884, 2N5886 2N5883, 2N5885 2N5884, 2N5886	$I_{CEX}$	– – – –	1.0 1.0 10 10	mAdc
Collector Cutoff Current ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ )	2N5883, 2N5885 2N5884, 2N5886	$I_{CBO}$	– –	1.0 1.0	mAdc
Emitter Cutoff Current ( $V_{EB} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	–	1.0	mAdc

## ON CHARACTERISTICS

DC Current Gain (Note 2)	( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ ) ( $I_C = 25\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$h_{FE}$	35 20 4.0	– 100	–
Collector–Emitter Saturation Voltage (Note 2)	( $I_C = 15\text{ Adc}$ , $I_B = 1.5\text{ Adc}$ ) ( $I_C = 25\text{ Adc}$ , $I_B = 6.25\text{ Adc}$ )	$V_{CE(sat)}$	– –	1.0 4.0	Vdc
Base–Emitter Saturation Voltage (Note 2)	( $I_C = 25\text{ Adc}$ , $I_B = 6.25\text{ Adc}$ )	$V_{BE(sat)}$	–	2.5	Vdc
Base–Emitter On Voltage (Note 2)	( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )	$V_{BE(on)}$	–	1.5	Vdc

## DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product (Note 3)	( $I_C = 1.0\text{ Adc}$ , $V_{CE} = 10\text{ Vdc}$ , $f_{test} = 1.0\text{ MHz}$ )	$f_T$	4.0	–	MHz
Output Capacitance ( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	2N5883, 2N5884 2N5885, 2N5886	$C_{ob}$	– –	1000 500	pF
Small–Signal Current Gain	( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ , $f_{test} = 1.0\text{ kHz}$ )	$h_{fe}$	20	–	–

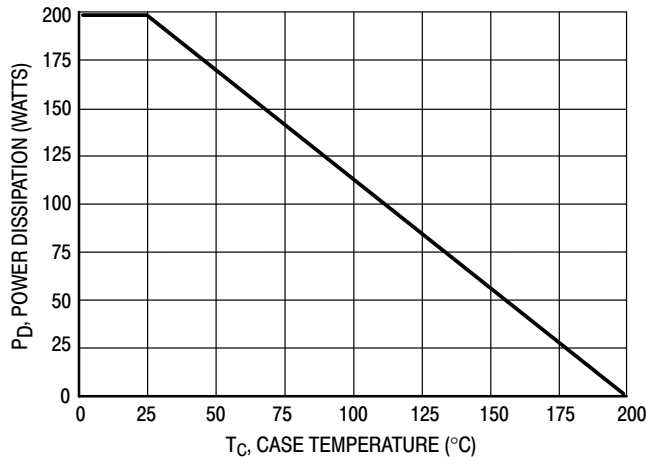
## SWITCHING CHARACTERISTICS

Rise Time	$(V_{CC} = 30\text{ Vdc}$ , $I_C = 10\text{ Adc}$ , $I_{B1} = I_{B2} = 1.0\text{ Adc}$ )	$t_r$	–	0.7	$\mu\text{s}$
Storage Time		$t_s$	–	1.0	$\mu\text{s}$
Fall Time		$t_f$	–	0.8	$\mu\text{s}$

\*Indicates JEDEC Registered Data.

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

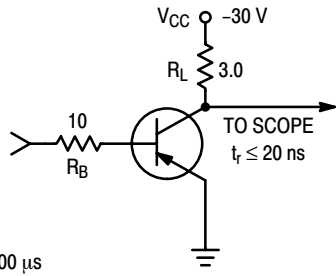
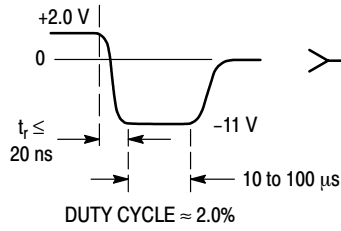
3.  $f_T = |h_{fe}| \cdot f_{test}$ .



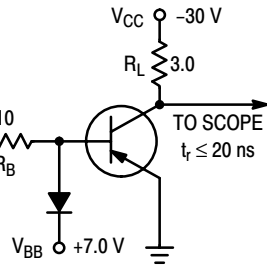
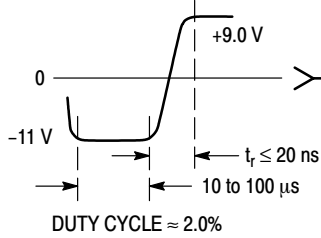
**Figure 1. Power Derating**

PNP 2N5883, 2N5884\*, NPN 2N5885, 2N5886\*

TURN-ON TIME



TURN-OFF TIME



FOR CURVES OF FIGURES 3 & 6,  $R_B$  &  $R_L$  ARE VARIED.  
 INPUT LEVELS ARE APPROXIMATELY AS SHOWN.  
 FOR NPN, REVERSE ALL POLARITIES.

Figure 2. Switching Time Equivalent Test Circuits

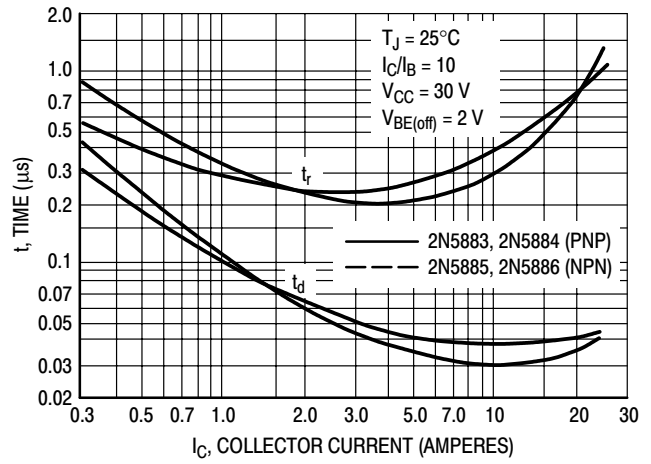


Figure 3. Turn-On Time

PNP 2N5883, 2N5884\*, NPN 2N5885, 2N5886\*

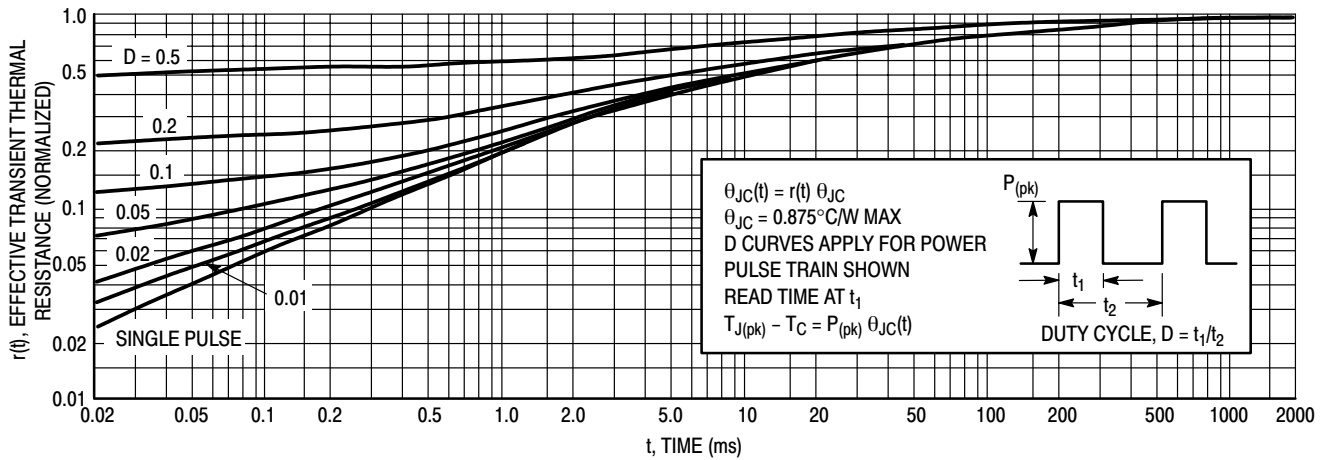


Figure 4. Thermal Response

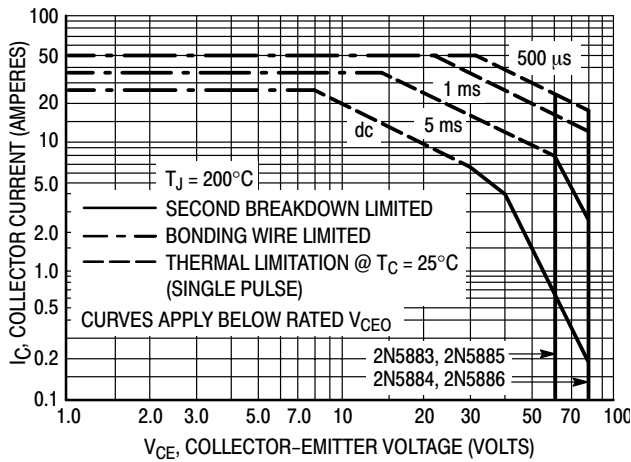


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

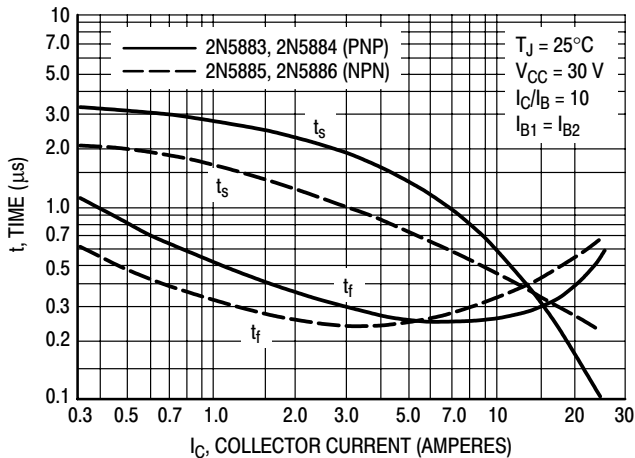


Figure 6. Turn-Off Time

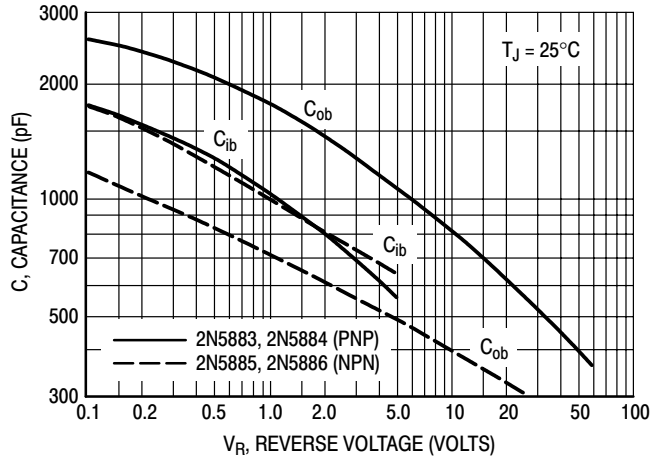


Figure 7. Capacitance

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## PNP DEVICES 2N5883 and 2N5884

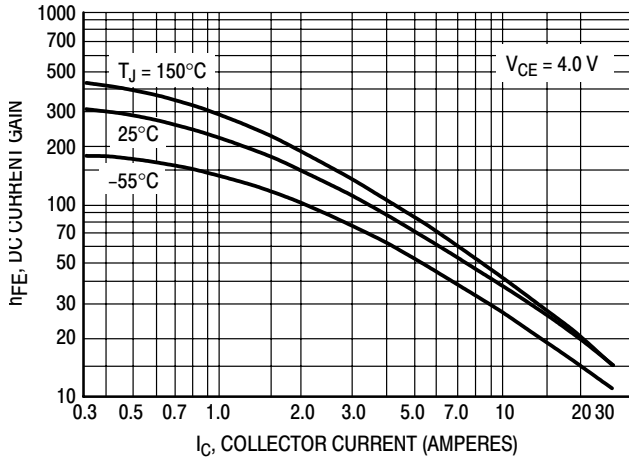


Figure 8. DC Current Gain

## NPN DEVICES 2N5885 and 2N5886

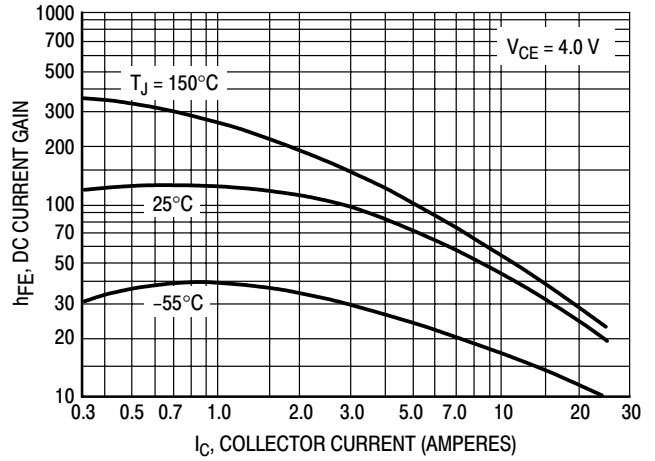


Figure 9. DC Current Gain

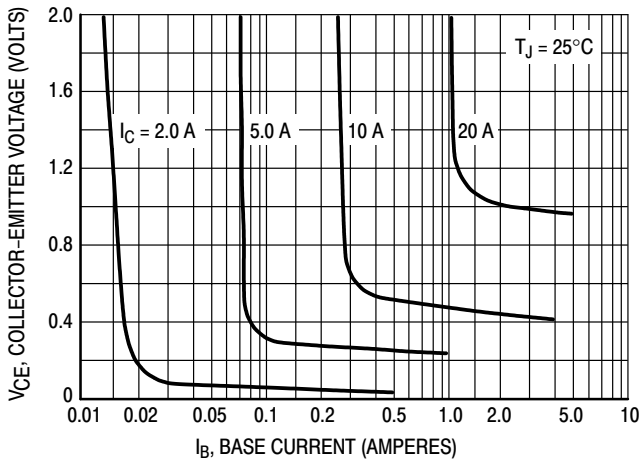


Figure 10. Collector Saturation Region

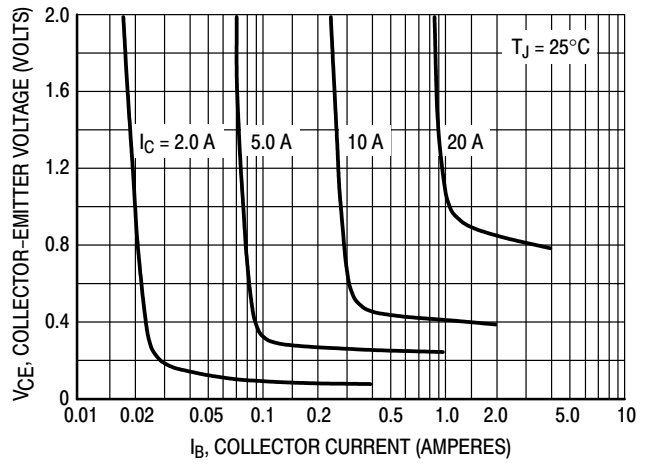


Figure 11. Collector Saturation Region

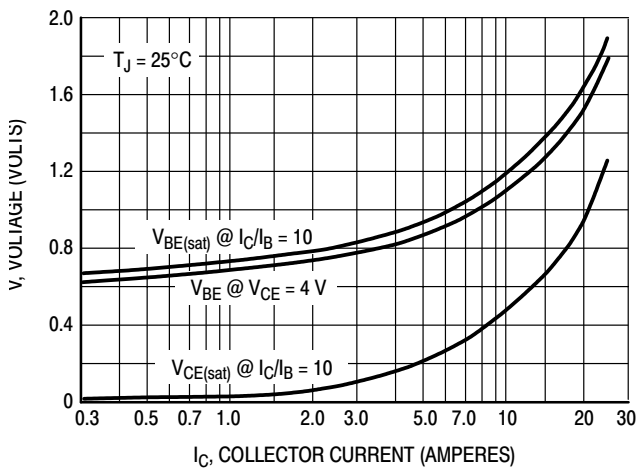


Figure 12. "On" Voltages

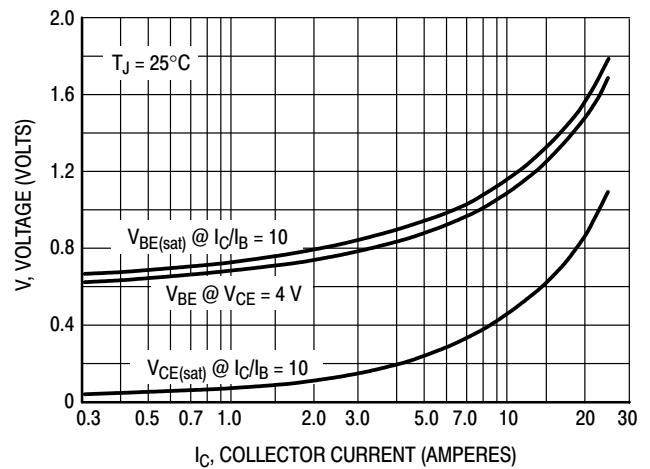
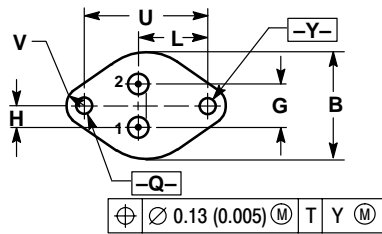
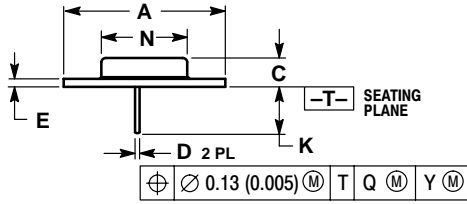


Figure 13. "On" Voltages

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PACKAGE DIMENSIONS

CASE 1-07  
TO-204AA (TO-3)  
ISSUE Z



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

- STYLE 1:
1. PIN 1. BASE
  2. EMITTER
- CASE: COLLECTOR

## Notes

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