# NIS5102

# High Side SMART HotPlug™ IC/Inrush Limiter/Circuit Breaker

The NIS5102 is a controller/FET IC that saves design time and reduces the number of components required for a complete hot swap application. It is designed for +12 V applications.

This chip includes a time delay for sequencing applications. It has a dual function OVLO pin that allows multiple units to be ganged together for simultaneous turn−on and shutdown, allowing units to be operated in parallel. It allows for user selectable undervoltage and overvoltage lockout levels. Its unique current limit circuit allows for adjustable current limit levels with no external power resistor. An internal temperature limiting circuit greatly increases the reliability of this device.

### Features

- Integrated Power Device
- Power Device Thermally Protected
- No External Current Shunt Required
- Simultaneous Shutdown and Startup for Parallel Operation
- Enable/Timer Pin
- Power Good
- 9.0 to 18 V Input Range
- 10 mΩ
- Main/Mirror MOSFET Current Ratio 1000:1
- Pb−Free Packages are Available

### Typical Applications

- High Availability Systems
- Electronic Circuit Breaker
- 12 V Distributed Architecture

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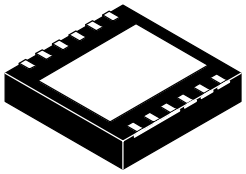
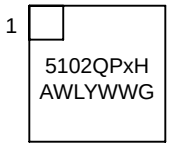


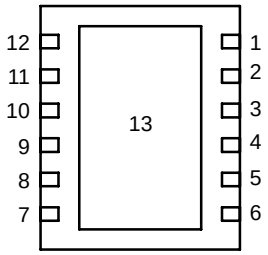
**9x9 MM, 12 PIN PLLP**
**CASE 488AB**

**MARKING DIAGRAM**




| | |
|---|---|
| x | = 1 or 2 |
| A | = Assembly Location |
| WL | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free |

**PIN CONNECTIONS**




(Bottom View)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NIS5102QP1HT1 (Latchoff) | 9x9 mm 12 Pin PLLP | 1500/Tape & Reel |
| NIS5102QP1HT1G (Latchoff) | 12 Pin PLLP (Pb−Free) | 1500/Tape & Reel |
| NIS5102QP2HT1 (Auto−Retry) | 9x9 mm 12 Pin PLLP | 1500/Tape & Reel |
| NIS5102QP2HT1G (Auto−Retry) | 12 Pin PLLP (Pb−Free) | 1500/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

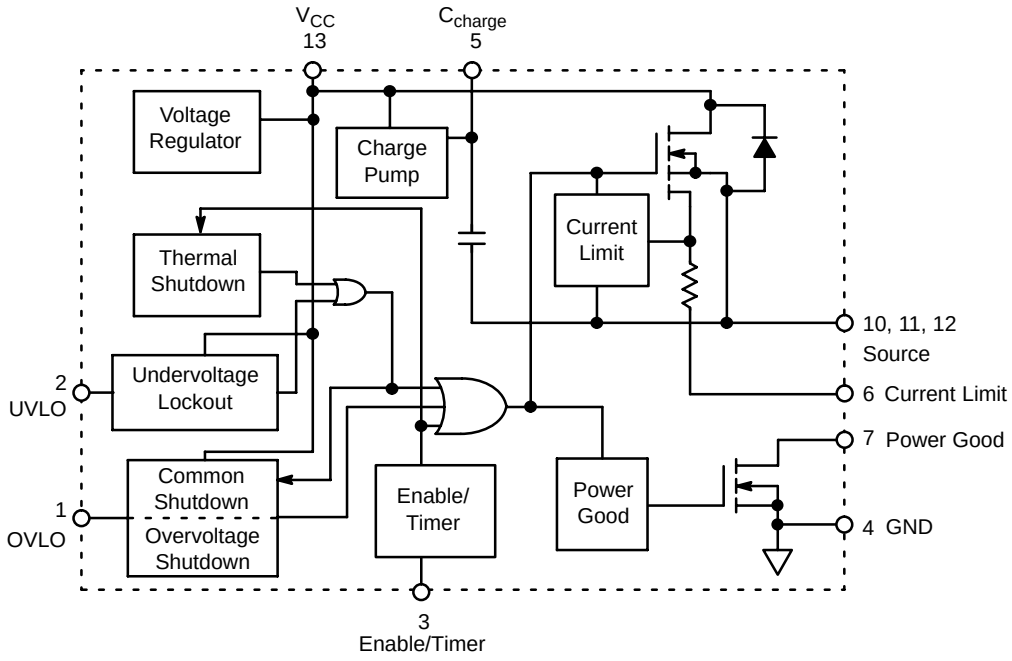



**Figure 1. Block Diagram**

**PIN FUNCTION DESCRIPTION**

| Pin | Function | Description |
|---|---|---|
| 1 | OVLO | The overvoltage shutdown point is programmed by a resistor from this pin to the $V_{CC}$ supply. When tied together with other devices, this pin also communicates a shutdown state due to undervoltage and overtemperature reasons. All devices connected will simultaneously shutdown. Startup for this condition may be simultaneous or sequenced. |
| 2 | UVLO | A resistor from $V_{CC}$ to the UVLO pin adjusts the voltage at which the device will turn on. |
| 3 | Enable/Timer | A high level signal on this pin allows the device to begin operation. Connection of a capacitor will delay turn on for timing purposes. A low input signal inhibits the operation, and communicates to any other paralleled devices (via the OVLO pin) to shutdown. This signal can also be used to reset the thermal latch. |
| 4 | Ground | Negative input voltage to the device. This is used as the internal reference for the IC. |
| 5 | $C_{charge}$ | An external capacitor is required from this pin to the source pin. This is the storage capacitor for the internal charge pump. A small internal capacitor is included for noise filtering. |
| 6 | $I_{LIMIT}$ | A resistor ($R_{LIMIT}$) tied from this pin to the source pin sets the current limit level. |
| 7 | Power Good | A high impedance signal on this pin indicates that the power device is conducting. |
| 8, 9 | No Connection | − |
| 10, 11, 12 | Source | Source of power FET, which is also the switching node for the load. |
| 13 | $V_{CC}$ | Positive input voltage to the device. |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage, Operating, Steady−State (Input + to Input −) | $V_{in}$ | −0.3 to 18 | V |
| Input Voltage, Operating, Transient (Input + to Input −), 1 second | $V_{in}$ | −0.3 to 25 | V |
| Drain Voltage, Operating, Steady−State (Drain to Input −) | $V_{DD}$ | −0.3 to 18 | V |
| Drain Voltage, Operating, Transient (Drain to Input −), 1 second | $V_{DD}$ | −0.3 to 25 | V |
| Drain Current, Peak | $I_{Dpk}$ | 20 | A |
| Continuous Current ($T_A$ = 25°C, 0.5 in$^2$ pad) | $I_{Davg}$ | 10 | A |
| Voltage on Power Good Pin (Pin 7) | $V_{max7}$ | 20 | V |
| Thermal Resistance, Junction−to−Air<br>0.5 in$^2$ Copper<br>1 in$^2$ Copper | $Q_{JA}$ | <br>76.5<br>41.2 | <br>°C/W<br>°C/W |
| Thermal Resistance, Junction−to−Lead | $Q_{JL}$ | 3.2 | °C/W |
| Power Dissipation ($T_A$ = 25°C, 0.5 in$^2$ pad) | $P_{max}$ | 1.4 | W |
| Operating Temperature Range (Note 1) | $T_J$ | −40 to 175 | °C |
| Non−Operating Temperature Range | $T_J$ | −55 to 175 | °C |
| Lead Temperature, Soldering (10 Sec) | $T_L$ | 235 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Actual maximum junction temperature is limited by an internal protection circuit and will not reach the absolute maximum temperature as specified.

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 12 V, $R_{LIMIT}$ = 36 Ω, $C_{Charge}$ = 100 pF, $T_J$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER FET** | | | | | |
| Delay Time (Enable High to $I_S$ = 100 mA) | $T_{dly}$ | − | 2.0 | − | ms |
| Charging Time ($I_S$ = 100 mA to $I_S$ = 5.0 A, $R_{LIMIT}$ = 36 Ω) | $t_{chg}$ | − | 1.0 | − | ms |
| ON Resistance ($V_{CC}$ = 12 V, $I_S$ = 5.0 A) (Note 2) | $R_{DSon}$ | − | 10 | 13 | mΩ |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 12 $V_{dc}$, $V_{GS}$ = 0 $V_{dc}$) | $I_{DSS1}$ | − | − | 10 | μA |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 18 $V_{dc}$, $V_{GS}$ = 0 $V_{dc}$) | $I_{DSS2}$ | − | − | 100 | μA |
| Output Capacitance ($V_{DS}$ = 12 $V_{dc}$, $V_{GS}$ = 0 $V_{dc}$, f = 10 kHz) | − | − | − | − | pF |
| **THERMAL LIMIT** | | | | | |
| Shutdown Temperature (Note 3) | $T_{SD}$ | 125 | 135 | 145 | °C |
| Hysteresis (Note 3) | $T_{hyst}$ | − | 40 | − | °C |
| **OVER/UNDERVOLTAGE** | | | | | |
| UVLO Turn−on (Input + Increasing, $Rext_{UVLO}$ = 620 k) | $V_{on}$ | 10.05 | 11.15 | 12.30 | V |
| UVLO Hysteresis (Input + Decreasing, $Rext_{UVLO}$ = 620 k) | $V_{hyst}$ | 0.45 | 0.62 | 0.75 | V |
| OVLO Turn−off (Input + Increasing, $Rext_{UVLO}$ = 620 k) | $V_{off}$ | 14.0 | 16.4 | 19.0 | V |
| OVLO Hysteresis (Input + Decreasing, $Rext_{UVLO}$ = 620 k) | $V_{hyst}$ | 0.6 | 0.78 | 1.0 | V |
| **PARALLEL SHUTDOWN** (Alternate Function on OVLO Pin) | | | | | |
| Device Fan−out (Minimum External Resistor Value = 2.0 kΩ (Note 3) | $N_{fan}$ | − | − | 4.0 | Devices |
| Shutdown Voltage Threshold (OVLO Pin) | $V_{SD}$ | 0.6 | 0.8 | − | V |
| Shutdown State Output Voltage (Isink = 2.0 mA) | $V_{low}$ | − | 0.3 | 0.4 | V |

2. Pulse Test: Pulse width 300 μs, duty cycle 2%.
3. Verified by design.

**ELECTRICAL CHARACTERISTICS (continued)** ($V_{CC}$ = 12 V, $R_{LIMIT}$ = 36 Ω, $C_{Charge}$ = 100 pF, $T_J$ = 25°C unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **CURRENT LIMIT** | | | | | |
| Current Limit (Short Circuit, $R_{LIMIT}$ = 36 Ω) | $I_{LIM1}$ | 3.8 | 4.8 | 5.8 | A |
| Current Limit (Overload, $R_{LIMIT}$ = 36 Ω) (Note 3) | $I_{LIM2}$ | 7.0 | 7.8 | 8.6 | A |
| **ENABLE/TIMER** | | | | | |
| Enable Voltage (Turn−On) | $V_{ENon}$ | 2.2 | − | − | V |
| Enable Voltage (Turn−Off) | $V_{ENoff}$ | − | − | 1.6 | V |
| Charging Current (Into External Capacitor) | $I_{Charge}$ | 65 | 77 | 88 | μA |
| Turn−on Delay (Time from Enable High to $I_{source}$ = 100 mA) | $t_{delay}$ | − | 2.2 | − | ms |
| **CHARGE PUMP** | | | | | |
| $C_{Charge}$ (Voltage on Pin 5 with Respect to Ground)<br>$V_{CC}$ = 18 Vdc | $V_{Ccharge}$ | −<br>− | 18<br>26 | −<br>− | V<br>V |
| **POWER GOOD** | | | | | |
| Power Good → High Z Signal when FET is Fully Enhanced | − | − | − | − | − |
| Low Z State Output Voltage ($I_{Sink}$ = 2 mA) | Vpin7 | − | 230 | 300 | mV |
| Leakage Current (Vpin7 = 12 V, High Z State) | $I_{Leak}$ | − | 2.0 | 10 | μA |
| Power Good Delay<br>(Time from Power FET is Fully Enhanced to Power Good FET Changing State) | $t_{pwrgood}$ | − | 15 | − | ms |
| **TOTAL DEVICE** | | | | | |
| Bias Current (Operational, $V_{CC}$ = 12 V) | $I_{Bias}$ | − | 1.3 | 2.0 | mA |
| Bias Current (Non−operational, $V_{CC}$ = 7 V)) | $I_{Bias}$ | − | 400 | 700 | μA |
| Minimum Operating Voltage | $Vcc_{min}$ | − | 8.5 | 9.0 | V |

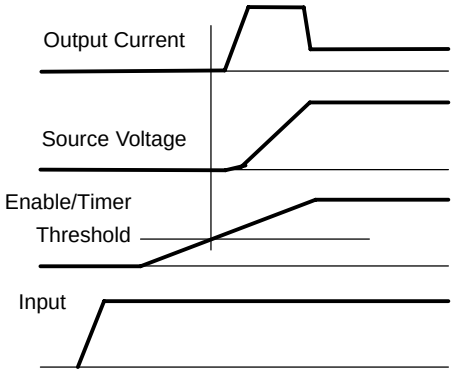



**Figure 2. Timing Diagram for External Enabled Delay**

## TYPICAL PERFORMANCE CURVES

($T_A$ = 25°C unless otherwise noted)

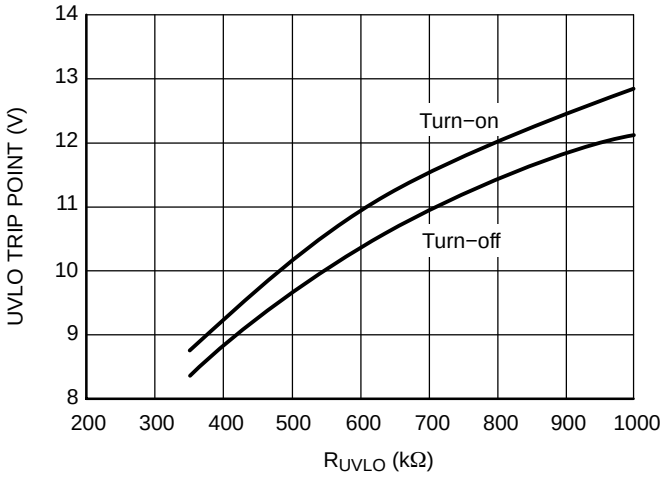



**Figure 3. UVLO Adjustment**

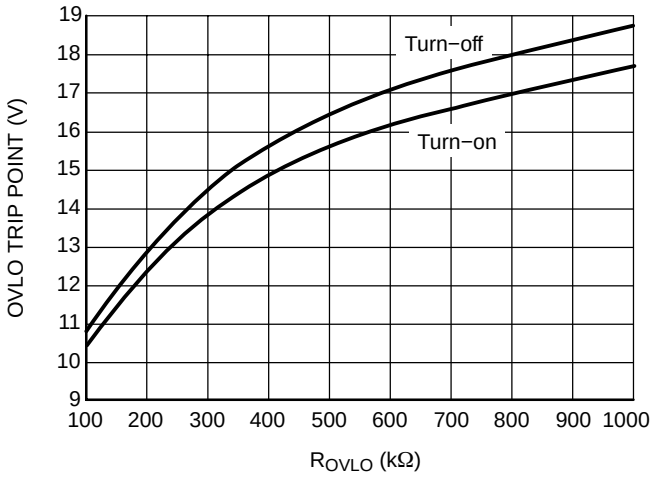



**Figure 4. OVLO Adjustment**

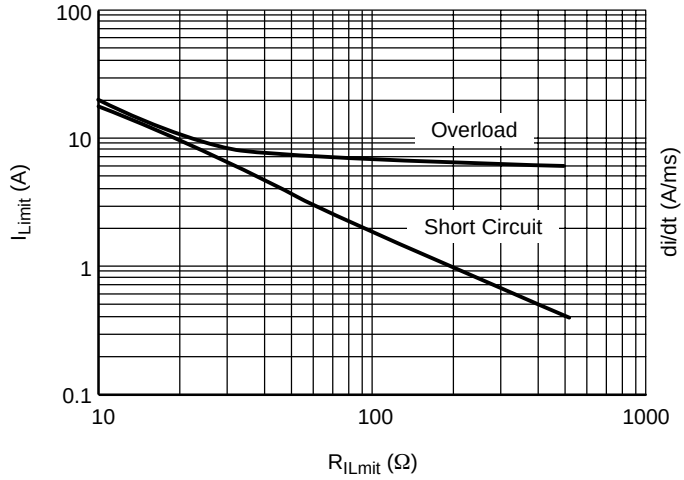



**Figure 5. Current Limit Adjustment**

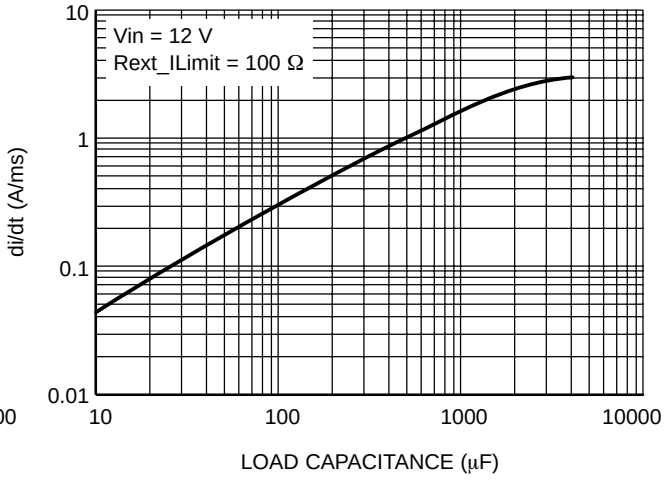



**Figure 6. Load Capacitance vs. Output di/dt**

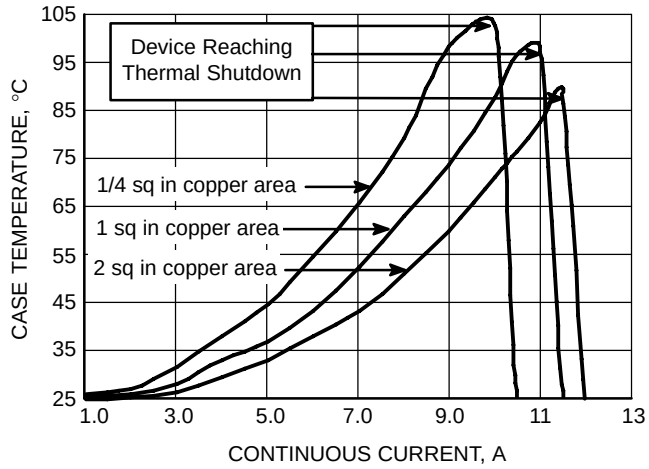



**Figure 7. Continuous Current vs. Case Temperature**
(Test performed on a double−sided copper board, 1 oz)

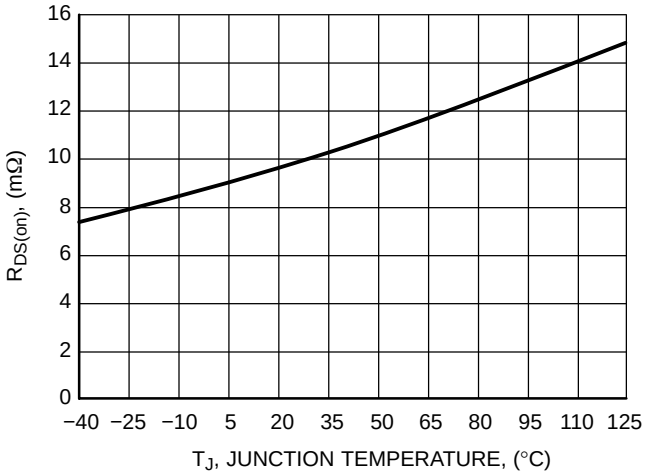



**Figure 8. Typical $R_{DS(on)}$ vs. Junction Temperature**

## TYPICAL APPLICATION CIRCUITS AND OPERATION WAVEFORMS

($T_A$ = 25°C unless otherwise noted)

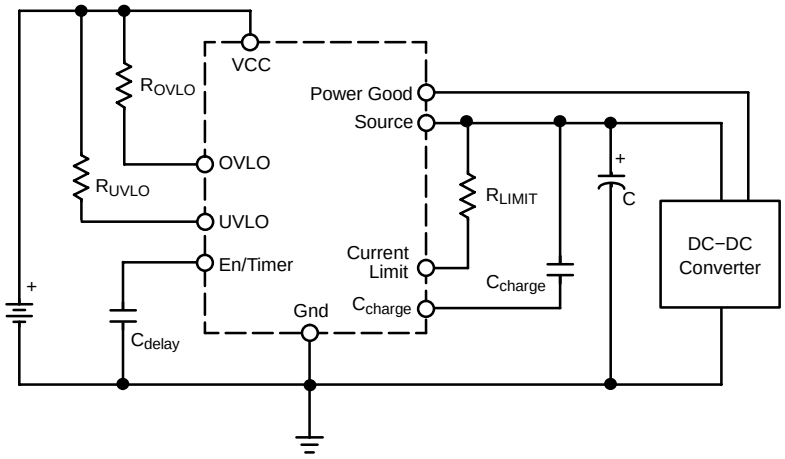



**Figure 9. Typical Applications Circuit**

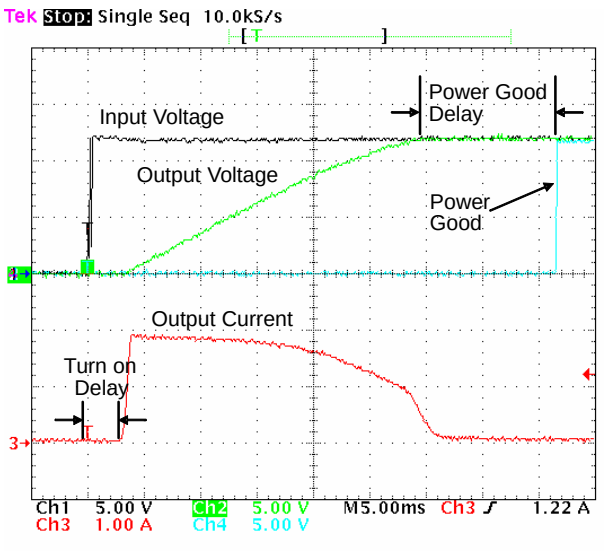



**Figure 10. Turn−on Waveforms for 3300 μF Load Capacitors**

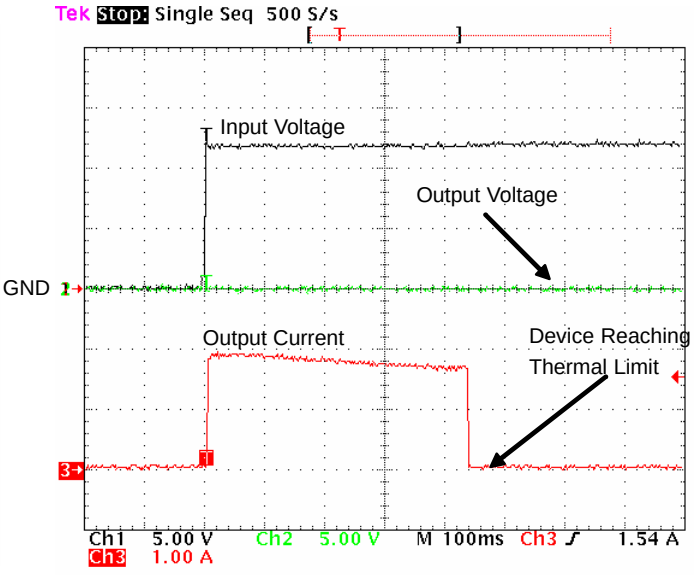



**Figure 11. Turn−on Waveforms for Shorted Output, Latchoff Device**

## TYPICAL APPLICATION CIRCUITS AND OPERATION WAVEFORMS (continued)

($T_A$ = 25°C unless otherwise noted)

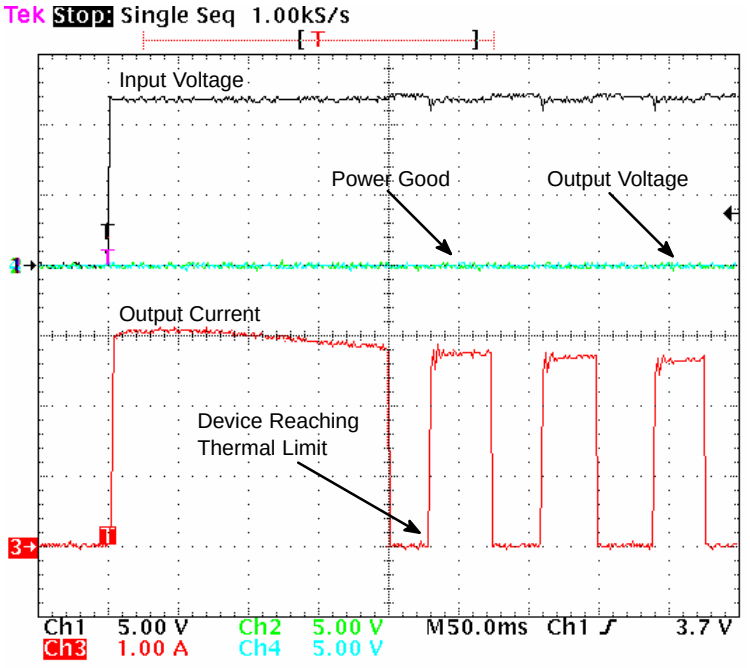



**Figure 12. Turn−On Waveforms for Shorted Output, Auto−Retry Device**

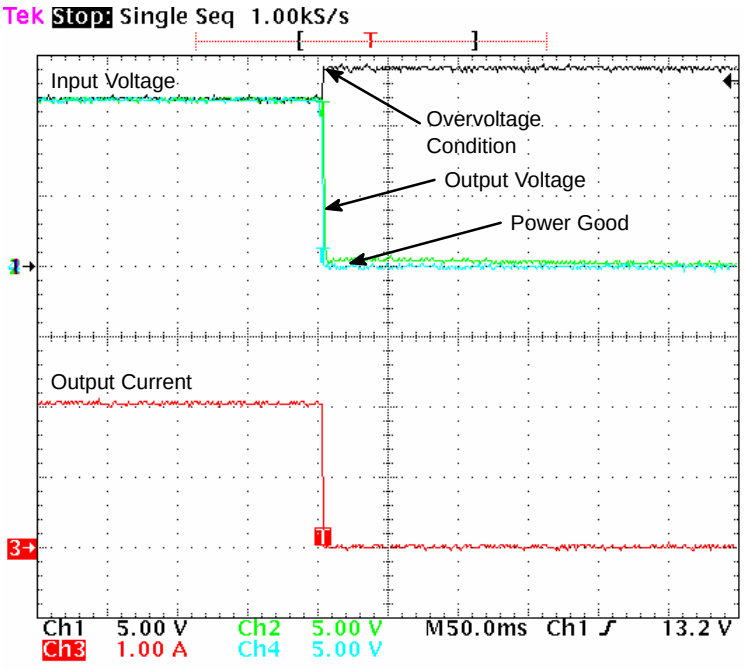



**Figure 13. Device Response During an Overvoltage Condition**

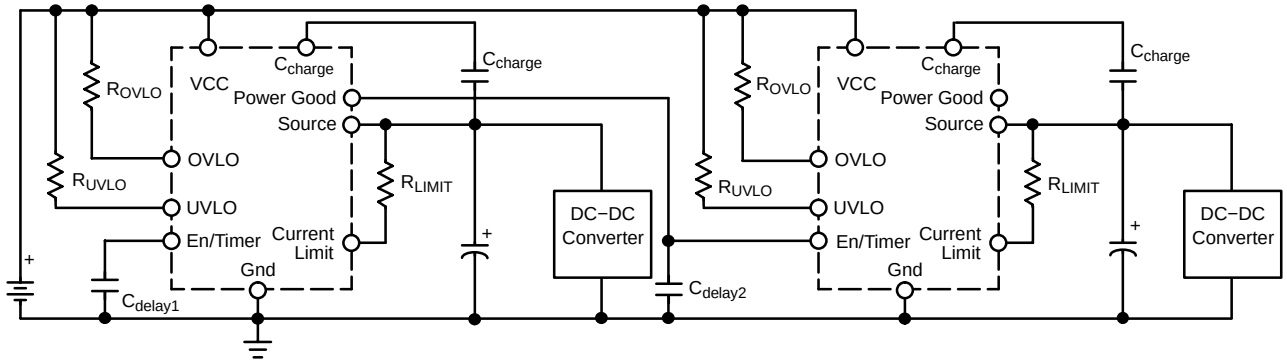



**Figure 14. Turn−on Sequencing Using Power Good Signal**

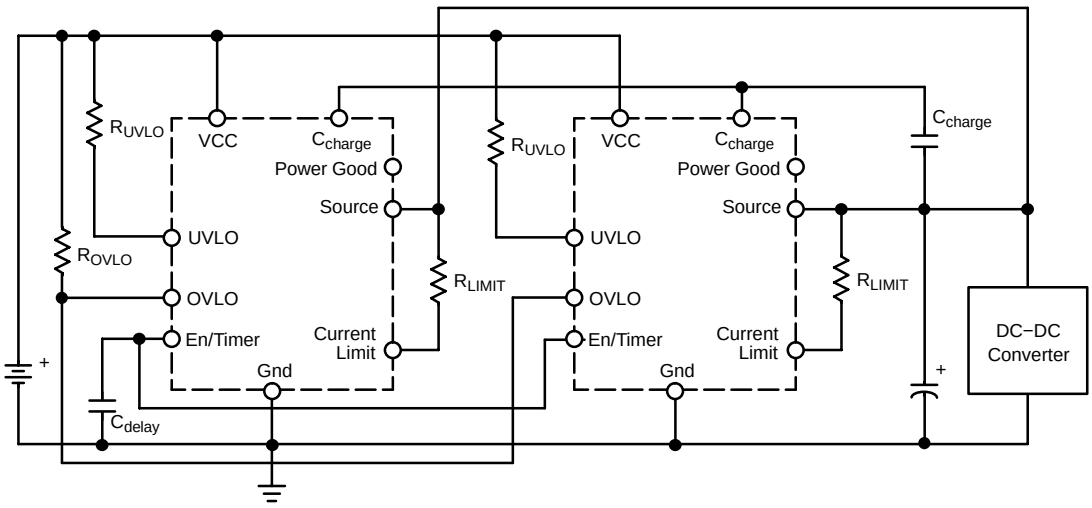



**Figure 15. Parallel Operation / Simultaneous Turn−on and Shutdown**

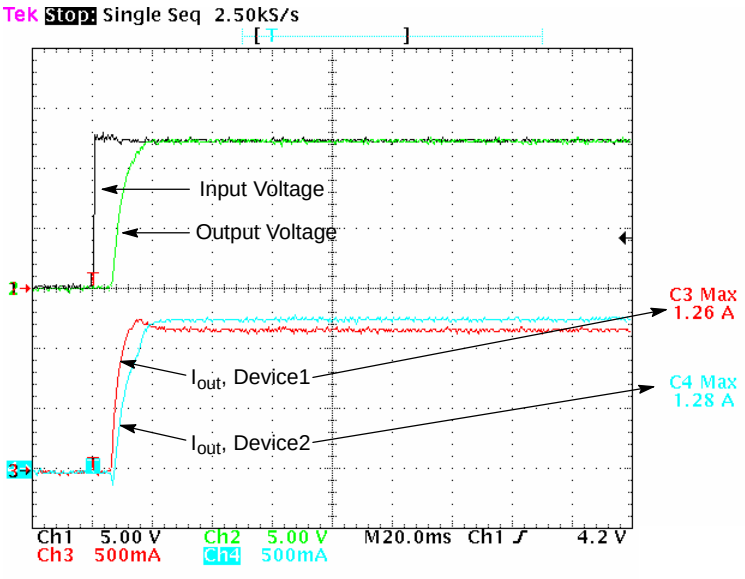



**Figure 16. Turn−on Waveforms for Parallel Operation**

## OPERATING DESCRIPTION

### Operation

The NIS5102 has a variety of shutdown and protection features that make this part extremely versatile as well as rugged. For the unit to operate, the input voltage must be within the operating range of the part which is set by the UVLO and OVLO bias resistors. The enable must also be high for operation. Current and thermal limit circuits constantly monitor the operation and will protect the unit if either of these parameters exceeds its preset limit.

An additional shutdown method, is the use of the OVLO pin, which can be tied in parallel. This allows multiple units to be either operated in parallel, and will shutdown and turn on simultaneously for any fault other than an overvoltage, or it allows these hot plug devices to control independent loads, and shutdown and turn on simultaneously.

### Faults

Once the load capacitance is charged, the SENSEFET™ will become fully enhanced as long as the current does not reach the current limit threshold, or is shutdown due to an overvoltage, undervoltage or thermal fault. Both the UVLO and OVLO circuits incorporate hysteresis to assure clean turn−on and turn−offs with no chatter. The thermal latching circuit will require the input power to be recycled to resume operation after a fault. The current limit is always active, so any transient or overload will always be limited.

### Circuit Description

#### Enable/Timer

The enable/timer pin can function either as a direct enable pin, or as a time delay. In the enable mode, an open collector device is connected to this pin. When the device is in its low impedance mode, this pin is low and the operation of the chip is disabled. If a time delay is required, a capacitor is added to this pin. Figure 17 shows the equivalent circuit for the enable.

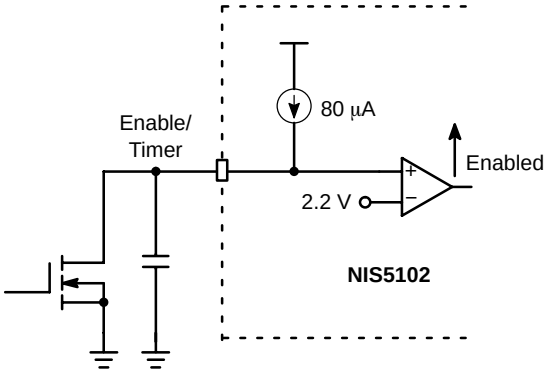



**Figure 17. Enable/Timer Circuit**

If a capacitor is added without an open collector device, the turn on will be delayed from the time at which the UVLO voltage is reached. If an open collector device is also used, the delay will start from the time that it goes into its high impedance state. The capacitor is charged by an internal current source.

There is an inherent delay in the turn on of the hot plug device, due to the method of gate drive used. The gate of the power FET is charged through a high impedance resistor, and from the time that the gate starts charging until the time that it reaches its threshold voltage, there will be no conduction. Once the gate reaches its threshold voltage, the output current will begin a controlled ramp up phase.

This delay will be added to any timing delay due to the enable/timer circuit.

#### Power Good

The power good circuit monitors the $V_{GS}$ voltage of the power SENSEFET and compares it with the output voltage of the internal charge pump. Once the $V_{GS}$ of the power SENSEFET reaches around 90% of the internal charge pump output voltage, the power good will change its state from low impedance to high impedance but only after the power good delay has elapsed. Figure 10 shows the power good behavior during the startup of the NIS5102 device, an external pullup resistor from power good to $V_{CC}$ was used.

The power good will change its state from high impedance to low impedance in the event of any fault condition such as short circuit and overvoltage.

#### Undervoltage Lockout

The UVLO circuit holds the chip off when the input voltage is less than the turn−on limit. It includes internal hysteresis to assure clean on/off switching. An internal divider sets the turn−on voltage level at 16 V. This voltage can be reduced by adding an external resistor from the UVLO pin to the $V_{CC}$ pin. The equivalent circuit is shown in Figure 18.

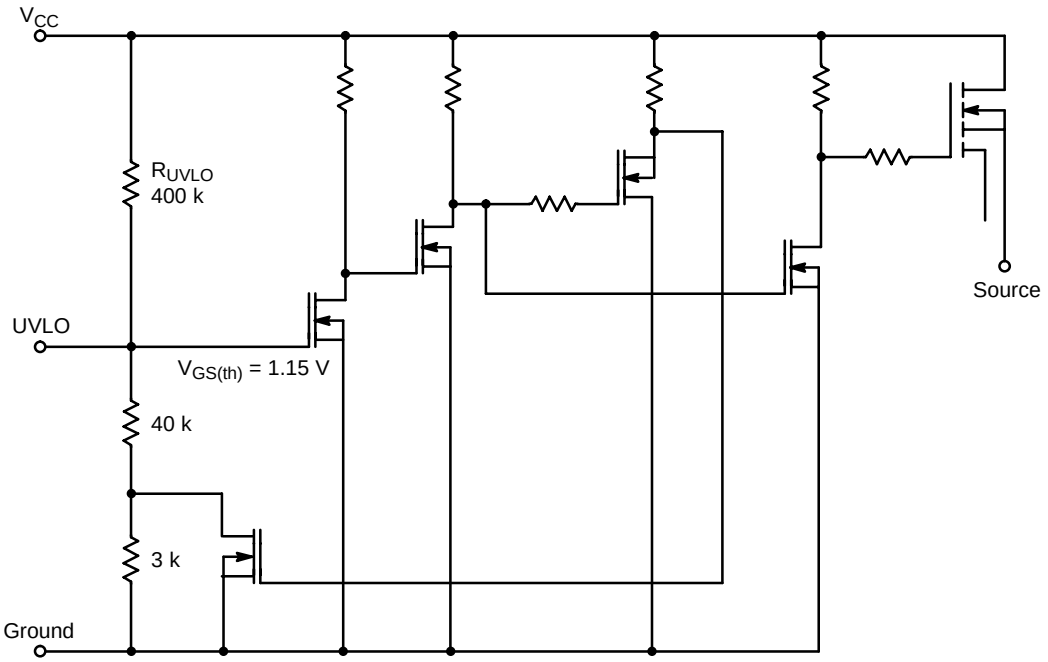



**Figure 18. Equivalent Undervoltage Lockout Circuit**

The theoretical equation for the UVLO turn−on voltage is:

$$R_{UVLO}\,(K\Omega) = \frac{400\,V_{in} - 460}{17.5 - V_{in}}$$

The UVLO trip point voltage calculated through the theoretical formula may show small variations with respect to Figure 3, therefore it is recommended to use the formulas gotten from the UVLO characterization, which are shown below:

$$R_{UVLO}\,(k\Omega) = e^{[(UVLO + 14.647)/3.9858]};\ \text{for}\ T_J = 25^{\circ}C$$

where “UVLO” is the desired undervoltage lockout value, and $R_{UVLO}$ is the programming resistor from the UVLO pin to the $V_{CC}$ pin.

To reduce nuisance tripping due to transients and noise spikes, a capacitor may be added from the UVLO pin to ground. This will create a low pass filter with a cutoff frequency of f. The required capacitance on this pin is:

$$C_{UVLO} = \frac{1}{2\pi \cdot f\left[43\ K + \left(\frac{R_{UVLO} \cdot 400\ K}{R_{UVLO} + 400\ K}\right)\right]}$$

**Overvoltage Lockout and Parallel Shutdown**

The overvoltage lockout (OVLO) is a dual function pin. This pin will normally be biased somewhere between ground and the input voltage, due to an internal voltage divider which sets the turn−off voltage level at 22 V. This voltage level can be reduced by adding an external resistor from the OVLO pin to the $V_{CC}$ pin. When the input voltage reaches the programmed trip point, operation of the device is inhibited.

Figure 19 shows the equivalent circuit.

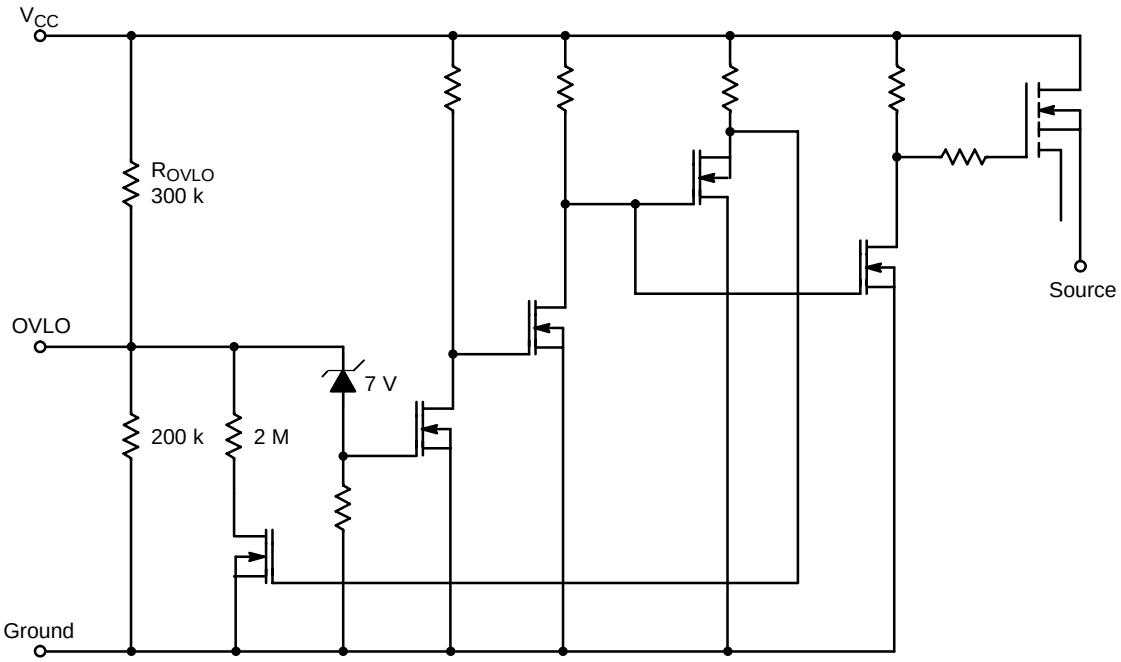



**Figure 19. Equivalent Overvoltage Lockout Circuit**

The theoretical equation for the OVLO turn−on voltage is:

$$R_{OVLO}\,(K\Omega) = \frac{300\,V_{in} - 2100}{21.8 - V_{in}}$$

The OVLO trip point voltage calculated through the theoretical formula may show small variations with respect to Figure 4, therefore it is recommended to use the formulas gotten from the OVLO characterization, which are shown below:

$$R_{OVLO}\,(k\Omega) = e\,[(OVLO + 5.2)/3.46];\,\text{for}\,T_J = 25^{\circ}C$$

where “OVLO” is the desired overvoltage lockout value, and $R_{OVLO}$ is the programming resistor from the OVLO pin to the $V_{CC}$ pin.

To reduce nuisance tripping due to transients and noise spikes, a capacitor may be added from the OVLO pin to ground. This will create a low pass filter with a cutoff frequency of f. The required capacitance on this pin is:

$$C_{OVLO} = \frac{[1 + (8.83\,E^{-6} \cdot R_{OVLO})]}{2\pi \cdot f \cdot R_{OVLO}}$$

This pin is also used as a common shutdown pin. In this mode, if this pin is pulled to ground, it will shutdown the chip and all chips connected to its OVLO pin.

The OVLO pin has an internal switch to ground that will pull it low, whenever the device is disabled due to any fault other than an Overvoltage condition. An enable pin shutdown is not considered a fault and will not cause a common shutdown. This feature allows multiple units to turn on and off simultaneously by tying the OVLO pins together in parallel. This can be used for operating several hot plug devices in parallel, or for use with separate loads, when all devices need to startup and shutdown simultaneously.

**Temperature Limit**

The temperature limit circuit senses the temperature of the Power FET and removes the gate drive if the maximum level is exceeded. For the auto−retry device, there is a nominal hysteresis of 40°C for this circuit. After a thermal shutdown, the device will automatically restart when the temperature drops to a safe level as determined by the hysteresis. The latching thermal circuit can be reset either by recycling the input power, or by toggling the enable signal.

**Current Limit**

An external resistor from the current limit pin to the source pins set the level at which the device will limit the current. The plot of resistance vs. current limit includes two curves, one for short circuit and one for overload.

A short circuit condition is one in which the SENSEFET is not fully enhanced, and is therefore in a high impedance mode of operation. In this case there are many hundreds of millivolts across the drain to source pins of the SENSEFET. This occurs when the output sees a very low impedance short as well as when the capacitor is charging at turn on. In both cases there are several volts or more across the FET.

An overload condition is one in which the SENSEFET is still fully enhanced and the drain to source voltage is the product of the drain current and the on resistance of the FET.

The sense voltage out of the SENSEFET has a different relation to the drain current in these two conditions. The difference in current limit levels for these two cases is called DI, where:

$$\Delta I = V_{ref}/R_{DSon}$$

For this equation, $V_{ref}$ is the reference voltage of the current limit circuit, and $R_{DSon}$ is the on resistance of the SENSEFET. For more information on this, see application note AND8140/D, “SMART HotPlug™ Current Limit Function”.

This inherent property of the SENSEFET allows for simple dual level current limiting, in which a short circuit condition will see a lower level of limiting than will an overload. This operation will exist in start up as well as under normal operation, so the device will be able to differentiate between a short and an overload.

As with all SMART HotPlug devices, the current limit will never shutdown the device. Only the thermal limit will stop the flow of current to the load. Once the current is stopped due to the thermal limit, it will remain off until input power is recycled for the latching version, or it will continuously retry to start again if it is the auto−retry version.

The ILimit graph shown in Figure 5 was generated from the data of the ILimit characterization, the formula for the short circuit curve is:

$$R_{ILimit}\,(\Omega) = \left(\frac{152.86}{ILimit}\right)^{1.02} \text{ for } T_J = 25^{\circ}C$$

where “ILimit” is the desired short circuit ILimit value, and $R_{ILimit}$ is the programming resistor from the ILimit pin to the source pin.

### Turn−on Surge

During the turn−on event, there is a large amount of energy dissipated due to the linear operation of the power device. The energy rating is the amount of energy that the device can absorb before the thermal limit circuit will shut the unit down. This is very important specially for the latch off device as it determines the maximum load capacitance that the device can charge before the thermal limit shuts the device down. The calculation of this is not very simple as it depends on several factors such as the input voltage (Vin), load capacitance (CL), current limit settings (ILimit) and device’s thermal transient response, therefore, it is recommended to do lab evaluations for these purposes. Figure 20 shows the device’s thermal transient response for minimum pad.

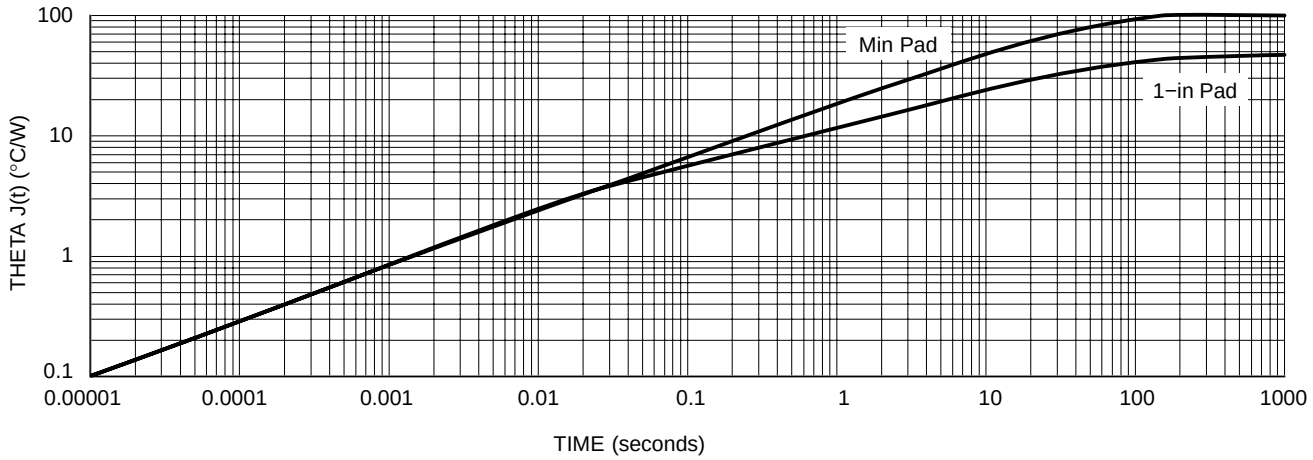
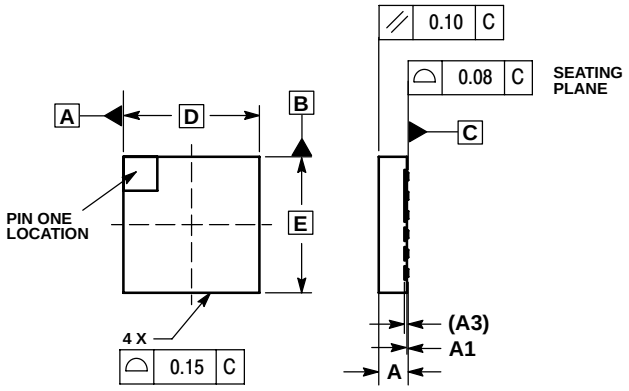


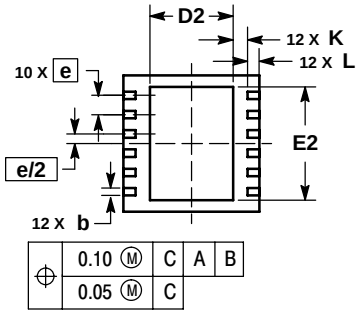

**Figure 20. Thermal Transient Response**

## PACKAGE DIMENSIONS

**PLLP−12, 9x9 mm**
CASE 488AB−01
ISSUE C




TOP VIEW SIDE VIEW



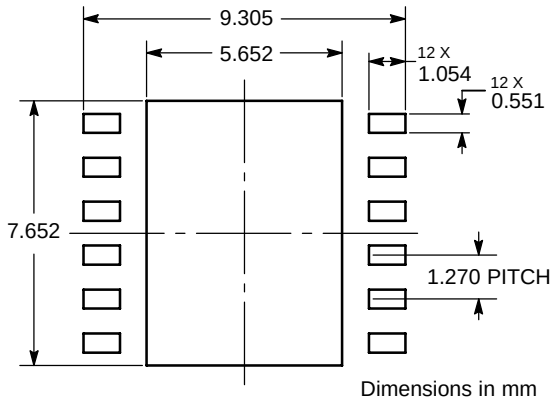

BOTTOM VIEW

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. COPLANARITY APPLIES TO THE LEAD, DIMENSION B, AND EXPOSED PAD.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 1.750 | 1.950 |
| A1 | 0.000 | 0.050 |
| A3 | 0.254 REF | |
| b | 0.400 | 0.600 |
| D | 9.000 BSC | |
| E | 9.000 BSC | |
| e | 1.270 BSC | |
| D2 | 5.400 | 5.600 |
| E2 | 7.400 | 7.600 |
| K | 0.850 REF | |
| L | 0.850 | 0.950 |

STYLE 1:
PIN 1. OVLO
2. UVLO
3. ENABLE/TIMER
4. GND
5. CCHARGE
6. CURRENT LIMIT
7. POWER GOOD
8. N/C
9. N/C
10. SOURCE
11. SOURCE
12. SOURCE

**SOLDERING FOOTPRINT***




Dimensions in mm

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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