MBT6429DW1T1

Amplifier Transistors

NPN Silicon

Features

- Pb−Free Package is Available

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	45	Vdc
Collector−Base Voltage	V_{CBO}	55	Vdc
Emitter−Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	200	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation (Note 1) T_A = 25°C	P_D	150	mW
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	833	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Device mounted on FR4 glass epoxy printed circuit board using the minimum recommended foot print.

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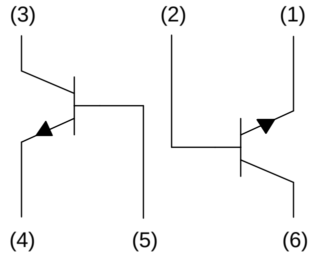
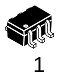
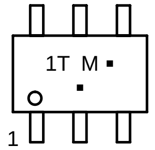




SC−88
(SOT−363)
419B

MARKING DIAGRAM



1T	= Specific Device Code
M	= Date Code
▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MBT6429DW1T1	SC−88	3000/Tape & Reel
MBT6429DW1T1G	SC−88 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

December, 2005 − Rev. 2

Publication Order Number:
MBT6429DW1T1/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	45	−	Vdc
Collector−Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	55	−	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc)	I_{CES}	−	0.1	μAdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	−	0.01	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	0.01	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.01 mAdc, V_{CE} = 5.0 Vdc) (I_C = 0.1 mAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	500 500 500 500	− 1250 − −	−
Collector−Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 0.5 mAdc) (I_C = 100 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	− −	0.2 0.6	Vdc
Base−Emitter On Voltage (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	$V_{BE(on)}$	0.56	0.66	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)	f_T	100	700	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	−	3.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ibo}	−	8.0	pF

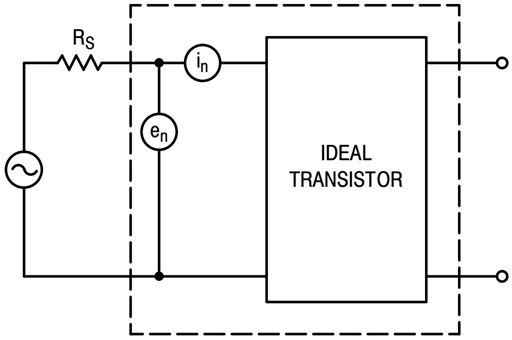


Figure 1. Transistor Noise Model

NOISE CHARACTERISTICS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

NOISE VOLTAGE

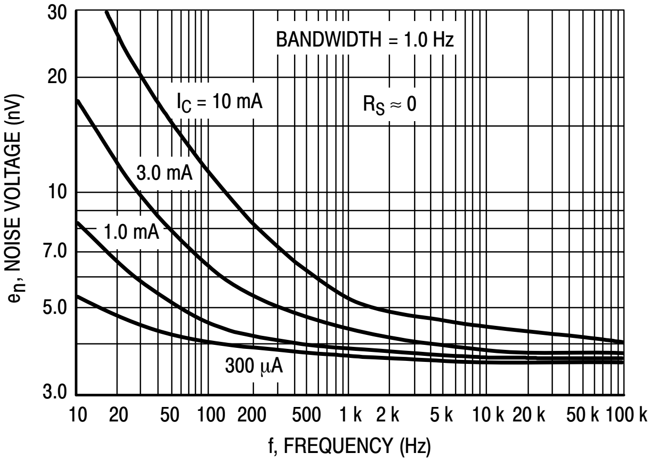


Figure 2. Effects of Frequency

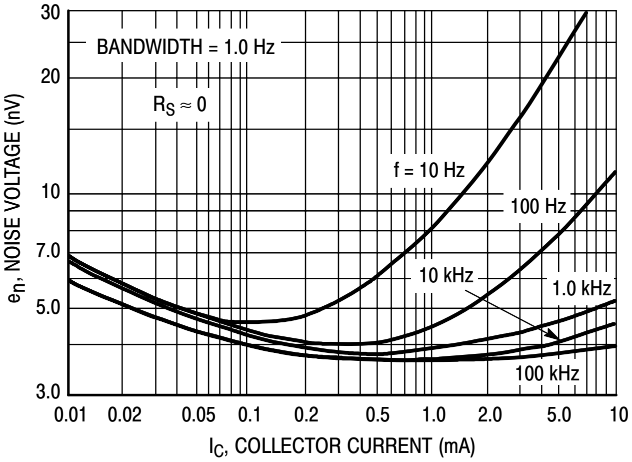


Figure 3. Effects of Collector Current

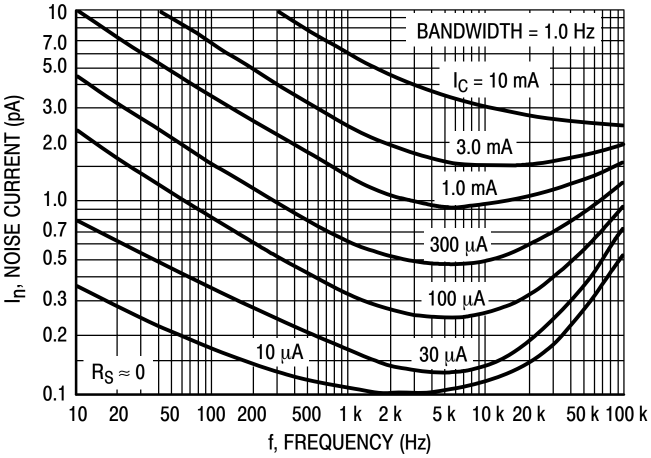


Figure 4. Noise Current

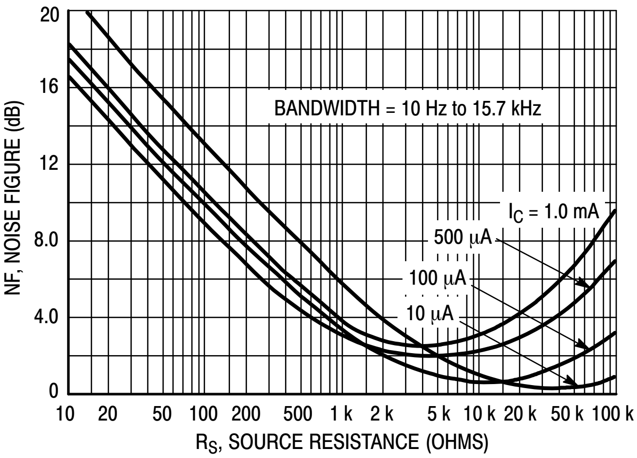


Figure 5. Wideband Noise Figure

100 Hz NOISE DATA

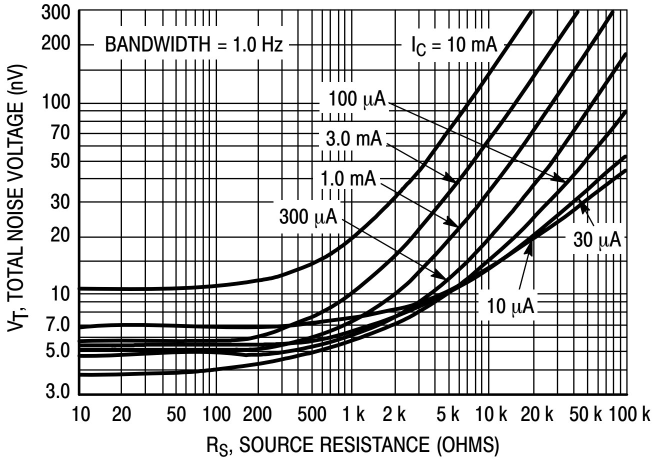


Figure 6. Total Noise Voltage

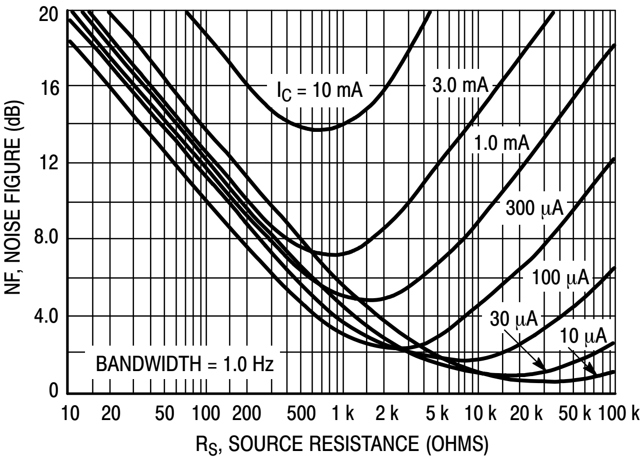


Figure 7. Noise Figure

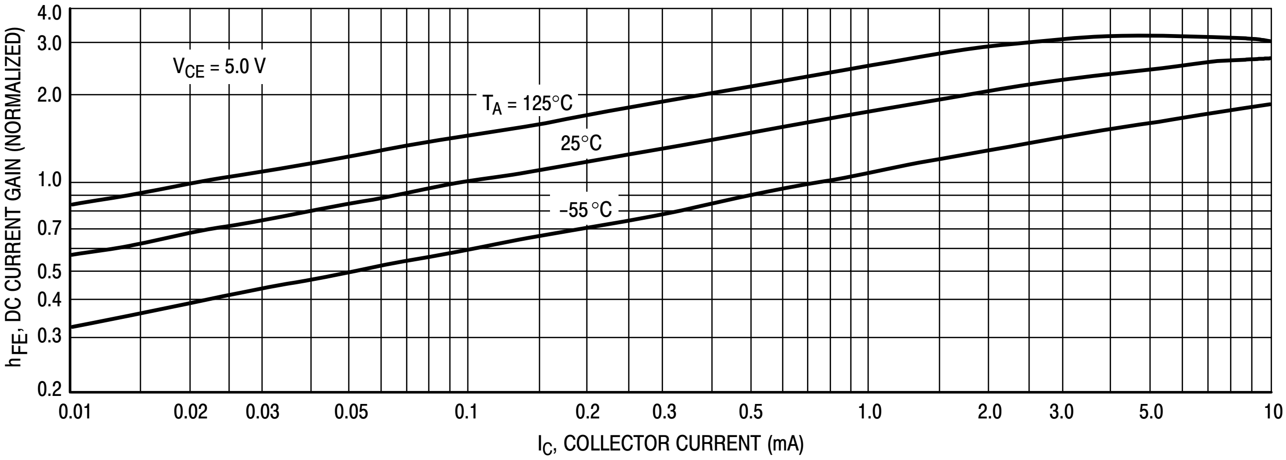


Figure 8. DC Current Gain

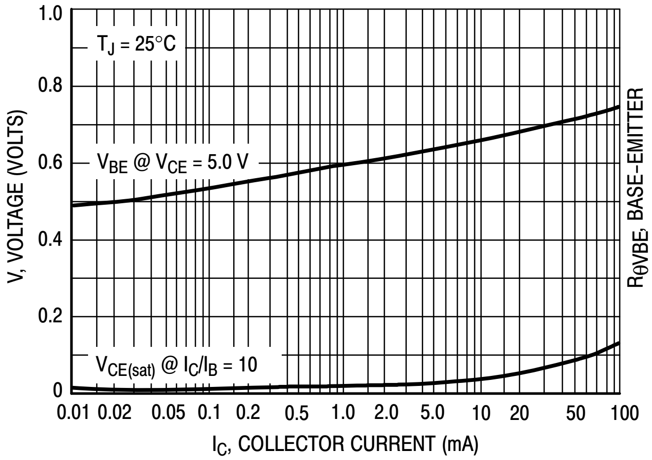


Figure 9. “On” Voltages

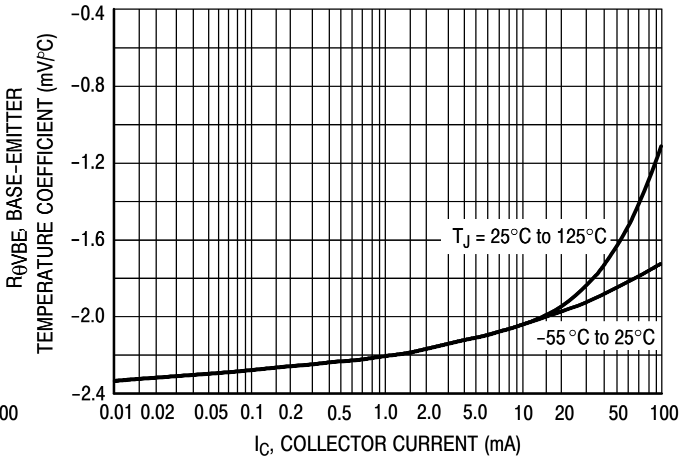


Figure 10. Temperature Coefficients

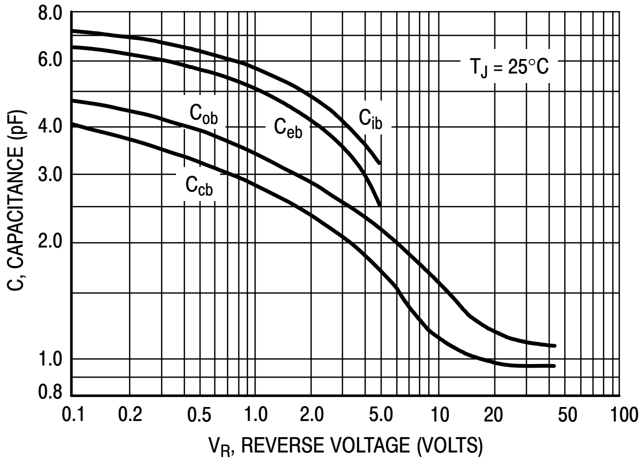


Figure 11. Capacitance

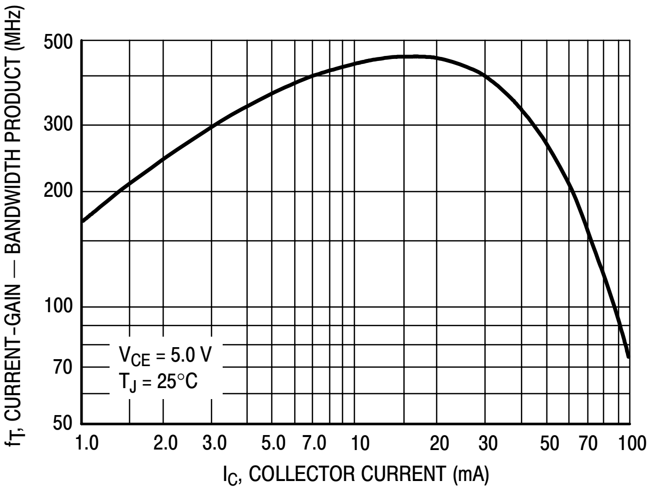
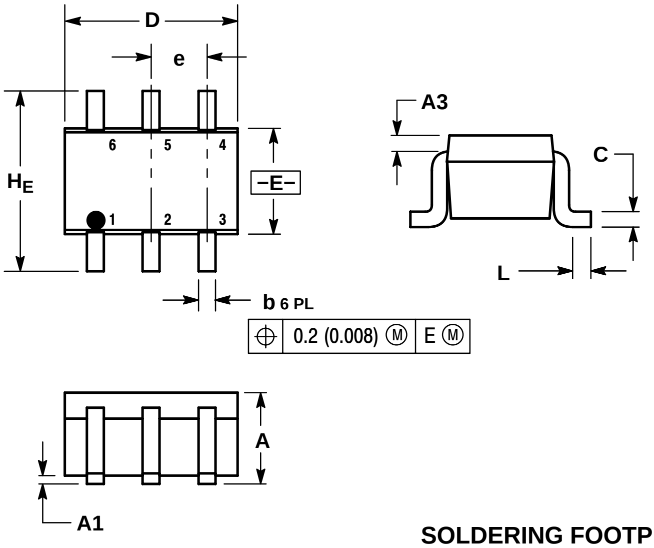


Figure 12. Current−Gain − Bandwidth Product

PACKAGE DIMENSIONS

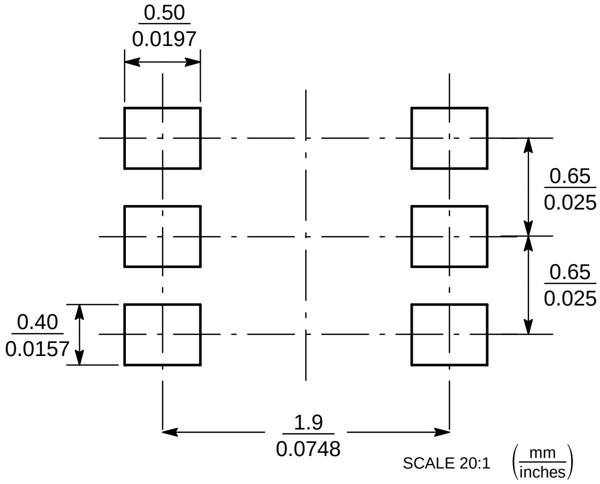
SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	MILLIMETERS			**INCHES**		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	2.00	2.10	2.20	0.078	0.082	0.086

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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