NL7SZ97

Configurable Multifunction Gate

The NL7SZ97 is an advanced high−speed CMOS multifunction gate. The device allows the user to choose logic functions MUX, AND, OR, NAND, NOR, INVERT and BUFFER. The device has Schmitt−trigger inputs, thereby enhancing noise immunity.

The NL7SZ97 input and output structures provide protection when voltages up to 7.0 V are applied, irregardless of the supply voltage.

Features

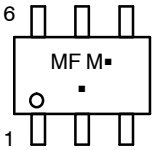
- High Speed: t_{PD} = 3.3 ns (Typ) @ V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 1 μA (Maximum) at T_A = 25°C
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra−Small Package
- This is a Pb−Free Device

ON Semiconductor®

http://onsemi.com

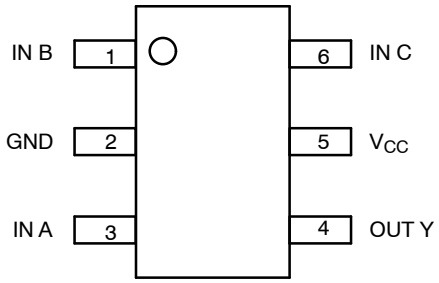
SC−88 (SOT−363)
CASE 419B

MARKING DIAGRAM



MF = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENTS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

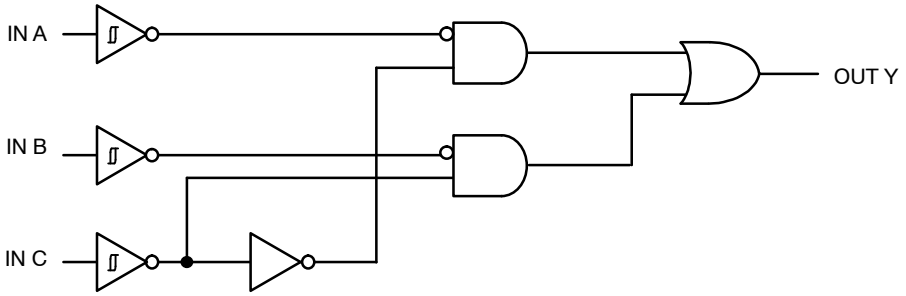


Figure 1. Function Diagram

PIN ASSIGNMENT

1	IN B
2	GND
3	IN A
4	OUT Y
5	V_{CC}
6	IN C

FUNCTION TABLE*

Input			Output
A	B	C	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	H
H	H	L	H
H	H	H	H

*To select a logic function, please refer to “Logic Configurations section”.

LOGIC CONFIGURATIONS

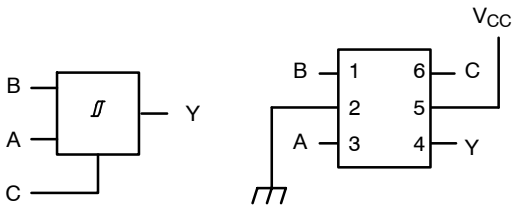


Figure 2. 2−Input MUX

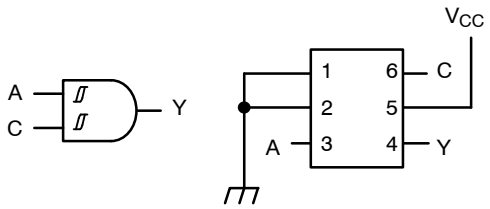


Figure 3. 2−Input AND (When B = “L”)

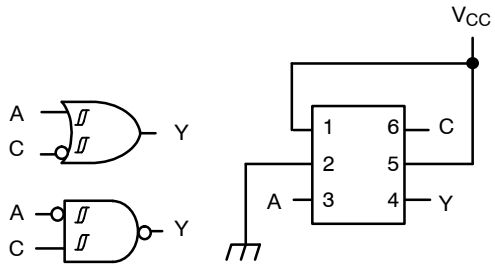


Figure 4. 2−Input OR with Input C Inverted (When B = “H”)

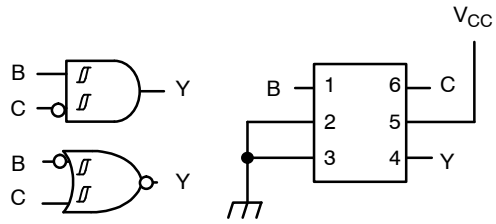


Figure 5. 2−Input AND with Input C Inverted (When A = “L”)

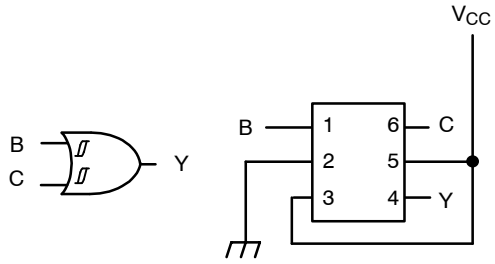


Figure 6. 2−Input OR (When A =”H”)

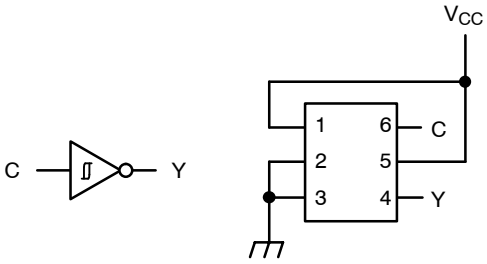


Figure 7. Inverter (When A = “L” and B = “H”)

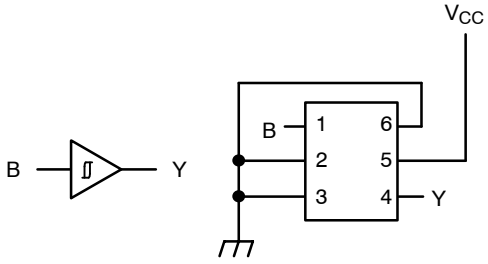


Figure 8. Buffer (When A = C = “L”)

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to +7.0	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND	−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC}	DC Supply Current Per Supply Pin		±100	mA
I_{GND}	DC Ground Current per Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SC−88	350	°C/W
P_D	Power Dissipation in Still Air at 85°C	SC−88	200	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating Oxygen	Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Mode (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
$I_{LATCHUP}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)		±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm^2 by 1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	Digital Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	5.5	V
T_A	Operating Free−Air Temperature (Note 6)		−55	+125	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	V_{CC} = 2.5 V ± 0.2 V V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0 0	No Limit No Limit No Limit	nS/V

6. The NL7SZ97 will not have degradation in its electrical spcifications or Mean−Time−Between−Failure (MTBF) when exposed to a temperature cycle test of 140°C for 21 hours, 135°C for 750 hours and of 130°C for 175 hours.

DC ELECTRICAL CHARACTERISTICS

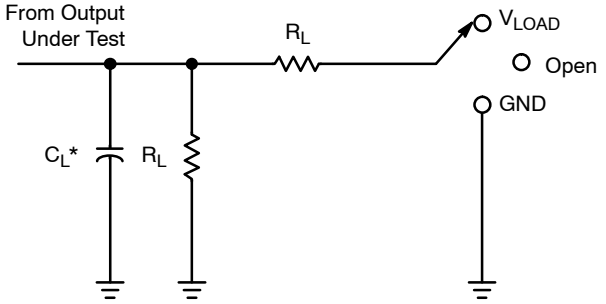
Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25°C			$T_A \leq$ +85°C		T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	Positive Threshold Voltage		1.65	0.79		1.16		1.16		1.16	V
			2.3	1.11		1.56		1.56		1.56	
			3.0	1.5		1.87		1.87		1.87	
			4.5	2.16		2.74		2.74		2.74	
			5.5	2.61		3.33		3.33		3.33	
V_{T-}	Negative Threshold Voltage		1.65	0.35		0.62	0.35		0.35		V
			2.3	0.58		0.87	0.58		0.58		
			3.0	0.84		1.19	0.84		0.84		
			4.5	1.41		1.9	1.41		1.41		
			5.5	1.78		2.29	1.78		1.78		
V_H	Hysteresis Voltage		1.65	0.30		0.62	0.30	0.62	0.30	0.62	V
			2.3	0.40		0.8	0.40	0.8	0.40	0.8	
			3.0	0.53		0.87	0.53	0.87	0.53	0.87	
			4.5	0.71		1.04	0.71	1.04	0.71	1.04	
			5.5	0.8		1.2	0.8	1.2	0.8	1.2	
V_{OH}	Minimum High−Level Output Voltage	$V_{IN} \leq V_{T-MIN}$ I_{OH} = −50 μA	1.65 − 5.5	V_{CC} − 0.1			V_{CC} − 0.1		V_{CC} − 0.1		V
		$V_{IN} \leq V_{T-MIN}$									
		I_{OH} = −4 mA	1.65	1.2			1.2		1.2		
		I_{OH} = −8 mA	2.3	1.9			1.9		1.9		
		I_{OH} = −16 mA	3.0	2.4			2.4		2.4		
		I_{OH} = −24 mA	3.0	2.3			2.3		2.3		
		I_{OH} = −32 mA	4.5	3.8			3.8		3.8		
V_{OL}	Maximum Low−Level Output Voltage	$V_{IN} \geq V_{T+MAX}$ I_{OL} = 50 μA	1.65 − 5.5			0.1		0.1		0.1	V
		$V_{IN} \geq V_{T+MAX}$									
		I_{OL} = 4 mA	1.65			0.45		0.45		0.45	
		I_{OL} = 8 mA	2.3			0.3		0.3		0.3	
		I_{OL} = 16 mA	3.0			0.4		0.4		0.4	
		I_{OL} = 24 mA	3.0			0.55		0.55		0.55	
		I_{OL} = 32 mA	4.5			0.55		0.55		0.55	
I_{IN}	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Quiescent Supply Current	0 ≤ V_{IN} ≤ V_{CC}	5.5			1.0		10		10	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	V_{CC} (V)	Test Condition	T_A = 25°C			$T_A \leq$ +85°C		T_A = −55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65 – 1.95		3.2	8.6	14.4	3.2	14.4	3.2	14.4	ns
		2.3 – 2.7		2.0	5.1	8.3	2.0	8.3	2.0	8.3	
		3.0 – 3.6		1.5	3.9	6.3	1.5	6.3	1.5	6.3	
		4.5 – 5.5		1.1	3.3	5.1	1.1	5.1	1.1	5.1	
C_{IN}	Input Capacitance				3.5						pF
C_{PD}	Power Dissipation Capacitance (Note 7)	5.0	f = 10 MHz		22						pF

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption: $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

TEST CIRCUIT AND VOLTAGE WAVEFORMS



*C_L includes probes and jig capacitance.

Figure 9. Load Circuit

Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 x V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 x V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5.5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	2 x V_{CC}	50 pF	500 Ω	0.3 V

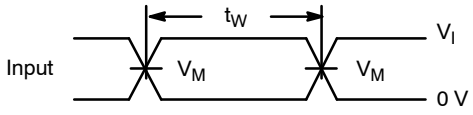


Figure 10. Voltage Waveforms Pulse Duration

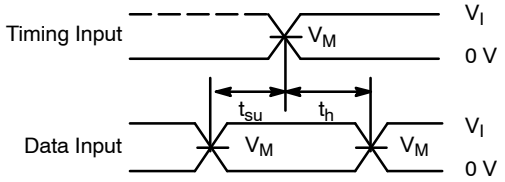


Figure 11. Voltage Waveforms Setup and Hold Times

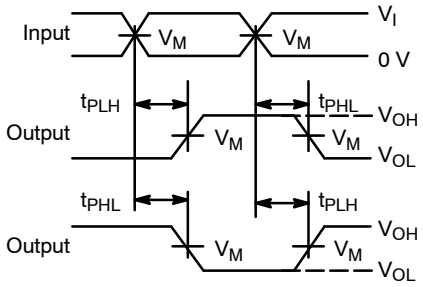


Figure 12. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

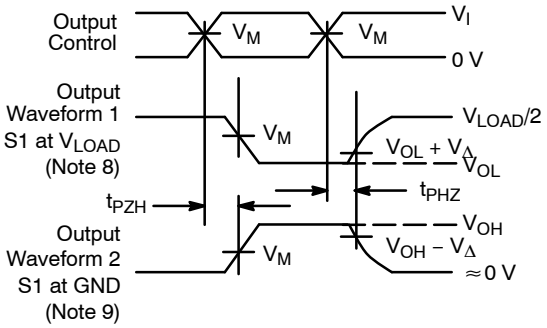


Figure 13. Voltage Waveforms Enable and Disable Times Low− and High−Level Enabling

8. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
9. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control
10. All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz, Z_O = 50 Ω.
11. The outputs are measured one at a time, with one transition per measurement.
12. All parameters are waveforms are not applicable to all devices.

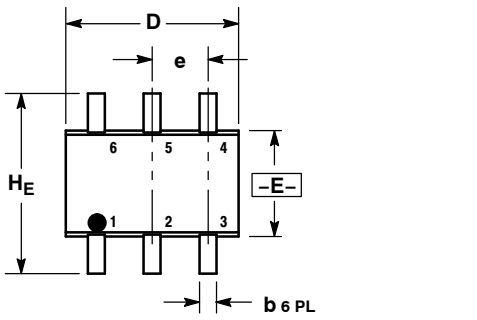
ORDERING INFORMATION

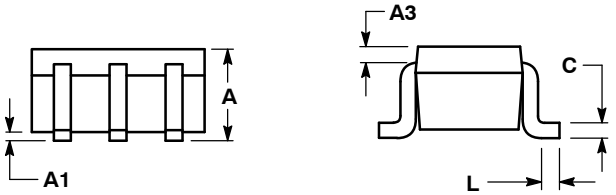
Device	Package	Shipping†
NL7SZ97DFT2G	SC−88 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE W

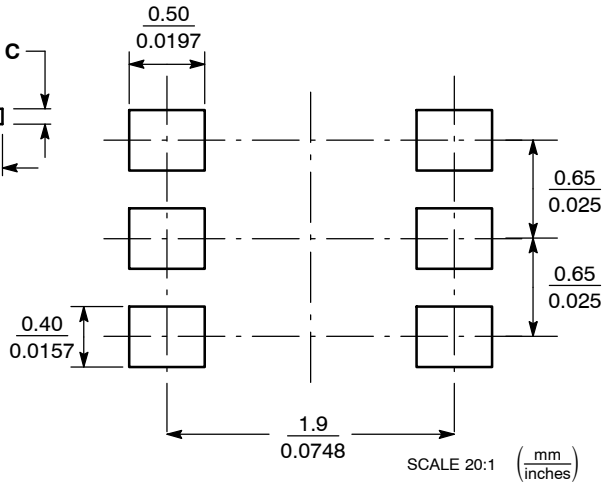




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	2.00	2.10	2.20	0.078	0.082	0.086

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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