

NLX1G57

Configurable Multifunction Gate

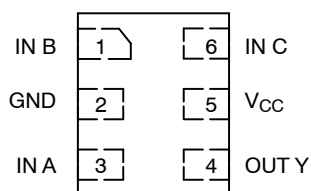
The NLX1G57 MiniGate™ is an advanced high-speed CMOS multifunction gate. The device allows the user to choose logic functions AND, OR, NAND, NOR, XNOR, INVERT and BUFFER. The device has Schmitt-trigger inputs, thereby enhancing noise immunity.

The NLX1G57 input and output structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 3.2 \text{ ns (Typ) @ } V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1 \mu\text{A (Maximum) at } T_A = 25^\circ\text{C}$
- Power Down Protection Provided on inputs
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input and Output Pins
- Ultra-Small Packages
- This is a Pb-Free Device

PIN ASSIGNMENTS



(Top View)



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAMS

	ULLGA6 1.0 x 1.0 CASE 613AD	
	ULLGA6 1.2 x 1.0 CASE 613AE	
	ULLGA6 1.45 x 1.0 CASE 613AF	
	UDFN6 1.0 x 1.0 CASE 517BX	
	UDFN6 1.2 x 1.0 CASE 517AA	
	UDFN6 1.45 x 1.0 CASE 517AQ	

D, P = Specific Device Code
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NLX1G57

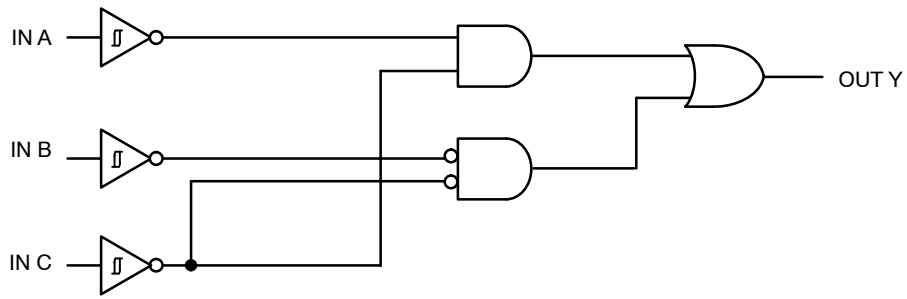


Figure 1. Function Diagram

PIN ASSIGNMENT

1	IN B
2	GND
3	IN A
4	OUT Y
5	V _{CC}
6	IN C

FUNCTION TABLE*

Input			Output
A	B	C	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

*To select a logic function, please refer to "Logic Configurations section".

LOGIC CONFIGURATIONS

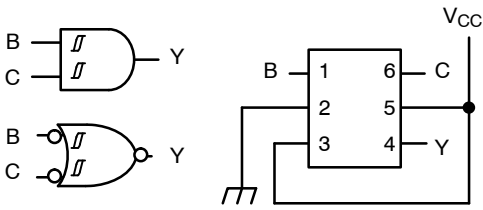


Figure 2. 2-Input AND (When A = "H")

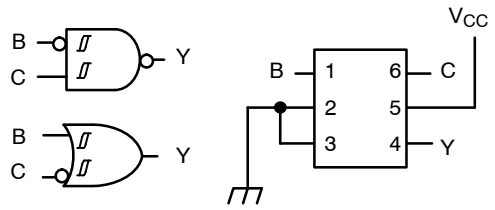


Figure 3. 2-Input NAND with input B inverted (When A = "L")

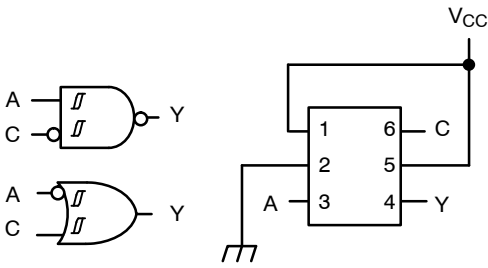


Figure 4. 2-Input NAND with Input C Inverted (When B = "H")

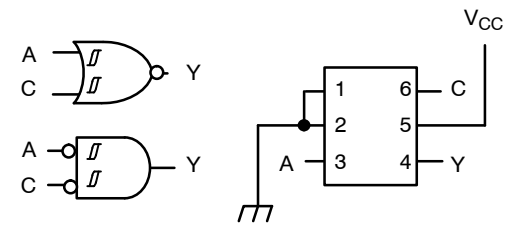


Figure 5. 2-Input NOR (When B = "L")

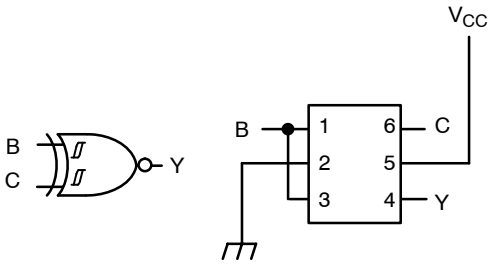


Figure 6. 2-Input XNOR (When A = B)

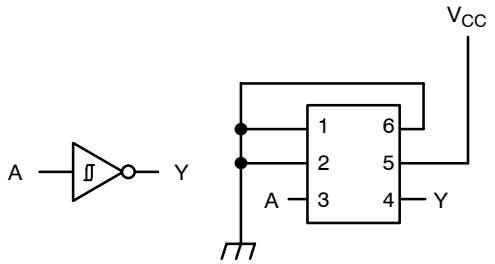


Figure 7. Inverter (When B = C = "L")

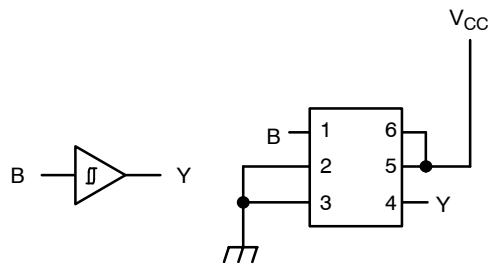


Figure 8. Buffer (When A = "L" and C = "H")

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{IN}	DC Input Voltage	-0.5 to +7.0	V
V _{OUT}	DC Output Voltage	-0.5 to +7.0	V
I _{IK}	DC Input Diode Current V _{IN} < GND	-50	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND	-50	mA
I _O	DC Output Source/Sink Current	± 50	mA
I _{CC}	DC Supply Current Per Supply Pin	± 100	mA
I _{GND}	DC Ground Current per Ground Pin	± 100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	150	°C
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >200 N/A	V
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND at 125°C (Note 5)	± 500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm by 1 inch, 2 ounce copper trace no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage	1.65	5.5	V
V _{IN}	Digital Input Voltage	0	5.5	V
V _{OUT}	Output Voltage	0	5.5	V
T _A	Operating Free-Air Temperature	-55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 2.5 V ± 0.2 V V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0 0	No Limit No Limit No Limit	nS/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C			T _A ≤ +85°C		T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{T+}	Positive Threshold Voltage		1.65	0.79		1.16		1.16		1.16	V
			2.3	1.11		1.56		1.56		1.56	
			3.0	1.5		1.87		1.87		1.87	
			4.5	2.16		2.74		2.74		2.74	
			5.5	2.61		3.33		3.33		3.33	
V _{T-}	Negative Threshold Voltage		1.65	0.35		0.62	0.35		0.35		V
			2.3	0.58		0.87	0.58		0.58		
			3.0	0.84		1.19	0.84		0.84		
			4.5	1.41		1.9	1.41		1.41		
			5.5	1.78		2.29	1.78		1.78		
V _H	Hysteresis Voltage		1.65	0.30		0.62	0.30	0.62	0.30	0.62	V
			2.3	0.40		0.8	0.40	0.8	0.40	0.8	
			3.0	0.53		0.87	0.53	0.87	0.53	0.87	
			4.5	0.71		1.04	0.71	1.04	0.71	1.04	
			5.5	0.8		1.2	0.8	1.2	0.8	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{T-MIN} or V _{T+MAX} I _{OH} = -50 μA	1.65 – 5.5	V _{CC} – 0.1			V _{CC} – 0.1		V _{CC} – 0.1		V
		V _{IN} = V _{T-MIN} or V _{T+MAX}									
		I _{OH} = -4 mA	1.65	1.2			1.2		1.2		
		I _{OH} = -8 mA	2.3	1.9			1.9		1.9		
		I _{OH} = -16 mA	3.0	2.4			2.4		2.4		
		I _{OH} = -24 mA	3.0	2.3			2.3		2.3		
		I _{OH} = -32 mA	4.5	3.8			3.8		3.8		
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{T-MIN} or V _{T+MAX} I _{OL} = 50 μA	1.65 – 5.5			0.1		0.1		0.1	V
		V _{IN} = V _{T-MIN} or V _{T+MAX}									
		I _{OL} = 4 mA	1.65			0.45		0.45		0.45	
		I _{OL} = 8 mA	2.3			0.3		0.3		0.3	
		I _{OL} = 16 mA	3.0			0.4		0.4		0.4	
		I _{OL} = 24 mA	3.0			0.55		0.55		0.55	
		I _{OL} = 32 mA	4.5			0.55		0.55		0.55	
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5 V	0 to 5.5			±0.1		±1.0		μA	
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		10		μA	

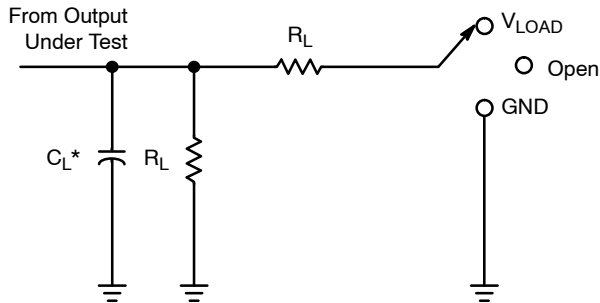
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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	V_{CC} (V)	Test Condition	$T_A = 25^\circ\text{C}$			$T_A \leq +85^\circ\text{C}$		$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} , t_{PHL}	Propagation Delay, Any Input to Output Y (See Test Circuit)	1.65 – 1.95		3.2	8.5	14.4	3.2	14.4	3.2	14.4	ns
		2.3 – 2.7		2	4.9	8.3	2	8.3	2	8.3	
		3.0 – 3.6		1.5	3.8	6.3	1.5	6.3	1.5	6.3	
		4.5 – 5.5		1.1	3.2	5.1	1.1	5.1	1.1	5.1	
C_{IN}	Input Capacitance				3.5						pF
C_{PD}	Power Dissipation Capacitance (Note 6)	5.0	$f = 10$ MHz		22						pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

TEST CIRCUIT AND VOLTAGE WAVEFORMS



Test	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

* C_L includes probes and jig capacitance.

Figure 9. Load Circuit

V_{CC}	Inputs		V_M	V_{LOAD}	C_L	R_L	V_A
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5.5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V

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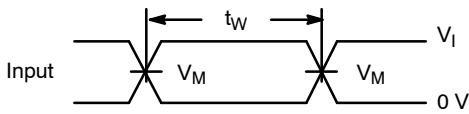


Figure 10. Voltage Waveforms Pulse Duration

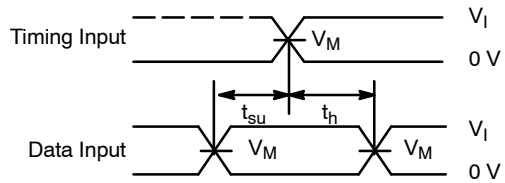


Figure 11. Voltage Waveforms Setup and Hold Times

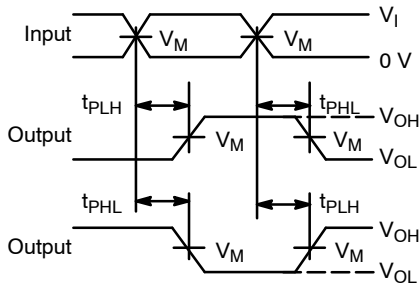


Figure 12. Voltage Waveforms Propagation Delay Times Inverting and Noninverting Outputs

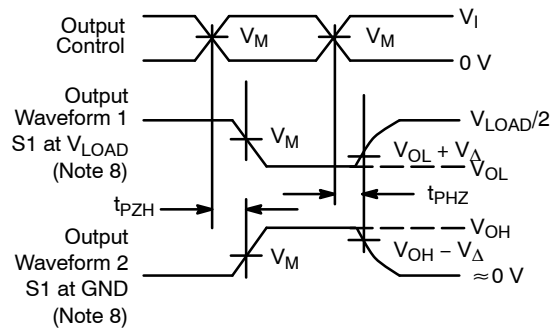


Figure 13. Voltage Waveforms Enable and Disable Times Low- and High-Level Enabling

7. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
8. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
9. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$.
10. The outputs are measured one at a time, with one transition per measurement.
11. All parameters are waveforms are not applicable to all devices.

ORDERING INFORMATION

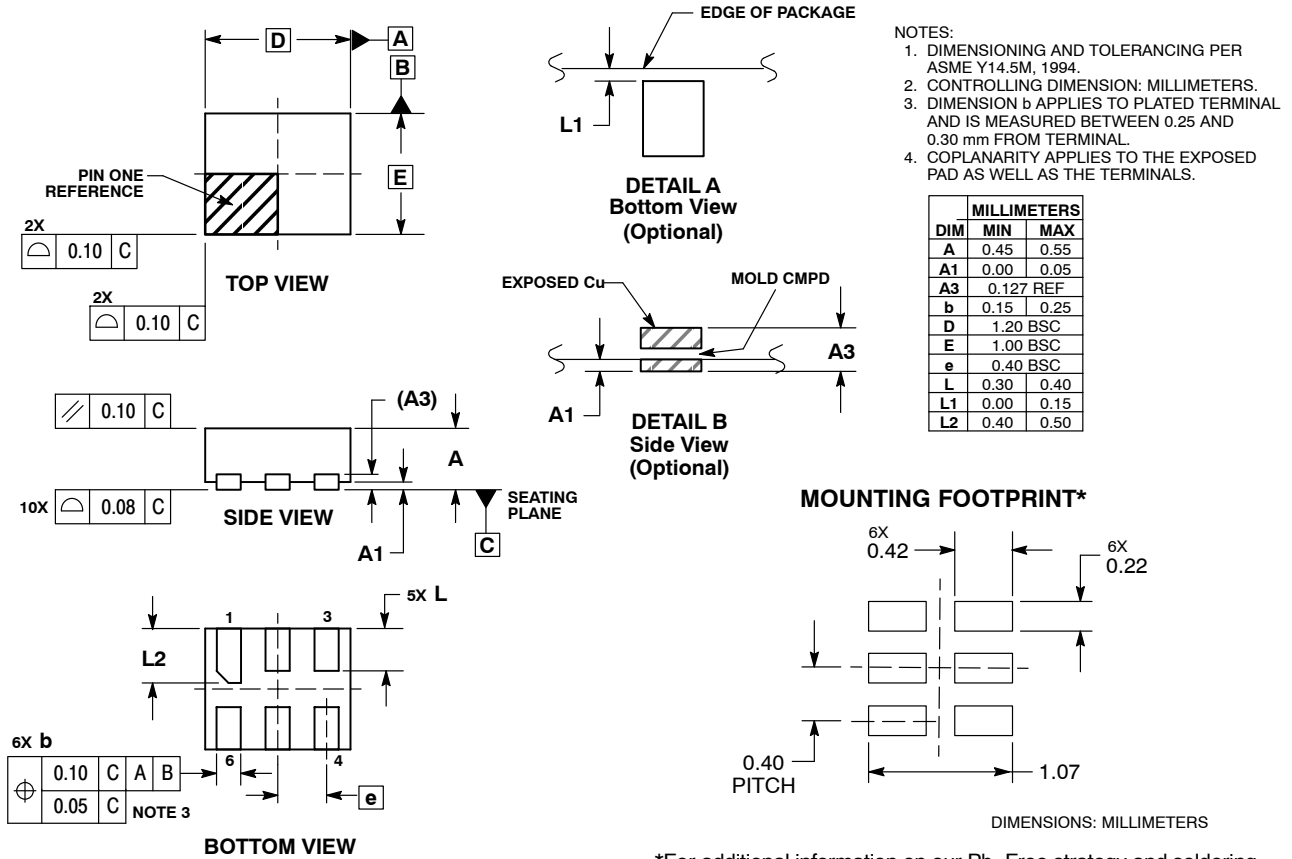
Device	Package	Shipping†
NLX1G57AMX1TCG	ULLGA6 – 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G57BMX1TCG	ULLGA6 – 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G57CMX1TCG	ULLGA6 – 0.35P (Pb-Free)	3000 / Tape & Reel
NLX1G57MUTCG (In Development)	UDFN6, 1.2 x 1.0, 0.4P (Pb-Free)	3000 / Tape & Reel
NLX1G57AMUTCG (In Development)	UDFN6, 1.45 x 1.0, 0.5P (Pb-Free)	3000 / Tape & Reel
NLX1G57CMUTCG (In Development)	UDFN6, 1.0 x 1.0, 0.35P (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

UDFN6 1.2x1.0, 0.4P
CASE 517AA
ISSUE O

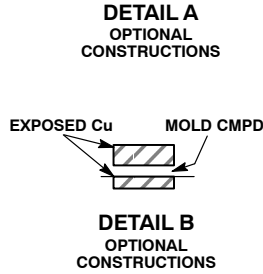
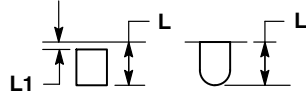
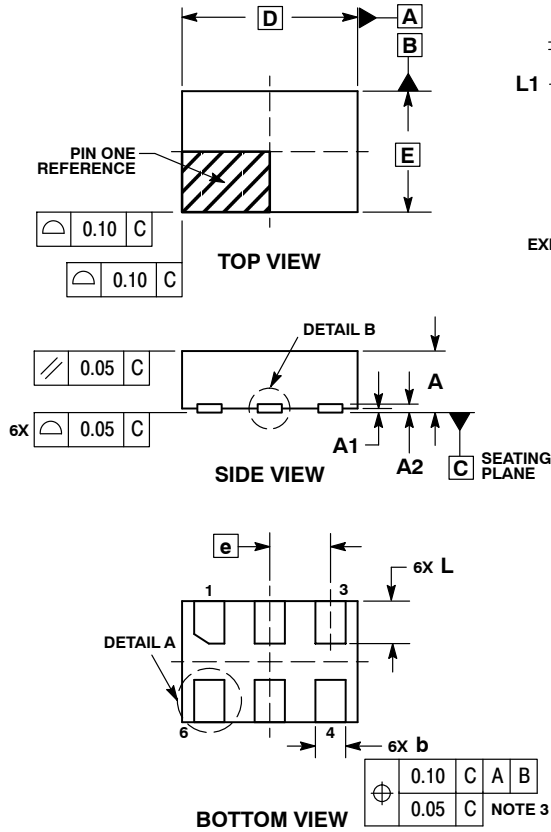


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NLX1G57

PACKAGE DIMENSIONS

UDFN6 1.45x1.0, 0.5P
CASE 517AQ
ISSUE O

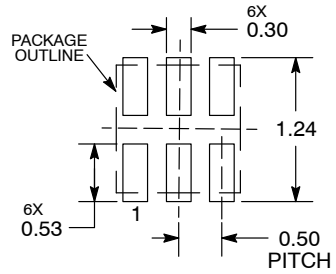


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A2	0.07 REF	
b	0.20	0.30
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.30	0.40
L1	---	0.15

MOUNTING FOOTPRINT



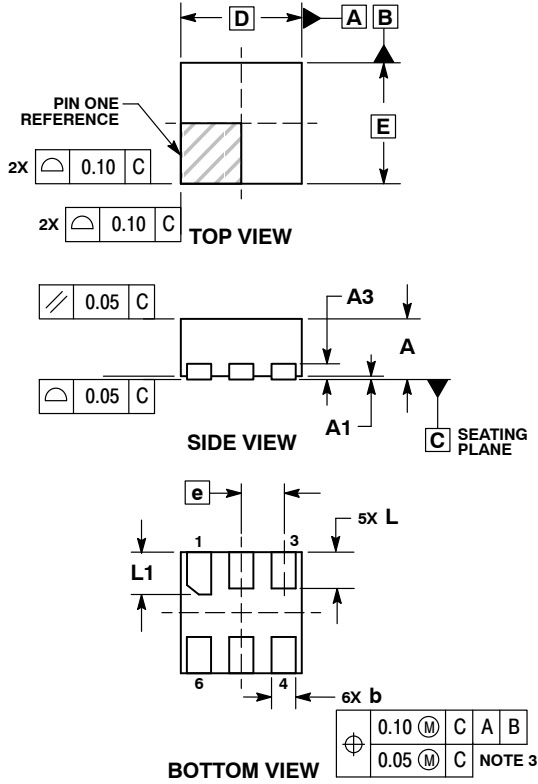
DIMENSIONS: MILLIMETERS

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NLX1G57

PACKAGE DIMENSIONS

UDFN6 1.0x1.0, 0.35P
CASE 517BX
ISSUE O

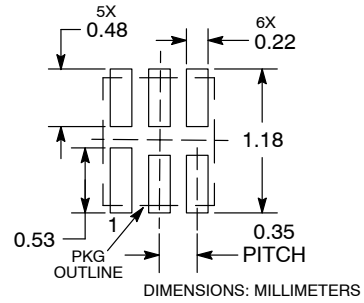


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. PACKAGE DIMENSIONS EXCLUSIVE OF BURRS AND MOLD FLASH.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

RECOMMENDED SOLDERING FOOTPRINT*

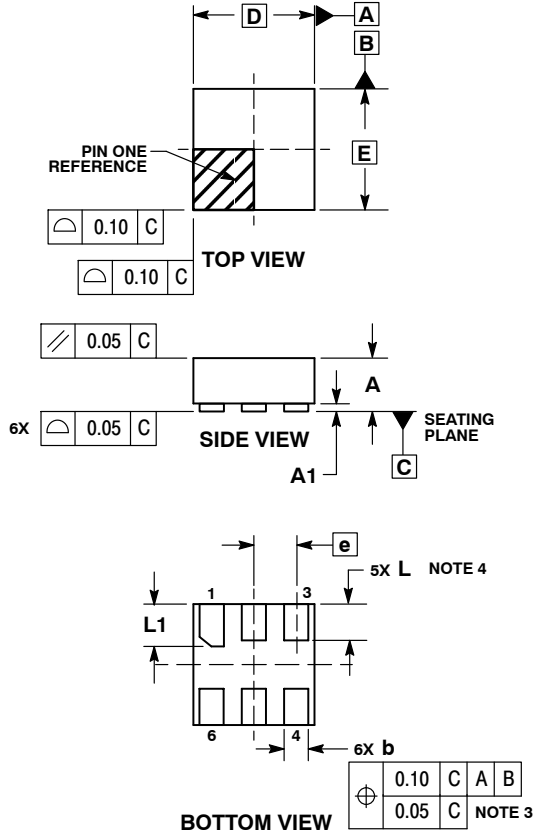


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NLX1G57

PACKAGE DIMENSIONS

ULLGA6, 1.0x1.0, 0.35P
CASE 613AD
ISSUE A

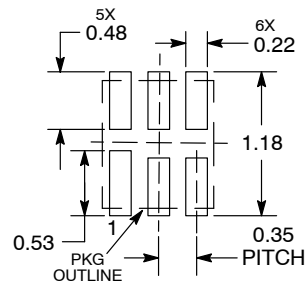


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.12	0.22
D	1.00 BSC	
E	1.00 BSC	
e	0.35 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



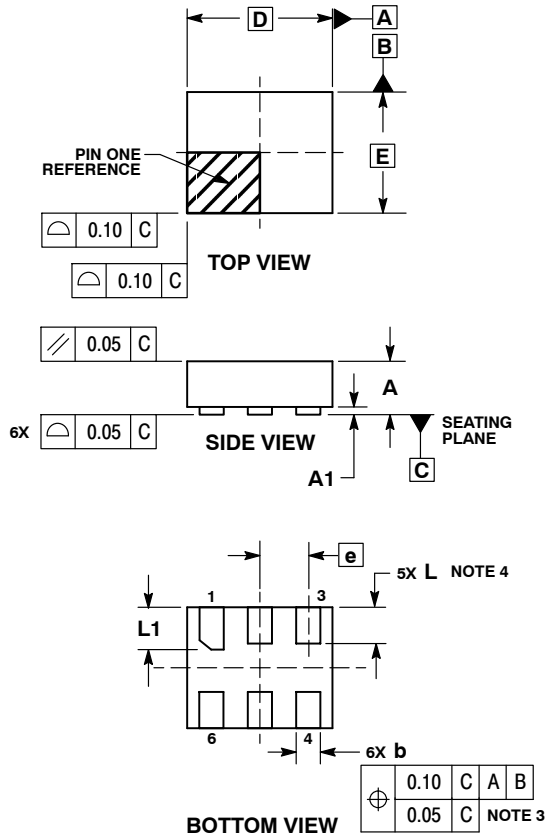
DIMENSIONS: MILLIMETERS

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NLX1G57

PACKAGE DIMENSIONS

ULLGA6, 1.2x1.0, 0.4P
CASE 613AE
ISSUE A

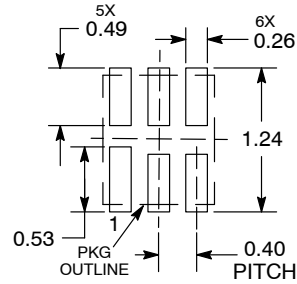


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.20 BSC	
E	1.00 BSC	
e	0.40 BSC	
L	0.25	0.35
L1	0.35	0.45

**MOUNTING FOOTPRINT
SOLDERMASK DEFINED***



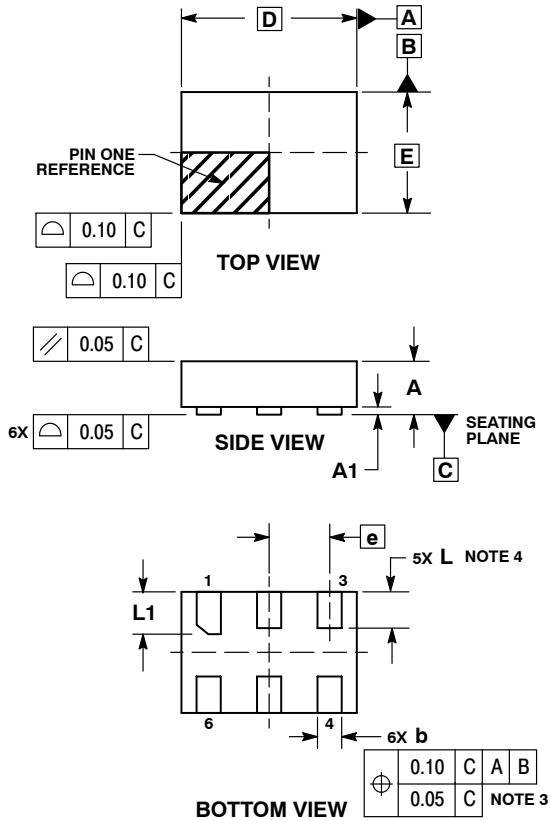
DIMENSIONS: MILLIMETERS

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NLX1G57

PACKAGE DIMENSIONS

ULLGA6, 1.45x1.0, 0.5P
CASE 613AF
ISSUE A

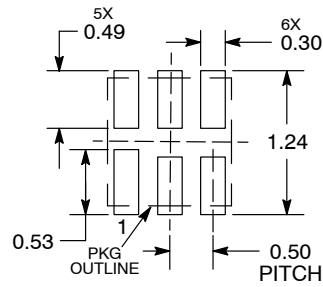


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

MILLIMETERS		
DIM	MIN	MAX
A	---	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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