NB3H83905C

1.8V/2.5V/3.3V Crystal Input to 1:6 LVTTL/LVCMOS Clock Fanout Buffer with OE

Description

The NB3H83905C is a 1.8 V, 2.5 V or 3.3 V V_{DD} core Crystal input 1:6 LVTTL/LVCMOS fanout buffer with outputs powered by flexible 1.8 V, 2.5 V, or 3.3 V supply (with $V_{DD} \geq V_{DDO}$). The core accepts a fundamental Parallel Resonant crystal from 3 MHz to 40 MHz or a Single Ended LVCMOS Clock from 3 MHz to 100 MHz. Core supply must be equal or greater voltage than the output supply.

Two synchronous LVTTL/LVCMOS Enable lines permit independent control over outputs BCLK[0:4] and output BCLK5; enabling or disabling only when the output is in LOW state eliminating potential output glitching or runt pulse generation. When unused, leave floating open for the default HIGH state.

The 6 outputs drive 50 Ω series or parallel terminated transmission lines. Parallel termination should be to 1/2 V_{CC}. Series terminated lines can drive 2 loads each, or 12 lines total. When unused, leave floating open with no board trace.

Fit, Form, and Function compatible with ICS83905 and PI6C10806.

Features

- 6 LVTTL/LVCMOS Output Clock copies
- Supply Operation $V_{DD} \geq V_{DDO}$:
  - 1.8 V ± 0.2 V, 2.5 V ± 5% or 3.3 V ± 5% Core V_{DD}
  - 1.8 V ± 0.2 V, 2.5 V ± 5%, or 3.3 V ± 5% Output V_{DDO}
- Crystal Oscillator Interface
- Crystal Input Frequency Range: 3 MHz to 40 MHz
- Clock Input Frequency Range: 3 MHz to 100 MHz
- LVCMOS compatible Enable Inputs
- 5 V Tolerant Enable Inputs
- Tight Output to Output Skew: 80 ps Max
- Synchronous Output Enable
- Phase Noise Floor −160 dBc (1 MHz)
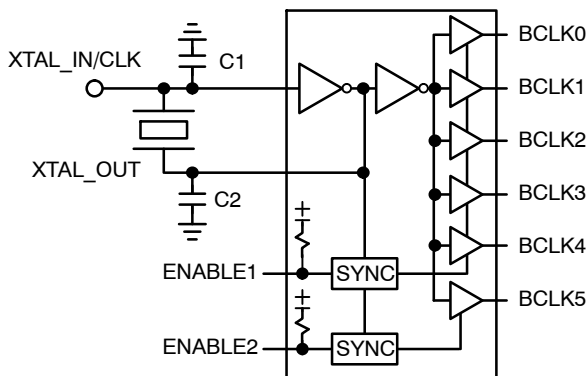- Industrial Temperature Range
- These are Pb−Free Devices

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MARKING DIAGRAMS*

SOIC−16
D SUFFIX
CASE 751B

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NB3H83905G
ALYYWW
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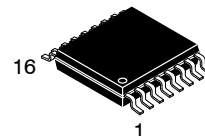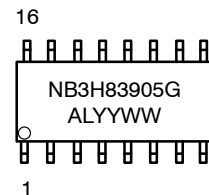
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DT SUFFIX
CASE 948F

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NB3H
905C
ALYW■
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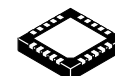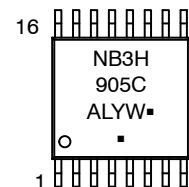
QFN20
MN SUFFIX
CASE 485E

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NB3H
83905C
ALYW■
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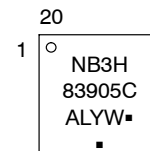
A = Assembly Location
L, WL = Wafer Lot
Y = Year
W, WW = Work Week
G or ■ = Pb−Free Package

(*Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

Figure 1. Clock Input Frequency Range: 3 MHz to 100 MHz

NB3H83905C

Figure 2. Pinout Configuration (Top View)

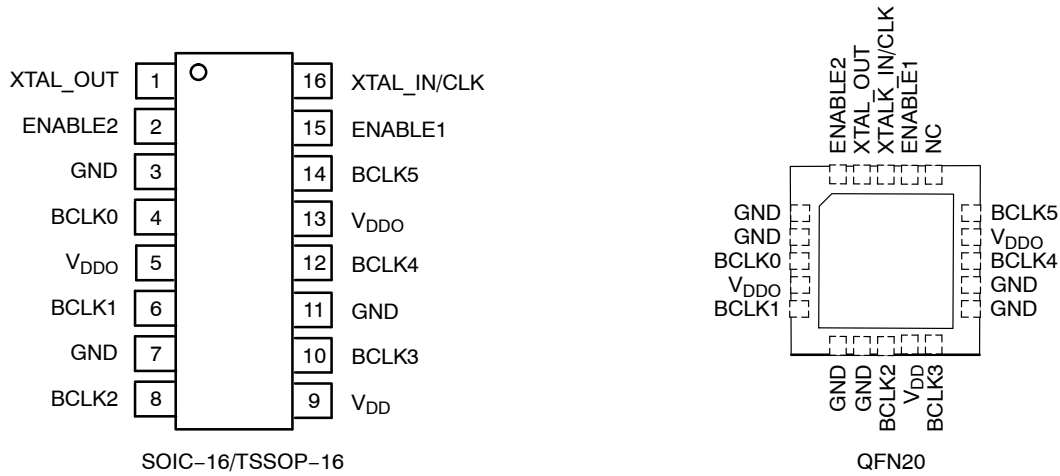## Table 1. PIN DESCRIPTION

SOIC−16 / TSSOP−16	QFN−20	Name	I/O	Description
1	19	XTAL_OUT	Crystal Interface	Oscillator Output to drive Crystal
2	20	ENABLE 2	LVTTL / LVCMOS Input	Synchronous Enable Input for BCLK5 Output. Switches only when HIGH. Open default condition HIGH due to an internal pullup resistor to V_{CC}.
3, 7, 11	1, 2, 6, 7, 11, 12	GND	GND	GND Supply pins. All GND, V_{DD} and V_{DDO} pins must be externally connected to power supply to guarantee proper operation.
4, 6, 8, 10, 12, 14	3, 5, 8, 10, 13, 15	BCLK0, 1, 2, 3, 4, 5	LVCMOS Outputs	Buffered Clock outputs
5, 13	4, 14	V_{DDO}	POWER	Output Positive Supply pins. All GND, V_{DD} and V_{DDO} pins must be externally connected to power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND.
9	9	V_{DD}	POWER	Output Positive Supply pins. All GND, V_{DD} and V_{DDO} pins must be externally connected to power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND.
15	17	ENABLE 1	LVTTL / LVCMOS Input	Synchronous Enable Input for BCLK0/1/2/3/4 Output block. Switches only when HIGH. Open default condition HIGH due to an internal pullup resistor to V_{CC}
16	16	XTAL_IN/ CL$\overline{K}$	Crystal Interface	Oscillator Input from Crystal. Single ended Clock Input.

Table 2. CLOCK ENABLE FUNCTION TABLE

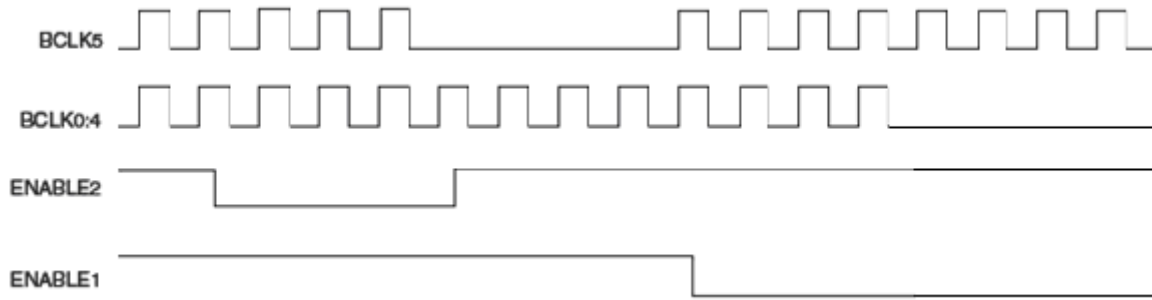| Control Inputs		Outputs	
ENABLE1*	ENABLE2*	BCLK0:BCLK4	BCLK5
0	0	LOW	LOW
0	1	LOW	Toggling
1	0	Toggling	LOW
1	1	Toggling	Toggling

*Defaults HIGH when floating open.

Figure 3. ENABLEx Control Timing Diagram

The ENABLEx control inputs will synchronously enable or disable the selected output(s). This control detects the falling edge of the internal signal and asserts or de−asserts the output after 3 clock cycles. When ENABLEx is LOW, the outputs are disabled to a LOW state. When ENABLEx is HIGH, the outputs are enabled to toggle.

Table 3. RECOMMENDED CRYSTAL PARAMETERS

Crystal	Fundamental AT−Cut
Frequency	10 to 40 MHz
Load Capacitance*	16−20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	35 to 50 Ω Max
Drive Level	1 mW

*See APPLICATION INFORMATION; Crystal Input Interface for CL loading

Table 4. ATTRIBUTES (Note 1)

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index	UL−94 code V−0 A 1/8" 28 to 34
Transistor Count		213 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 5. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 1	Rating	Unit
V_{DDx}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Input Voltage			$-0.5 \leq V_I \leq V_{DD} + 0.5$	V
T_A	Operating Temperature Range, Industrial			-40 to $\leq +85$	°C
T_{stg}	Storage Temperature Range			-65 to $+150$	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	SOIC−16 SOIC−16	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	SOIC−16	33−36	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	TSSOP−16 TSSOP−16	138 108	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	TSSOP−16	33−36	°C/W
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm	QFN−20 QFN−20	47 33	°C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 3)	QFN−20	18	°C/W
T_{sol}	Wave Solder	3 sec @ 248°C		265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Unit
$V_{DD} = V_{DDO} = 3.135$ V to 3.465 V (3.3 V $\pm 5\%$); GND = 0 V, $T_A = -40°C$ to $+85°C$					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			10	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			5	mA
V_{IH}	Input HIGH Voltage ENABLEx	2		V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage ENABLEx	−0.3		0.8	V
V_{OH}	Output HIGH Voltage (Note 4)	2.6			V
V_{OL}	Output LOW Voltage (Note 4)			0.5	V
C_{IN}	Input Capacitance		4		pF
C_{PD}	Power Dissipation Capacitance (per Output) (Note 4)		19		pF
R_{OUT}	Output Impedance (Note 4)		7		Ω
$V_{DD} = V_{DDO} = 2.375$ V to 2.625 V (2.5 V $\pm 5\%$); GND = 0 V, $T_A = -40°C$ to $+85°C$					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			8	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			4	mA
V_{IH}	Input HIGH Voltage ENABLEx	1.7		V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage ENABLEx	−0.3		0.7	V
V_{OH}	Output HIGH Voltage ($I_{OH} = -1$ mA) Output HIGH Voltage (Note 4)	2.0 1.8			V
V_{OL}	Output LOW Voltage ($I_{OL} = 1$ mA) Output LOW Voltage (Note 4)			0.4 0.45	V
C_{IN}	Input Capacitance		4		pF
C_{PD}	Power Dissipation Capacitance (per Output) (Note 4)		18		pF
R_{OUT}	Output Impedance (Note 4)		7		Ω
$V_{DD} = V_{DDO} = 1.6$ V to 2.0 V (1.8 V ± 0.2 V); GND = 0 V, $T_A = -40°C$ to $+85°C$					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			5	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			3	mA
V_{IH}	Input HIGH Voltage ENABLEx	$0.65*V_{DD}$		V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage ENABLEx	−0.3		$0.35*V_{DD}$	V
V_{OH}	Output HIGH Voltage (Note 4)	V_{DDO}−0.3			V
V_{OL}	Output LOW Voltage (Note 4)			0.35	V
C_{IN}	Input Capacitance		4		pF
C_{PD}	Power Dissipation Capacitance (per Output) (Note 4)		16		pF
R_{OUT}	Output Impedance (Note 4)		10		Ω
$V_{DD} = 3.135$ V to 3.465 V (3.3 V $\pm 5\%$); $V_{DDO} = 2.375$ V to 2.625 V (2.5 V $\pm 5\%$); GND = 0 V, $T_A = -40°C$ to $+85°C$					
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			10	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			4	mA
V_{IH}	Input HIGH Voltage ENABLEx	2		V_{DD} + 0.3 V	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Parallel terminated 50 Ω to $V_{DDO}/2$ (see Figure 5).

Table 6. DC CHARACTERISTICS (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
**V$_{DD}$ = 3.135 V to 3.465 V (3.3 V ±5%); V$_{DDO}$ = 2.375 V to 2.625 V (2.5 V ±5%); GND = 0 V, T$_A$ = −40°C to +85°C**
V$_{IL}$	Input LOW Voltage ENABLEx	−0.3		0.8	V
V$_{OH}$	Output HIGH Voltage (I$_{OH}$ = −1 mA) Output HIGH Voltage (Note 4)	2.0 1.8			V
V$_{OL}$	Output LOW Voltage (I$_{OL}$ = 1 mA) Output LOW Voltage (Note 4)			0.4 0.45	V
C$_{IN}$	Input Capacitance		4		pF
C$_{PD}$	Power Dissipation Capacitance (per Output) (Note 4)		18		pF
R$_{OUT}$	Output Impedance (Note 4)		7		Ω
**V$_{DD}$ = 3.135 V to 3.465 V (3.3 V ±5%); V$_{DDO}$ = 1.6 V to 2.0 V (1.8 V ±0.2 V.); GND = 0 V, T$_A$ = −40°C to +85°C**
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			10	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			3	mA
V$_{IH}$	Input HIGH Voltage ENABLEx	2		V$_{DD}$ + 0.3 V	V
V$_{IL}$	Input LOW Voltage ENABLEx	−0.3		0.8	V
V$_{OH}$	Output HIGH Voltage (Note 4)	V$_{DDO}$−0.3			V
V$_{OL}$	Output LOW Voltage (Note 4)			0.35	V
C$_{IN}$	Input Capacitance		4		pF
C$_{PD}$	Power Dissipation Capacitance (per Output) (Note 4)		16		pF
R$_{OUT}$	Output Impedance (Note 4)		10		Ω
**V$_{DD}$ = 2.375 V to 2.625 V (2.5 V ±5%); V$_{DDO}$ = 1.6 V to 2.0 V (1.8 V ±0.2 V); GND = 0 V, T$_A$= −40°C to +85°C**
IDD	Core Quiescent Power Supply Current (ENABLEx = LOW)			8	mA
IDDO	Output Quiescent Power Supply Current (ENABLEx = LOW)			3	mA
V$_{IH}$	Input HIGH Voltage ENABLEx	1.7		V$_{DD}$ + 0.3 V	V
V$_{IL}$	Input LOW Voltage ENABLEx	−0.3		0.7	V
V$_{OH}$	Output HIGH Voltage (Note 4)	V$_{DDO}$−0.3			V
V$_{OL}$	Output LOW Voltage (Note 4)			0.35	V
C$_{IN}$	Input Capacitance		4		pF
C$_{PD}$	Power Dissipation Capacitance (per Output) (Note 4)		16		pF
R$_{OUT}$	Output Impedance (Note 4)		10		Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Parallel terminated 50 Ω to V$_{DDO}$/2 (see Figure 5).

Table 7. AC CHARACTERISTICS

Symbol	Characteristic	Min	Typ	Max	Unit
$V_{DD} = V_{DDO}$ = 3.135 V to 3.465 V (3.3 V ± 5%); GND = 0 V, T_A = −40°C to +85°C (Note 5)					
F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	48		52	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase−Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		−123 −142 −153 −164		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.08 0.08		ps
tr/tf	Output rise and fall times (20%; 80%)	200		800	ps
$V_{DD} = V_{DDO}$ = 2.375 V to 2.625 V (2.5 V ± 5%); GND = 0 V, T_A = −40°C to +85°C (Note 5)					
F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	47		53	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase−Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		−118 −137 −151 −165		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.13 0.13		ps
tr/tf	Output rise and fall times (20%; 80%)	200		800	ps
$V_{DD} = V_{DDO}$ = 1.6 V to 2.0 V (1.8 V ± 0.2 V); GND = 0 V, T_A = −40°C to +85°C (Note 5)					
F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	47		53	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase−Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		−129 −145 −147 −157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.27 0.27		ps
tr/tf	Output rise and fall times (20%; 80%)	200		900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Crystal inputs ≤ F_{max}. Outputs loaded with 50 Ω to V_{DDO}/2. CLOCK (LVCMOS levels at XTAL1 input) 50% duty cycle. See Figures 4 and 7. See APPLICATION INFORMATION; Crystal Input Interface for CL loading.
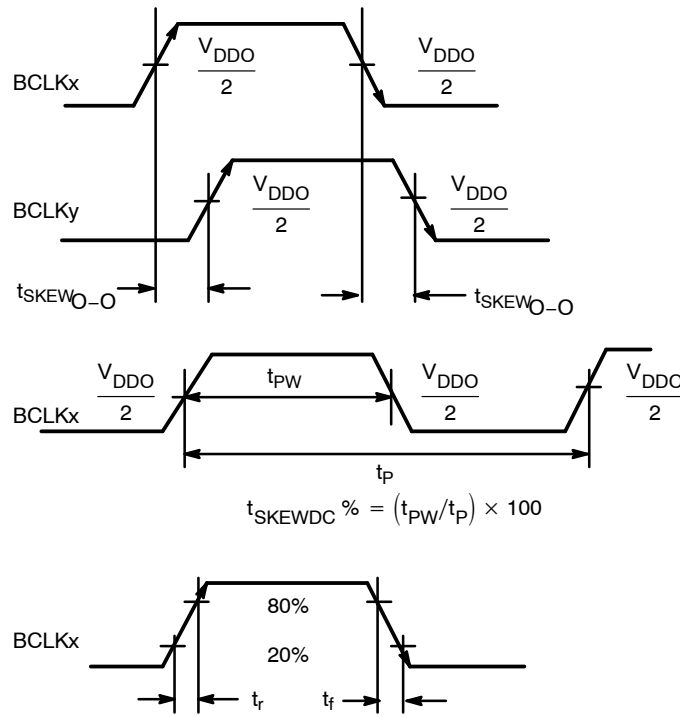
Table 7. AC CHARACTERISTICS (continued)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD} = 3.135 V to 3.465 V (3.3 V $\pm$5%); V_{DDO} = 2.375 V to 2.625 V (2.5 V $\pm$5%); GND = 0 V, T_A = $-40°C$ to +85°C					
F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	48		52	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase−Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		−129 −145 −147 −157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.14 0.14		ps
tr/tf	Output rise and fall times (20%; 80%)	200		800	ps
V_{DD} = 3.135 V to 3.465 V (3.3 V $\pm$5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V $\pm$0.2 V); GND = 0 V, T_A = $-40°C$ to +85°C					
F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	48		52	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase−Noise Performance f_{out} = 25 MHz 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		−129 −145 −147 −157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.18 0.18		ps
tr/tf	Output rise and fall times (20%; 80%)	200		900	ps
V_{DD} = 2.375 V to 2.625 V (2.5 V $\pm$5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V $\pm$0.2 V); GND = 0 V, T_A = $-40°C$ to +85°C					
F_{max}	Input Frequency Crystal	3		40	MHz
	Input Frequency Clock (XTAL1)	DC		100	
t_{EN} / t_{DIS}	Delay for Output Enable / Disable Time ENABLEx to BCLKn			4	Cycles
$tSKEW_{DC}$	Duty Cycle Skew (See Figure 4)	47		53	%
$tSKEW_{O-O}$	Output to Output Skew Within A Device (same conditions)	0	50	80	ps
ΦNOISE	Phase−Noise Performance f_{out} = 25 MHz/ 100 Hz off Carrier 1 kHz off Carrier 10 kHz off Carrier 100 kHz off Carrier		−129 −145 −147 −157		dBc/Hz
tJIT(Φ)	RMS Phase Jitter 25 MHz carrier, Integration Range 12 kHz to 20 MHz 25 MHz carrier, Integration Range 100 Hz to 1 MHz		0.19 0.19		ps
tr/tf	Output rise and fall times (20%; 80%)	200		900	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. Crystal inputs $\leq$ F_{max}. Outputs loaded with 50 Ω to V_{DDO}/2. CLOCK (LVCMOS levels at XTAL1 input) 50% duty cycle.
See Figures 4 and 7. See APPLICATION INFORMATION; Crystal Input Interface for CL loading.
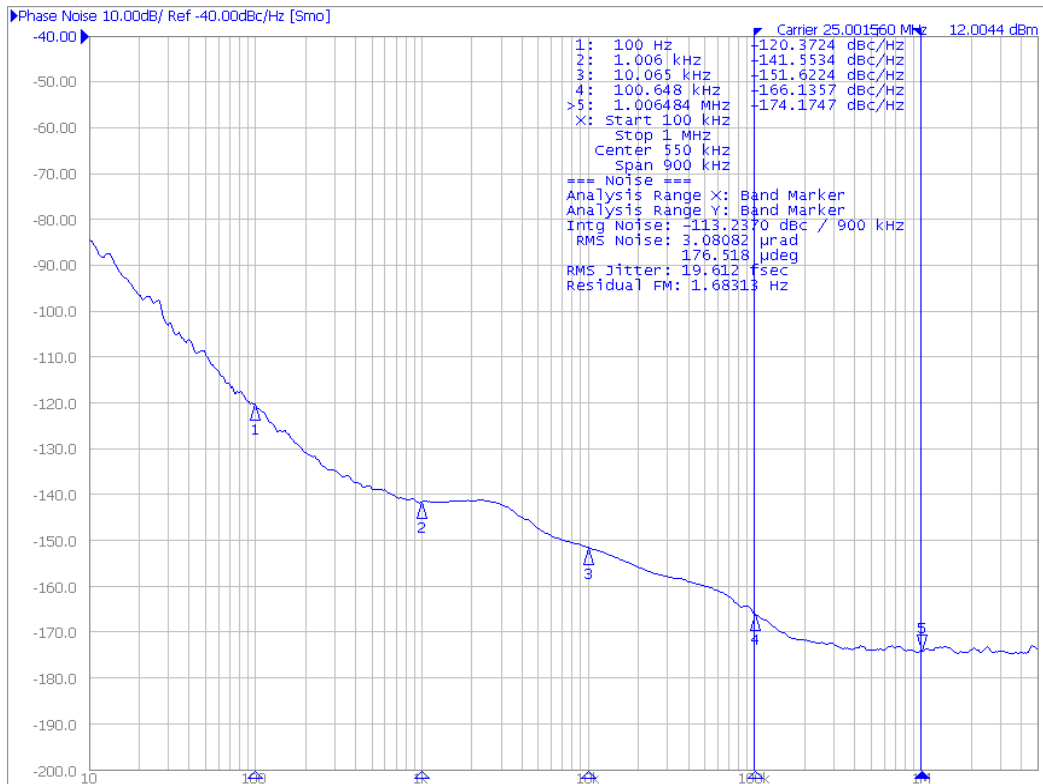
Figure 4. AC Reference Measurement

Figure 5. Typical Phase Noise Plot of the NB3H83905C Operating at 25 MHz V_{CC} = V_{CCO}= 3.3 V
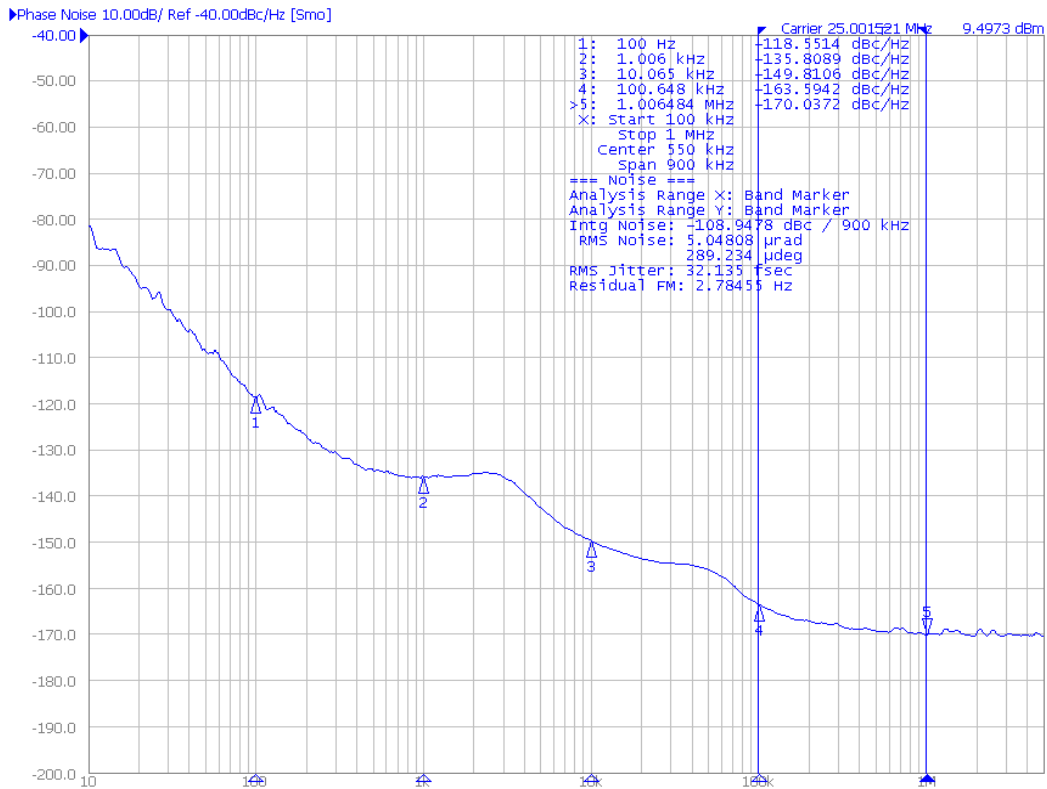
Figure 6. Typical Phase Noise Plot of the NB3H83905C Operating at 25 MHz V_{CC} = V_{CCO} = 2.5 V
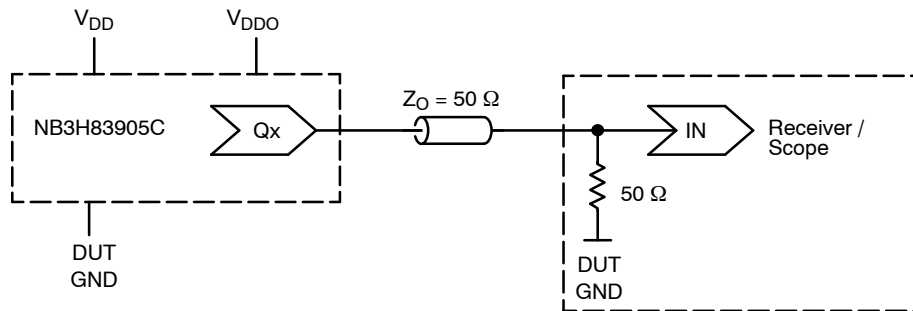

Figure 7. Typical Device Evaluation and Termination Setup

Table 8. TEST SUPPLY SETUP. V_{DDO} SUPPLY MAY BE CENTERED ON 0.0 V (SCOPE GND) TO PERMIT DIRECT CONNECTION INTO "50 Ω TO GND" SCOPE MODULE. V_{DD} SUPPLY TRACKS DUT GND PIN

Spec Condition:	Test Setup V_{DD}:	Test Setup V_{DDO}:	Test Setup DUT GND:
V_{DD} = V_{DDO} = 3.135 V to 3.465 V (3.3 V ±5%)	1.56 to 1.73 V	1.56 to 1.73 V	−1.56 to −1.73 V
V_{DD} = V_{DDO} = 2.375 V to 2.625 V (2.5 V ±5%)	1.1875 to 1.3125 V	1.1875 to 1.3125 V	−1.1875 to −1.3125 V
V_{DD} = V_{DDO} = 1.6 V to 2.0 V (1.8 V ±0.2 V)	0.8 to 1.0 V	0.8 to 1.0 V	−0.8 to −1.0 V
V_{DD} = 3.135 V to 3.465 V (3.3 V ±5%); V_{DDO} = 2.375 V to 2.625 V (2.5 V ±5%)	1.955 to 2.1525 V	1.1875 to 1.3125 V	−1.1875 to −1.3125 V
V_{DD} = 3.135 V to 3.465 V (3.3 V ±5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ±0.2 V)	2.335 to 2.465 V	0.8 to 1.0 V	−0.8 to −1.0 V
V_{DD} = 2.375 V to 2.625 V (2.5 V ±5%); V_{DDO} = 1.6 V to 2.0 V (1.8 V ±0.2 V)	1.575 to 1.625 V	0.8 to 1.0 V	−0.8 to −1.0 V

NB3H83905C

APPLICATION INFORMATION

Crystal Input Interface

Figure 8 shows the NB3H83905C device crystal oscillator interface using a typical parallel resonant crystal. A parallel crystal with loading capacitance C_L = 18 pF would use C1 = 32 pF and C2 = 32 pF as nominal values, assuming 4 pF of stray cap per line. The frequency accuracy and duty cycle skew can be fine tuned by adjusting the C1 and C2 values. For example, increasing the C1 and C2 values will reduce the operational frequency. Note R1 is optional and may be 0 Ω.
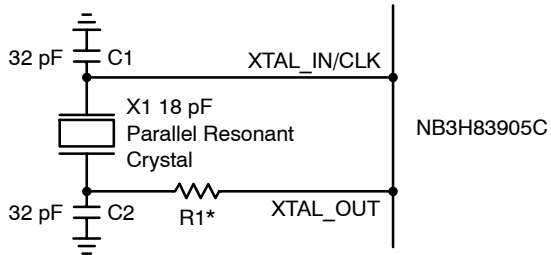
Figure 8. NB3H83905C Crystal Oscillator Interface
* R1 is optional

Termination

NB3H83905C device output series termination may be used by locating a 28 Ω series resistor at the driver pin as shown in Figure 8. Alternatively, a Thevenin Parallel termination may be used by locating a 100 Ω pullup resistor to V_{DD} and a 100 Ω pullup resistor to GND at the receiver pin, instead of an Rs source termination resistor.

Unused Input and Output Pins

All LVCMOS control pins have internal pull−ups or pull−downs; additional external resistors are not required (optionally 1 kΩ resistors may be used). All unused LVCMOS outputs can be left floating with no trace attached.

Bypass

The V_{DD} and V_{DDO} supply pins should be bypassed with both a 10 μF and a 0.1 μF cap from supply pins to GND.

ORDERING INFORMATION

Device	Package	Shipping[†]
NB3H83905CDG	SOIC−16 (Pb − Free)	48 Units / Rail
NB3H83905CDR2G	SOIC−16 (Pb − Free)	2500 Units / Tape & Reel
NB3H83905CDTG	TSSOP−16 (Pb − Free)	96 Units /Rail
NB3H83905CDTR2G	TSSOP−16 (Pb − Free)	2500 Units / Tape & Reel
NB3H83905CMNG	QFN−20 (Pb−Free)	92 Units / Rail
NB3H83905CMNTXG	QFN−20 Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB3H83905C

PACKAGE DIMENSIONS

SOIC−16
CASE 751B−05
ISSUE K
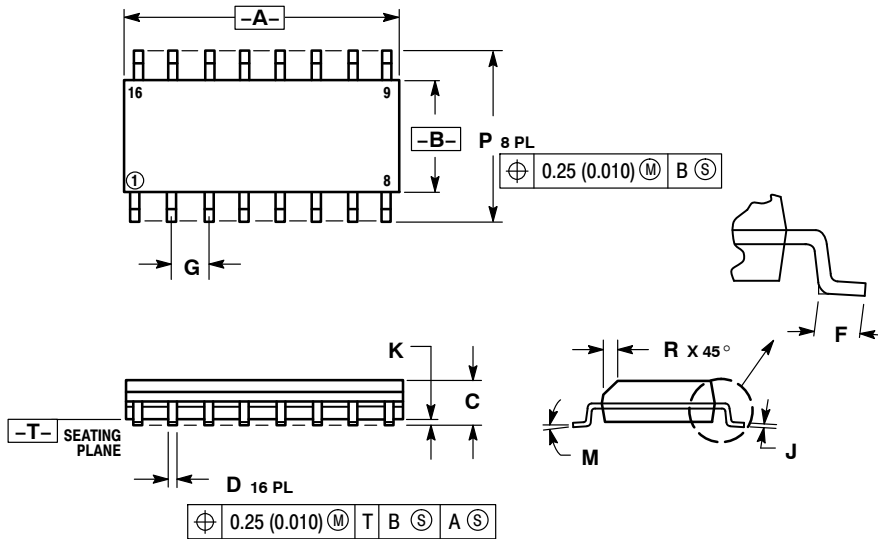
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*
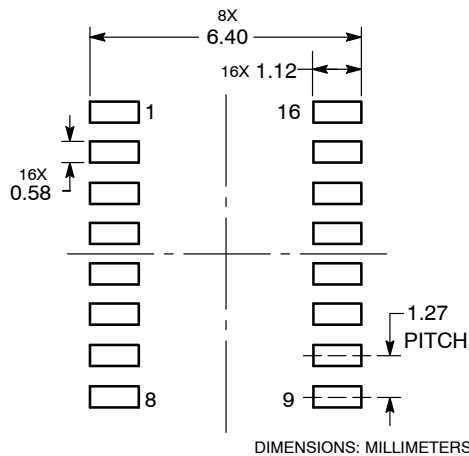
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NB3H83905C

PACKAGE DIMENSIONS
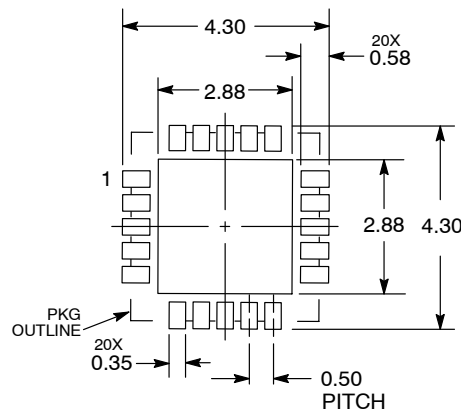
TSSOP−16
CASE 948F−01
ISSUE B
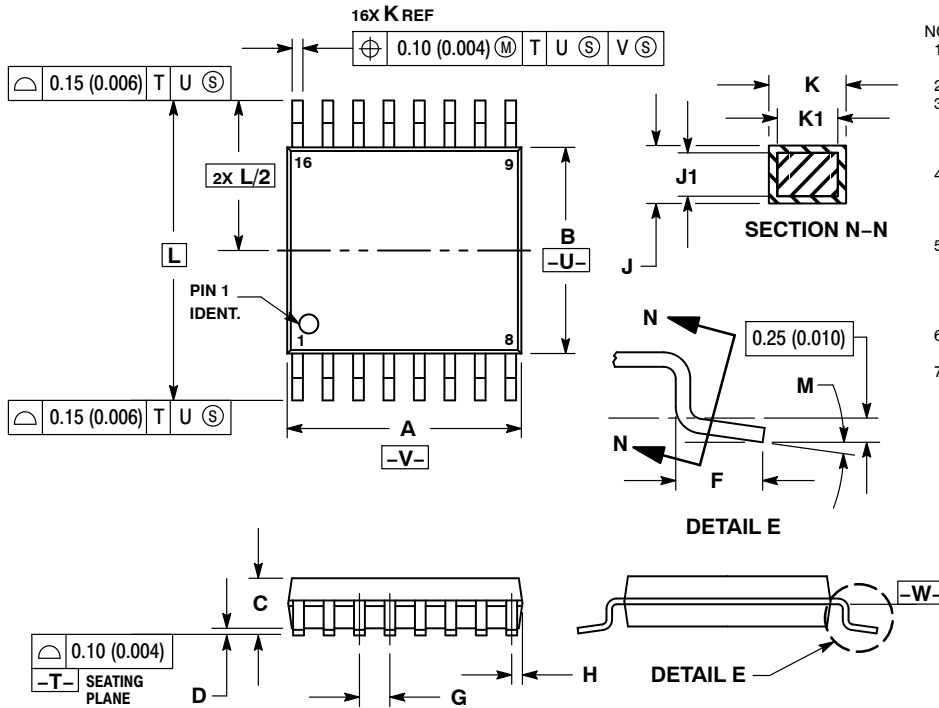
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*
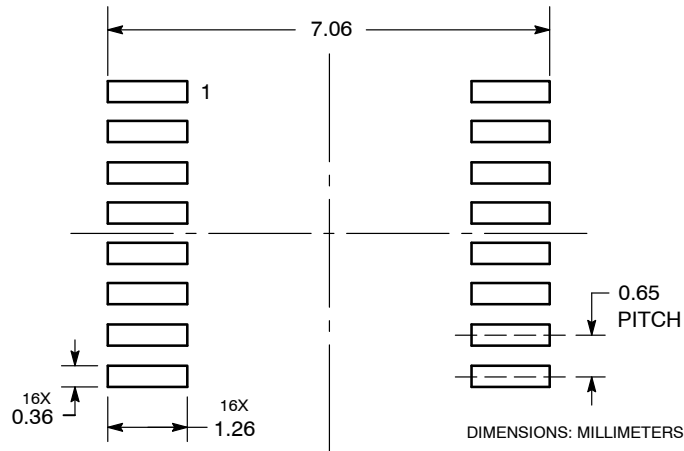
7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NB3H83905C

PACKAGE DIMENSIONS

QFN20, 4x4, 0.5P
CASE 485E–01
ISSUE B
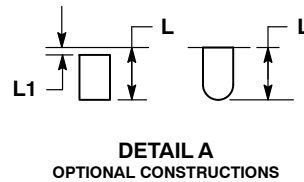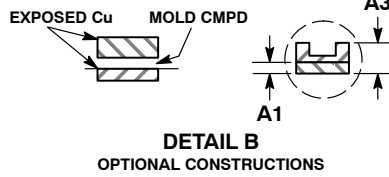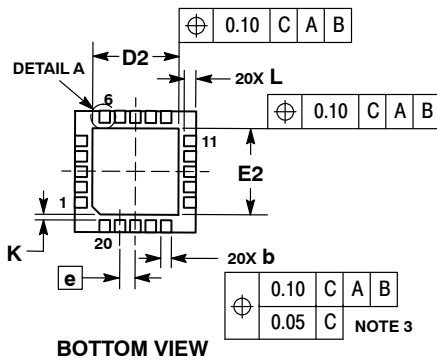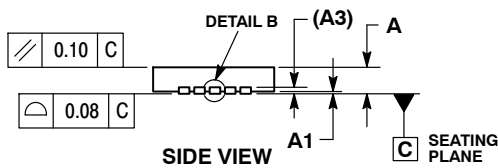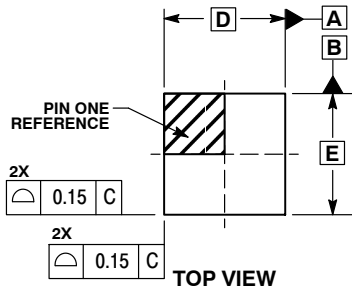
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| DIM | MILLIMETERS | |
	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.90
E	4.00 BSC	
E2	2.60	2.90
e	0.50 BSC	
K	0.20 REF	
L	0.35	0.45
L1	0.00	0.15

TOP VIEW

DETAIL B
OPTIONAL CONSTRUCTIONS

SIDE VIEW

DETAIL A
OPTIONAL CONSTRUCTIONS

BOTTOM VIEW

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NB3H83905C/D