

NCV7240

Octal Low-Side Relay Driver

The NCV7240 is an automotive eight channel low-side driver providing drive capability up to 600 mA per channel. Output control is via a SPI port and offers convenient reporting of faults for open load (or short to ground), over load, and over temperature conditions. Additionally, parallel control of the outputs is addressable (in pairs) via the INx pins.

A dedicated limp-home mode pin (LHI) enables OUT1-OUT4 while disabling OUT5-OUT8.

Each output driver is protected for over load current and includes an output clamp for inductive loads.

The NCV7240 is available in a SSOP-24 fused lead package.

Features

- 8 Channels
- 600 mA Low-Side Drivers
 - ◆ $R_{DS(on)}$ 1.5 Ω (Typ), 3 Ω (Max)
- 16-bit SPI Control
 - ◆ Frame Error Detection (8-bit)
 - ◆ Daisy Chain Capable
- Parallel Input Pins for PWM operation
- Power Up Without Open Circuit Detection Active (for LED applications)
- Low Quiescent Current in Sleep and Standby Modes
- Limp Home Functionality
- 3.3 V and 5 V compatible Digital Input Supply Range
- Fault Reporting
 - ◆ Open Load Detection (selectable)
 - ◆ Over Load
 - ◆ Over Temperature
- Power-on Reset (VDD, VDDA)
- SSOP-24 Package (internally fused leads)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

Applications

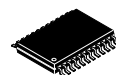
- Automotive Body Control Unit
- Automotive Engine Control Unit
- Relay Drive
- LED Drive
- Stepper Motor Driver



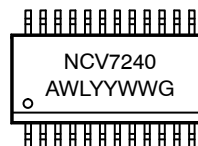
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



SSOP-24
CASE 565AL



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 25 of this data sheet.

NCV7240

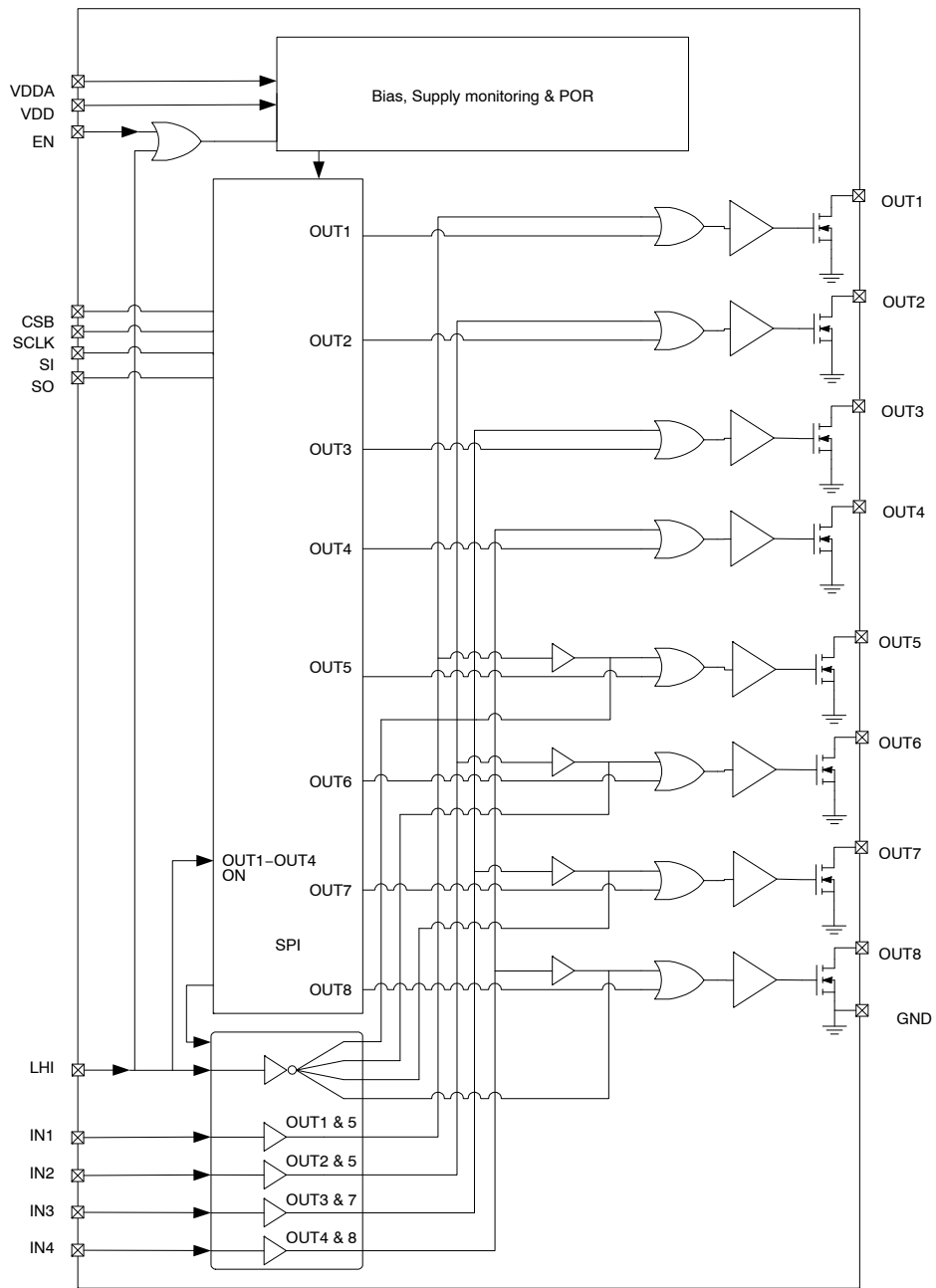


Figure 1. Basic Block Diagram

NCV7240

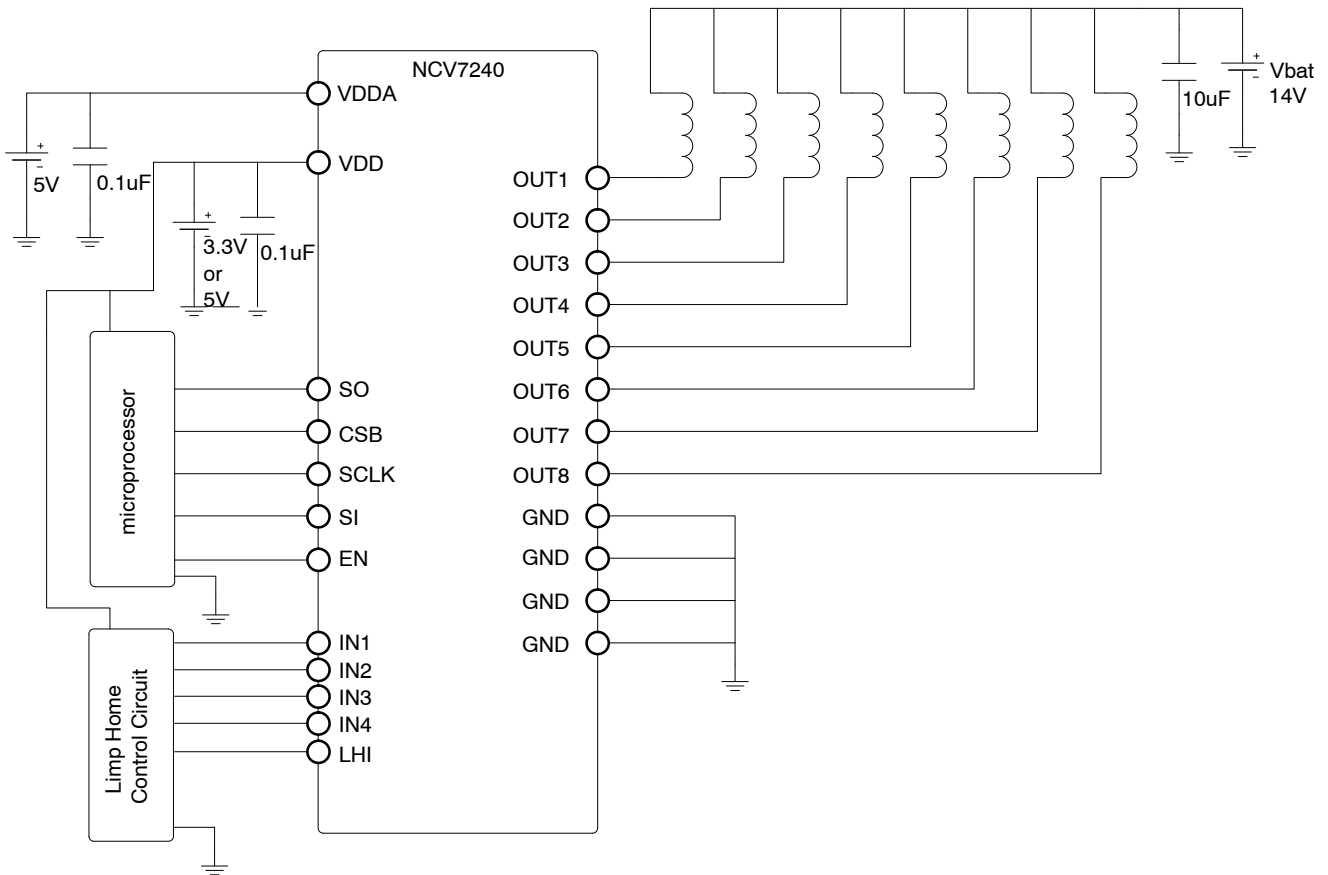


Figure 2. Application Diagram (relay loads)

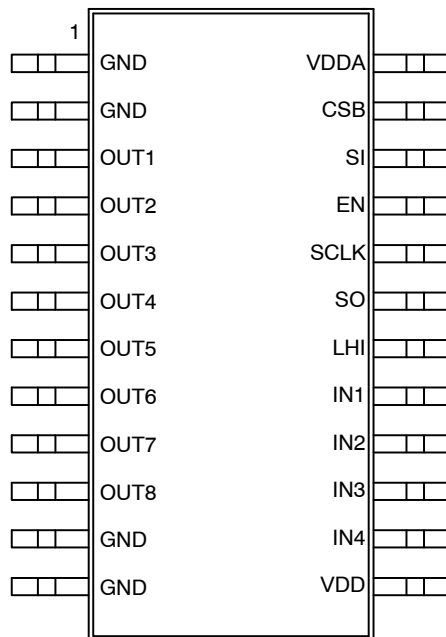


Figure 3. Pinout

NCV7240

PACKAGE PIN DESCRIPTION

SSOP-24	Symbol	Description
1	GND	Ground.
2	GND	Ground.
3	OUT1	Channel 1 low-side drive output. Requires an external pull-up device for operation.
4	OUT2	Channel 2 low-side drive output. Requires an external pull-up device for operation.
5	OUT3	Channel 3 low-side drive output. Requires an external pull-up device for operation.
6	OUT4	Channel 4 low-side drive output. Requires an external pull-up device for operation.
7	OUT5	Channel 5 low-side drive output. Requires an external pull-up device for operation.
8	OUT6	Channel 6 low-side drive output. Requires an external pull-up device for operation.
9	OUT7	Channel 7 low-side drive output. Requires an external pull-up device for operation.
10	OUT8	Channel 8 low-side drive output. Requires an external pull-up device for operation.
11	GND	Ground.
12	GND	Ground.
13	VDD	Digital Power Supply for SO output (3.3 V or 5 V).
14	IN4	Parallel control of OUT4 and OUT8 Ground if not used for best EMI performance. Alternatively keep open and internal pull-down will hold the input low. (120 k Ω pull down resistor).
15	IN3	Parallel control of OUT3 and OUT7 Ground if not used for best EMI performance. Alternatively keep open and internal pull-down will hold the input low. (120 k Ω pull down resistor).
16	IN2	Parallel control of OUT2 and OUT6. Ground if not used for best EMI performance. Alternatively keep open and internal pull-down will hold the input low. (120 k Ω pull down resistor).
17	IN1	Parallel control of OUT1 and OUT5. Ground if not used for best EMI performance. Alternatively keep open and internal pull-down will hold the input low. (120 k Ω pull down resistor).
18	LHI	Limp Home Input. Active High. A high on this pin powers up the device and activates the respective output drive INx designator while disabling outputs OUT5-OUT8. Input SPI commands are ignored, but the output register reports faults. (Read capability only. No write capability.) All registers are reset coming out of LHI mode. Ground if not used for best EMI performance. Alternatively keep open and internal pull-down resistor (120 k Ω) will hold the input low.
19	SO	SPI serial data output. Output high voltage level referenced to pin VDD.
20	SCLK	SPI clock (120 k Ω pull down resistor).
21	EN	Global Enable (active high). (120 k Ω pull down resistor).
22	SI	SPI serial data input (120 k Ω pull down resistor).
23	CSB	SPI Chip Select "Bar" (120 k Ω pull up resistor to VDD).
24	VDDA	Analog Power Supply Input voltage (5 V).

MAXIMUM RATINGS

Parameter	Min	Max	Unit
Supply Input Voltage (VDDA, VDD) DC	-0.3	5.5	V
Digital I/O pin voltage (EN, LHI, Inx, CSB, SCLK, SI) (SO)	-0.3 -0.3	5.5 $V_{DD} + 0.3$	V
High Voltage Pins (OUTx) DC Peak Transient	-0.3	36 44 (Note 1)	V
Output Current (OUTx)	-1	1.3	A
Clamping Energy Maximum (single pulse) Repetitive (multiple pulse) (Note 2)	- -	75 -	mJ
Operating Junction Temperature Range	-40	150	°C
Storage Temperature Range	-55	150	°C
ESD Capability, Human body model (100 pF, 1.5 kΩ) (OUTx pins) Human body model (100 pF, 1.5 kΩ) (all other pins)	-4000 -2000	4000 2000	V
ESD Capability Machine Model (200 pF)	-200	200	V
AECQ10x-12-RevA Short Circuit Reliability Characterization	Grade A	-	

PACKAGE

Moisture Sensitivity Level	MSL2	-
Lead Temperature Soldering: SMD style only, Reflow (Note 3) Pb-Free Part 60 – 150 sec above 217°C, 40 sec max at peak	265 peak	°C
Package Thermal Resistance (per JESD51) SSOP-24 Junction-to-Ambient (1s0p + 600 mm ² Cu) (Note 4) Junction-to-Ambient (2s2p) (Notes 4 and 5) Junction-to-Pin (pins 1, 2, 11, 12) (Note 6)	 68 62 30	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Internally limited. Specification applies to unpowered and powered modes. (0 V to VDDA, 0 V to VDD)
2. Testing particulars, 2M pulses, $V_{bat} = 15\text{ V}$, $63\ \Omega$, 390 mH, $T_A = 25^\circ\text{C}$. (See Figure 4)
3. For additional information, see or download ON Semiconductor's Soldering and Mounting Techniques Reference Manual, SOLDERRM/D and Application Note AND8083/D.
4. 76 mm x 76 mm x 1.5 mm FR4 PCB with additional heat spreading copper (2 oz) of 600 mm², LS1 to LS8 dissipating 100 mW each. No vias.
5. Include 2 inner 1 oz copper layers. No vias.
6. One output dissipating 100 mW.

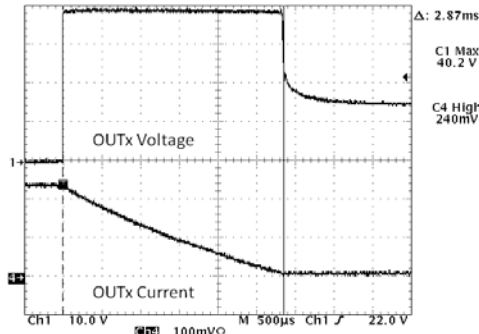


Figure 4. Repetitive Clamping Energy Test

NCV7240

ELECTRICAL CHARACTERISTICS (3.0 V < VDD < VDDA, 4.5 V < VDDA (Note 7) < 5.5 V, -40°C ≤ T_J ≤ 150°C, EN = VDD, LHI = 0 V unless otherwise specified).

Characteristic	Conditions	Min	Typ	Max	Unit
GENERAL					
Operating Current (VDDA) ON Mode (All Channels On)		-	3	5	mA
Quiescent Current (VDDA) Global Standby Mode (All Channels Off)	SI = SCLK = 0 V, CSB = VDD T _J = 25°C T _J = 85°C T _J = 150°C	- - -		32 35 40	μA
Quiescent Current (VDDA) Low Iq Mode	SI = SCLK = EN = 0 V, CSB = VDD T _J = 25°C T _J = 85°C T _J = 150°C	- - -	- - -	10 10 20	μA
Operating Current (VDD) ON Mode (All Channels On)	EN=high, SCLK = I _{nx} = 0 V, CSB = VDD = VDDA	-	0.3	0.5	mA
Quiescent Current (VDD) Global Standby Mode (All Channels Off)	CSB = VDD = VDDA, f _{SCLK} = 0 Hz T _J = 25°C T _J = 85°C T _J = 150°C	- - -	- - -	20 20 40	μA
Quiescent Current (VDD) Low Iq Mode	EN = 0 V T _J = 25°C T _J = 85°C T _J = 150°C	- - -	- - -	5 5 20	μA
Power-on Reset threshold (VDDA)	VDDA rising	-	3.8	4.5	V
Power-on Reset Hysteresis (VDDA)		150	200	350	mV
Power-on Reset threshold (VDD)	VDD rising	-	2.4	2.7	V
Power-on Reset Hysteresis (VDD)		75	100	240	mV
Thermal Shutdown (Note 8)	Not ATE tested.	150	175	200	°C
Thermal Hysteresis	Not ATE tested.	10	25	-	°C

OUTPUT DRIVER

Output Transistor R _{DS(on)}	IOUTx = 180 mA	-	1.5	3.0	Ω
Overload Detection Current		0.6	0.95	1.3	A
Output Leakage	OUTx = 13.5 V, 25°C OUTx = 13.5 V OUTx = 36 V	- - -	- - -	1 5 10	μA
Output Clamp Voltage	VDD = 0 V to 5.5 V VDDA = 0 V to 5.5 V IOUTx = 50 mA	36	40	44	V
Output Body Diode Voltage	IOUTx = -180mA	-	-	1.5	V
Open Load Detection Threshold Voltage (Vol)		1.0	1.75	2.5	V
Open Load Diagnostic Sink Current (Iol)	1 V < OUTx < 13.5 V, Output Disabled	20	60	100	μA

OUTPUT TIMING SPECIFICATIONS

Enable (EN) wake-up time	CSB = 0 V EN going high 80% to SO active	-	-	200	μs
Enable (EN) and LHI (Note 9) Signal Duration		50	-	-	μs

7. Reduced performance down to 4 V provided VDDA Power-On Reset threshold has not been breached.

8. Each output driver is protected by its' own individual thermal sensor.

9. Input signals H→L→H greater than 50usec are guaranteed to be detected.

NCV7240

ELECTRICAL CHARACTERISTICS (3.0 V < VDD < VDDA, 4.5 V < VDDA (Note 7) < 5.5 V, -40°C ≤ T_J ≤ 150°C, EN = VDD, LHI = 0 V unless otherwise specified).

Characteristic	Conditions	Min	Typ	Max	Unit
OUTPUT TIMING SPECIFICATIONS					
Serial Control Output turn-on time All Channels	CSB going high 80% to OUTx going low 20% V _{bat} , V _{bat} = 13.5 V, I _{DS} = 180 mA resistive load	-	30	50	μs
Serial Control Output turn-off time All Channels	CSB going high 80% to OUTx going high 80% V _{bat} , V _{bat} = 13.5 V, I _{DS} = 180 mA resistive load	-	30	50	μs
Parallel Control Output turn-on time All Channels	INx going high 80% to OUTx going low 20% V _{bat} , V _{bat} = 13.5 V, I _{DS} = 180 mA resistive load	-	30	50	μs
Parallel Control Output turn-off time All Channels	Inx going low 20% to OUTx going high 80% V _{bat} , V _{bat} = 13.5 V, I _{DS} = 180 mA resistive load	-	30	50	μs
Over Load Shut-Down Delay Time		3	15	50	μs
Open Load Detection Time		30	115	200	μs

DIGITAL INTERFACE CHARACTERISTICS

INPUT CHARACTERISTICS

Digital Input Threshold (CSB, SI, SCLK, LHI, EN, INx)		0.8	1.4	2.0	V
Digital Input Hysteresis (CSB, SI, SCLK, INx)		50	175	300	mV
Digital Input Hysteresis (LHI, EN)		150	400	800	mV
Input Pulldown Resistance (SI, SCLK, LHI, EN, INx)	Inx = SI = SCLK = LHI = EN = VDD	50	120	190	kΩ
Input Pullup Resistance (CSB)	CSB = 0 V	50	120	190	kΩ
CSB Leakage to VDD	CSB = 5 V, VDD = 0 V	-	-	100	μA
CSB Leakage to VDDA	CSB = 5 V, VDDA = 0 V	-	-	100	μA

OUTPUT CHARACTERISTICS

SO – Output High	I(out) = -1.5 mA	V _{DD} - 0.4	-	-	V
SO – Output Low	I(out) = 2.0 mA	-	-	0.6	V
SO Tri-state Leakage	CSB = VDD	-3	0	3	μA

SPI TIMING (all timing specifications measured at 20% and 80% voltage levels)

SCLK Frequency		-	-	5	MHz
SCLK Clock Period		200	-	-	ns
SCLK High Time	Figure 5, #1	85	-	-	ns
SCLK Low Time	Figure 5, #2	85	-	-	ns
SI Setup Time	Figure 5, #11	50	-	-	ns
SI Hold Time	Figure 5, #12	50	-	-	ns
CSB Setup Time	Figure 5, #5, 6	100	-	-	ns
CSB High Time	Figure 5, #7	1.5	-	-	μs
SCLK Setup Time	Figure 5, #3, 4	85	-	-	ns
SO Output Enable Time (CSB falling to SO valid)	Figure 5, #8, C _{load} = 50 pF Not ATE tested	-	-	200	ns
SO Output Disable Time (CSB rising to SO tri-state)	Figure 5, #9 Not ATE tested	-	-	200	ns
SO Output Data Valid Time with capacitive load	Figure 5, #10, C _{load} = 50 pF Not ATE tested	-	-	100	ns

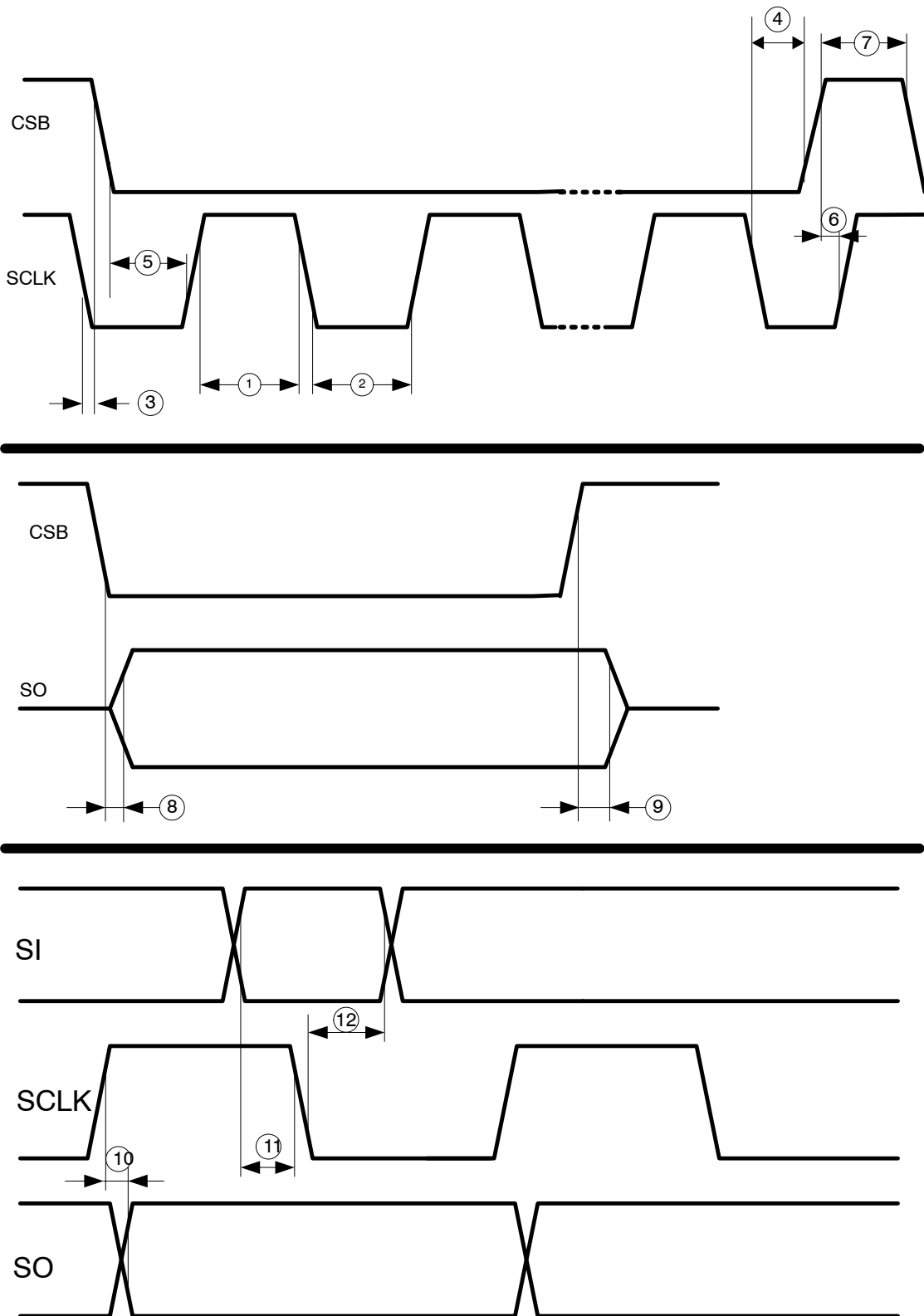


Figure 5. Detailed SPI Timing (measured at 20% and 80% voltage levels)

TYPICAL PERFORMANCE GRAPHS

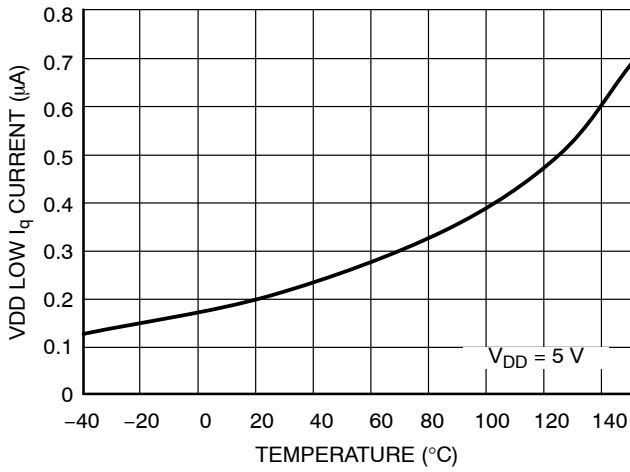


Figure 6. VDD Low I_q Current vs. Temperature

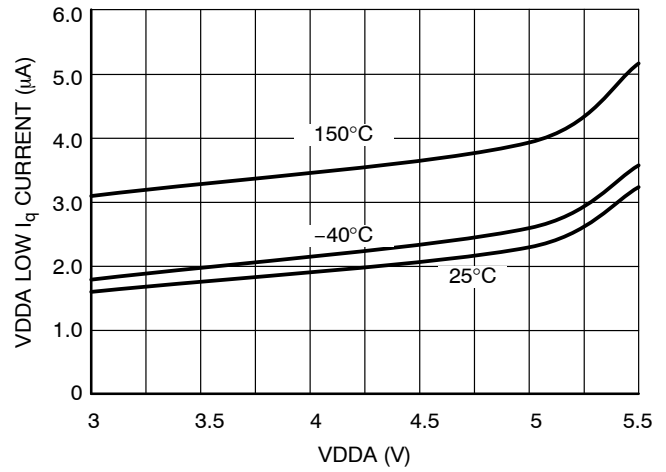


Figure 7. VDDA Low I_q Quiescent Current vs. VDDA

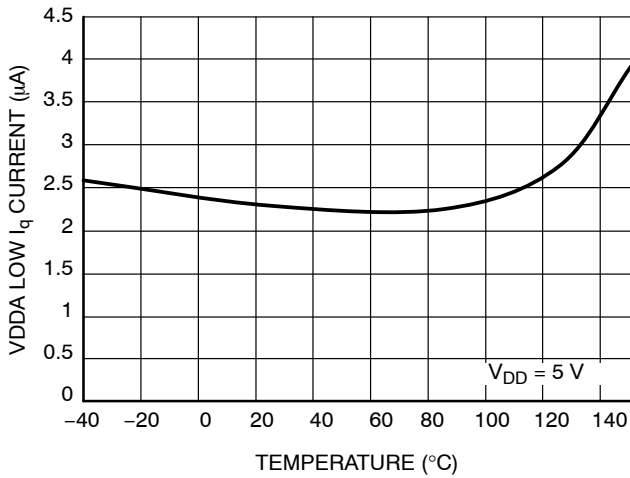


Figure 8. VDDA Low I_q Current vs. Temperature

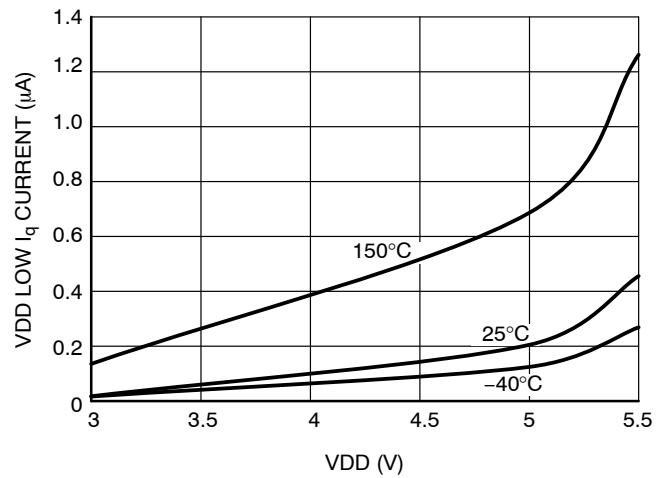


Figure 9. VDD Low I_q Current vs. VDD

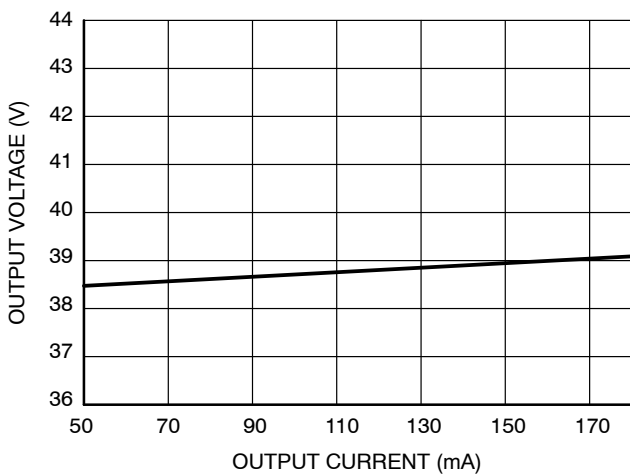


Figure 10. Output Clamp Voltage vs. Current

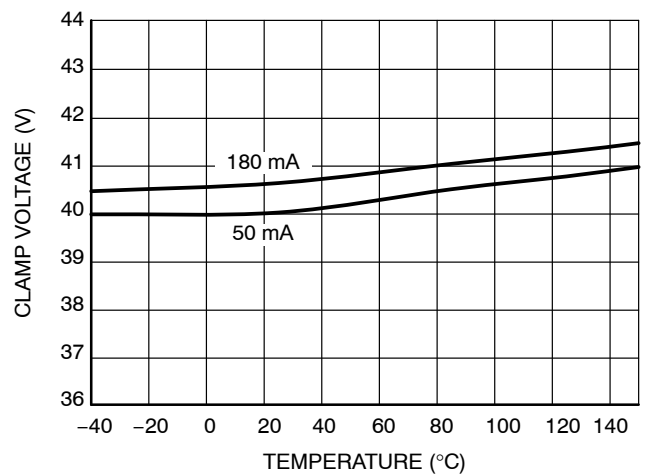


Figure 11. Output Clamp Voltage vs. Temperature

TYPICAL PERFORMANCE GRAPHS

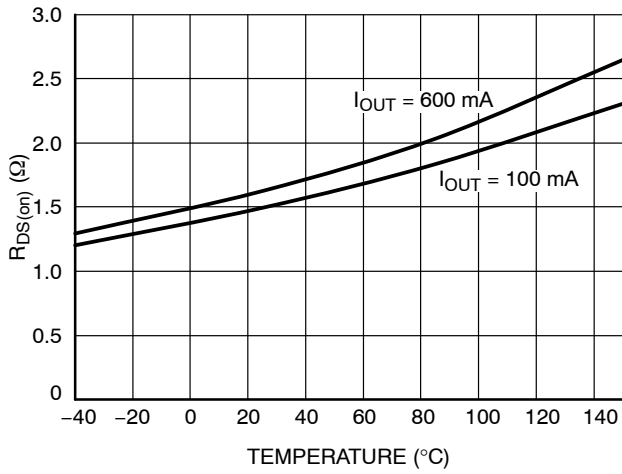


Figure 12. Output R_{DS(on)} vs. Temperature

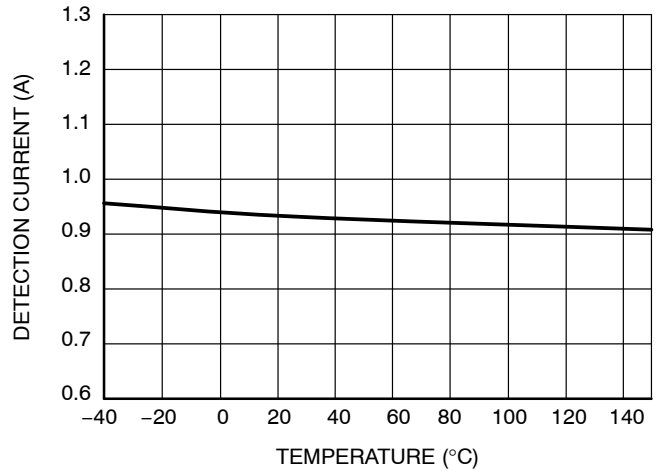


Figure 13. Over Load Current vs. Temperature

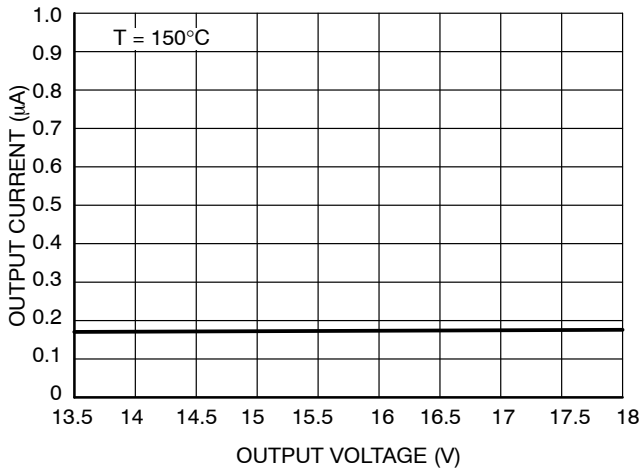


Figure 14. Output Leakage vs. Voltage (150°C)

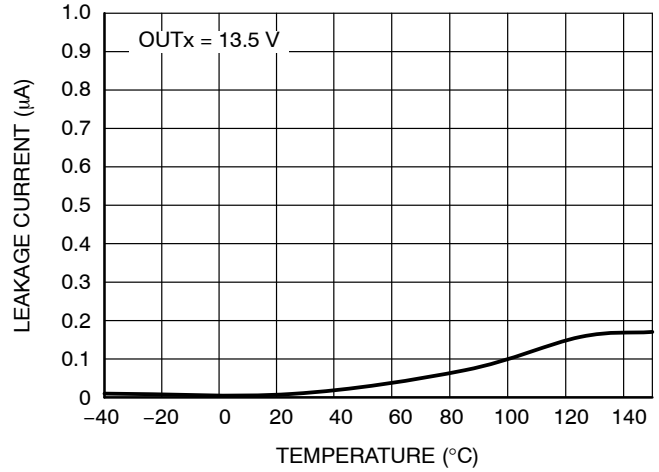


Figure 15. Output Leakage vs. Temperature

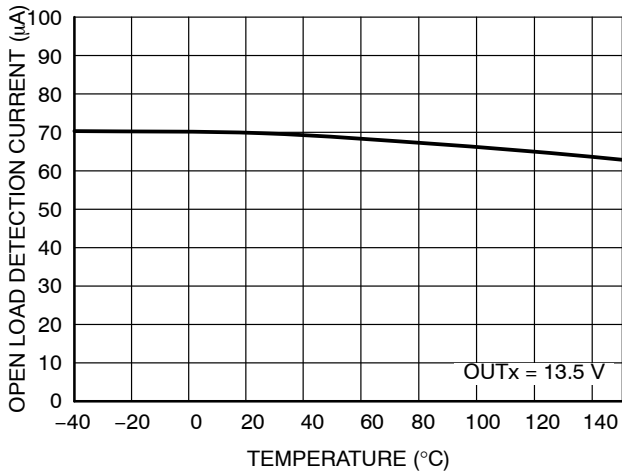


Figure 16. Output Load Detection Current vs. Temperature

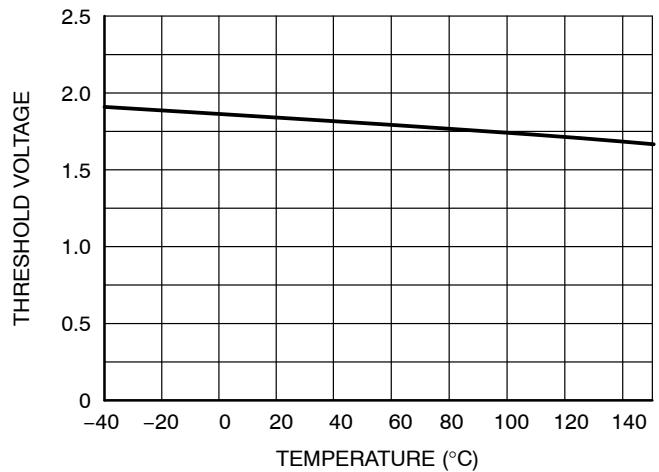


Figure 17. Open Load Detection Voltage vs. Temperature

NCV7240

TYPICAL PERFORMANCE GRAPHS

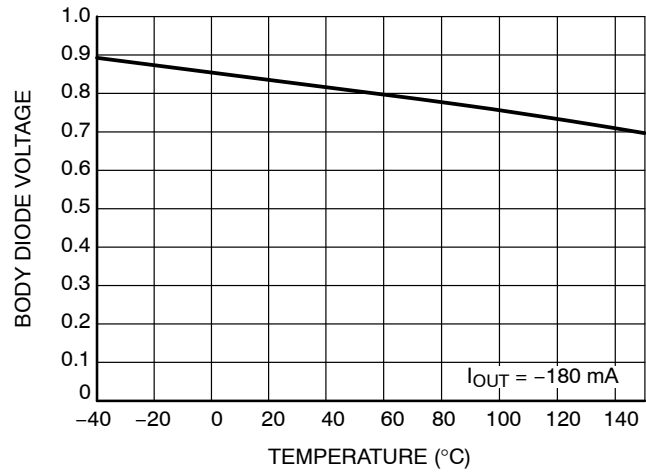


Figure 18. Output Body Diode Voltage vs. Temperature

DETAILED OPERATING DESCRIPTION

Power Outputs

The NCV7240 provides eight independent 600mA power transistors with their source connection referenced to the ground pin and with their drain connection brought out to individual pins resulting in 8 independent low-side drivers. Output driver location on one side of the IC layout provides for optimum pcb layout to the loads.

Internal clamping structures are provided to limit transient voltages when switching inductive loads. Each output has an over load detection current of 0.6 A (min) where the drivers turn-off and stay latched off. An Over Load Current Shut-Down Delay Time of 3 μs (min) is designed into the IC as a filter allowing for spikes in current which may occur during normal operation and allowing for protection from overload conditions.

Faults can be cleared with the SPI input register (**command 00**) or via a power-on-reset. Fault detection is provided in real time. Detection is provided both during output turn-on and with output already on. (See Page 17, Clearing the Fault Registers)

The NCV7240 is available in a SSOP-24 package.

Output Control (SPI)

Each output driver is controlled via a digital SPI port after the device has powered up (out of POR) and enabled via the

EN pin. The NCV7240 device will go through a power up reset each time the EN pin is toggled high resulting in a device setup of default values as described in the Register Specifics section. Standby Mode, Input Mode, ON Mode, and OFF Mode are all selectable via the SPI for each channel independently.

Power up, Power-On Reset (UVLO mode)

Both VDD and VDDA supply an independent power-on-reset function to the IC. Coming out of power-on-reset all input bits are set to a 1 (OFF Mode) and all output bits are set to a 0 except for the TER bit which is set to a 1. The device cannot operate without both supplies above their respective power-on reset thresholds with the exception of LHI mode. During LHI mode, VDD POR is ignored and the device is only affected by VDDA POR.

The NCV7240 powers up into the Global OFF Mode without the open circuit diagnostic current enabled. This allows the device to be turned on via EN = 0 to EN = 1 with LED loads avoiding illumination of the LED loads (reference Figure 21 State Diagram). All other paths to Global OFF Mode enable open circuit diagnostic current.

Table 1. MODES OF OPERATION

Modes of Operation	Conditions	Description
UVLO Mode	VDD or VDDA below their respective POR thresholds	All outputs off in this mode. Coming out of this mode with EN = 1 sets all channels in the OFF mode without open circuit diagnostic current enabled. With LHI = 1 and EN = x, the part enters limp home mode.
OFF Mode	SPI Control (Command 11)	Output off. Open circuit diagnostic current is disabled (powerup mode). Open circuit diagnostic current is enabled (normal mode).
Global OFF Mode	SPI Control All Channels (Command 11)	Output off. Open circuit diagnostic current is disabled (powerup mode). Open circuit diagnostic current is enabled (normal mode).
ON Mode	SPI Control (Command 10)	Output on.
Limp Home Mode (LHI)	LHI = high, EN = x	Dedicated output turn on control of OUT1-OUT4 using IN1-IN4. OUT5-OUT8 are in OFF Mode.
Low Iq Mode	EN = LHI = low	Provides a state with the lowest quiescent current for V _{DD} and VDDA.
Standby Mode	SPI Control (Command 00)	Provides an OFF state with Open circuit diagnostic current disabled.
Global Standby Mode	SPI Control All Channels (Command 00)	Provides a reduced quiescent current mode. Provides an OFF state with Open circuit diagnostic current disabled.
Input Mode	SPI Control (Command 01)	Directs output channel to be driven from INx input pins.

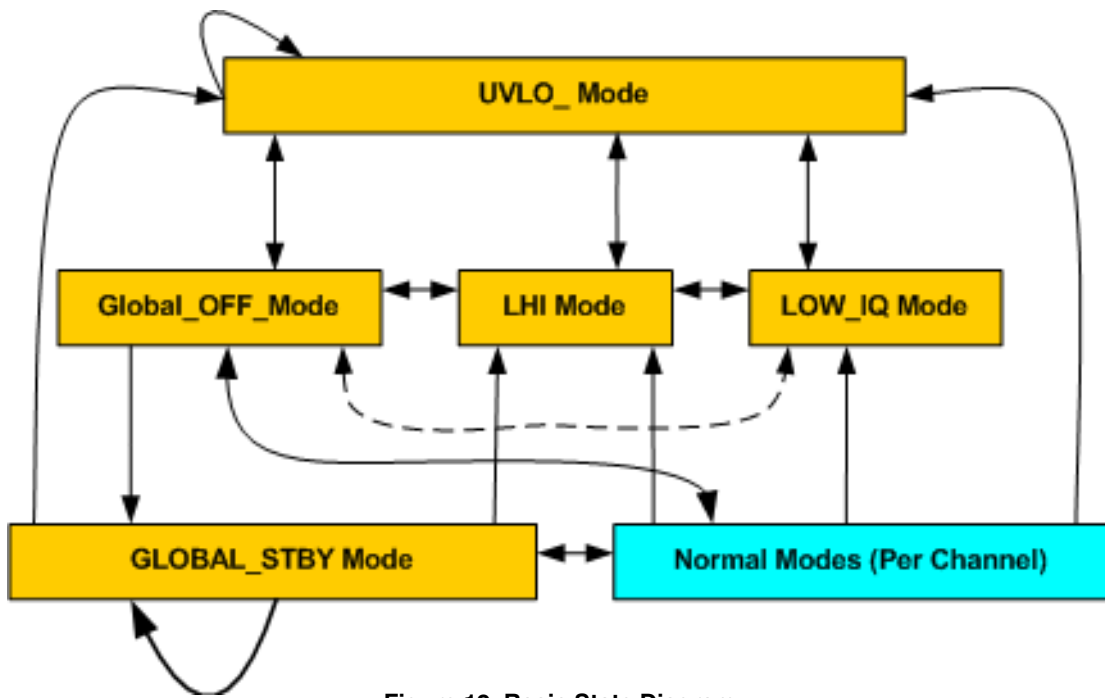


Figure 19. Basic State Diagram

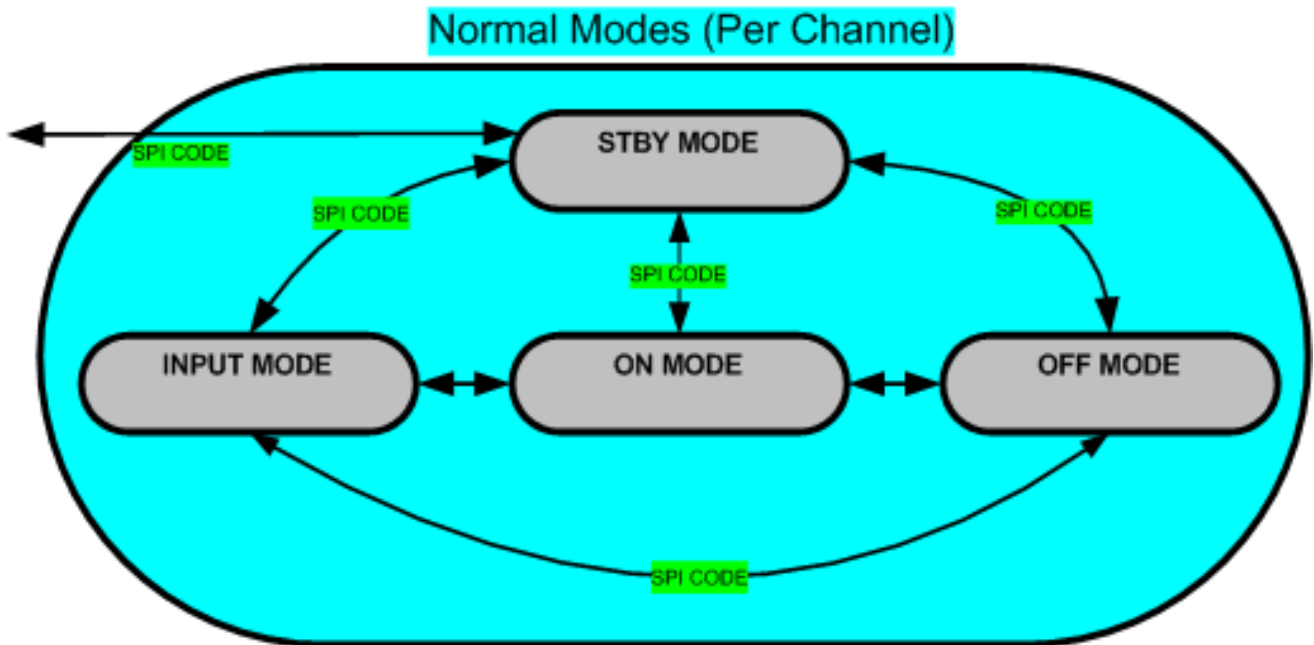


Figure 20. Normal Operation State Diagram

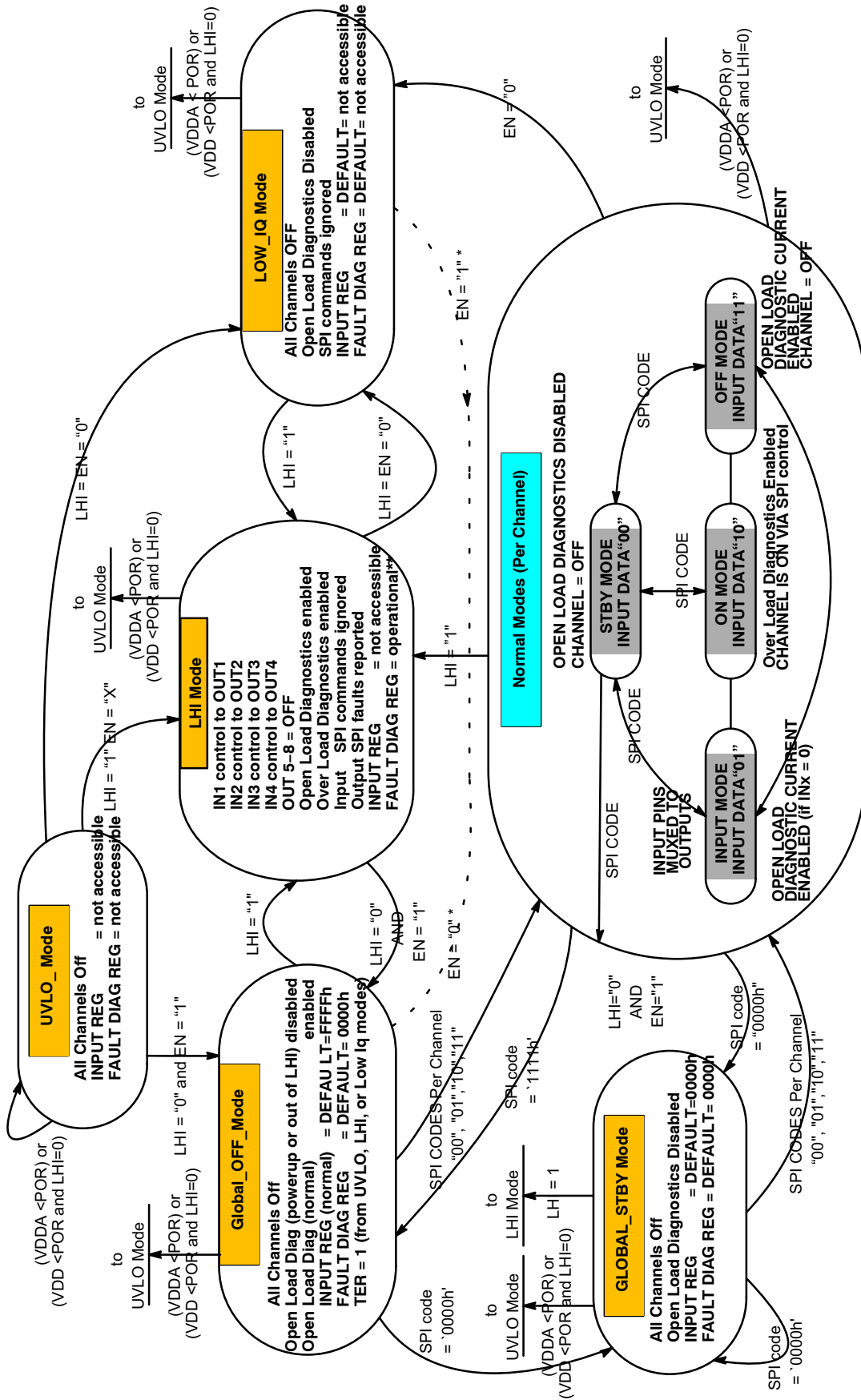


Figure 21. Detailed State Diagram

Limp Home and PWM operation (INx control)

Pulse Width Modulation techniques are allowed utilizing the parallel inputs (INx).

Output pins (OUTx) are programmed for use in conjunction with the INx pins using the SPI command (**command 01**).

The LHI pin controls the operation of the INx pins.

LHI = Low and EN = High

With LHI=low, default pairs of outputs are controlled by the INx pins (via SPI programming).

IN1 controls channels OUT1 and OUT5.

IN2 controls channels OUT2 and OUT6.

IN3 controls channels OUT3 and OUT7.

IN4 controls channels OUT4 and OUT8.

Alternatively, any of the eight channels can be commanded off (e.g. if OUT5 is commanded off via a SPI command, only OUT1 will be controlled via IN1).

Output pins (OUTx) are programmed for use in conjunction with the INx pins using the SPI command (**command 01**).

It is important to note faults occurring during PWM operation (LHI = low) must be cleared via the SPI port.

LHI = High

To go into limp home mode, bring LHI=high, the corresponding outputs of IN1–IN4 will turn on or off, and OUT5–OUT8 will be forced off.

During Limp Home Mode, over load and over temperature sensing are functional, and are reported via the SPI port. But, since input SPI commands are ignored with LHI = high, driver turn-off (overload or over temperature) occurring when LHI=high can only be re-initiated by toggling LHI or through a POR of VDDA.

All registers are reset coming out of LHI mode. The device enters OFF mode (EN = 1) or Low Iq Mode (EN = 0) depending on the state of the EN pin. Open Load diagnostics are disabled in both cases.

UVLO (Under Voltage Lockout with LHI = High)

A breach of VDDA Power-On Reset thresholds will cause the outputs to turn off and enter the UVLO mode. In LHI mode (LHI = 1), VDD POR is ignored. If VDD is below the operation of SO drive capability, fault information is preserved and can be retrieved when SO drive capability is restored.

TER

A transmission error bit (TER) is set ("1") when exiting the Limp Home Mode into Global Off Mode.

See Frame Detection Transmission Error Section for operation details.

Enable Input (EN)

The EN input pin is a logic controlled input with a voltage threshold between 0.8 V and 2.0 V. The device powers up when EN goes from low to high, and exits Low Iq Mode (with LHI = 0 V) into global Off Mode. Device power up is also controlled via the Limp Home Input (LHI) as an OR'd condition. The EN input is a don't care when the LHI pin is driven from low to high. In this situation, the device enters Limp Home Mode.

Output Drive Clamping

Internal zener diodes (Z1 & Z2, Figure 22) help to protect the output drive transistors from the expected fly back energy generated from an inductive load turning off. Z1 provides the voltage setting of the clamp (along with V_{gs} of the output transistor and Z2) while Z2 isolates Z1 from normal turn-on activity.

The output clamp voltage is specified between 36 V and 44 V. This includes clamping operation during unpowered input supplies (VDD and VDDA). Device protection will be provided when the load is driven from an alternative driver source. This is an important feature when considering protecting for load dump with an un-powered IC.

NCV7240

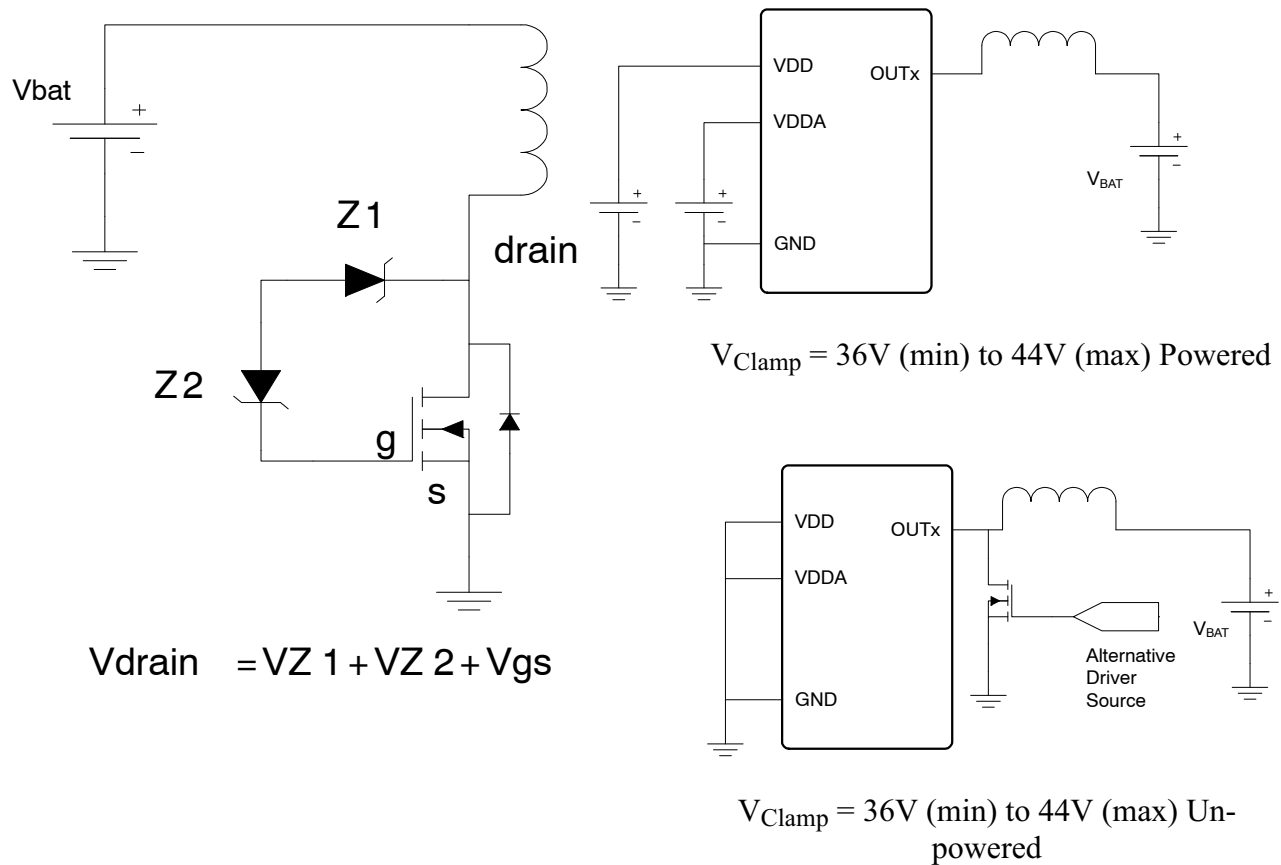


Figure 22. Output Clamp

Over Temperature / Thermal Shutdown

The NCV7240 incorporates eight individual thermal sensors located in proximity to each output driver. A channel is latched off upon the detection of an Over Temperature event. This allows operation of unaffected channels before, during, and after a channel detection of over temperature. The thermal shutdown detection threshold is typically 175°C with 25°C of hysteresis.

Open Load Detection

Open Load Detection is achieved for each output with the Open Load Detection Threshold Voltage reference voltage (Vol) and its' corresponding Open Load Diagnostic Sink Current (when the output driver (OUTx) is off). The output driver maintains its' functionality with and without the open bit set (i.e. it can turn on and off).

During normal operation, the open circuit impedance (Roc) is 0 Ω. This sets the voltage on OUTx to V_{BAT} volts. As long as V_{BAT} is above Vol no open circuit fault will be recognized. The voltage appearing on OUTx is a result of V_{BAT} and the voltage drop across Roc realized by the current flow created by Iol.

The NCV7240 voltage level trip points are referenced to ground. The threshold range is between 1.0 V and 2.5 V.

With a nominal battery voltage (V_{BAT}) of 14 V, the resultant worst case thresholds of detection are as follows.

$$\frac{(V_{\text{BAT}} - \text{OpenLoadDetectionThresholdVoltage})}{\text{OpenLoadDiagnosticSinkCurrent}} = \text{OpenLoad Impedance}$$

$$\frac{(14 \text{ V} - 2.5 \text{ V})}{100 \text{ } \mu\text{A}} = 115 \text{ k}\Omega$$

$$\frac{(14 \text{ V} - 1.0 \text{ V})}{20 \text{ } \mu\text{A}} = 650 \text{ k}\Omega$$

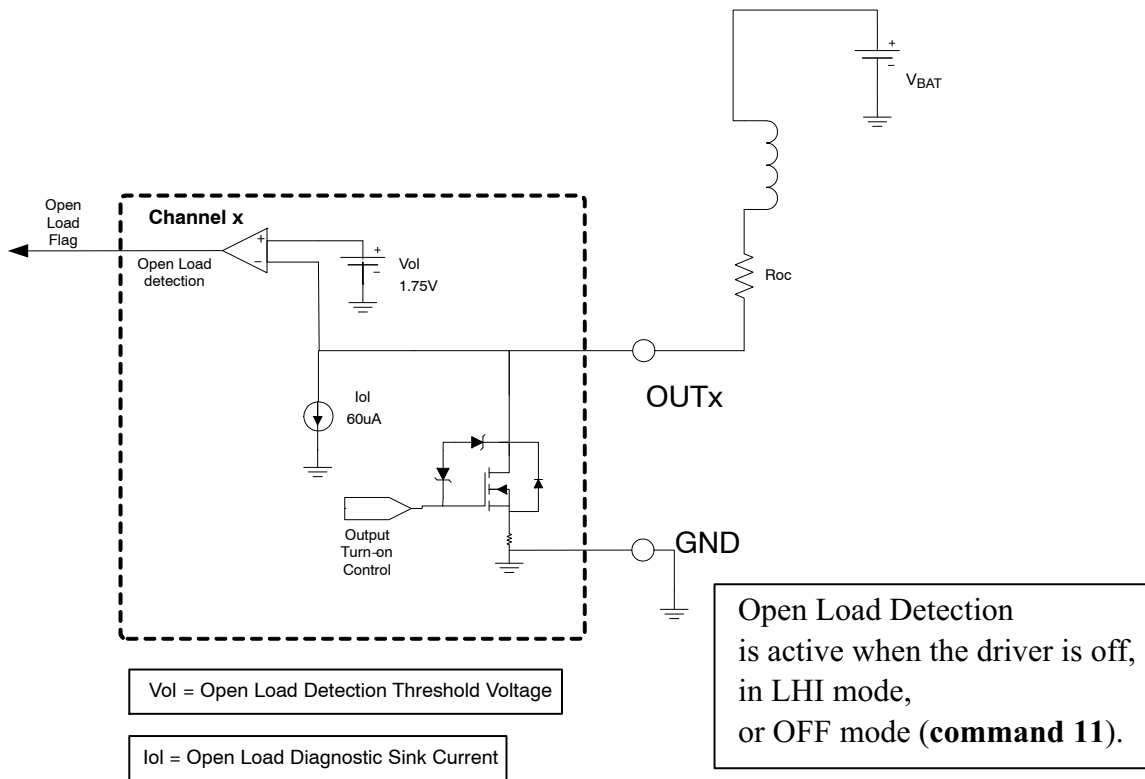


Figure 23. Open Load Detection

NOTE: Detection of an open load condition is limited by the Parallel Control Output turn-off time and the Open Load Detection Time specifications. The maximum allowable frequency of operation for PWM (pulse width modulation) using the INx inputs is calculated from the maximum limits of these specifications. INx must be low for longer than the sum of these maximum specifications (50 μsec and 200 μsec). Assuming a 50% duty cycle yields a maximum frequency of operation of $[1/(2*(50\mu + 200\mu))]=2$ kHz.

LED Loads

The NCV7240 features a power up feature for the Global OFF Mode enabling the part to power up in a mode without the open load diagnostic current enabled. This averts any unintended illumination of LED loads during power up.

Programming Features

The NCV7240 provides two registers.

1. Input Register. Input for IC mode state and output driver state control.
2. Output Register. Provides diagnostic information on the output driver condition.

Clearing the Fault Registers

Registers are reset with the following conditions.

1. Channel in Standby Mode.
2. Power-on reset of VDD.
3. Power-on reset of VDDA.
4. EN low.
5. Coming out of Limp Home Mode(LHI).

SPI-Interface

The device provides a 16 bit SPI-interface for output drive control and fault reporting. Data is imported into the NCV7240 through the SI (serial input) pin. Data is exported out of the NCV7240 through the SO (serial output) pin.

The input-frame (SI) (2 bits / channel) is used to command the output stages.

The response frame (SO) provides channel-specific (2 bits / channel) status information fault reporting.

Words should be composed of 16 bits MSB (most significant bit) transmitted first.

Frame Detection Transmission Error (TER)

The NCV7240 detects the number of bits transmitted after CSB goes low. Bit counts not a multiple of 8 (16 bit minimum) are reported as a fault on the TER bit. The transmission error information (TER) is available on SO after CSB goes low until the first rising SCLK edge. Reference the Serial Peripheral Interface diagram (Figure 27).

In addition to unqualified bit counts setting TER = 1, the bit will also be set by

1. Coming out of UVLO.
2. Transitioning from Limp Home Mode to Global Off Mode.
3. Transitioning from Low Iq Mode to Global Off Mode.

The TER bit is cleared by sending a valid SPI command.

The TER bit is multiplexed with the SPI SO data and OR'd with the SI input (Figure 24) to allow for reporting in a serial daisy chain configuration. A TER error bit as a "1" automatically propagates through the serial daisy chain circuitry from the SO output of one device to the SI input of the next. This is shown in Figures 25 and 26 first as the daisy chained devices connected with no Transmission Error (Figure 25) and subsequently with a Transmission Error in device 1 propagating through to device 2 (Figure 26).

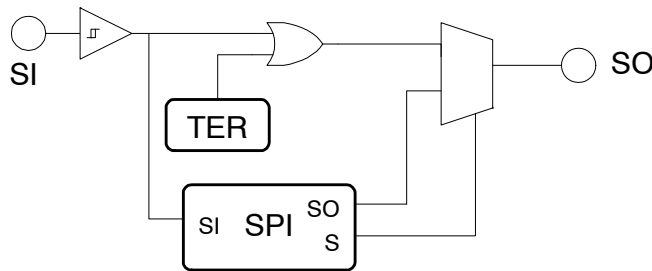


Figure 24. TER SPI Link

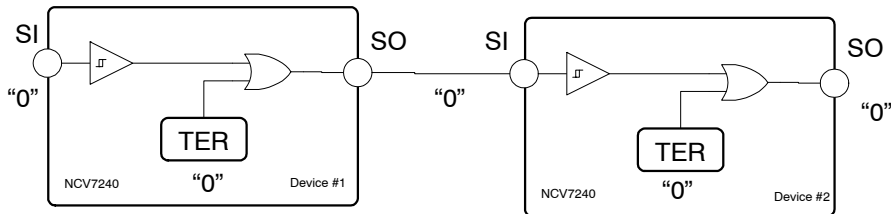


Figure 25. TER (no error)

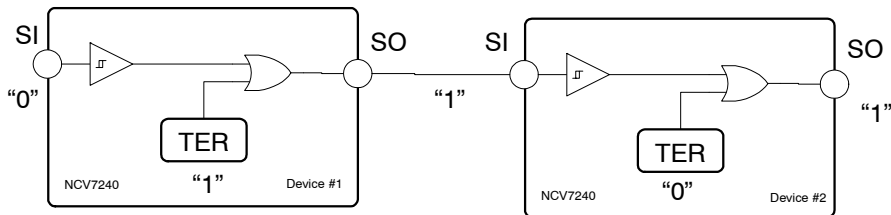


Figure 26. TER Error Propagation

NOTE: TER is valid from CSB going low until the 1st low-to-high transition of SCLK to allow for propagation of the SI signal. Reference Figure 27.
For proper TER status retrieval, SI should be in a low state.

TER Information Retrieval

TER information retrieval is as simple as bringing CSB high-to-low. No clock signals are required.

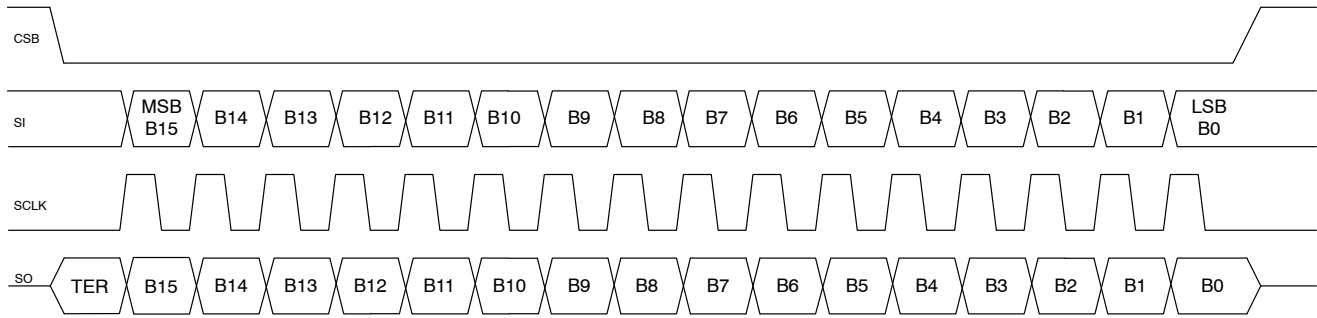


Figure 27. Serial Peripheral Interface

The timing diagram highlighted in Figure 27 shows the SPI interface communication.

Note:

1. The MSB (most significant bit) is the first transmitted bit.
2. Data is sampled from SI on the falling edge of SCLK
3. Data is shifted out from SO on the rising edge of SCLK
4. SCLK should be in a low state when CSB makes a transition.

Frame Detection

Input word integrity (SI) is evaluated by the use of a frame consistency check. The word frame length is compared to an $n * 8$ bit (where n is an integer) acceptable word length (16-bit minimum) before the data is latched into the input register. This guarantees the proper word length has been imported and allows for daisy chain operation applications with 8-bit SPI devices.

The frame length detector is enabled with the CSB falling edge and the SCLK rising edge.

Reference the valid SPI frame shown below. (Figure 27)

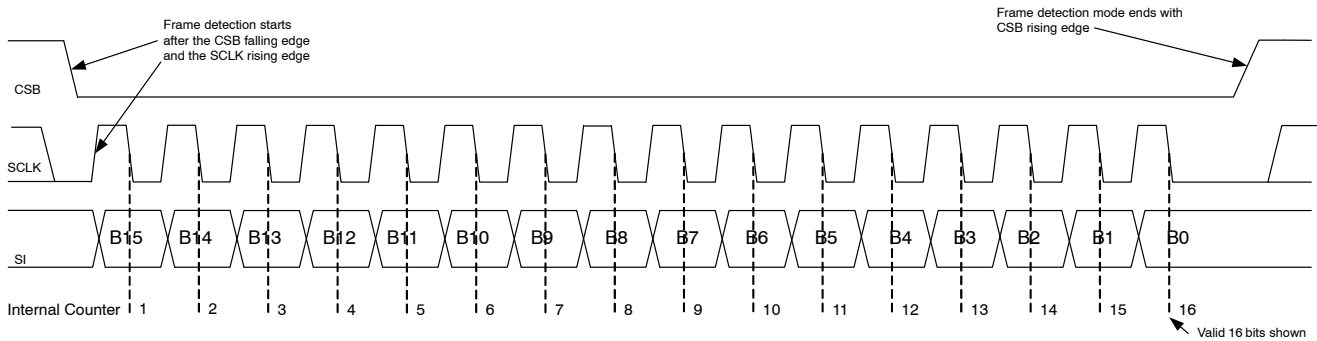


Figure 28. Frame Detection

DAISY CHAIN SETUP

NCV7240

Serial Connection

Daisy chain setups are possible with the NCV7240. The serial setup shown in Figure 29 highlights the NCV7240 along with any 16 bit device using a similar SPI protocol. Particular attention should be focused on the fact that the first 16 bits which are clocked out of the SO pin when the CSB pin transitions from a high to a low will be the Diagnostic Output Data from the Fault Output Register. These are the bits representing the status of the IC. Additional programming bits should be clocked in which follow the Diagnostic Output bits. The timing diagram shows a typical transfer of data from the microprocessor to the SPI connected IC's.

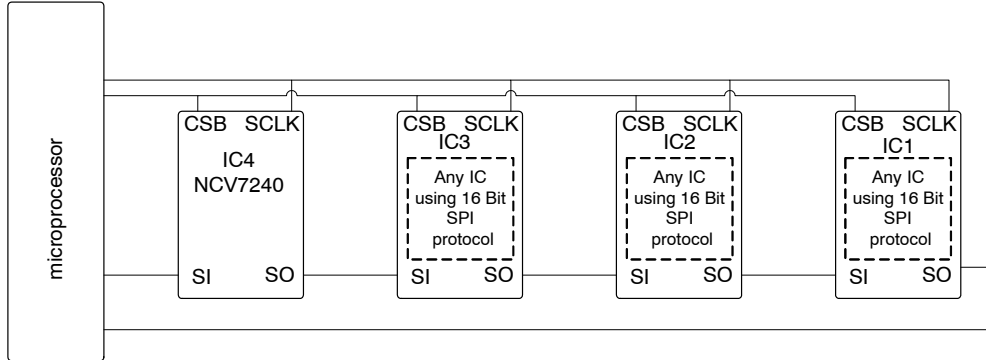


Figure 29. Serial Daisy Chain

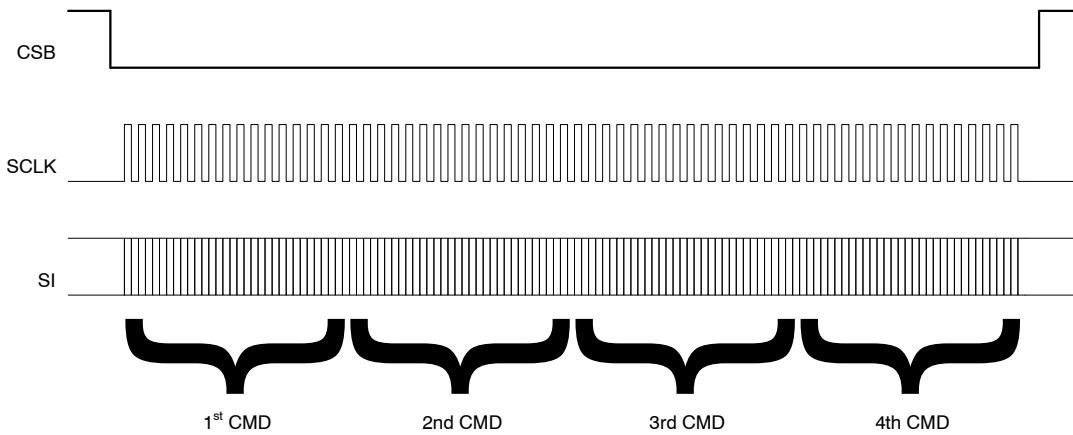


Figure 30. Serial Daisy Chain Timing Diagram

Table 2. SERIAL DAISY CHAIN DATA PATTERN

	CLK = 16 bits	CLK = 32 bits	CLK = 48 bits	CLK = 64 bits
IC4	1st CMD	2nd CMD	3rd CMD	4th CMD
IC3	IC4 DIAG	1st CMD	2nd CMD	3rd CMD
IC2	IC3 DIAG	IC4 DIAG	1st CMD	2nd CMD
IC1	IC2 DIAG	IC3 DIAG	IC4 DIAG	1st CMD
micro	IC1 DIAG	IC2 DIAG	IC3 DIAG	IC4 DIAG

Table 2 refers to the transition of data over time of the Serial Daisy Chain setup of Figure 29 as word bits are shifted through the system. 64 bits are needed for complete transport of data in the example system. Each column of the table displays the status after transmittal of each word (in 16 bit increments) and the location of each word packet along the way.

8-bit Devices

The NCV7240 is also compatible with 8 bit devices due to the features of the frame detection circuitry. The internal bit counter of the NCV7240 starts counting clock pulses when CSB goes low. The 1st valid word consists of 16 bits and each subsequent word must be comprised of just 8-bits (reference the Frame Detection Section).

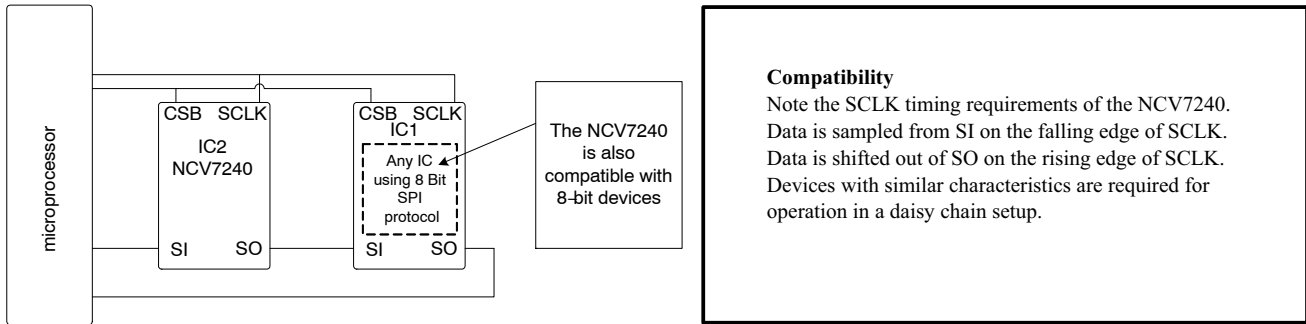


Figure 31. Serial Daisy Chain with 8-bit Devices

Parallel Connection

A more efficient way (time focused) to control multiple SPI compatible devices is to connect them in a parallel fashion and allow each device to be controlled in a multiplex mode. Figure 32 shows a typical connection between the microprocessor or microcontroller and multiple SPI compatible devices. In a serial daisy chain configuration, the programming information for the last device in the serial string must first pass through all the previous devices. The parallel control setup eliminates that requirement, but at the cost of additional control pins from the microprocessor for each individual CSB (chip select bar) pin for each controllable device. Serial data is only recognized by the device that is activated through its' respective CSB pin.

Figure 33 shows the waveforms for typical operation when addressing IC1.

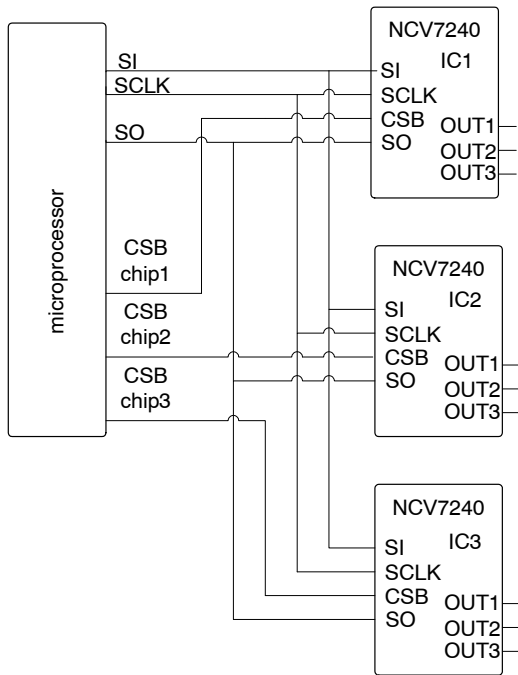


Figure 32. Parallel Connection

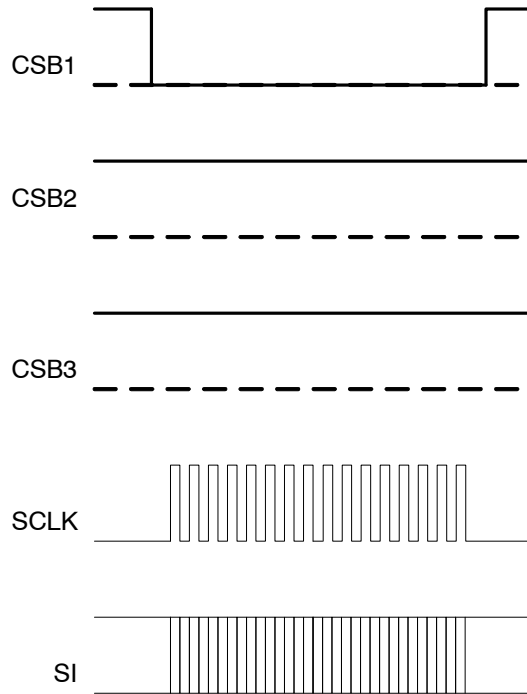


Figure 33. Parallel Connection Timing Diagram

Stepper Motor Operation

The NCV7240 device is capable of driving stepper motors. Each stepper motor requires 4 low-side drive outputs. Consequently, each NCV7240 device is capable of driving two stepper motors. Figure 34 below illustrates a Unipolar stepper motor setup. For proper operation, the code listed in Table 3 should be used (and repeated) for one way operation (clockwise). For reverse direction, simply reverse the code and repeat (counterclockwise). Outputs 1–4 are utilized for one stepper usage. For a 2nd stepper motor, repeat the code used for outputs 1–4 to outputs 5–8. During operation waveforms similar to Figure 35 can be expected on the OUTx pins.

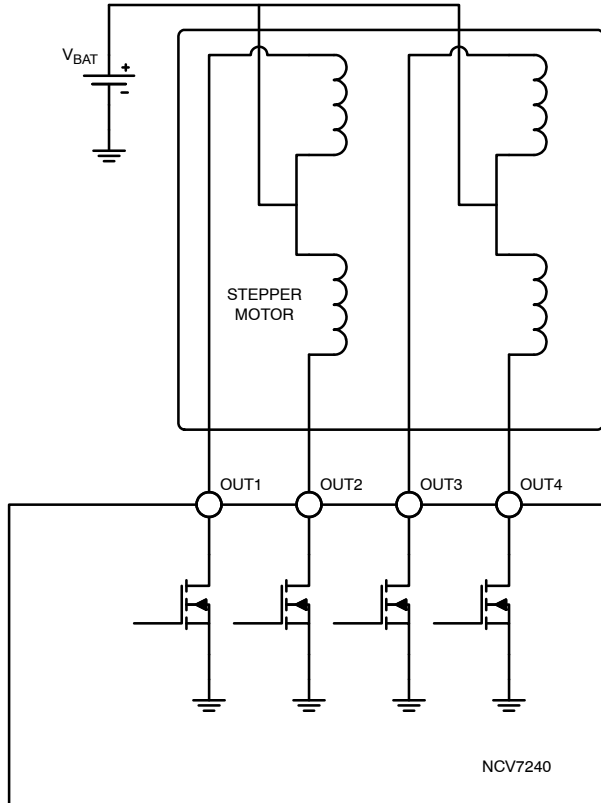


Figure 34. Stepper Motor Operation Setup

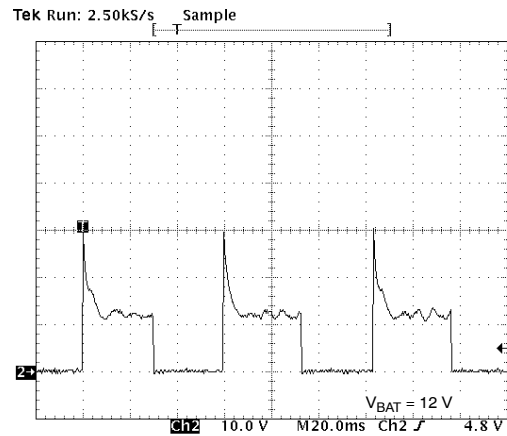


Figure 35. Typical Stepper Motor Waveform (Unipolar Portescap 35L048L32U)

Table 3. NCV7240 STEPPER MOTOR CODE

OUT 4	OUT 3	OUT 2	OUT 1
OFF	ON	OFF	ON
ON	OFF	OFF	ON
ON	OFF	ON	OFF
OFF	ON	ON	OFF

{Repeat}

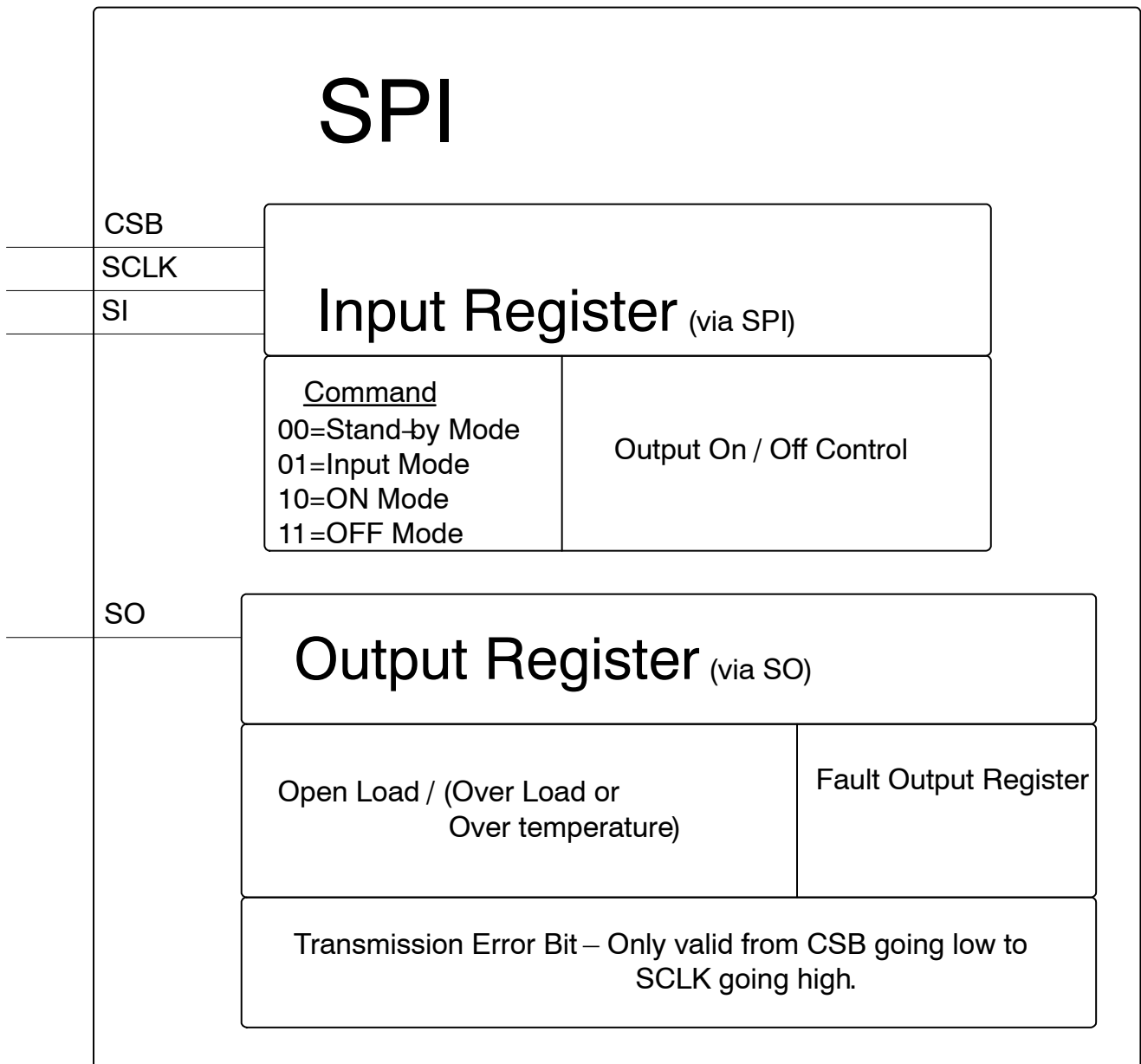


Figure 36. SPI Register Overview

Figure 36 displays the functions controlled and reported via the SPI port. The input register controls the input source (parallel or SPI) and the SPI input data. The output register transmits the output fault bits and the frame detection integrity.

NCV7240

SI SPI Input Data (16-bit serial structure of input word)

The 16-bit data received (SI) is decoded into instructions for each channel per the table below.

After a power-on reset, all register bits are set to a 1.

Table 4. SPI INPUT DATA

Channel 8		Channel 7		Channel 6		Channel 5		Channel 4		Channel 3		Channel 2		Channel 1	
MSB														LSB	
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

INPUT DATA REGISTER

Field	Bits	Description		
channel x (x = 1–8)	15, 14 13, 12 11, 10 9, 8 7, 6 5, 4 3, 2 1, 0	Command		
		00	Channel Stand-by Mode Fast channel turn off Fault Registers reset	
			Diagnostic Current	Disabled
		01	Input Mode Channel Input directed to INx. (reference PWM operation section).	
			Diagnostic Current	Enabled in OFF State.
		10	ON Mode Channel turned on.	
			Diagnostic Current	Disabled
		11	OFF Mode Channel turned off.	
			Diagnostic Current	Enabled (Disabled after POR)*

*For proper LED load operation.

SO (fault diagnostic retrieval)

Output fault diagnostics from the output fault diagnostic register are shifted out on any 16 bit word clocked into Serial Input (SI).

Only output fault diagnostics and frame detection errors are available through the serial output (SO).

Table 5. SPI OUTPUT DATA

TER	OL8	D8	OL7	D7	OL6	D6	OL5	D5	OL4	D4	OL3	D3	OL2	D2	OL1	D1
-----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----	-----	----

FAULT DIAGNOSTIC REGISTER

Field	Bits	Description
TER	CSB high-to-low prior to 1st SCLK low-to-high	Transmission Error. 0 Successful transmission in previous communication. 1 Frame detection error in previous transmission or exiting Limp Home Mode or exiting UVLO Mode.
OLn (n = 1 – 8)	1, 3, 5, 7, 9, 11, 13, 15	Open Load 0 Normal Operation 1 Fault detected
Dn (n = 1 – 8)	0, 2, 4, 6, 8, 10, 12, 14	Over Load or Over Temperature 0 Normal Operation 1 Fault detected

NCV7240

Table 6. FAULT CONDITIONS

Output Fault Condition	Fault Memory	Miscellaneous
Open Load	Latched	Detected in Driver Off State (1.75 V [Typ] threshold) when detection is enabled. Reported in Output Fault Diagnostics Register until cleared via the SPI port. Output will maintain turn-on capability.
Short to Ground	Latched	Detected as part of the Open Load circuitry described above.
Short to V _{bat}	N/A	Protected via Over Load and Over Temperature functions.
Over Load	Latched	Detected in Driver On State 0.6 A [min], 1.3 A [max]. A latched off condition must be cleared via the SPI port before it can be turned on.
Over Temperature	Latched	Detected in IC On State (T _J = 175°C [Typ]) A latched off condition must be cleared via the SPI port before it can be turned on.

DEVICE ORDERING INFORMATION

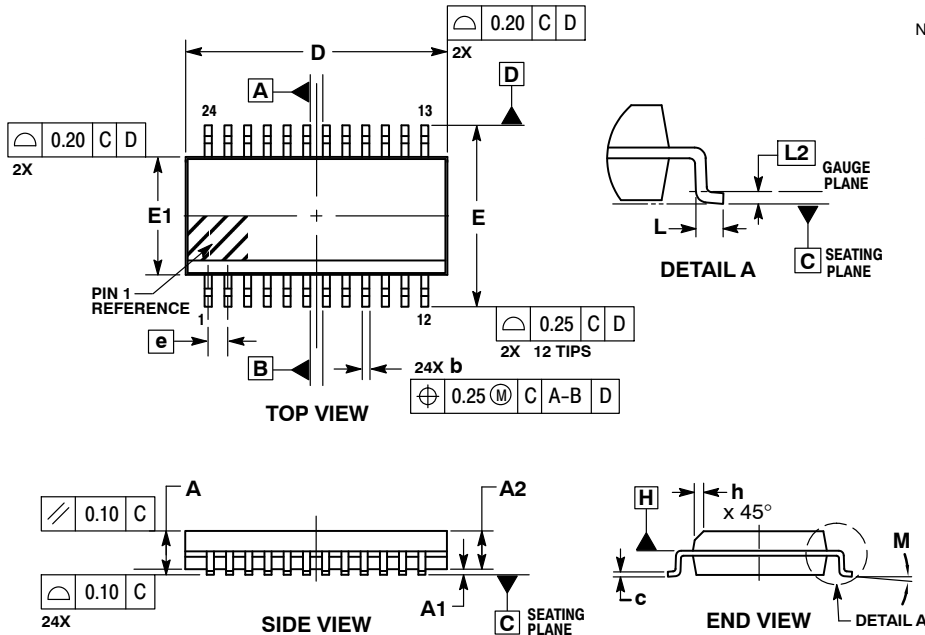
Part Number	Package Type	Shipping [†]
NCV7240DPR2G	SSOP-24 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCV7240

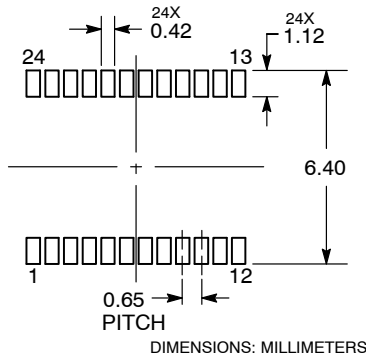
PACKAGE DIMENSIONS

SSOP24 NB
CASE 565AL
ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
 4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.

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