NCS5651

Product Preview

2 Amp PLC Line Driver

ON Semiconductor®

http://onsemi.com

1 20

QFN20
CASE 485E

MARKING DIAGRAM

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

Description

The NCS5651 is a high efficiency, Class A/B, low distortion power line driver. It is optimized to accept a signal from a Power Line Carrier modem. The device consists of two Operational Amplifiers (opamps).

The output opamp is designed to drive up to 2 A peak into an isolation transformer or simple coil coupling to the mains. At an output current of 1.5 A, the output voltage is guaranteed to swing within 1 V or less of either rail giving the user improved SNR.

In addition to the output amplifier, a small−signal opamp is provided which can be configured as a unity gain follower buffer or can provide the first stage of a 4−pole low pass filter.

The NCS5651 offers a current limit, programmable with a single resistor, R−Limit, together with a current limit flag. The device provides two independent thermal flags with hysteresis: a thermal warning flag to let the user know the internal junction temperature has reached a user programmable thermal warning threshold and a thermal error flag that indicates the internal junction temperature has exceeded 150°C.

The NCS5651 has a power supply voltage range of 6−12 V. It can be shut down, leaving the outputs highly−impedant. The NCS5651 comes in a 20−lead QFN package ($4 \times 4 \times 1$ mm^3) with an exposed thermal pad for enhanced thermal reliability.

Features

- Rail−to−Rail: Drop of Only ±1 V with I_{out} = 1.5 A
- V_{BB} Supply Voltage: 6−12 V
- Flexible 4th−Order Filtering
- Current−Limit Set with One Resistor
- Diagnostic Flags Level Shifted to V_{CC} to Simplify Interface with External MCU
  - Thermal Warning Flag with Flexible Threshold Setting
  - Thermal Error flag and Shutdown
  - Overcurrent Flag
- Enable/Shutdown Control
- Extended Junction Temperature Range: −40°C to +125°C
- Small Package: 20−pin $4 \times 4 \times 1$ mm^3 NQFP with Exposed Thermal Pad
- Optimized for Operation in the Cenelec A to D Frequency Band
- This is a Pb−Free Device

Typical Applications

- Power Line Communication Driver in AMM and AMR Metering Systems
- Valve, Actuator, and Motor Driver
- Audio

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ORDERING INFORMATION

Device	Package	Shipping
NCS5651MNTXG	QFN20 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part or orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

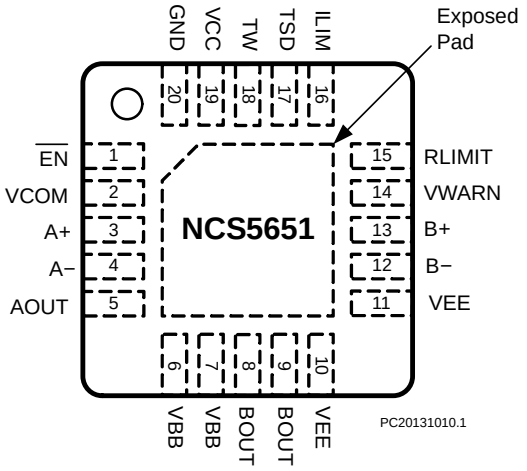


Figure 1. Pin Out NCS5651 in 20−pin NQFP (top view)

Table 1. NCS5651 PINOUT

Signal Name	Type	Pin #	Pin Description
ENB	Input	1	Enable input (active low)
VCOM	Power	2	Virtual Common Voltage = (VCC − VEE)/2 (Note 1)
A+	Input	3	Non inverting input of Op Amp A
A−	Input	4	Inverting input of Op Amp A
AOUT	Output	5	Output of Op Amp A
VBB	Power	6, 7	Positive Power Supply Amplifiers
BOUT	Output	8, 9	Output of Op Amp B
VEE	Power	10, 11	Negative Power Supply Amplifiers
B−	Input	12	Inverting input of Op Amp B
B+	Input	13	Non inverting input of Op Amp B
VWARN	Input	14	Thermal Warning Temp Set
RLIMIT	Input	15	Output B Current Limit Set Resistor
ILIM	Output	16	Current Limit Flag
TSD	Output	17	Thermal Shutdown Flag
TW	Output	18	Thermal Warning Flag
VCC	Power	19	Logic supply
GND	Power	20	Logic ground
EXP	Power	−	Exposed pad. To be connected to VEE potential

1. The principal purpose of pin 2 is to facilitate the implementation of the 4th−order low pass filter when operating on single−sided supply by providing a virtual common at mid−supply. When operating on dual balanced supplies, Pin 2 must be left floating and the external common of the dual supplies should be used for the filter implementation

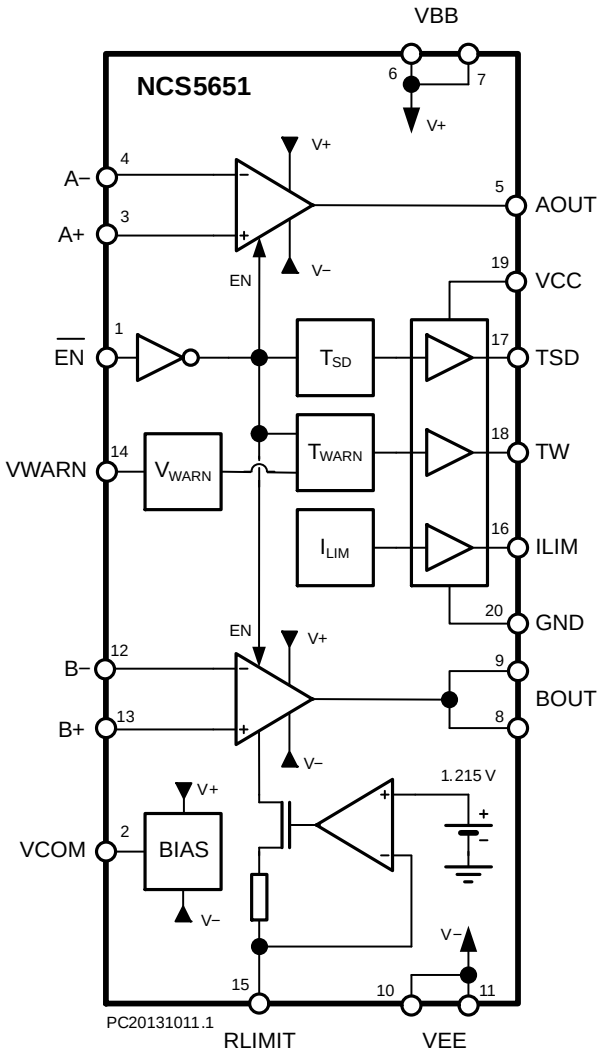


Figure 2. NCS5651 Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
T_J	Junction temperature	−40	+160	°C
T_{STG}	Storage temperature	−65	+165	°C
V_S	Supply voltage (V_{BB} to V_{EE})	−0.3	13.2	V
V_{ICR}	Common Mode Voltage Range input	V_{EE} − 0.3	V_{BB} + 0.3; < V_S	V
V_{CCM}	Logic Supply Voltage		5.5	V
V_I	Logic Input Voltage	GND − 0.3	V_{CC} + 0.3; < V_{CCM}	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. THERMAL CHARACTERISTICS $R_{\theta JA}$ obtained with 2S2P test boards according to JEDEC JESD51 standard.

Symbol	Rating	Typical Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Air (Note 3)	38	°C/W

Table 4. RECOMMENDED OPERATING CONDITIONS (Note 2)

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Temperature	−40	+125	°C
V_S	Supply voltage (V_{BB} to V_{EE})	6	12	V
V_{CC}	Logic Supply voltage)	3.0	5.0	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
2. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.

Table 5. ELECTRICAL CHARACTERISTICS V_{BB} = 12 V; −40°C ≤ T_J ≤ +125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OPERATIONAL AMPLIFIER A						
V_{OS}	Input offset voltage			± 3	± 10	mV
PSRR	Power supply rejection ratio			25	150	μV/V
I_B	Input bias current (Note 3)				1	nA
e_n	Input voltage noise density	f = 1 kHz; V_{IN} = GND; BW = 131 kHz		250		nV/√Hz
V_{CM}	Common Mode voltage range		V_{EE} − 0.1		V_{BB} − 3	V
CMRR	Common Mode Rejection Ration	V_{EE} − 0.1 ≤ V_{CM} ≤ V_{CC} − 3	70	85		dB
Zi_{DIF}	Differential Input Impedance			0.2 | 1.5		GΩ | pF
Zi_{CM}	Common Mode Input Impedance			0.2 | 3		GΩ | pF
A_{OL}	Open Loop Gain (Note 3)	R_L = 500 Ω	80	100		dB
GBW	Gain Bandwidth Product			80		MHz
FPBW	Full Power Bandwidth (Note 3)	CLG = +5; V_{OUT} = 11 V_{PP}		1.5		MHz
SR	Slew Rate			60		V/μs
THD+N	Total Harmonic Distortion + Noise	CLG = +1; R_L = 500 Ω; V_O = 8 V_{PP}; f = 1 kHz; C_{in} = 220 μF; C_{out} = 330 μF		0.015		%
		CLG = +1; R_L = 50 Ω; V_O = 8 V_{PP}; f = 1 kHz; C_{in} = 220 μF; C_{out} = 330 μF		0.023		%
V_{OH}	Output swing from Positive Rail	R_L = 500 Ω to Mid−Supply		0.3	1	V
V_{OL}	Output swing from Negative Rail			0.3	1	V
I_{SC}	Short−Circuit Current			280		mA
Z_O	Output Impedance	CLG = 4; f = 100 kHz		0.25		Ω
C_{LOAD}	Capacitive Load Drive			100		pF
OPERATIONAL AMPLIFIER B						
V_{OS}	Input offset voltage			± 3	± 10	mV
PSRR	Offset versus power supply			25	150	μV/V
I_B	Input bias current (Note 3)				1	nA
e_n	Input voltage noise density	f = 1 kHz; V_{IN} = GND; BW = 131 kHz		125		nV/√Hz
V_{CM}	Common Mode voltage range		V_{EE} − 0.1		V_{BB} − 3	V
CMRR	Common Mode Rejection Ratio	V_{EE} − 0.1 ≤ V_{CM} ≤V_{BB} − 3	70	85		dB
Zi_{DIF}	Differential Input Impedance			0.2 | 11		GΩ | pF
Zi_{CM}	Common Mode Input Impedance			0.2 | 22		GΩ | pF
A_{OL}	Open Loop Gain (Note 3)	R_L = 5 Ω	80	100		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Guaranteed by characterization or design
4. CLG = Closed Loop Gain

Table 5. ELECTRICAL CHARACTERISTICS V_{BB} = 12 V; −40°C ≤ T_J ≤ +125°C

Symbol	Parameter	Condition	Min	Typ	Max	Unit
OPERATIONAL AMPLIFIER B						
GBW	Gain Bandwidth Product			60		MHz
FPBW	Full Power Bandwidth (Note 3)	CLG = +5; V_{OUT} = 11 V_{PP}	200	400		kHz
SR	Slew Rate			70		V/μs
THD+N	Total Harmonic Distortion + Noise	CLG = +1; R_L = 50 Ω; V_O = 8 V_{PP}; f = 1 kHz		0.015		%
		CLG = +1; R_L = 50 Ω; V_O = 8 V_{PP}; f = 100 kHz		0.023		%
V_{OH}	Output swing from Positive Rail	Sourcing resp. Sinking I_{OUT} = 1.5 A		0.7	1	V
V_{OL}	Output swing from Negative Rail			0.4	1	V
I_{SC}	Short−Circuit Current			280		mA
Z_O	Output Impedance	CLG = 1; f = 100 kHz; ENB = 0		0.065		Ω
Z_O	Output Impedance	ENB = 1		12		MΩ
C_{LOAD}	Capacitive Load Drive			500		nF
BOTH AMPLIFIERS COMBINED						
$T_{J,SD}$	Junction temperature shutdown treshold		+150	+160		°C
$T_{J,SD,R}$	Junction temperature shutdown recovery treshold			+135		°C
T_W	Thermal warning tolerance (Note 4)	T_W is determined by the ratio of 2 resistors		± 10		°C
I_{LIM}	Current Limit Tolerance	I_{LIM} is determined by a single resistor		± 50		mA
V_S	Operating Voltage Range			6 .. 12	13.2	V
I_{QE}	Quiescent Current, enabled	ENB = 0		20	40	mA
I_{QD}	Quiescent Current, disabled	ENB = 1		120	150	μA
V_{COM}	Common mode voltage	Internal resistive divider	5.8	6.0	6.2	V
LOGIC						
V_{CC}	Logic Supply		3.0	3.3	5.5	V
V_{IH}	ENB input level high		GND + 2		V_{CC}	V
V_{IL}	ENB input level low		GND		GND + 0.8	V
I_{IH}	ENB input current high			10		μA
I_{IL}	ENB input current low			0.1		μA
V_{OH}	Flag Output High level		GND + 2			V
V_{OL}	Flag Output Low level				GND + 0.8	V
t_{sd}	Output Shutdown time			60		ns
t_{en}	Output Enable time			5	10	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Guaranteed by characterization or design
4. CLG = Closed Loop Gain

TYPICAL CHARACTERISTICS

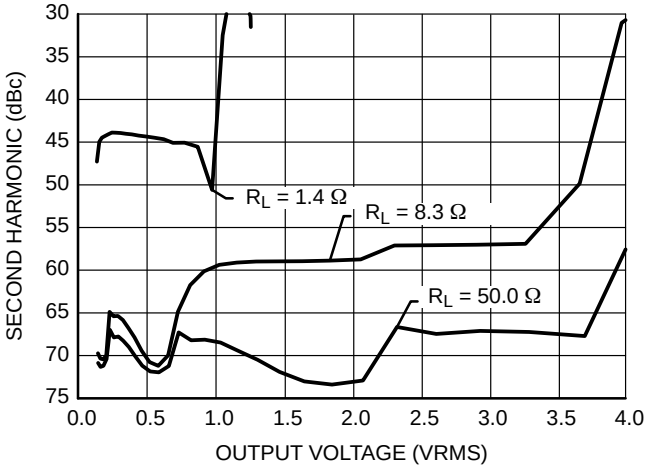


Figure 3. Second Harmonic Distortion of the Output opamp vs. Output Amplitude, for *f* = 100 kHz and R_L (top to bottom) = 1.4 Ω, 8.3 Ω, 50 Ω.

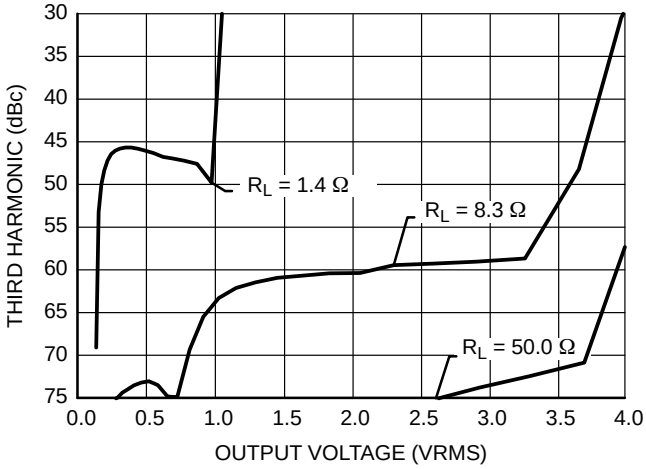


Figure 4. Third Harmonic Distortion of the Output opamp vs. Output Amplitude, for *f* = 100 kHz and R_L (top to bottom) = 1.4 Ω, 8.3 Ω, 50 Ω.

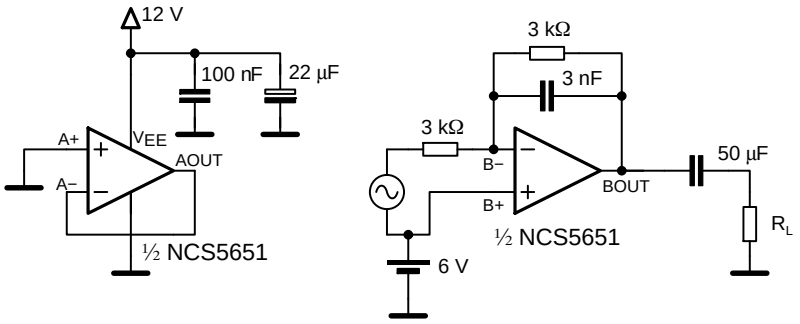


Figure 5. Test Circuit for Figures 3 and 4

TYPICAL APPLICATION

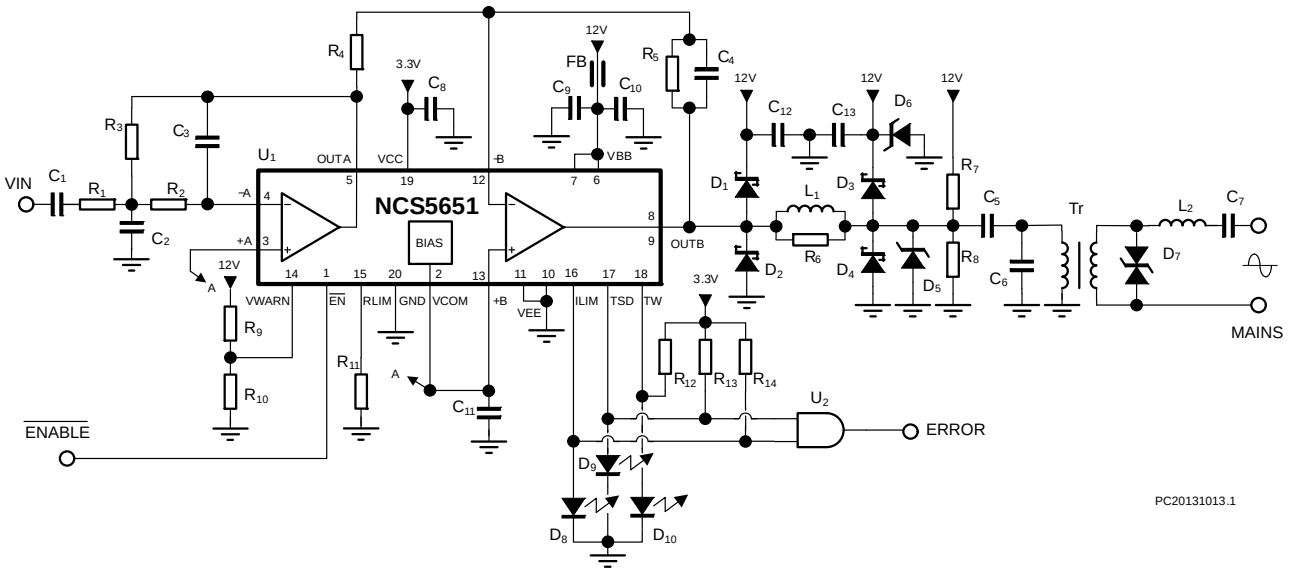


Figure 6. Typical Application Schematic for PLC modem

Table 6. BILL OF MATERIALS

Reference Designator	Value (typical)	Note	Manufacturer	Part Number
U_1		Power Operational Amplifier	ON Semiconductor	NCS5651
U_2		AND gate	ON Semiconductor	MC74VHC1G32
D_1, D_2		Schottky Power Diode	ON Semiconductor	MBRA140
D_3, D_4		Schottky Power Diode	ON Semiconductor	MBRA340
D_5		Zener Transient Voltage suppressor	ON Semiconductor	1SMA11ATG3
D_6		Zener Transient Voltage suppressor	ON Semiconductor	1SMA12ATG3
D_7		Zener Transient Voltage suppressor	ON Semiconductor	P6SMB11CAT3G
D_8, D_9, D_{10}		Low power indication LED		
R_x	TBD			
C_x	TBD			
L_1	3,3 μH	Saturation current ≥ 2 A		
L_2	10−27 μH	Depending on transformer and communication carrier frequency		
FB	600Z	Ferrite bead, ≥ 1.5 A current rating		
Tr		Coupling transformer		

APPLICATION INFORMATION

Exposed Thermal Pad

The NCS5651 is capable of delivering 1.5 A, into a reactive load. Output signal swing should be kept as high as possible to minimize internal heat generation to keep the internal junction temperature as low as possible. The NCS5651 can swing to within 1 V of either rail without adding distortion. An exposed thermal pad is provided on the bottom of the device to facilitate heat dissipation. Application Note AND8402/D provides considerable details for optimizing the soldering down of the exposed pad.

Multi−Feedback Filter (MFB)

CENELEC EN 50065−1 is a European standard for signaling on low−voltage electrical installations in the frequency range 3 kHz to 148. 5 kHz. More specifically Part 1 of that specification deals with frequency bands and electromagnetic disturbances introduced into the electrical mains. A practical solution to meet this requirement is to place a 4th−order filter between the output of the modem and the isolation transformer connected to the mains. In this datasheet a MFB filter topology is proposed to help meet the requirements of the CENELEC standard. Four (4) pole filters require two op amps for implementation. The NCS5651 has an input pre−amplifier and an output power amplifier. Therefore only passive components (R's and C's) need to be added. In addition the NCS5651 has a mid−supply virtual common at pin 2 (V_{com}) to facilitate implementation of the filter topology.

Figure 7 below shows the frequency response for each stage and the overall filter.

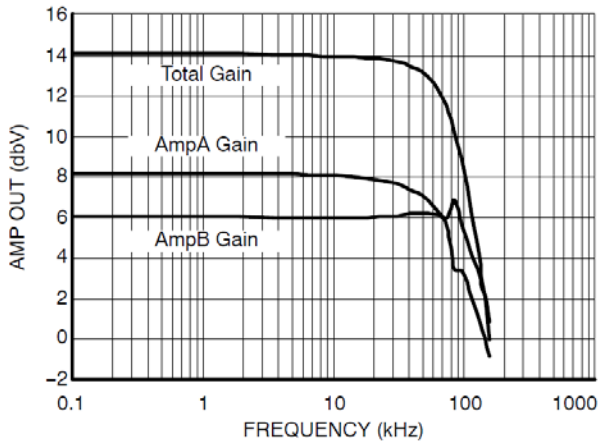


Figure 7. Amplifier Voltage versus Frequency

Decoupling

Optimal stability and noise rejection will be implemented with power−supply bypassing placed as physically close to the device as possible. A parallel combination of 10 μF and 10 nF is recommended for each sensitive point. For either single−supply operation or split supply operation, bypass should be placed directly across V_{BB} to V_{EE}. In addition add bypass from V_{CC} to GND (Figure 8).

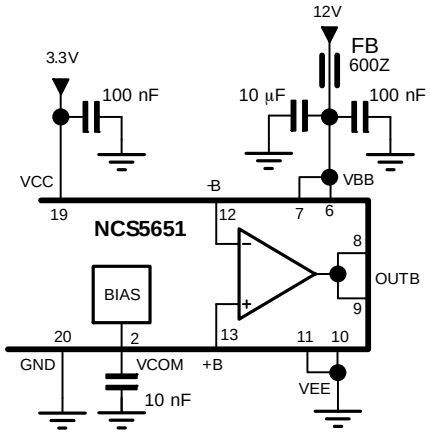


Figure 8. Decoupling Capacitors

Current Limit (R−Limit)

The 2 A output current of the NCS5651 can be programmed by the simple addition of a resistor (R_{LIM}) from pin 15 to V_{EE} (see Figure 6). If the load current tries to exceed the set current limit, the ILIM flag will go logic High signaling the user to take any necessary action. When the current output recovers, the ILIM flag will return to logic Low. The curve in Figure 7 is tolerance typically to ±50 mA. Unlike traditional power amplifiers the NCS5651 current limits functions both when sourcing and sinking current. To calculate the resistance required to program a desired current limit the following equation can be used:

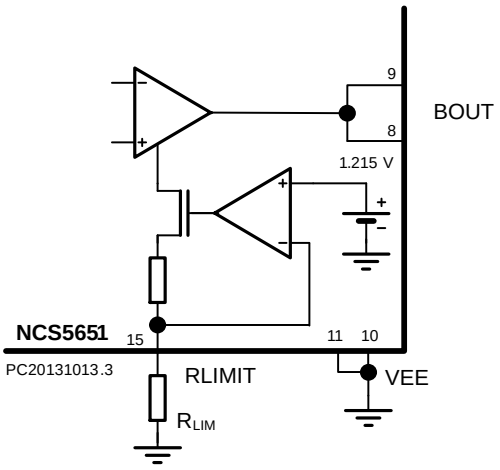


Figure 9. Programming the Current Limit

Figure 10 illustrates the required resistance to program the current limit.

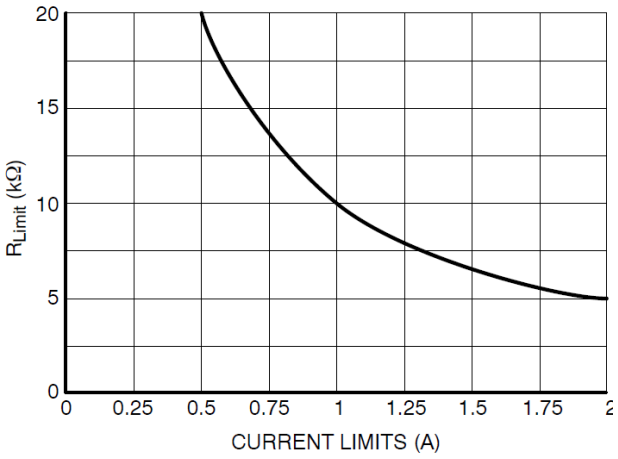


Figure 10. R_{LIM} in Function of the I_{LIM}

Thermal Shutdown and Thermal Warning Flag

In the event load conditions cause internal over−heating the amplifier will go into shutdown to prevent damage. Under these conditions pin 17 the TSD flag (Thermal Shut Down) will go logic High. Thermal shutdown takes place at an internal junction temperature of approximately 160°C; the amplifier will recover to the Enabled mode when the junction temperature cools back down to approximately 135°C.

The user has the option to avoid entering into the TSD mode by monitoring the junction temperature via the Thermal Warning feature.

Figure 11 shows how the user can select any junction temperature (Twarn) in the range 105°C to 145°C by applying the appropriate voltage to pin 14. A simple way to implement this feature is by setting the ratio of a voltage divider between VBB (pins 6,7) and VEE (the negative supply, pin 10 or 11). The voltage ratio required to program the thermal warning of the NCS5651 can be calculated using the following equation:

$$V_{TW} = 6.665 \times 10^{-3}\left(T_J\right) + 1.72 \qquad \text{(eq. 1)}$$

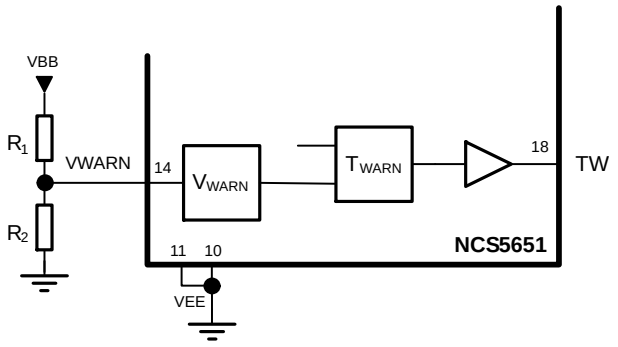


Figure 11. Setting the Thermal Warning Limit by Applying the Corresponding Threshold Voltage to Pin 14 (VWARN)

Figure 12 illustrates the linearity of the internal junction temperature to the required voltage on pin 14 (Twarn).

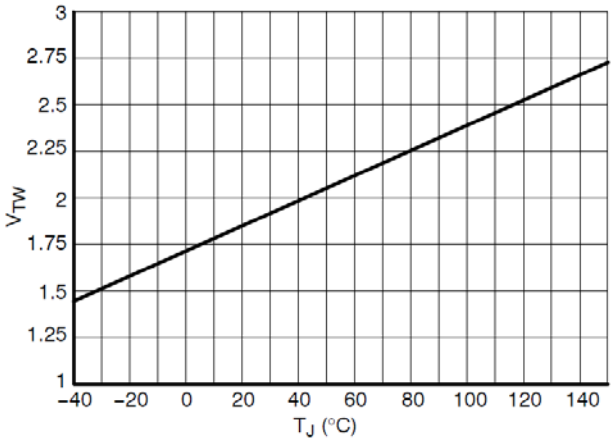


Figure 12. Thermal Warning Threshold in Function of Junction Temperature

Virtual Common (V_{com})

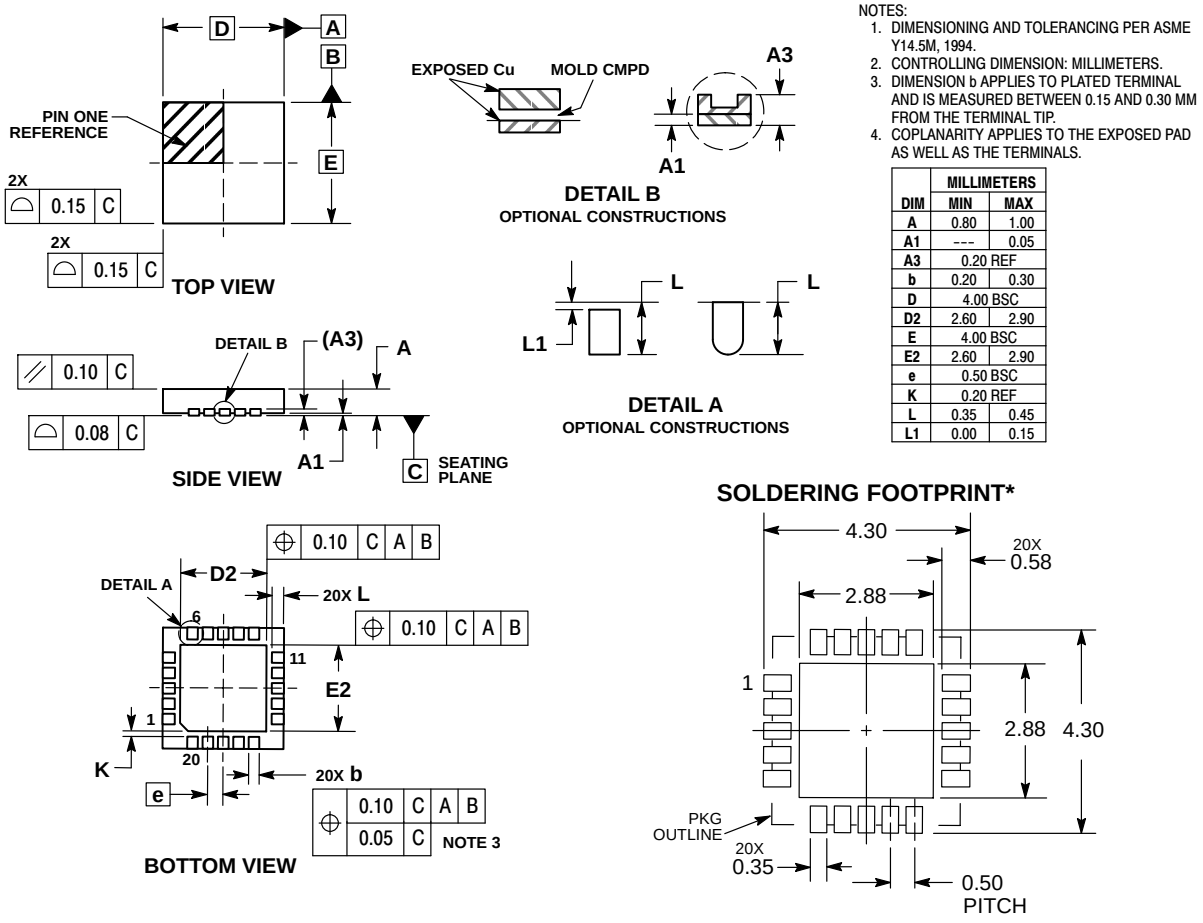
The principal purpose of V_{com} is to provide a convenient virtual common for implementing the 4th−order CENELEC filter when operating on single−sided power supply. When operating on balanced split supplies it is recommended to use the power supply common for the filter implementation and to leave V_{com} floating

Digital Power Supply GND−Reference and Translators

In many mixed signal applications analog GND and digital GND are not at the same potential. To minimize GND loop issues, the NCS5651 has a separate GND pin (pin 20) which should be used to reference the digital supply and the warning flags (pins 16, 17, and 18). In most applications this would be the same GND reference used for the PLC modem. Please note that at some point in the application digital GND and analog GND must be tied together.

PACKAGE DIMENSIONS

QFN20, 4x4, 0.5P
CASE 485E
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.20	0.30
D	4.00 BSC	
D2	2.60	2.90
E	4.00 BSC	
E2	2.60	2.90
e	0.50 BSC	
K	0.20 REF	
L	0.35	0.45
L1	0.00	0.15

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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