

BLC8G21LS-160AV

Power LDMOS transistor

Rev. 2 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

160 W LDMOS transistor for base station applications at frequencies from 1805 MHz to 2025 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a Doherty demo board.

Test signal	f (MHz)	I _{DQ} (mA)	V _{DS} (V)	P _{L(AV)} (W)	G _p (dB)	η _D (%)	ACPR (dBc)
1-carrier W-CDMA	1805 to 1880	350	28	22	16	49	-30 [1]
1-carrier W-CDMA	1880 to 2025	350	28	22	15.5	47	-30 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

- Designed for broadband operation (1805 MHz to 2025 MHz)
- Decoupling leads to enable improved video bandwidth
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Internally matched for ease of use
- High power gain
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base station and multi-carrier applications in the 1805 MHz to 2025 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	video decoupling (main)		
6	video decoupling (peak)		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC8G21LS-160AV	-	air cavity plastic earless flanged package; 6 leads	SOT1275-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; V_{DS} = 28\text{ V}; I_{DQ} = 400\text{ mA}$		
		$P_L = 23\text{ W}$	0.371	K/W
		$P_L = 89\text{ W}$	0.278	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.72\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 72\text{ mA}$	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 432\text{ mA}$	1.6	2.1	2.4	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	14	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 72\text{ mA}$	-	0.60	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 2.52\text{ A}$	-	205	323	$\text{m}\Omega$
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.1\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 110\text{ mA}$	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 660\text{ mA}$	1.6	2.0	2.4	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	20	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 110\text{ mA}$	-	0.97	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 3.85\text{ A}$	-	145	215	$\text{m}\Omega$

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; $f_1 = 1880\text{ MHz}; f_2 = 2025\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}; I_{Dq} = 200\text{ mA}$ (main); $V_{GS(amp)peak} = 0.5\text{ V}; T_{case} = 25\text{ °C}$; unless otherwise specified; in an asymmetrical Doherty production test circuit at 1880 MHz to 2025 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 22.5\text{ W}$	13.8	15	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 22.5\text{ W}$	-	-10	-6	dB
η_D	drain efficiency	$P_{L(AV)} = 22.5\text{ W}$	40	45	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 22.5\text{ W}$	-	-30	-25	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; $f = 2025\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}; I_{Dq} = 200\text{ mA}$ (main); $V_{GS(amp)peak} = 0.5\text{ V}; T_{case} = 25\text{ °C}$; unless otherwise specified; in an asymmetrical Doherty production test circuit at 1880 MHz to 2025 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)} = 60\text{ W}$	4.3	4.9	-	dB
$P_{L(M)}$	peak output power		158	185	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC8G21LS-160AV is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq} = 200\text{ mA}$ (main); $V_{GS(amp)peak} = 0.5\text{ V}$; $P_L = 120\text{ W}$ (CW); $f = 1880\text{ MHz}$.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; $I_{Dq} = 450\text{ mA}$ (main); $V_{DS} = 28\text{ V}$.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_P [2] (dB)
Maximum power load					
1805	1.63 – j7.04	2.69 – j7.69	87.05	55.92	16.44
1880	2.43 – j7.93	2.69 – j7.69	84.00	55.41	16.40
1920	3.64 – j9.19	3.32 – j8.33	82.41	58.81	17.29
2025	9.22 – j10.74	2.69 – j7.69	83.16	60.51	17.28
Maximum drain efficiency load					
1805	1.63 – j7.04	7.07 – j5.17	55.89	69.34	19.16
1880	2.43 – j7.93	5.49 – j4.59	55.05	68.21	19.14
1920	3.64 – j9.19	4.63 – j4.53	54.27	67.40	18.94
2025	9.22 – j10.74	3.29 – j5.36	55.68	65.66	18.96

[1] Z_S and Z_L defined in [Figure 1](#).

[2] at 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; $I_{Dq} = 600\text{ mA}$ (peak); $V_{DS} = 28\text{ V}$.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_P [2] (dB)
Maximum power load					
1805	1.11 – j6.63	3.23 – j7.06	126.00	56.38	16.26
1880	1.60 – j7.94	3.23 – j7.06	122.98	55.66	16.28
1920	3.45 – j8.58	3.23 – j7.06	120.56	55.34	16.18
2025	5.33 – j7.56	3.97 – j7.59	128.56	58.56	16.97
Maximum drain efficiency load					
1805	1.11 – j6.63	5.83 – j3.19	80.08	66.92	18.77
1880	1.60 – j7.94	4.65 – j3.75	84.85	65.61	18.59
1920	3.45 – j8.58	3.94 – j3.76	81.80	64.85	18.37
2025	5.33 – j7.56	3.24 – j4.34	82.20	65.52	18.89

[1] Z_S and Z_L defined in [Figure 1](#).

[2] at 3 dB gain compression.

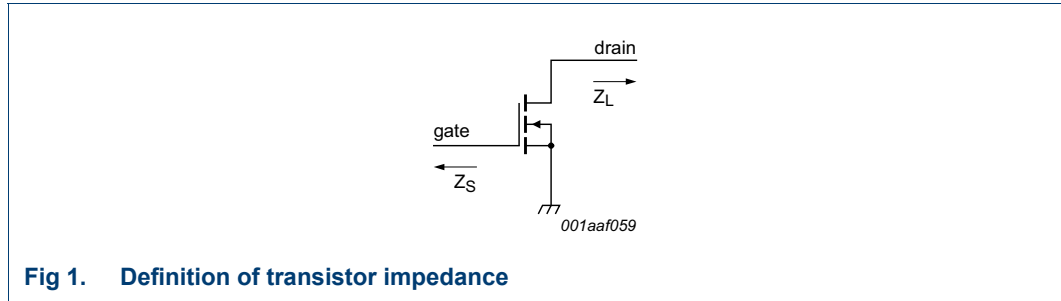


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main device at 1 : 1 load

Measured load-pull data of main device; $I_{Dq} = 450 \text{ mA (main)}$; $V_{DS} = 28 \text{ V}$.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (dBm)	η_D [3] (%)	G_p [3] (dB)
1805	1.63 – j7.04	4.46 – j6.76	48.9	40.0	21.0
1880	2.43 – j7.93	4.46 – j6.76	48.6	41.0	21.3
1920	3.64 – j9.19	4.46 – j6.76	48.6	41.0	21.3
2025	9.22 – j10.74	3.23 – j7.06	48.7	41.0	21.1

[1] Z_S and Z_L defined in [Figure 1](#).

[2] at 3 dB gain compression.

[3] at $P_{L(AV)} = 43.5 \text{ dBm}$.

Table 12. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; $I_{Dq} = 450 \text{ mA (main)}$; $V_{DS} = 28 \text{ V}$.

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (dBm)	η_D [3] (%)	G_p [3] (dB)
1805	1.63 – j7.04	7.87 – j2.50	46.2	49.5	22.2
1880	2.43 – j7.93	7.43 – j2.21	45.8	53.1	22.9
1920	3.64 – j9.19	7.43 – j2.21	45.8	53.1	22.9
2025	9.22 – j10.74	3.94 – j3.76	45.9	54.6	22.9

[1] Z_S and Z_L defined in [Figure 1](#).

[2] at 3 dB gain compression.

[3] at $P_{L(AV)} = 43.5 \text{ dBm}$.

7.4 VBW in Doherty operation

The BLC8G21LS-160AV shows 110 MHz (typical) video bandwidth in Doherty demo board in 1880 MHz at $V_{DS} = 28 \text{ V}$; $I_{Dq} = 200 \text{ mA}$ and $V_{GS(amp)peak} = 0.5 \text{ V}$.

7.5 Test circuit

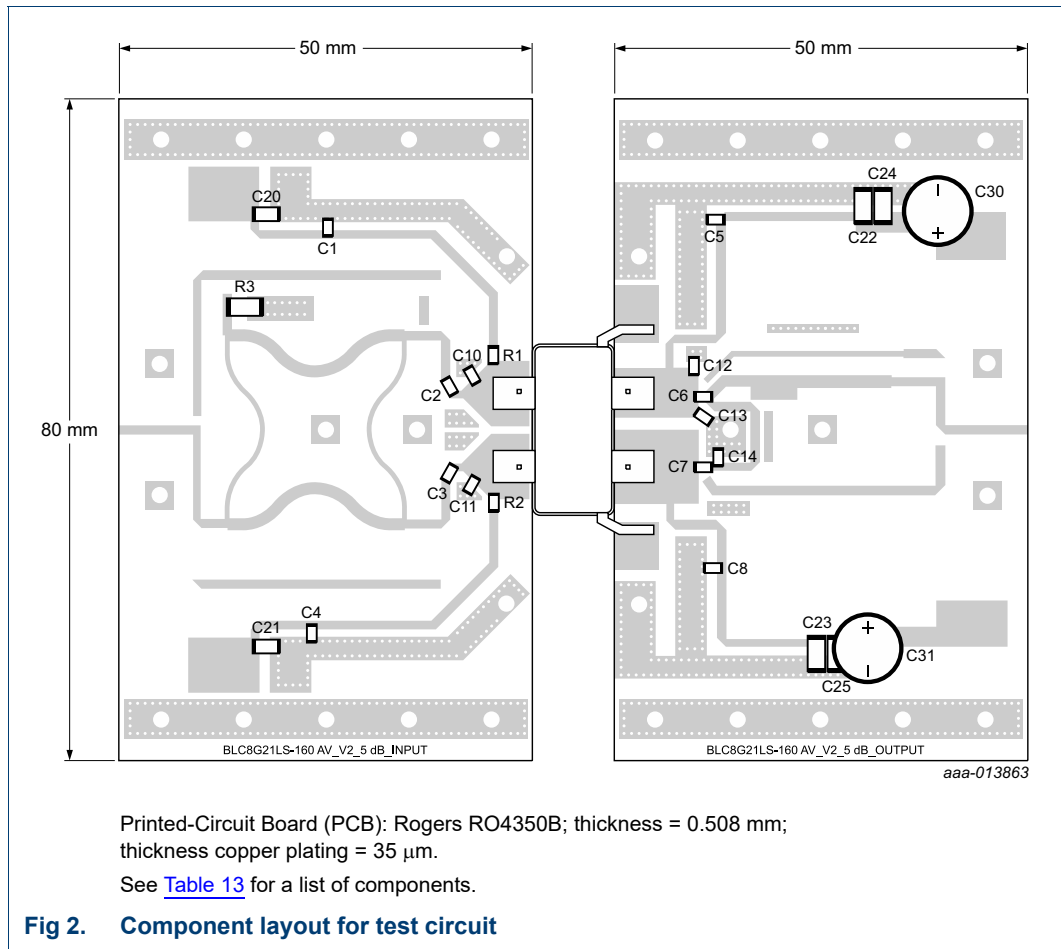
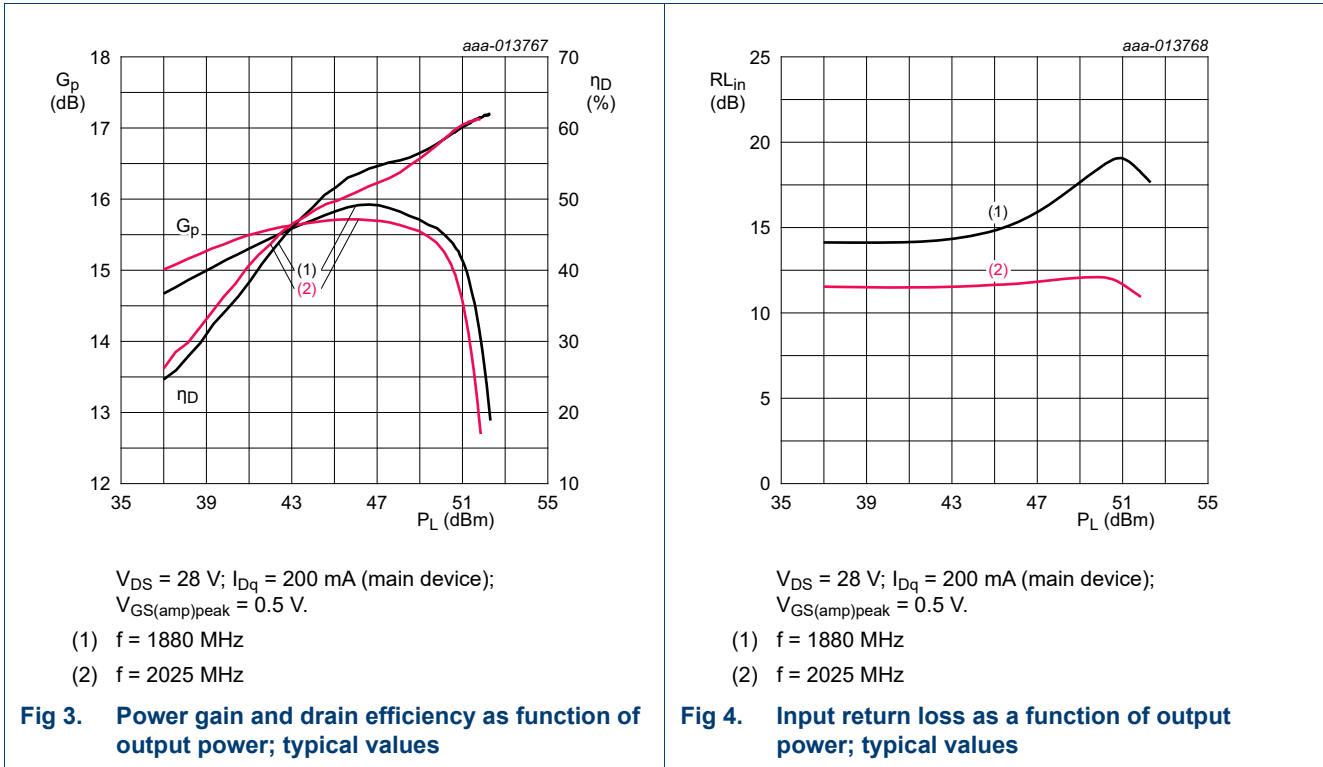


Table 13. List of components
See [Figure 2](#) for component layout.

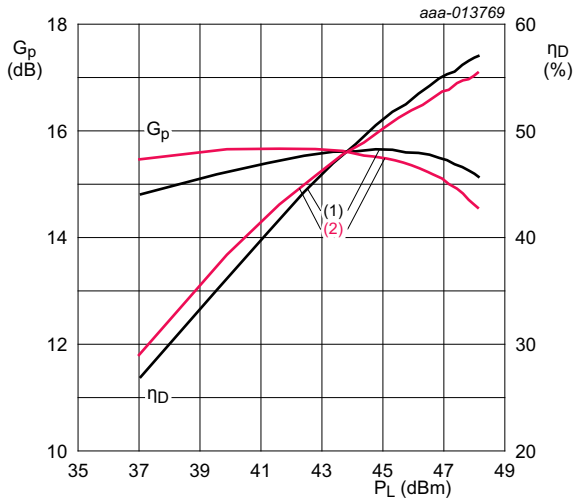
Component	Description	Value	Remarks
C1, C2, C3, C4, C5, C6, C7, C8	multilayer ceramic chip capacitor	22 pF	
C10	multilayer ceramic chip capacitor	0.3 pF	
C11	multilayer ceramic chip capacitor	0.8 pF	
C12	multilayer ceramic chip capacitor	0.5 pF	
C13	multilayer ceramic chip capacitor	0.7 pF	
C14	multilayer ceramic chip capacitor	1.1 pF	
C20, C21, C22, C23	multilayer ceramic chip capacitor	1 μ F, 50 V	
C24, C25	multilayer ceramic chip capacitor	10 μ F, 50 V	
C30, C31	electrolytic capacitor	2200 μ F, 50 V	
R1, R2	SMD resistor	5.1 Ω	
R3	wire resistor	50 Ω	

7.6 Graphical data

7.6.1 Pulsed CW

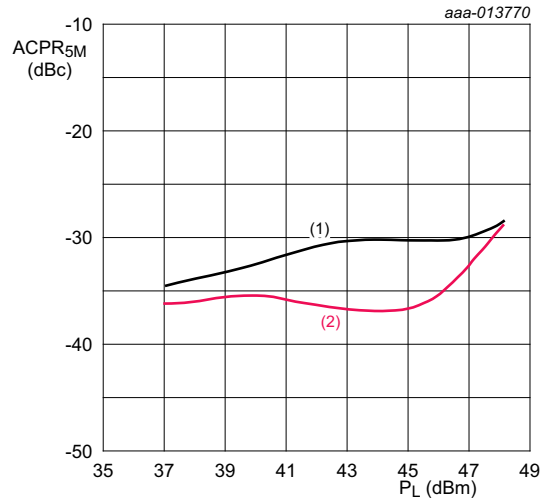


7.6.2 1-Carrier W-CDMA



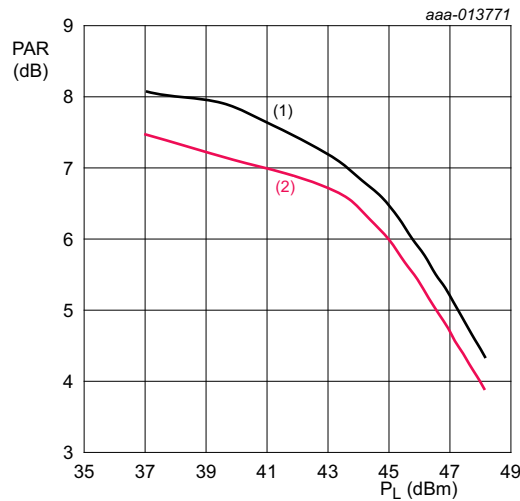
$V_{DS} = 28\text{ V}$; $I_{Dq} = 200\text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.5\text{ V}$.
 (1) $f = 1880\text{ MHz}$
 (2) $f = 2025\text{ MHz}$

Fig 5. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 200\text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.5\text{ V}$.
 (1) $f = 1880\text{ MHz}$
 (2) $f = 2025\text{ MHz}$

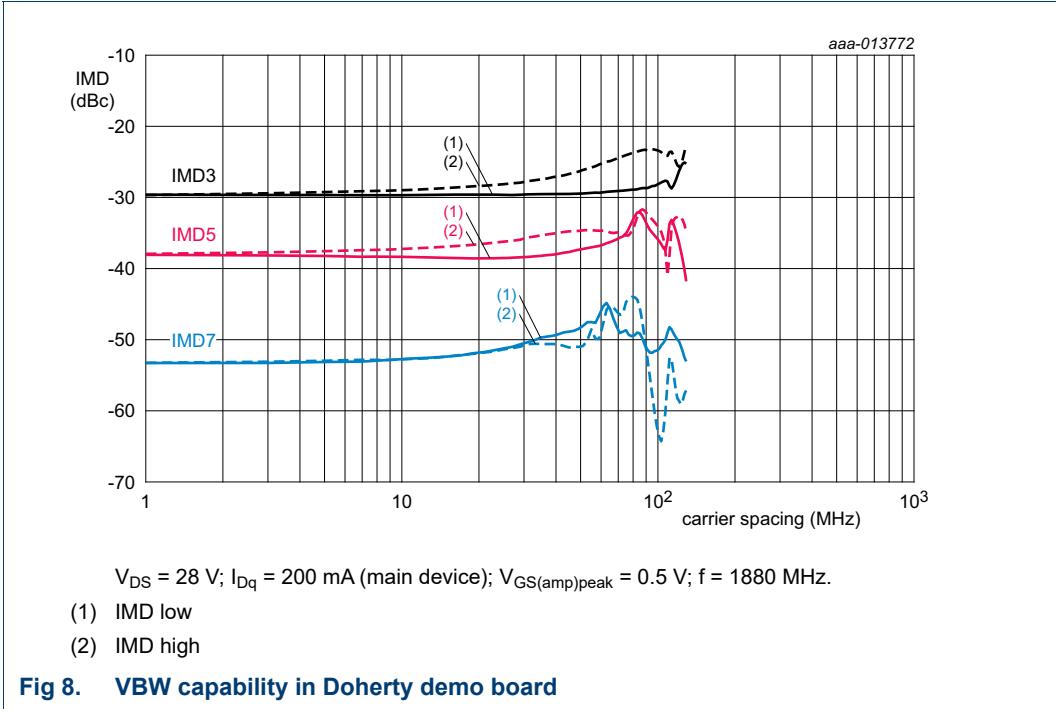
Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 200\text{ mA}$ (main device); $V_{GS(amp)peak} = 0.5\text{ V}$.
 (1) $f = 1880\text{ MHz}$
 (2) $f = 2025\text{ MHz}$

Fig 7. Peak-to-average power ratio as a function of output power; typical values

7.6.3 2-Tone VBW



8. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1275-1

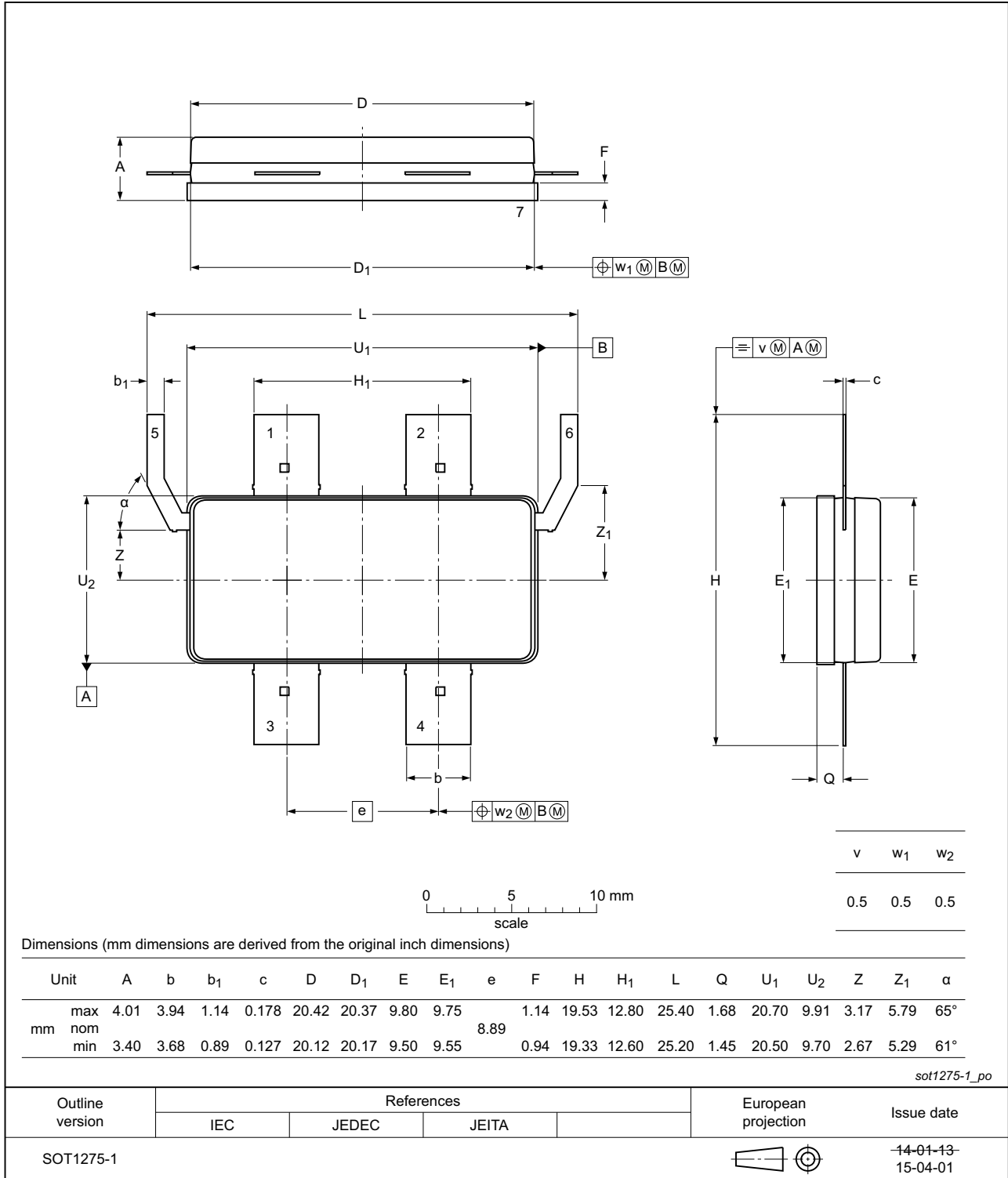


Fig 9. Package outline SOT1275-1

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 14. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC8G21LS-160AV#2	20150901	Product data sheet	-	BLC8G21LS-160AV v.1
Modifications:	<ul style="list-style-type: none"> The format of this document has been redesigned to comply with the new identity guidelines of Ampleon. Legal texts have been adapted to the new company name where appropriate. 			
BLC8G21LS-160AV v.1	20140812	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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