RSL10

Bluetooth® 5 无线片上系统(SoC)

引言

RSL10是一款超低功率、高度灵活的多协议2.4 GHz无线器件，专为高性能可穿戴应用和医疗应用而设计。凭借Arm® Cortex® M3处理器和LPDSP32 DSP核心，RSL10可支持蓝牙低功耗技术和 2.4 GHz专有协议栈，而不会影响功耗。

关键特性

- Rx (接收)灵敏度(蓝牙低能耗模式，1 Mbps)：−94 dBm
- 数据速率：62.5至2000 kbps
- 发射功率：−17至+6 dBm
- 峰值Rx(接收)电流 = 5.6 mA (1.25 V VBAT)
- 峰值Rx(接收)电流 = 3.0 mA (3 V VBAT)
- 峰值Tx(发射)电流(0 dBm) = 8.9 mA (1.25 V VBAT)
- 峰值Tx(发射)电流(0 dBm) = 4.6 mA (3 V VBAT)
- 蓝牙5认证，提供LE 2M PHY 支持
- Arm Cortex−M3处理器，时钟速度最高可达48 MHz
- LPDSP32(适用于音频编解码器)
- 电源电压范围：1.1−3.3 V
- 电流消耗(1.25 V VBAT)：
  - 深度睡眠，IO唤醒：50 nA
  - 深度睡眠，8 kB RAM (用于保留数据)：300 nA
  - 以7 kHz音频带宽串流音频时： 1.8 mA RX，1.8 mA TX
- 电流消耗(3 V VBAT)：
  - 深度睡眠，IO唤醒：25 nA
  - 深度睡眠，8 kB RAM (用于保留数据)：100 nA
  - 以7 kHz音频带宽串流音频时：0.9 mA RX，0.9 mA TX
- 384 kB闪存
- 高度集成的片上系统(SoC)
- 支持FOTA (Firmware Over−The−Air，空中固件升级)更新

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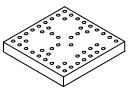
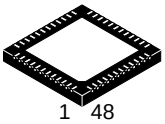


WLCSP51
CASE 567MT



QFN48
CASE 485BA

(QFN48)

(WLCSP51)

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y or YY = Year
WW = Work Week
G or ▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCH−RSL10−101WC51−ABG	WLCSP51 (Pb−Free)	5000 / Tape & Reel
NCH−RSL10−101Q48−ABG	QFN48 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

产品特性

- **Arm Cortex−M3处理器：**32位核心，适用于实时应用，专为打造用于各种低功耗应用的高性能、低成本平台而开发。
- **LPDSP32：**32位双Harvard DSP核心，为无线通信所需的音频编解码器提供高效支持。在RSL10开发工具中包含多个库，可为客户提供各种编解码器。
- **射频前端：**在2.4 GHz射频收发器的基础上，RFFE对蓝牙低功耗技术标准和其他专有或定制协议实现了物理层。
- **协议基带硬件：**蓝牙5认证，支持2 Mbps射频链路支持和定制协议选项。RSL10基带栈通过支持结构进行补充，该结构允许实施安森美半导体和客户设计的定制协议。
- **高度集成的SoC：**双核架构结合高效电源管理单元、振荡器、闪存和RAM存储器、DMA控制器，以及完备的周边设备和接口。
- **深度睡眠模式：**在不需要运行时，RSL10可进入深度睡眠模式。提供各种深度睡眠模式配置，包括：
  - “IO唤醒”配置。在深度睡眠模式下，功耗为50 nA (1.25 V VBAT)。
  - 嵌入式32 kHz振荡器，可通过计时器或外部引脚中断运行。总电流损耗为90 nA (1.25 V VBAT)。
  - 如上所述，产品包含8 kB RAM，用于保留数据。总电流损耗为300 nA (1.25 V VBAT)。
  - 除了“仅IO唤醒”配置外，还可以启用芯片上的降压转换器，在深度睡眠模式下减少电流消耗(VBAT电压较高时)。
- **待机模式：**可用于减小低占空比下的平均功耗，范围通常从几毫秒到几百毫秒不等。待机模式下，典型的芯片功耗为30 μA。
- **多协议支持：**利用LPDSP32、Arm Cortex−M3处理器和射频前端所带来的灵活性，可支持专有协议和其他定制协议。
- **灵活的电源电压范围：**RSL10集成了高效功率调节器，VBAT电压范围为1.1至3.3 V。请看表2：推荐工作条件。
- **高度可配置的接口：**I^2C、UART、两个SPI接口、PCM接口、多个GPIO。还支持数字麦克风接口(DMIC)和输出驱动器(OD)。
- **异步采样率转换器(ASRC)模块和音频信宿时钟模块**提供了一种在音频来源和音频信宿之间同步音频采样率的方式。音频信宿时钟还提供了一种高精确度机制，测量RTC或协议时序所使用的输入时钟。
- **灵活的计时方案：**发射或接收射频通信时，必须从射频前端的XTAL/PLL以48 MHz的时钟速度对RSL10计时。在不发射/接收射频通信时，RSL10可关闭48 MHz XTAL、内部RC振荡器、32 kHz 振荡器或外部时钟。低频RTC时钟(32 kHz)还可在深度睡眠模式下使用。可以将内部XTAL、RC 振荡器或数字输入焊盘作为来源。
- **多种存储架构：**提供76 kB的SRAM程序存储和88 kB的SRAM数据存储。提供共384 kB的闪存，用于存储蓝牙栈和其他应用。Arm Cortex−M3处理器可从SRAM和/或闪存执行。
- **IP保护功能：**确保第三方无法复制客户的闪存内容。可有效防止在启动芯片后，从外部访问任何核心或存储器。
- **超低功耗应用示例：**
  - 音频信号串流：IDD = 1.8 mA @ VBAT 1.25 V (Rx模式)，使用安森美半导体专有定制音频协议，接收、解码和发送7 kHz带宽音频信号至SPI接口。
  - 低占空比广播：IDD 1.1 μA，以5秒的间隔在所有三个信道进行广播(VBAT 3 V，DCDC转换器启用)。
- **RoHS认证设备**

RSL10内部框图

RSL10芯片框图如图1所示。

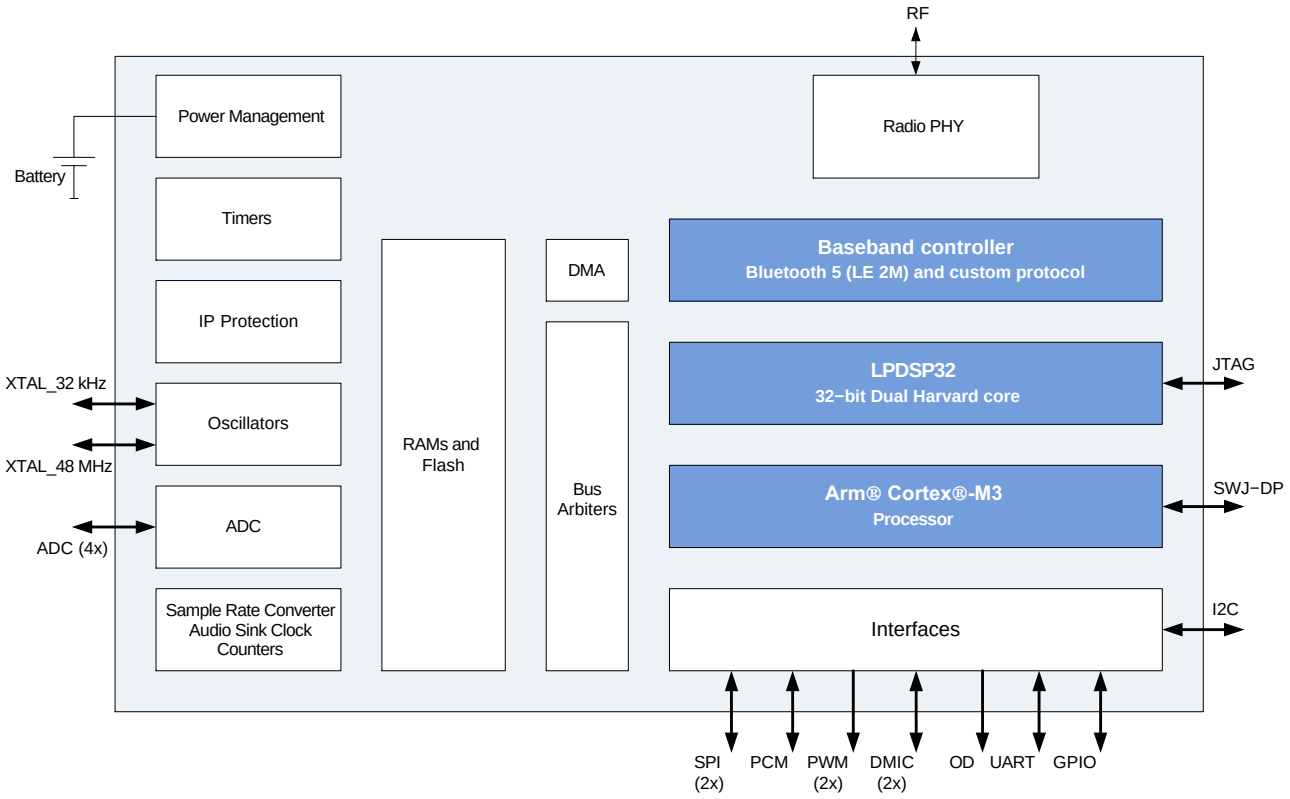


Figure 1. RSL10 Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VBAT	Power supply voltage	−	3.63	V
VDDO	I/O supply voltage	−	3.63	V
VSSRF	RF front−end ground	−0.3	−	V
VSSA	Analog ground	−0.3	−	V
VSSD	Digital core and I/O ground	−0.3	−	V
Vin	Voltage at any input pin	VSSD−0.3	VDDO + 0.3	V
T functional	Functional temperature range	−40	85	°C
T storage	Storage temperature range	−40	85	°C
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V) The QFN package meets 450 V CDM level				

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
(参考译文)
如果电压超过最大额定值表中列出的值范围，器件可能会损坏。如果超过任何这些限值，将无法保证器件功能，可能会导致器件损坏，影响可靠性。

Table 2. RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Conditions	Min	Typ	Max	Units
Supply voltage operating range	VBAT	Input supply voltage on VBAT pin (Note 1)	1.18	1.25	3.3	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
(参考译文)
高于推荐工作范围表格中所列电压时，不保证能够正常运行。长时间在推荐工作范围表格中规定范围以外的电压下运行，可能会影响器件的可靠性。

1. In order to be able to use a VBAT Min of 1.1 V, the following reduced operating conditions should be observed:
   − Maximum Tx power 0 dBm.
   − SYSCLK ≤ 24 MHz.
   − Functional temperature range limited to 0−50 deg C
   The following trimming parameters should be used:
   − VCC = 1.10 V
   − VDDC = 0.92 V
   − VDDM = 1.05 V, will be limited by VCC at end of battery life
   − VDDRF = 1.05 V, will be limited by VCC at end of battery life. VDDPA should be disabled
   RSL10 should enter in end−of−battery−life operating mode if VCC falls below 1.03 V. VCC will remain above 1.03 V if VBAT ≥ 1.10 V under the restricted operating conditions described above.

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS

Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
OVERALL						
Current consumption RX, V_{BAT} = 1.25 V, low latency	I_{VBAT}	RX Mode, ON Semiconductor proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay.	−	1.8	−	mA
Current consumption TX, V_{BAT} = 1.25 V, low latency	I_{VBAT}	TX Mode, ON Semiconductor |proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. Transmit power: 0 dBm	−	1.8	−	mA
Current consumption RX, V_{BAT} = 1.25 V	I_{VBAT}	RX Mode, ON Semiconductor proprietary audio streaming protocol at 7 kHz audio BW, 37 ms delay.	−	1.15	−	mA
Deep sleep current, example 1, V_{BAT} = 1.25 V	Ids1	Wake up from wake up pin.	−	50	−	nA
Deep sleep current, example 2, V_{BAT} = 1.25 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.	−	90	−	nA
Deep sleep current, example 3, V_{BAT} = 1.25 V	Ids3	As Ids2 but with 8 kB RAM data retention.	−	300	−	nA
Standby Mode current, V_{BAT} = 1.25 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.	−	30	−	μA
Current consumption RX, V_{BAT} = 3 V	I_{VBAT}	RX Mode, ON Semiconductor proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay.	−	0.9	−	mA
Current consumption TX, V_{BAT} = 3 V	I_{VBAT}	TX Mode, ON Semiconductor proprietary audio streaming protocol at 7 kHz audio BW, 5.5 ms delay. Transmit power: 0 dBm	−	0.9	−	mA
Deep sleep current, example 1, V_{BAT} = 3 V	Ids1	Wake up form wake up pin.	−	25	−	nA
Deep sleep current, example 2, V_{BAT} = 3 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.	−	40	−	nA
Deep sleep current, example 3, V_{BAT} = 3 V	Ids3	As Ids2 but with 8 kB RAM data retention.	−	100	−	nA
Standby Mode current, V_{BAT} = 3 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.	−	17	−	μA

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
EEMBC ULPMark BENCHMARK, CORE PROFILE						
ULPMark CP 3.0 V		Arm Cortex−M3 processor running from RAM, VBAT= 3.0 V, IAR C/C++ Compiler for ARM 8.20.1.14183	−	1090	−	ULP Mark
ULPMark CP 2.1 V		Arm Cortex−M3 processor running from RAM, VBAT= 2.1 V, IAR C/C++ Compiler for ARM 8.20.1.14183	−	1260	−	ULP Mark
EEMBC CoreMark BENCHMARK for the Arm Cortex−M3 Processor and the LPDSP32 DSP						
Arm Cortex−M3 processor running from RAM		At 48 MHz SYSCLK. Using the IAR 8.10.1 C compiler, certified	−	159	−	Core Mark
LPDSP32 running from RAM		At 48 MHz SYSCLK Using the 2017.03−SP3−2 release of the Synopsys LPDSP32 C compiler	−	133	−	Core Mark
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK	−	108	−	Core Mark/ mA
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 3 V		At 48 MHz SYSCLK	−	257	−	Core Mark/ mA
INTERNALLY GENERATED VDDC: Digital Block Supply Voltage						
Supply voltage: operating range	VDDC		0.92	1.15	1.32 (Note 2)	V
Supply voltage: trimming range	$VDDC_{RANGE}$		0.75	−	1.38	V
Supply voltage: trimming step	$VDDC_{STEP}$		−	10	−	mV
INTERNALLY GENERATED VDDM: Memories Supply Voltage						
Supply voltage: operating range	VDDM		1.05	1.15	1.32 (Note 3)	V
Supply voltage: trimming range	$VDDM_{RANGE}$		0.75	−	1.38	V
Supply voltage: trimming step	$VDDM_{STEP}$		−	10	−	mV
INTERNALLY GENERATED VDDRF: Radio Front end supply voltage						
Supply voltage: operating range	VDDRF		1.00	1.10	1.32 (Notes 4 and 5)	V
Supply voltage: trimming range	$VDDRF_{RANGE}$		0.75	−	1.38	V
Supply voltage: trimming step	$VDDRF_{STEP}$		−	10	−	mV
INTERNALLY GENERATED VDDPA: Optional Radio Power Amplifier Supply Voltage						
Supply voltage: operating range	VDDPA		1.05	1.3	1.68	V
Supply voltage: trimming range	$VDDPA_{RANGE}$		1.05	−	1.68	V
Supply voltage: trimming step	$VDDPA_{STEP}$		−	10	−	mV
Supply voltage: trimming step	$DCDC_{STEP}$		−	10	−	mV
VDDO PAD SUPPLY VOLTAGE: Digital Level High Voltage						
Digital I/O supply	VDDO		1.1	1.25	3.3	V
INDUCTIVE BUCK DC−DC CONVERTER						
VBAT range when the DC−DC converter is active (Note 6)	$DCDC_{IN\_RANGE}$		1.4	−	3.3	V
VBAT range when the LDO is active	LDO_{IN_RANGE}		1.1	−	3.3	V
Output voltage: trimming range	$DCDC_{OUT\_RANGE}$		1.1	1.2	1.32	V
Supply voltage: trimming step	$DCDC_{STEP}$		−	10	−	mV

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
POWER−ON RESET						
POR voltage	$VBAT_{POR}$		0.4	0.8	1.0	V
RADIO FRONT−END: General Specifications						
RF input impedance	Z_{in}	Single ended	−	50	−	Ω
Input reflection coefficient	S_{11}	All channels	−	−	−8	dB
Data rate FSK / MSK / GFSK	R_{FSK}	OQPSK as MSK	62.5	1000	3000	kbps
Data rate 4−FSK			−	−	4000	kbps
On−air data rate	bps	GFSK	250	−	2000	kbps
RADIO FRONT−END: Crystal and Clock Specifications						
Xtal frequency	F_{XTAL}	Fundamental		48		MHz
Equiv. series Res.	ESR_{XTAL}	RSL10 has internal load capacitors, additional external capacitors are not required	20	−	80	Ω
Differential equivalent load capacitance	CL_{XTAL}	Internal load capacitors (NO EXTERNAL LOAD CAPACITORS REQUIRED)	6	8	10	pF
Settling time			−	0.5	1.5	ms
RADIO FRONT−END: Synthesizer Specifications						
Frequency range	F_{RF}	Supported carrier frequencies	2360	−	2500	MHz
RX frequency step		RX Mode frequency synthesizer resolution	−	−	100	Hz
TX frequency step		TX Mode frequency synthesizer resolution	−	−	600	Hz
PLL Settling time, RX	t_{PLL_RX}	RX Mode	−	15	25	μs
PLL Settling time, TX	t_{PLL_TX}	TX mode, BLE modulation	−	5	10	μs
RADIO FRONT−END: Receive Mode Specifications						
Current consumption at 1 Mbps, V_{BAT} = 1.25 V	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle	−	5.6	−	mA
Current consumption at 2 Mbps, V_{BAT} = 1.25 V	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle	−	6.2	−	mA
Current consumption at 1 Mbps, V_{BAT} = 3 V, DC−DC	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle	−	3.0	−	mA
Current consumption at 2 Mbps, V_{BAT} = 3 V, DC−DC	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle	−	3.4	−	mA
RX Sensitivity, 0.25 Mbps		0.1% BER (Notes 7, 8)	−	−97	−	dBm
RX Sensitivity, 0.5 Mbps		0.1% BER (Notes 7, 8)	−	−96	−	dBm
RX Sensitivity, 1 Mbps, BLE		0.1% BER (Notes 7, 8) Single−ended on chip antenna match to 50 Ω	−	−94	−	dBm
RX Sensitivity, 2 Mbps, BLE		0.1% BER (Notes 7, 8)	−	−92	−	dBm
RSSI effective range		Without AGC	−	60	−	dB
RSSI step size			−	2.4	−	dB
RX AGC range			−	48	−	dB
RX AGC step size		Programmable	−	6	−	dB
Max usable signal level		0.1% BER	0	5	−	dBm

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
RADIO FRONT−END: Transmit Mode Specifications						
Tx peak power consumption at VBAT = 1.25 V (Note 9)	$IBAT_{RFTX}$	Tx power 0 dBm, VDDRF = 1.07 V, VDDPA: off, LDO mode	−	8.9	−	mA
		Tx power 3 dBm, VDDRF = 1.1 V, VDDPA = 1.26 V, LDO mode	−	17.4	−	mA
		Tx power 6 dBm, VDDRF = 1.1 V, VDDPA = 1.60 V, LDO mode	−	25	−	mA
Tx peak power consumption at VBAT = 3 V (Note 9)	$IBAT_{RFTX}$	Tx power 0 dBm, VDDRF = 1.07 V, VDDPA: off, DC−DC mode	−	4.6	−	mA
		Tx power 3 dBm, VDDRF = 1.1 V, VDDPA = 1.26 V, DC−DC mode	−	8.6	−	mA
		Tx power 6 dBm, VDDRF = 1.1 V, VDDPA = 1.60 V, DC−DC mode	−	12	−	mA
Transmit power range		BLE or 802.15.4 OQPSK	−17	+0.5	+6	dBm
Transmit power step size		Full band.	−	2	−	dB
Transmit power accuracy		Tx power 3 dBm. Full band. Relative to the typical value.	−1.5	−	+1	dB
		Tx power 0 dBm. Full band. Relative to the typical value.	−1.5	−	1.5	dB
Power in 2nd harmonic		0 dBm mode. 50 Ω for “Typ” value. (Note 10)	−	−31	−18	dBm
Power in 3rd harmonic		0 dBm mode. 50 Ω for “Typ” value. (Note 10)	−	−40	−31	dBm
Power in 4th harmonic		0 dBm mode. 50 Ω for “Typ” value. (Note 10)	−	−49	−42	dBm
ADC						
Resolution	ADC_{RES}		8	12	14	bits
Input voltage range	ADC_{RANGE}		0	−	2	V
INL	ADC_{INL}		−2	−	+2	mV
DNL	ADC_{DNL}		−1	−	+1	mV
Channel sampling frequency	ADC_{CH_SF}	For the 8 channels sequentially, SLOWCLK = 1 MHz	0.0195	−	6.25	kHz
32 kHz ON−CHIP RC OSCILLATOR						
Untrimmed Frequency	$Freq_{UNTR}$		20	32	50	kHz
Trimming steps	Steps		−	1.5	−	%
3 MHz ON−CHIP RC OSCILLATOR						
Untrimmed Frequency	$Freq_{UNTR}$		2	3	5	MHz
Trimming steps	Steps		−	1.5	−	%
Hi Speed mode	Fhi		−	10	−	MHz
32 kHz ON−CHIP CRYSTAL OSCILLATOR (Note 11)						
Output Frequency	$Freq_{32k}$	Depends on xtal parameters	−	32768	−	Hz
Startup time			−	1	3	s
Internal load trimming range		Steps of 0.4 pF	0		25.2	pF
Load Capacitance		No external load capacitors required. Maximum external parasitic capacity allowed (package, routing, etc.)	−	−	3.5	pF
ESR			−	−	100	kΩ
Duty Cycle			40	50	60	%

Table 3. ELECTRICAL PERFORMANCE SPECIFICATIONS (continued)
Unless otherwise noted, the specifications mentioned in the table below are valid at 25°C at VBAT = VDDO = 1.25 V.

Description	Symbol	Conditions	Min	Typ	Max	Units
DC CHARACTERISTICS OF THE DIGITAL PADS − With VDDO = 2.97 V – 3.3 V, nominal: 3.0 V Logic						
Voltage level for high input	V_{IH}		2	−	VDDO+0.3	V
Voltage level for low input	V_{IL}		VSSD−0.3	−	0.8	V
DC CHARACTERISTICS OF THE DIGITAL PADS − With VDDO = 1.1 V – 1.32 V, nominal: 1.2 V Logic						
Voltage level for high Input	V_{IH}		0.65* VDDO	−	VDDO+0.3	V
Voltage level for low input	V_{IL}		VSSD−0.3	−	0.35* VDDO	V
DIO DRIVE STRENGTH						
DIO drive strength	IDIO		2	12	12	mA
FLASH SPECIFICATIONS						
Endurance of the 384 kB of flash			100,000	−	−	write/ erase cycles
Endurance for sections NVR1, NVR2, and NVR3 (6 kB in total)			1000	−	−	write/ erase cycles
Retention			25	−	−	years

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
(参考译文)
除非另有说明，“电气特性”表格中列出的是所列测试条件下的产品性能参数。如果在不同条件下运行，产品性能可能与“电气特性”表格中所列性能参数不一致。

2. The maximum VDDC voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
3. The maximum VDDM voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
4. The maximum VDDRF voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
5. The VDDRF calibrated targets are:
   − 1.10 V (TX power > 0 dBm, with optimal RX sensitivity)
   − 1.07 V (TX power = 0 dBm)
   − 1.20 V (TX power = 2 dBm)
   The VDDPA calibrated targets are:
   − 1.30 V
   − 1.26 V (TX power = 3 dBm, assumes VDDRF = 1.10 V)
   − 1.60 V (TX power = 6 dBm, assumes VDDRF = 1.10 V)
6. The LDO can be used to regulate down from VBAT and generate VCC. For VBAT values higher than 1.5 V, the LDO is less efficient and it is possible to save power by activating the DC−DC converter to generate VCC.
7. Signal generated by RF tester.
8. 0.5 to 1.0 dB degradation in the RX sensitivity is present on the QFN package vs WLCSP. This is attributed to the presence of the metal slug of the QFN package which is in close proximity to on−chip inductors.
9. All values are based on evaluation board performance at the antenna connector, including the harmonic filter loss
10. The values shown here are without RF filter. Harmonics need to be filtered with an external filter (See “RF Filter” on Table 6).
11. These specifications have been validated with the Epson Toyocom MC – 306 crystal

Table 4. VDDM Target Trimming Voltage in Function of VDDO Voltage

VDDM Voltage (V)	DIO_PAD_CFG DRIVE	Maximum VDDO Voltage (V)
1.05	1	2.7
1.05	0	3.2
1.10	0	3.3

NOTE: These are trimming targets at room/ATE temperature 25～30°C.

Table 5. VDDC Target Trimming Voltage in Function of SYSCLK Frequency

VDDC Voltage (V)	Maximum SYSCLK Frequency (MHz)	Restriction
0.92	≤ 24	The ADC will be functional in low frequency mode and between 0 and 85°C only.
1.00	≤ 24	Fully functional
1.05	48	Fully functional

NOTE: These are trimming targets at room/ATE temperature 25～30°C.

Table 6. RECOMMENDED EXTERNAL COMPONENTS:

Components	Function	Recommended typical value	Tolerance
Cap (VBAT−VSSA)	VBAT decoupling	4.7 μF // 100 pF (Note 12)	±20%
Cap (VDDO−VSSD)	VDDO decoupling	1 μF	±20%
Cap (VDDRF−VSSRF)	VDDRF decoupling	2.2 μF	±20%
Cap (VCC−VSSA)	VCC decoupling	Low ESR 2.2 μF (Note 13) or 4.7 μF	±20%
Cap (VDDA−VSSA)	VDDA decoupling	1 μF	±20%
Cap (CAP0−CAP1)	Pump capacitor for the charge pump	1 μF	±20%
Inductor (DC−DC)	DC−DC converter inductance	Low ESR 2.2 μH (See Table 7 below)	±20%
Xtal_32 kHz	Xtal for 32 kHz oscillator	− MC – 306, Epson − CM8V−T1A, Micro Crystal Switzerland	
Xtal_48 MHz	Xtal for 48 MHz oscillator	8Q−48.000MEEV−T, TXC Corporation, Taiwan	
RF filter (Note 14)	External harmonic filter	1.5 pF / 3 nH / 1.5 pF / 1.8 nH	±20%

NOTE: All capacitors used must have good RF performance.

12. The recommended decoupling capacitance uses 2 capacitors with the values specified.
13. Example: AMK105BJ225_P, Taiyo Yuden.
14. For improved harmonic performance in environments where RSL10 is operating in close proximity to smartphones or base stations, FBAR filters such as the Broadcom ACPF−7924 can be applied instead of the suggested discrete harmonic filter.

Table 7. RECOMMENDED DC−DC CONVERTER INDUCTANCE TABLE

Manufacturer	Part Number	Case Size	Comments
Taiyo Yuden	CKP2012N_2R2	0805 SMD with T_{max} = 1.0 mm	A degradation of 1 dB in the RX sensitivity is expected in DC−DC mode (Vbat = 3.3 V) versus LDO mode operation.
Taiyo Yuden	CBMF1608T2R2M	0603 SMD with T_{max} = 1.0 mm	A degradation of <1 dB in RX sensitivity is expected in DC−DC mode (Vbat = 3.3 V) versus LDO mode operation. Also, the current drawn from the battery will be 4−10% higher than when the CKP2012N_2R2 is used depending on operation mode and settings.

NOTE: Values have been measured on the QFN version of the RSL10 development board.

PCB设计指南

1. 解耦电容应当尽可能靠近相关焊球放置。
2. 差分输出信号传输路径应当尽可能对称。
3. 应当尽可能屏蔽掉模拟输入信号。
4. 密切注意寄生耦合电容。
5. 设计PCB时应当特别注意，以获得良好的射频性能。
6. 应当采用多层PCB，并在天线匹配电路正下方的内层设置禁区，以降低影响射频性能的杂散电容。
7. 所有电源电压应当通过高性能射频电容，尽可能靠近其相应引脚解耦。这些电源应当相互分隔布置，尽量布置在不同层(通过PCB上的短线从芯片引脚连接至电源)。
8. 数字信号传输路径不得靠近晶体或电源线。
9. 适当的DC−DC元件设置和布局对DC−DC模式下的RX灵敏度性能至关重要。

Table 8. BUMP AND COATING SPECIFICATIONS

Subject	Specification
Bump metallization	Sn 97.7%/Ag 2.3%
Backside coating specification	Lintec Adwill LC2850
Backside coating thickness	25 μm

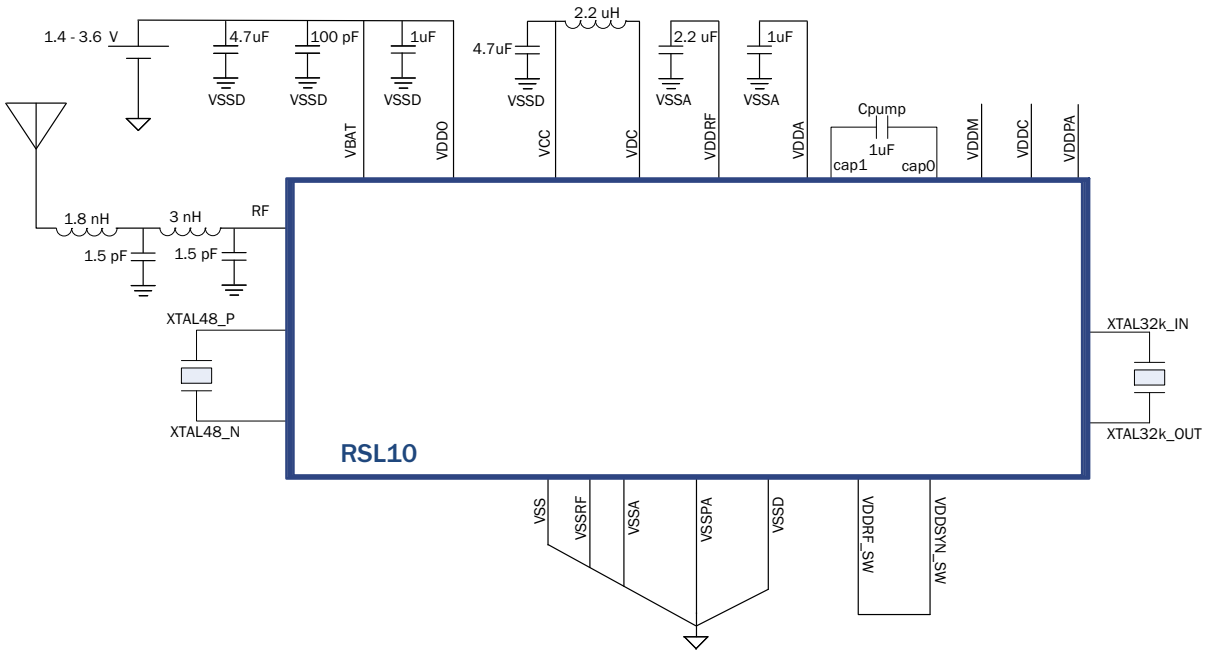
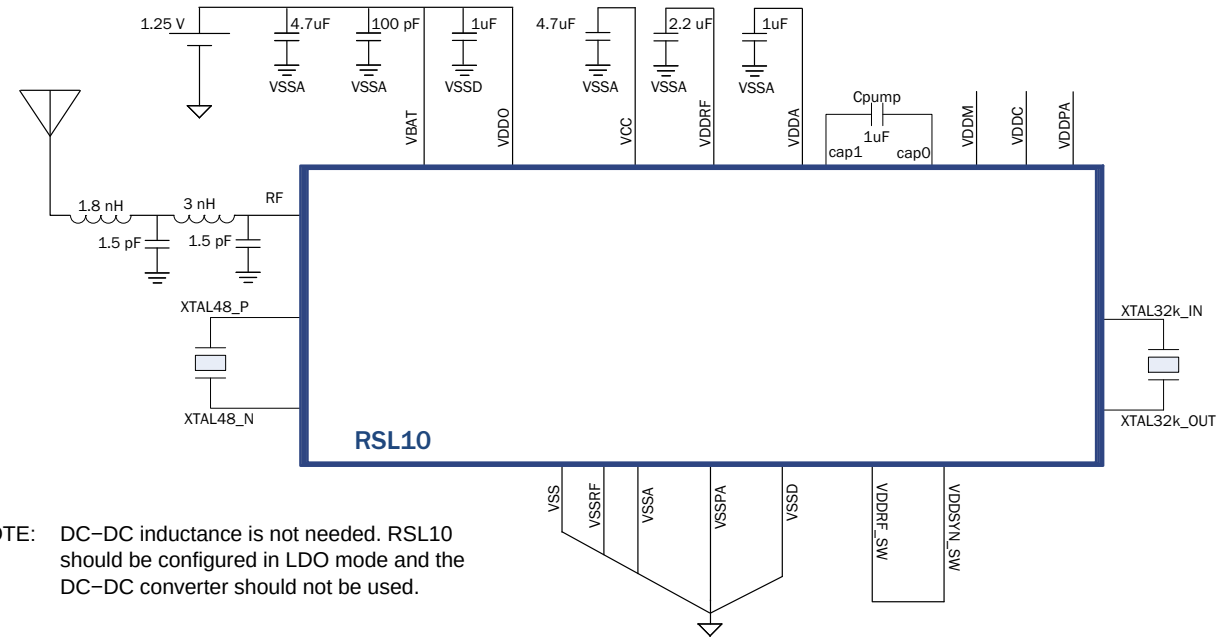


Figure 2. RSL10 Application Diagram in Buck Mode



NOTE: DC−DC inductance is not needed. RSL10 should be configured in LDO mode and the DC−DC converter should not be used.

Figure 3. RSL10 Application Diagram in LDO Mode

Table 9. CHIP INTERFACE SPECIFICATIONS

Pad Name	Description	Power Domain	I/O	A/D	Pull	Pad #, WLCSP	Pad #, QFN48
VBAT	Battery input voltage	VBAT	I	P		K5,K7,K10	9
VDC	DC−DC output voltage to external LC filter		O	A		J11	10
VCC	DC−DC filtered output		I	P/A		K11	12
XTAL32_IN	Xtal input pin for 32 kHz xtal		I/O	A		L10	14
XTAL32_OUT	Xtal output pin for 32 kHz xtal		I/O	A		L11	13
VSSA	Analog ground		I/O	P		E10	8
RES	RESERVED		I	D	D	F8	11
VDDA	Charge pump output for analog and flash supplies	VDDA	I/O	P/A		F11	5
VDDRF	LDO's output for radio voltage supply		I/O	P/A		A11	48
CAP0	Pump capacitor connection		O	A		H11	7
CAP1	Pump capacitor connection		O	A		G10	6
AOUT	Analog test pin		O	A		L6	4
VDDRF_SW	Supply pin for the RF	VDDRF_SW		P/A		A9	47
VDDSYN_SW	Supply pin for the radio synthesizer			P/A		B8	45
VSSRF	RF analog ground		I/O	P		B9	46
XTAL48_N	Negative input for the 48 MHz xtal block		I/O	A		A6	43
XTAL48_P	Positive input for the 48 MHz xtal block		I/O	A		A8	44
VDDPA	Radio power amplifier voltage supply	VDDPA	I/O	P/A		C11	2
VSSPA	Radio power amplifier ground		I/O	P		D11	3
RF	RF signal input/output (Antenna)	RF	I/O	A		B11	1
VPP	Flash high voltage access	VPP	I/O	A		J6	17

Table 9. CHIP INTERFACE SPECIFICATIONS (continued)

Pad Name	Description	Power Domain	I/O	A/D	Pull	Pad #, WLCSP	Pad #, QFN48
NRESET	Reset pin	VDDO	I	D	U1	L9	16
WAKEUP	Wake−up pin for power modes		I	A		L8	15
VDDC	LDO output for Core logic voltage supply		I/O	P		H6	19
VDDM	LDO output for memories voltage supply		I/O	P		F4	21
VDDO	Digital I/O voltage supply		I	P		B4	36
VSSD	Digital ground pad for I/O		I/O	P		F3, D6, F9	28, 35
VSS (*)	Substrate connection for the RF part		I/O	P		B6	42
EXTCLK	External clock input		I	D	U	F1	31
DIO[0]	Digital input output / ADC 0		I/O	A/D	U/D	L4	18
DIO[1]	Digital input output / ADC 1		I/O	A/D	U/D	L3	20
DIO[2]	Digital input output / ADC 2		I/O	A/D	U/D	L2	23
DIO[3]	Digital input output / ADC 3		I/O	A/D	U/D	L1	25
DIO[4]	Digital input output 4		I/O	D	U/D	K2	24
DIO[5]	Digital input output 5		I/O	D	U/D	K1	27
DIO[6]	Digital input output 6		I/O	D	U/D	J1	29
DIO[7]	Digital input output 7		I/O	D	U/D	H1	30
DIO[8]	Digital input output 8		I/O	D	U/D	G2	26
DIO[9]	Digital input output 9		I/O	D	U/D	E2	22
DIO[10]	Digital input output 10		I/O	D	U/D	D1	32
DIO[11]	Digital input output 11		I/O	D	U/D	B2	38
DIO[12]	Digital input output 12		I/O	D	U/D	A1	37
DIO[13]	Digital input output / CM3−JTAG Test Reset		I/O	D	U/D	A2	39
DIO[14]	Digital input output / CM3−JTAG Test Data In		I/O	D	U/D	A3	41
DIO[15]	Digital input output / CM3−JTAG Test Data Out		I/O	D	U/D	A4	40
JTCK	CM3−JTAG Test Clock		I/O	D	U	C1	33
JTMS	CM3−JTAG Test Mode State		I/O	D	U	B1	34

*VSS should be connected to VSSRF at the PCB level.

NOTE: It is recommended that the QFN package metal slug be left open/floating for optimal Rx sensitivity performance

Legend:
Type: A = analog; D = digital; I = input; O = output; P = power
Pull: U = pull up; D = pull down
Pull up: selectable between 10 kΩ and 250 kΩ. U1 = pull up, 200 kΩ.
Pull down: 250 kΩ
All digital pads have a Schmitt trigger input.
All DIO pads have a programmable I^2C low pass filter. All DIOs can be configured to no pull.

架构概览

RSL10芯片架构如图4所示。

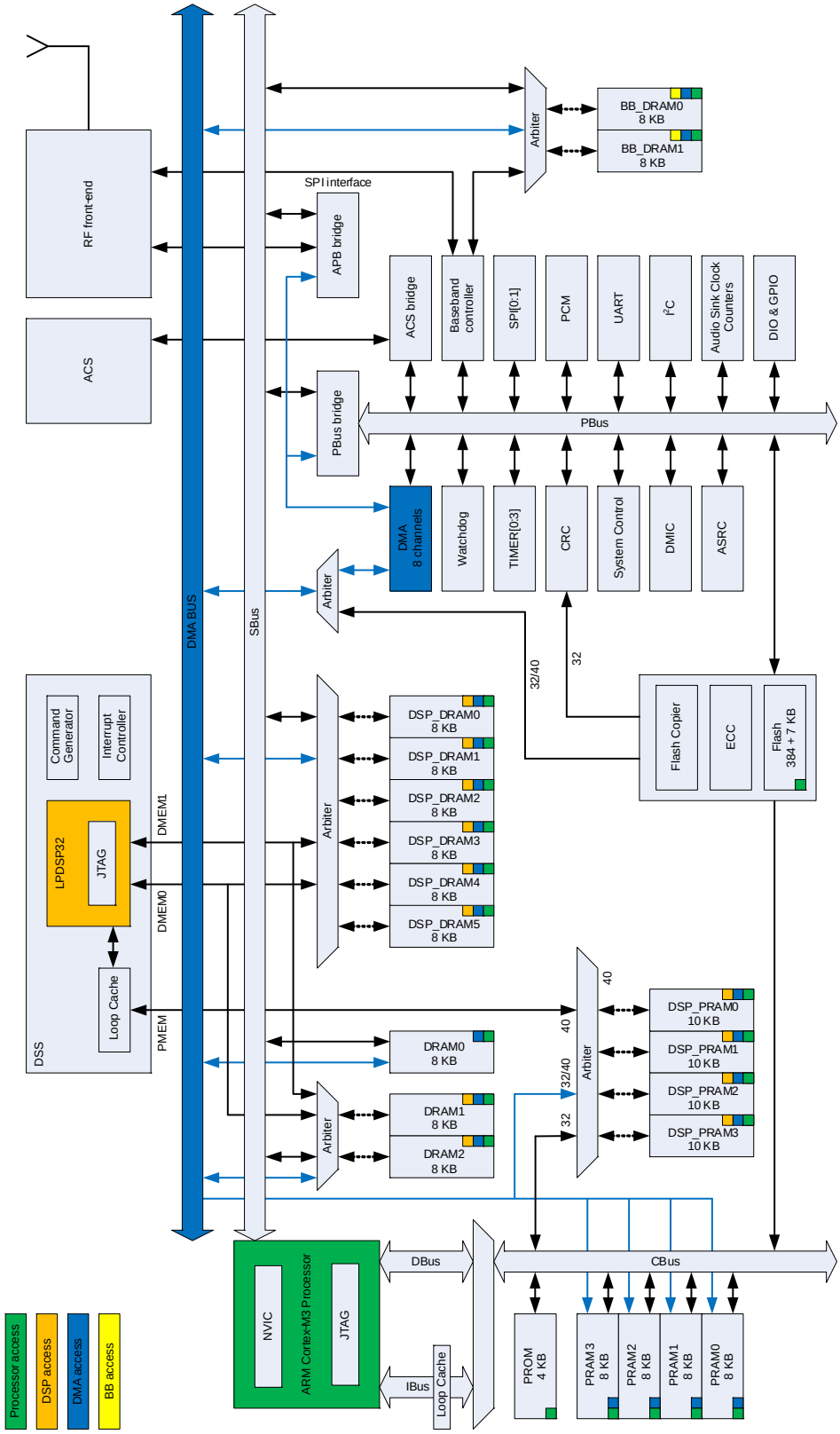


Figure 4. RSL10 Architecture

电源管理单元

电池电压低于可靠运行所需的指定最低电压时，RSL10电源管理单元可防止系统欠压。其作用原理如下：

1. 监控电源，并在需要时，安全地关闭系统。
2. 在插入或移除电池时，防止可能对RSL10造成的损坏。
3. 在低功耗情况下，允许在较宽的温度和电压范围内运行。

在电池电压高于1.4 V时，RSL10允许使用DC−DC转换器，以获得更高的效率，或者在VBAT低于1.4 V时，使用内部LDO。DC−DC转换器或LDO调节器输出用于对RSL10的其他电压调节器模块供电。这些模块包括：

- 对数字核心(VDDC)供电的可编程电压调节器
- 对存储器(VDDM)供电的可编程电压调节器
- 对模拟模块和闪存(VDDA)供电的电荷泵
- 对射频前端(VDDRF)供电的可编程电压调节器
- 对射频功率放大器(VDDPA)供电的可编程电压调节器：此调节器仅用于输出功率为+6 dBm的封装，或者我们想以+3 dBm的输出功率和低于1.4 V的电池电压输电的情况。如果RSL10不必在高功率下输电，可禁用VDDPA调节器，且应当仅使用VDDRF。

时钟和计时选项

RSL10的系统时钟(SYSCLK)有各种来源：

- 48 MHz晶体振荡器，用于正常工作模式
- 内部可微调的RC振荡器，提供3–12 MHz时钟，在系统启动时使用
- 实时时钟，用于待机模式，由以下来源产生：
  - 32 kHz RC振荡器
  - 32 kHz 晶体振荡器
  - DIO0至DIO3其中一个的外部输入
- JTAG时钟，用于调试模式，源于JTCK焊盘
- 外部时钟来源，源于EXTCLK焊盘

在不需要时，可禁用系统中产生的每一个时钟。此外，每一个时钟均有关联的可配置预分频器，可最大限度地降低时钟树上的功率损耗。

时钟检测单元可用于监控系统时钟和/或睡眠及待机模式下的RTC时钟。如果时钟频率低于特定阈值，RSL10 IC将复位。时钟检测器标称阈值为2 kHz。此模块及其触发的复位默认为启用，但都可禁用。

射频前端

RSL10 2.4 GHz射频前端对蓝牙低能耗技术标准和其他标准、专有或定制协议实现了物理层。工作于可在全球部署的2.4 GHz ISM波段(2.4000至2.4835 GHz)并支持：

- 蓝牙5认证，提供LE 2M PHY支持
- 安森美半导体的定制协议和其他定制协议

RSL10射频前端包括了必要的硬件，以支持下列协议：

- IEEE 802.15.4标准，用作许多标准和专有协议的物理层，包括ZigBee和Thread
- 专有协议或专有音频协议。

2.4 GHz射频前端基于低中频架构，并包含以下构建基块：

- 高性能单端射频端口
- 带50 Ω射频输入的芯片上匹配网络
- 高增益、低功率LNA (低噪声放大器)和混合器
- 输出功率为+3 dBm的PA (功率放大器)，用于蓝牙和802.15.4 OQPSK应用，功率最高可达+6 dBm，且使用专用PA电压
- ADC转换器
- RSSI (接收信号强度指示)，具有60 dB的标称值范围，步长为2.4 dB (不考虑AGC)
- 完全集成超低功率频率合成，具有快速的稳定时间，直接的数字传输调制(脉冲波形可编程)
- 48 MHz XTAL参考(可精调)
- 完全集成的FSK调制解调器，具有可编程脉冲波形、数据速率和调制指数
- 数字基带(DBB)具备多种链路层功能，包括自动数据包处理报头和同步、CRC以及单独的Rx和Tx 128字节FIFO
- 串行和并行数字接口

2.4 GHz射频前端包含具有以下功能的完整收发器：

- IEEE 802.15.4芯片编码和解码
- 曼彻斯特编码
- 数据白化

2.4 GHz射频前端包含高度灵活的数字基带(调制、可配制性和可编程性方面)，以便支持蓝牙低功耗技术、802.15.4 OQPSK和DSSS，以及专有协议。支持从62.5 kbps至2 Mbps的可编程数据速率以及具有可编程脉冲波形和调制指数的FSK。

2.4 GHz射频前端还具有IEEE 802.15.4芯片编码和解码、曼彻斯特编码和数据白化功能。数据包处理包括：

- 自动插入报头和同步文字
- 自动数据包长度处理程序
- 基本地址检查
- 使用可编程CRC多项式，自动进行CRC计算和验证
- 多帧支持
- 2x 128字节FIFO

基带控制器和软件栈

RSL10的蓝牙基带控制器连接至射频前端。该控制器将配置RSL10的物理层，以用作蓝牙低功耗技术设备。它为用于射频测试的直接测试模式(DTM)层提供了接口和支持，并从蓝牙栈实现了部分链路层以及其他控制器层级的元件。该控制器专用于低级别逐位运算和数据包处理。

RSL10为蓝牙5认证产品，提供LE 2 Mbps支持和蓝牙低功耗技术早期版本的所有可选功能。

RSL10设备还支持用于以下功能的定制软件栈：

- 支持低延迟音频串流的定制音频协议
- 支持通过远程加密狗进行低功耗音频串流的定制音频协议

此外，还支持蓝牙和定制协议共存。例如，通过远程加密狗串流音频时，可能还会使用电话来控制使用标准蓝牙低功耗技术协议的音频设备。

软件栈，包括配置文件和应用程序，用于处理协议功能，将在Arm Cortex−M3处理器上执行。蓝牙IP在软硬件中分开实现，如图5所示。

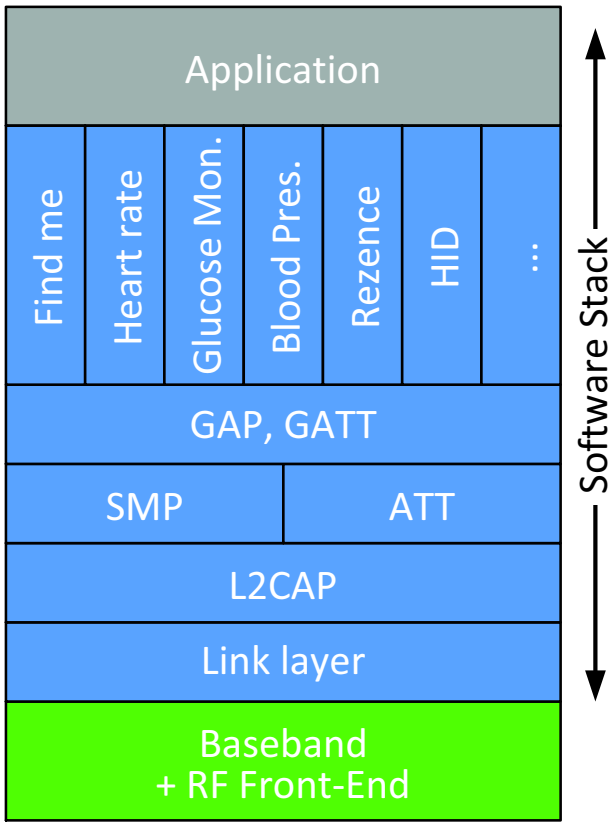


Figure 5. Bluetooth Protocol Implementation

以下是RSL10支持的蓝牙低功耗配置文件示例。更多信息以及所提供的配置文件完整列表，请下载RSL10开发工具套件。

- 找到我
- 接近
- 健康体温计
- 心率
- 时间
- 血压
- 血糖监测
- HID over GATT (HOG)
- 提醒通知
- 电话提醒状态
- 跑步速度
- 骑行速度
- 骑行功率
- 定位与导航
- Rezence (AirFuel™ Alliance定义的定制协议，支持无线电池充电)

Arm Cortex−M3处理器子系统

Arm Cortex−M3处理器子系统包含Arm Cortex−M3处理器，这是RSL10芯片的主处理器。此外，还包含蓝牙基带控制器，以及所有接口和其他周边设备。

Arm Cortex−M3处理器

Arm Cortex−M3处理器搭载先进的32位核心，以及嵌入式乘法器和ALU，用于处理典型的控制功能。软件开发可用C语言进行。

它的特点是具有低门数、低中断延迟，以及低成本调试功能。主要用于需要低功耗、快速中断响应的深层嵌入式应用。此处理器采用了Arm架构v7−M。对于电源管理，可在固件控制中将处理器设置为待机模式，在此模式下，处理器时钟将被禁用。但嵌套中断向量控制(NVIC)会继续运行，以在中断时启用现有待机模式。

LPDSP32

LPDSP32是由安森美半导体开发的32位DSP，可用C语言编程。LPDSP32是一款高效的双Harvard DSP，支持单(32位)和双精度(64位)算法。

LPDSP32的双MAC单元—加载存储架构经过专门优化，可支持音频处理工作。这种先进架构还提供了：

- 两个72位ALU，能够执行单双精度算法和逻辑运行
- 两个32位整数/分数乘法器
- 四个64位累加器，具有8位溢出(扩展位)

LPDSP32通常支持部署音频设备通信用例所需的音频编解码器。这包括(但不限于)支持以下各项的编解码器：

- 16 kHz采样率，产生7 kHz带宽信号(例如SBC、G.722或mSBC编解码器)
- 24 kHz采样率，产生11 kHz带宽信号(例如采用OPUS标准的G.722、CELT 编解码器)

与Arm Cortex−M3处理器的通信通过中断和共享存储器完成。软件开发使用C语言进行，可根据Synopsys的要求提供开发工具。

接口

RSL10包含：

- 两个独立的SPI接口，可在主模式和从模式中配置。
- 一个完全可配置的PCM接口
- 一个标准的通用I^2C接口
- 一个标准的通用UART接口
- 两个PWM (脉冲宽度调制)驱动器，可在指定频率下产生单点输出信号

- 一个双通道数字麦克风(DMIC)输入
- 一个输出驱动器(OD)，用于直接连接高阻抗扬声器。
- 一个用于Arm Cortex−M3处理器的 SWJ−DP 接口
- 一个用于LPDSP32的JTAG接口

RSL10还有16个DIO焊盘(数字输入/输出)，均可指定给上述任何接口，或用作通用DIO。

外设

RSL10包含：

- 四个通用计时器
- 一个DMA (直接存储器访问)控制器，用于在周边设备和存储器间传送数据，不会对核心产生任何干扰
- 一个闪存拷贝器，用于初始化SRAM存储器，并且可与CRC模块一起用于验证闪存内容
- 一个模拟到数字转换器(ADC)，通过Arm Cortex−M3处理器访问。ADC可读取4个外部值(DIO[0]−DIO[3])、AOUT、VDDC、VBAT/2和ADC补偿值。
- 两个标准的循环冗余码(CRC)模块，用于确保用户应用程序代码和数据的完整性
- 一个异步采样率转换器(ASRC)模块和音频信宿时钟模块，用于提供一种在无线电链路和主机设备之间同步音频采样率的方式。
- 一个看门狗计时器，用于检测RSL10故障并进行恢复。
- 四个32位自主活动计数器。这些计数器可帮助分析系统运行时间，以及应用中使用了多少Arm Cortex−M3处理器、LPDSP32和闪存。这些信息对于评估和优化应用功耗十分有用。
- 一个IP保护系统，用于确保闪存内容无法被第三方复制。可用于在RSL10启动后，防止从外部访问RSL10的任何核心或存储器。
- 用于各处理器的程序存储器循环缓存，可降低RSL10功耗。通过缓冲在这些循环中读取的程序文字，可减少闪存和RAM存储器的访问次数。

RSL10存储器结构

表10列出了RSL10所连接的存储器结构，以及各存储器结构的大小和宽度。

Table 10. RSL10 MEMORY STRUCTURES

Memory type	Data Width	Memory Size	Accessed by
Program memory (ROM)	32	4 kB	Arm Cortex−M3 processor
Program memory (RAM)	32	4 instances of 8 kB	Arm Cortex−M3 processor
Program memory (RAM)	40	4 instances of 10 kB	LPDSP32 / Arm Cortex−M3 processor
Data memory (RAM)	32	1 instances of 8 kB	Arm Cortex−M3 processor
Data memory (RAM)	32	2 instances of 8 kB	Arm Cortex−M3 processor / LPDSP32
Data memory (RAM)	32	6 instances of 8 kB	LPDSP32 / Arm Cortex−M3 processor
Data memory (RAM)	32	2 instances of 8 kB	Baseband / Arm Cortex−M3 processor
Flash	32	384 kB	Arm Cortex−M3 processor / Flash copier

芯片标识

使用系统标识来识别不同的系统组件。对于RSL10芯片，密钥标识符元素和值如下所示：

- 芯片系列：0x09
- 芯片版本：0x01
- 芯片修订版本：0x01

静电放电(ESD)敏感器件

警告：ESD敏感器件。高能量静电放电可能对器件造成永久性损坏。建议在处理、封装和测试时采用适当的ESD预防措施，避免性能下降或功能丧失。

焊料信息

RSL10 QFN封装采用所有RoHS标准符合要求的物质，并应相应回流焊接。

此器件是湿度敏感度等级类MSL3，必须相应地存储和处理。重新回流焊接按IPC/JEDEC标准J−STD−020C，及联合行业标准：回流敏感度分类非密封固态表面贴装器件。手工焊接不推荐用于这器件。

更多信息，请访问www.onsemi.cn输入SOLDERRM/D查阅。

开发工具

RSL10提供全套综合工具支持您的设计，包括：

- 一个易于使用的开发板
- 软件开发套件(SDK)包括一个基于Oxygen Eclipse的开发环境、蓝牙协议栈、示例代码、程序库和文件

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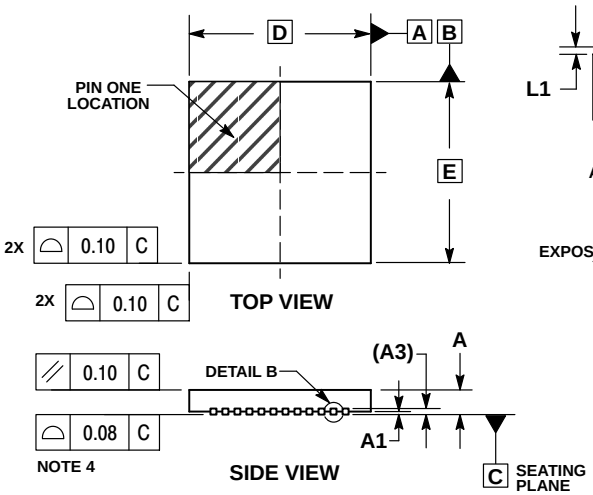
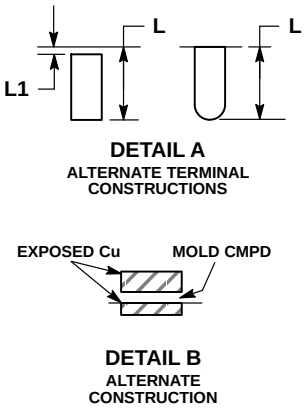
PACKAGE DIMENSIONS

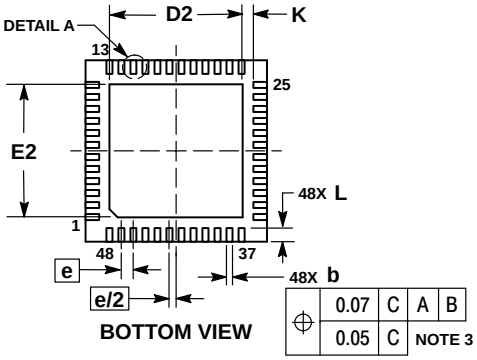
QFN48 6x6, 0.4P
CASE 485BA
ISSUE A



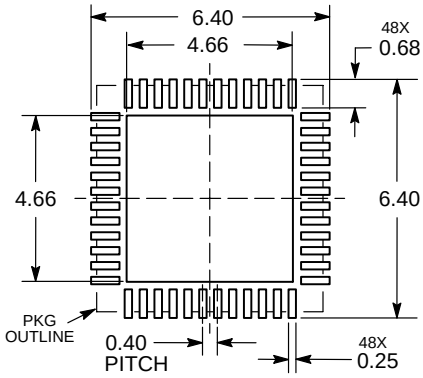


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.15	0.25
D	6.00 BSC	
D2	4.40	4.60
E	6.00 BSC	
E2	4.40	4.60
e	0.40 BSC	
K	0.20 MIN	
L	0.30	0.50
L1	0.00	0.15



SOLDERING FOOTPRINT*

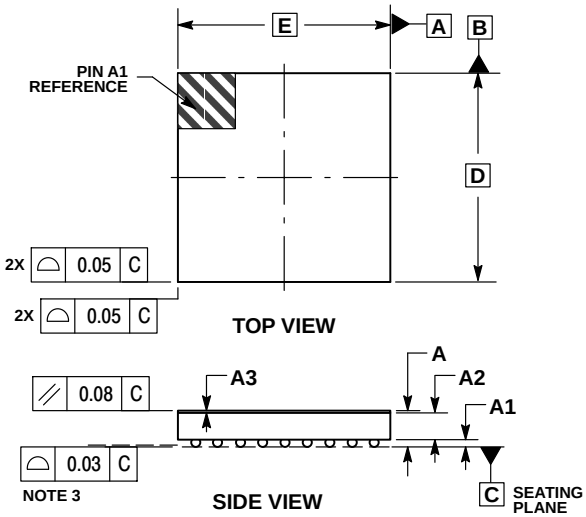


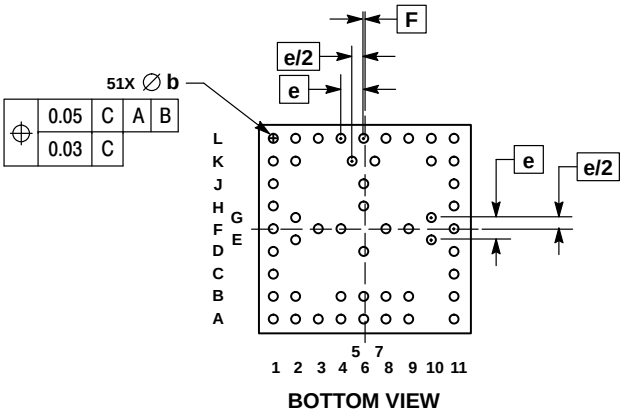
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

WLCSP51, 2.364x2.325
CASE 567MT
ISSUE A

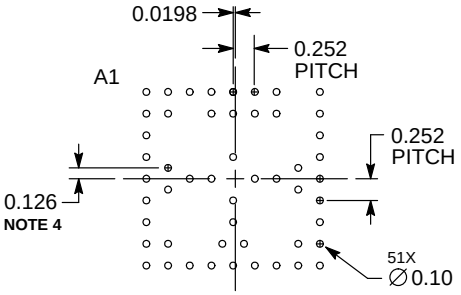




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.
4. PACKAGE CENTER AND FOOTPRINT CENTER ARE NOT COINCIDENT. REFER TO DIMENSION F FOR OFFSETS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.319	0.350	0.381
A1	0.060	0.075	0.090
A2	0.237	0.250	0.263
A3	0.022	0.025	0.028
b	0.09	0.10	0.12
D	2.325 BSC		
E	2.364 BSC		
e	0.252 BSC		
F	0.0198 BSC		

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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