DATA SHEET

TDA8007B
Multiprotocol smart card interface

Objective specification
File under Integrated Circuits, IC02

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Philips
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Multiprotocol smart card interface TDA8007B

FEATURES

- 8-bit parallel interface for control and communication, compatible with multiplexed or non-multiplexed memory access
- Specific ISO UART with parallel access on I/O for automatic convention processing, variable baud rate through frequency or division ratio programming, error management at character level for T = 0, extra guard time register
- 1 to 8 characters FIFO in reception mode
- Parity error counter in reception mode
- Dual V_{CC} generation (5 V ±5% or 3 V ±5%, 65 mA (max.) with controlled rise and fall times)
- Dual smart card clock generation (up to 10 MHz), with two times synchronous frequency doubling
- Cards clock STOP HIGH, clock STOP LOW or 1.25 MHz (from internal oscillator) for cards power-down mode
- Automatic activation and deactivation sequence through an independent sequencer
- Supports asynchronous protocols T = 0 and T = 1, in accordance with ISO 7816 and EMV
- Versatile 24-bit timeout counter for ATR (Answer To Reset) and waiting times processing
- 22 ETU counter for Block Guard Time
- Supports synchronous cards
- Short-circuit current limitations
- Special circuit for killing spikes during power-on/-off
- Supply supervisor for power-on/-off reset
- Step-up converter (supply voltage from 2.5 to 6 V), doubler, tripler or follower according to V_{CC} and V_{DD}
- Additional I/O pin, allowing use of the ISO UART for another analog interface (I/OAUX)
- Additional interrupt pin, allowing detection of level toggling on an external signal (INTAUX)
- Fast and efficient swapping between card 1, card 2 and a third card whose I/O is tied to IOAUX, due to separate buffering of parameters for each card
- Chip select input, allowing use of several devices in parallel and memory space paging
- Enhanced ESD protections on card side (6 kV min.)
- Software library for easy integration within the application
- Power-down mode, reducing current consumption during periods of non-activity.

APPLICATIONS

- Multiple smart card readers for multiprotocol applications (EMV banking, Digital pay TV, Access control etc.).

GENERAL DESCRIPTION

The TDA8007B is a low cost card interface for dual smart card readers. Controlled through a parallel bus, it takes care of all ISO 7816, EMV and GSM11-11 requirements. It may be interfaced to the P0/P2 ports of an 80C51 family microcontroller, and be addressed as a memory through MOVX instructions. It may also be addressed on a non-multiplexed 8-bit data bus, by means of register addresses AD0, AD1, AD2 and AD3. The integrated ISO UART and the timeout counters allow easy use, even at high baud rates with no real time constraints. Due to its chip select and external I/O and INT features, it greatly simplifies the realization of any number of types of card readers. It gives the cards and the mode a very high level of security, due to its special hardware against ESD, short circuits, power failure, etc. Its integrated step-up converter allows operation within a supply voltage range of 2.5 to 6 V.

A software library has been developed, taking care of all actions required for T = 0, T = 1 and synchronous protocols, see Application Reports.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		2.5	–	6	V
$I_{DD(pd)}$	supply current in inactive mode (power-down)	V_{DD} = 3.3 V; cards inactive; XTAL oscillator stopped	–	–	350	µA
		V_{DD} = 3.3 V; cards active at V_{CC} = 5 V; CLK stopped; XTAL oscillator stopped	–	–	3	mA
$I_{DD(sm)}$	supply current in sleep mode	cards powered at 5 V but clock stopped	–	–	5	mA
$I_{DD(om)}$	supply current in operating mode	V_{DD} = 3.3 V; XTAL = 20 MHz V_{CC1} = V_{CC2} = 5 V; I_{CC1} = I_{CC2} = 80 mA	–	–	300	mA
V_{CC}	card supply voltage	including static loads (5 V card)	4.75	5.0	5.25	V
		with 40 nAs dynamic loads on 200 nF capacitor (5 V card)	4.6		5.4	V
		including static loads (3 V card)	2.80		3.20	V
		with 40 nAs dynamic loads on 200 nF capacitor (3 V card)	2.75		3.25	V
I_{CC}	card supply current	operating	–	–	65	mA
		overload detection	–	80	–	mA
I_{CC1} + I_{CC2}	sum of both cards' currents		–	–	80	mA
SR	slew rate on V_{CC} (rise and fall)	maximum load capacitor 300 nF	0.10	0.16	0.22	V/µs
T_{deact}	deactivation cycle time		–	–	100	µs
T_{act}	activation cycle time		–	–	225	µs
f_{xtal}	crystal frequency		4	–	25	MHz
f_{op}	operating frequency	external frequency applied on pin XTAL1	0	–	25	MHz
T_{amb}	ambient temperature		–25	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8007BHL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4mm	SOT313-2

BLOCK DIAGRAM

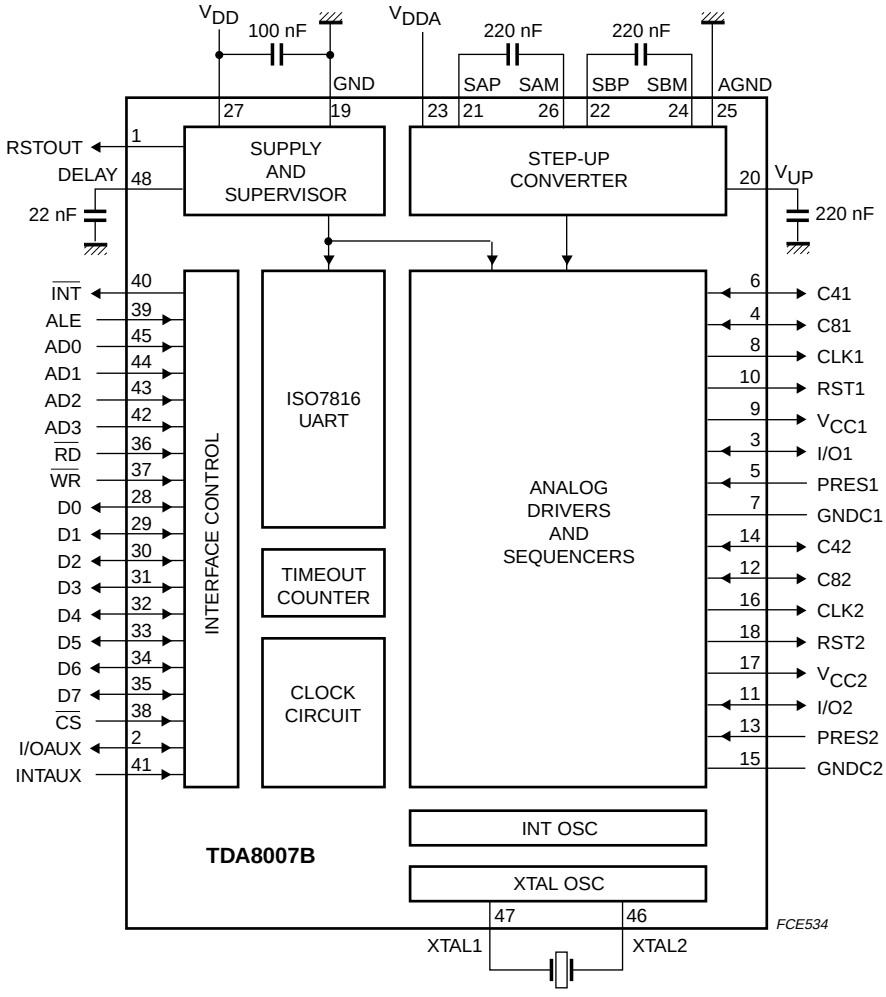


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
RSTOUT	1	open-drain output for resetting external ICs
I/OAUX	2	input or output for an I/O line to an auxiliary smart card interface
I/O1	3	data line to/from card 1 (ISO C7 contact)
C81	4	auxiliary I/O for ISO C8 contact (synchronous cards for instance) for card 1
PRES1	5	card 1 presence contact input (active HIGH or LOW by mask option)
C41	6	auxiliary I/O for ISO C4 contact (synchronous cards for instance) for card 1
GNDC1	7	ground for card 1
CLK1	8	clock output to card 1 (ISO C3 contact)
V_{CC1}	9	card 1 supply output voltage (ISO C1 contact)
RST1	10	card 1 reset output (ISO C2 contact)
I/O2	11	data line to/from card 2 (ISO C7 contact)
C82	12	auxiliary I/O for ISO C8 contact (synchronous cards for instance) for card 2
PRES2	13	card 2 presence contact input (active HIGH or LOW by mask option)
C42	14	auxiliary I/O for ISO C4 contact (synchronous cards for instance) for card 2
GNDC2	15	ground for card 2
CLK2	16	clock output to card 2 (ISO C3 contact)
V_{CC2}	17	card 2 supply output voltage (ISO C1 contact)
RST2	18	card 2 reset output (ISO C2 contact)
GND	19	ground
V_{UP}	20	output voltage of the step-up converter
SAP	21	contact 1 for the step-up converter (connect a low ESR 220 nF capacitor between pins SAP and SAM)
SBP	22	contact 3 for the step-up converter (connect a low ESR 220 nF capacitor between pins SBP and SBM)
V_{DDA}	23	analog positive supply voltage for the step-up converter
SBM	24	contact 4 for the step-up converter (connect a low ESR 220 nF capacitor between pins SBP and SBM)
AGND	25	ground connection for the step-up converter
SAM	26	contact 2 for the step-up converter (connect a low ESR 220 nF capacitor between pins SAP and SAM)
V_{DD}	27	positive supply voltage
D0	28	data 0 or address 0
D1	29	data 1 input/output or address 1 input
D2	30	data 2 input/output or address 2 input
D3	31	data 3 input/output or address 3 input
D4	32	data 4 input/output or address 4 input
D5	33	data 5 input/output or address 5 input
D6	34	data 6 input/output or address 6 input
D7	35	data 7 input/output or address 7 input
$\overline{RD}$	36	read selection signal input (read or write in non-multiplexed configuration) (active LOW)

SYMBOL	PIN	DESCRIPTION
$\overline{WR}$	37	write selection signal input (enable in the event of non-multiplexed configuration) (active LOW)
$\overline{CS}$	38	chip select input (active HIGH or LOW)
ALE	39	address latch enable in the event of multiplexed configuration (connect to V_{DD} in non-multiplexed configuration)
$\overline{INT}$	40	interrupt output (active LOW)
INTAUX	41	auxiliary interrupt input
AD3	42	register selection address 3 input
AD2	43	register selection address 2 input
AD1	44	register selection address 1 input
AD0	45	register selection address 0 input
XTAL2	46	connection pin for an external crystal
XTAL1	47	connection pin for an external crystal, or input for an external clock signal
DELAY	48	connection pin for an external delay capacitor

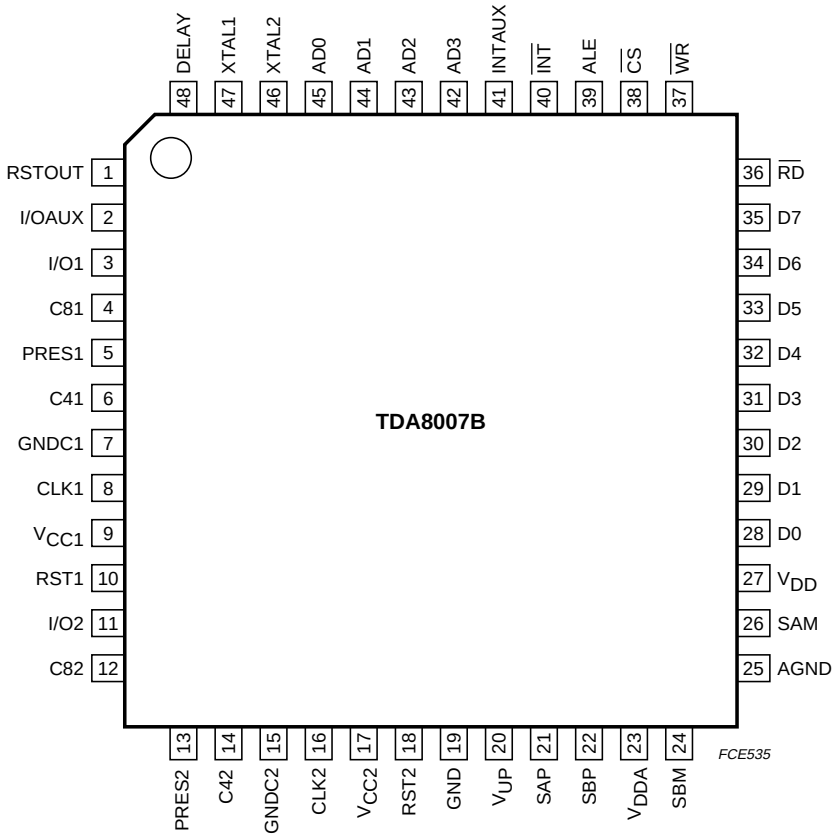
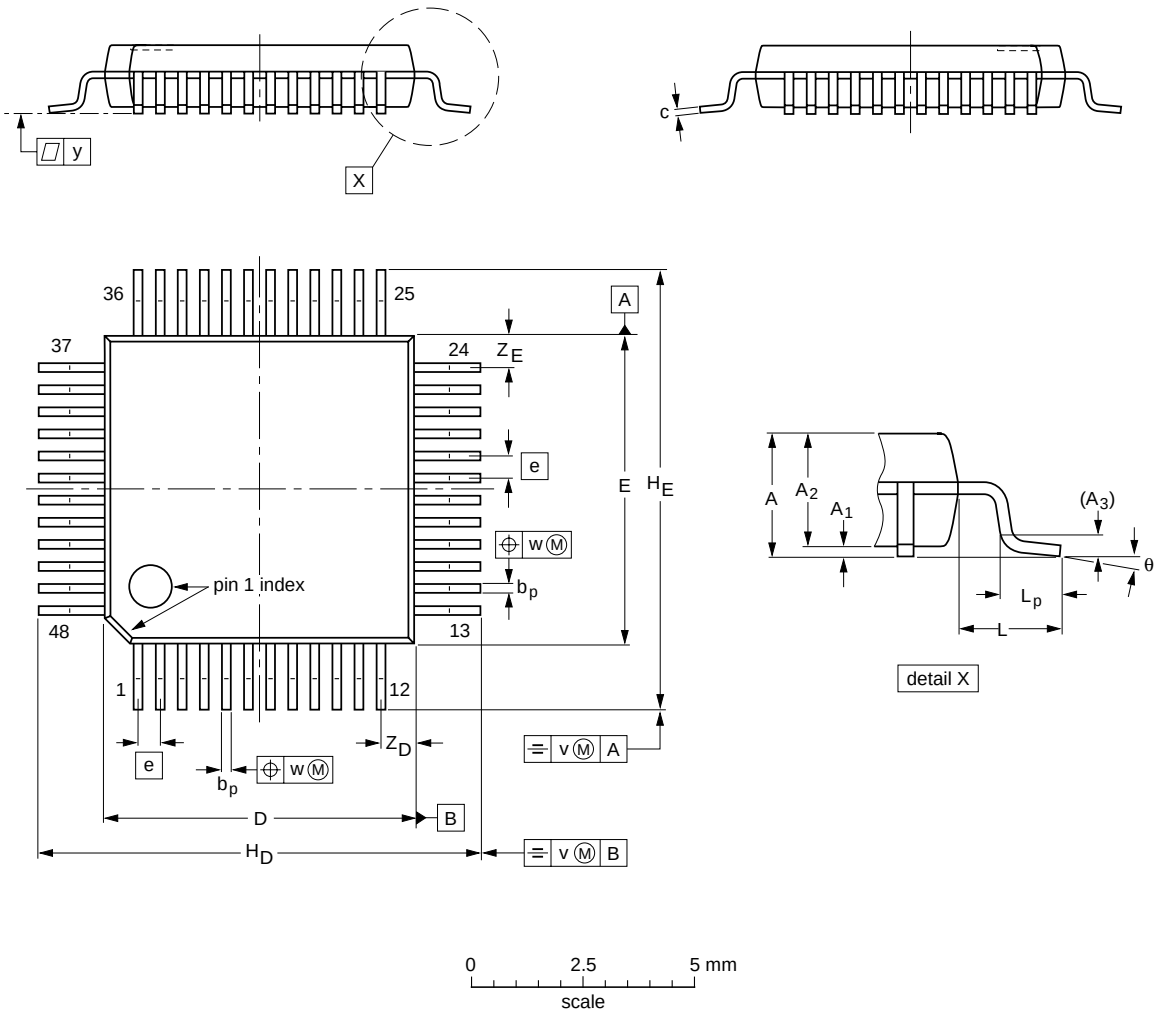


Fig.2 Pin configuration.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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