



# SGM2023

## Quad, Low Power, Low Dropout, 200mA, RF-Linear Regulators

### GENERAL DESCRIPTION

The SGM2023 is a quad, low-power, low-dropout, CMOS linear voltage regulator that operates from 2.5V to 5.5V input and delivers up to 200mA continuous current at each channel. An ultra low ground current (350 $\mu$ A at 0mA output current) makes this part attractive for battery operated power systems.

The SGM2023 also offers low dropout voltage (220mV at 200mA output) to prolong battery life in portable electronics. Systems requiring a quiet voltage source, such as RF applications, will benefit from the SGM2023 series' ultra low output noise (30 $\mu$ V<sub>RMS</sub>) and high PSRR. An external noise bypass capacitor connected to the device's BP pin can further reduce the noise level.

Other features include a 10nA logic-controlled shutdown mode, output current limit and thermal shut-down protection.

SGM2023 is available in Pb-free TQFN-16 (3mm $\times$ 3mm) package. It operates over an ambient temperature range of -40°C to +85°C.

### FEATURES

- **Low Output Noise: 30 $\mu$ V<sub>RMS</sub> TYP (10Hz to 100kHz)**
- **Low Dropout Voltage:  
220mV at 200mA Output Load Current**
- **Low 350 $\mu$ A No-Load Supply Current**
- **High PSRR: 70dB at 1kHz**
- **Thermal-Overload Protection**
- **Output Current Limit**
- **10nA Logic Controlled Shutdown**
- **-40°C to +85°C Operating Temperature Range**
- **Available in Pb-Free TQFN-16 Package**

### APPLICATIONS

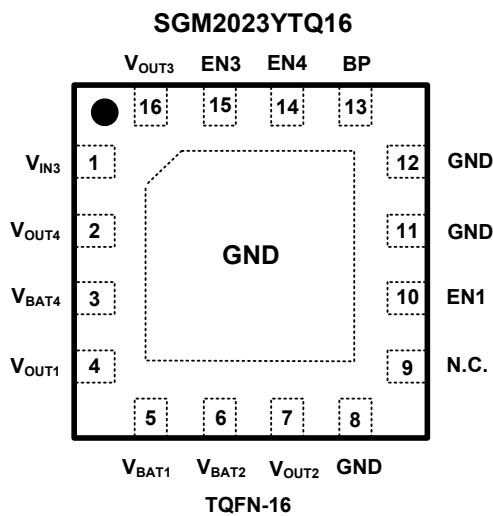
Cellular Telephones  
Cordless Telephones  
PHS Telephones  
PCMCIA Cards  
Modems  
MP3 Player  
Hand-Held Instruments  
Palmtop Computers  
Electronic Planners  
Portable/Battery-Powered Equipment



**PACKAGE/ORDERING INFORMATION**

MODEL	PIN-PACKAGE	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM2023	TQFN-16 (3mm x 3mm)	-40°C to +85°C	SGM2023YTQ16/TR	2023TQ	Tape and Reel, 3000

**PIN CONFIGURATION (TOP VIEW)**



**ABSOLUTE MAXIMUM RATINGS**

IN to GND.....	-0.3 V to 6V
Output Short-Circuit Duration .....	Infinite
EN to GND.....	-0.3V to $V_{IN}$
OUT, BP to GND.....	-0.3V to ( $V_{IN} + 0.3V$ )
Operating Temperature.....	-40°C to +85°C
Junction Temperature.....	150°C
Storage Temperature.....	-65 °C to +150°C
Lead Temperature (soldering, 10s).....	260°C
ESD Susceptibility	
HBM.....	4000V
MM.....	400V

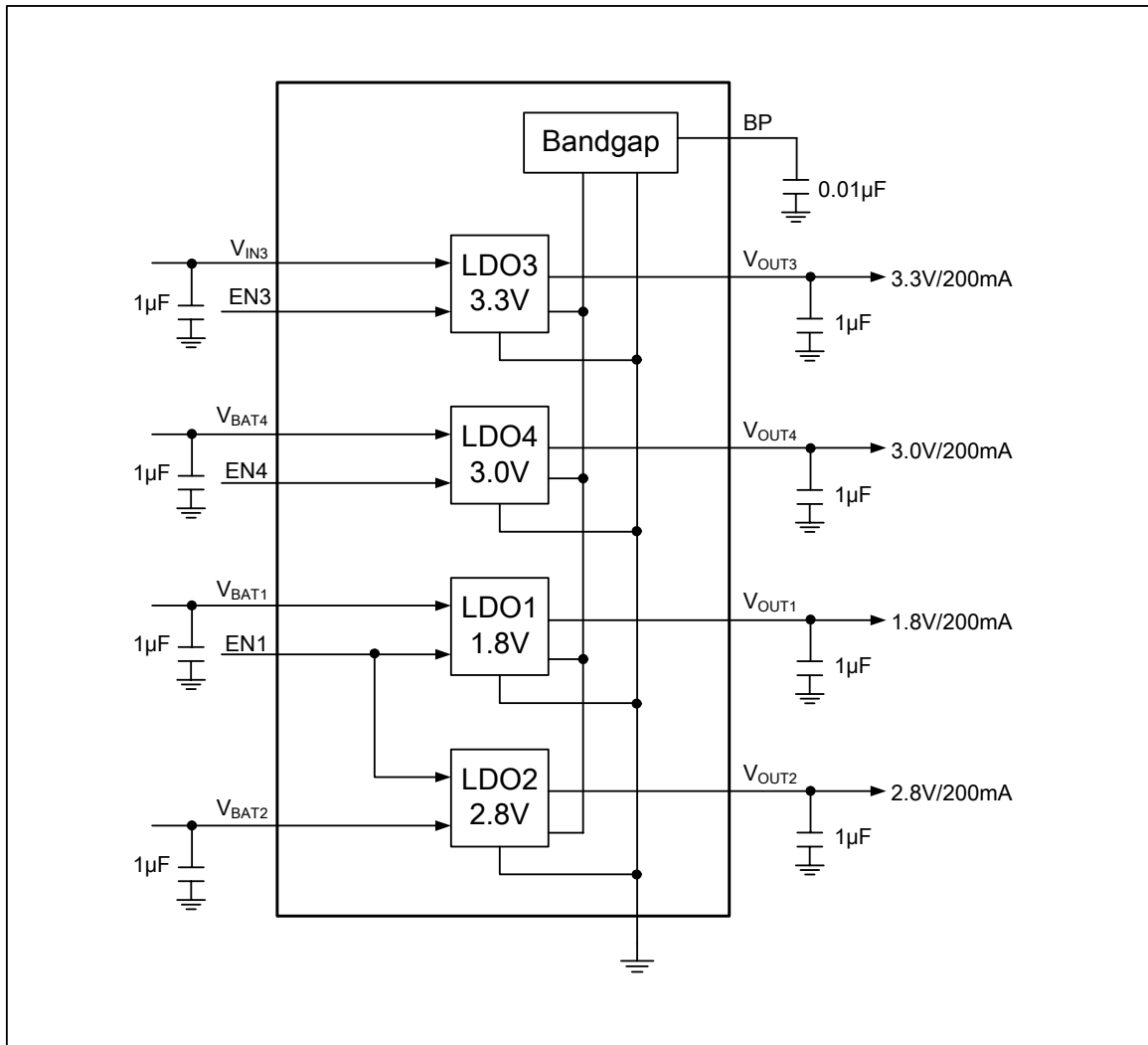
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAUTION**

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTION DIAGRAM



## PIN DESCRIPTION

PIN	NAME	FUNCTION
1	$V_{IN3}$	Regulator Input. Bypass with a 1 $\mu$ F capacitor to GND. In application $V_{IN3}$ is always powered by $V_{BUS}$ of USB interface.
5,6,3	$V_{BAT1,2,4}$	Regulator Input. Bypass with a 1 $\mu$ F capacitor to GND. Connected together externally. In application $V_{BAT1,2,4}$ are always connected to battery directly.
8,11,12	GND	Ground. All GND pins must be connected together externally.
10,15,14	EN1,3,4	Shutdown Input. A logic low reduces the supply current to 10nA. Connect to $V_{IN3}$ or $V_{BAT1,4}$ for normal operation.
13	BP	Reference-Noise Bypass (fixed voltage version only). Bypass with a low-leakage 0.01 $\mu$ F ceramic capacitor for reduced noise at the output.
4	$V_{OUT1}$	LDO-1 Regulator Output. Sources up to 200mA. Bypass with a 1 $\mu$ F Capacitor to GND for $V_{OUT1} = 1.8V/200mA$ .
7	$V_{OUT2}$	LDO-2 Regulator Output. Sources up to 200mA. Bypass with a 1 $\mu$ F Capacitor to GND for $V_{OUT2} = 2.8V/200mA$ .
16	$V_{OUT3}$	LDO-3 Regulator Output. Sources up to 200mA. Bypass with a 1 $\mu$ F Capacitor to GND for $V_{OUT3} = 3.3V/200mA$ .
2	$V_{OUT4}$	LDO-4 Regulator Output. Sources up to 200mA. Bypass with a 1 $\mu$ F Capacitor to GND for $V_{OUT4} = 3.0V/200mA$ .
9	N.C.	Not Internally Connected.

**ELECTRICAL CHARACTERISTICS**(V<sub>IN</sub> = V<sub>OUT(NOMINAL)</sub> + 0.5V or 2.5V<sup>(1)</sup>, T<sub>A</sub> = -40°C to +85°C. Typical values are at T<sub>A</sub> = +25°C, unless otherwise noted.)

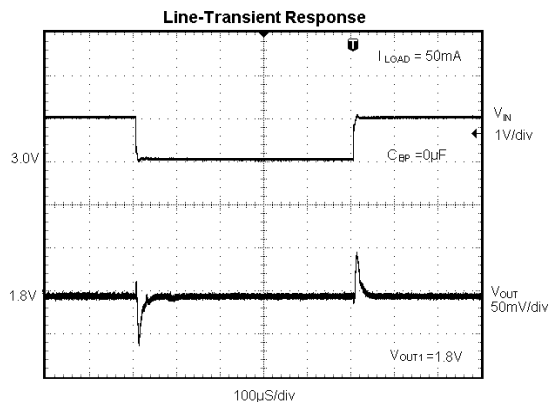
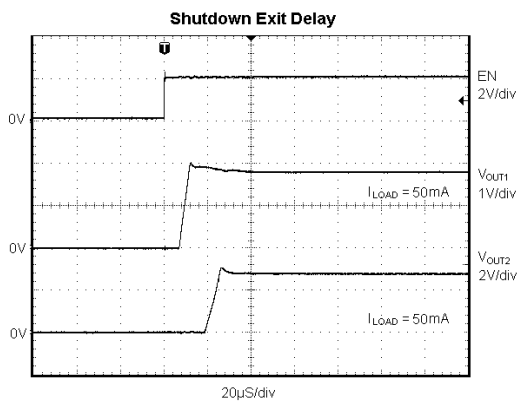
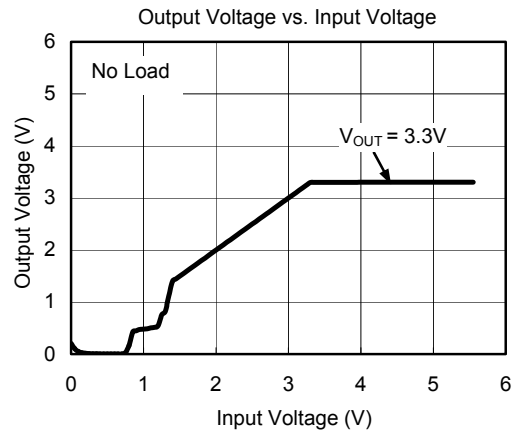
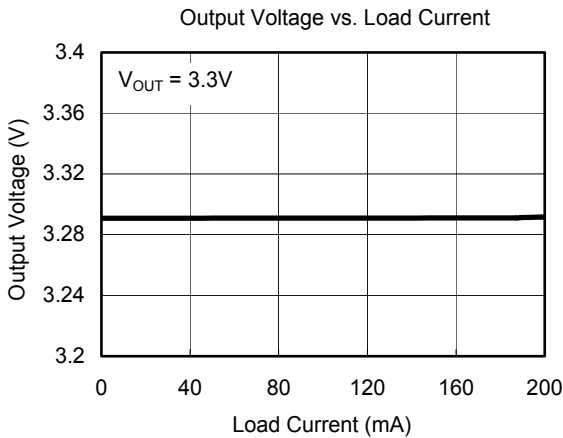
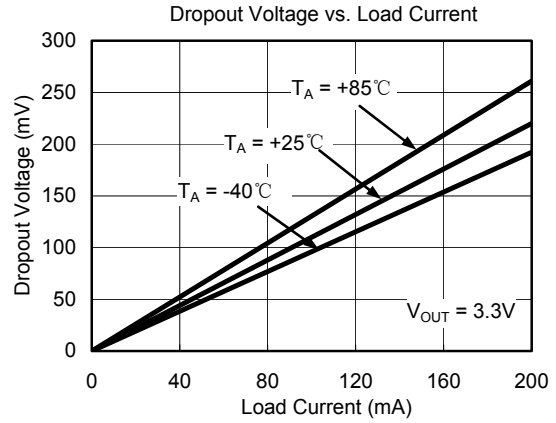
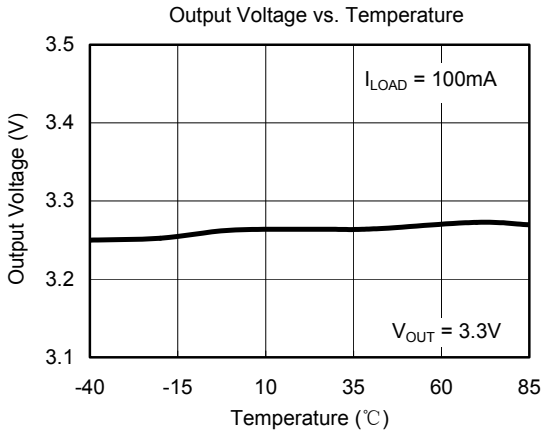
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Input Voltage	V <sub>IN</sub>		2.5		5.5	V	
Output Voltage Accuracy <sup>(1)</sup>		I <sub>OUT</sub> = 0.1mA, T <sub>A</sub> = +25°C	-2		+2	%	
Maximum Output Current			200			mA	
Current Limit	I <sub>LIM</sub>		210	350		mA	
Ground Pin Current	I <sub>Q</sub>	No load, EN = 2V		350	550	μA	
Dropout Voltage <sup>(2)</sup>		I <sub>OUT</sub> = 1mA		1		mV	
		I <sub>OUT</sub> = 200mA		220	330		
Line Regulation <sup>(1)</sup>	ΔV <sub>LNR</sub>	V <sub>IN</sub> = 2.5V or (V <sub>OUT</sub> + 0.5V) to 5.5V, I <sub>OUT</sub> = 1mA		0.01	0.15	%/V	
Load Regulation	ΔV <sub>LDR</sub>	I <sub>OUT</sub> = 0.1mA to 200mA, C <sub>OUT</sub> = 1μF		0.0005	0.004	%/mA	
Output Voltage Noise	e <sub>n</sub>	f = 10Hz to 100kHz, C <sub>BP</sub> = 0.1μF, C <sub>OUT</sub> = 10μF		30		μV <sub>RMS</sub>	
Power Supply Rejection Rate	PSRR	C <sub>BP</sub> = 0.1μF, I <sub>LOAD</sub> = 50mA, C <sub>OUT</sub> = 1μF	f = 100Hz		72		dB
			f = 1kHz		70		dB
<b>SHUTDOWN</b>							
EN Input Threshold	V <sub>IH</sub>	V <sub>IN</sub> = 2.5V to 5.5V	1.5			V	
	V <sub>IL</sub>				0.4		
EN Input Bias Current	I <sub>B(SHDN)</sub>	EN = 0V and EN = 5.5V	T <sub>A</sub> = +25°C	0.01	1	μA	
			T <sub>A</sub> = +85°C	0.01	1		
Shutdown Supply Current	I <sub>Q(SHDN)</sub>	EN = 0.4V	T <sub>A</sub> = +25°C	0.01	1	μA	
			T <sub>A</sub> = +85°C	0.01	1		
Shutdown Exit Delay <sup>(3)</sup>		C <sub>BP</sub> = 0.01μF, C <sub>OUT</sub> = 1μF, No load	T <sub>A</sub> = +25°C	30		μs	
<b>THERMAL PROTECTION</b>							
Thermal Shutdown Temperature	T <sub>SHDN</sub>			160		°C	
Thermal Shutdown Hysteresis	ΔT <sub>SHDN</sub>			15		°C	

Specifications subject to changes without notice.

**Note 1:** V<sub>IN</sub> = V<sub>OUT(NOMINAL)</sub> + 0.5V or 2.5V, whichever is greater.**Note 2:** The dropout voltage is defined as V<sub>IN</sub> - V<sub>OUT</sub>, when V<sub>OUT</sub> is 100mV below the value of V<sub>OUT</sub> for V<sub>IN</sub> = V<sub>OUT</sub> + 0.5V. (Only applicable for V<sub>OUT</sub> = +2.5V to +3.3V.)**Note 3:** Time needed for V<sub>OUT</sub> to reach 95% of final value.

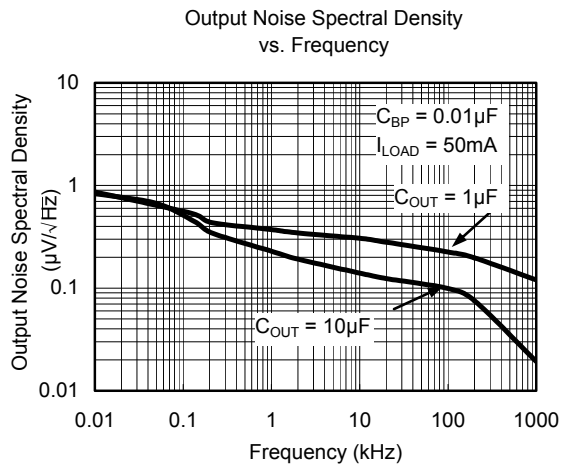
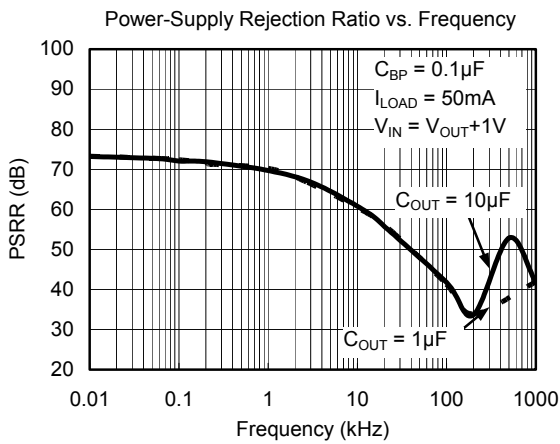
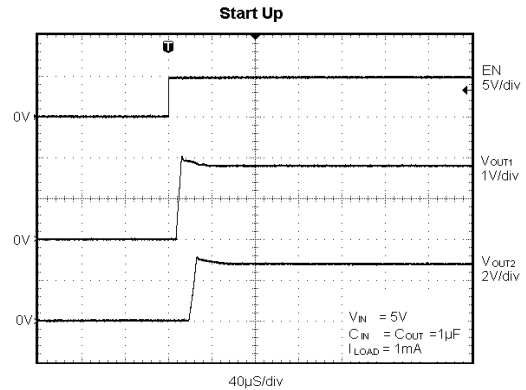
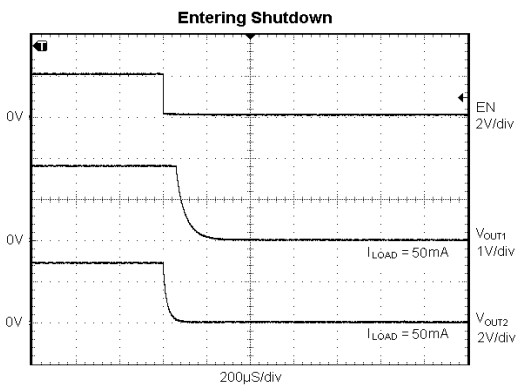
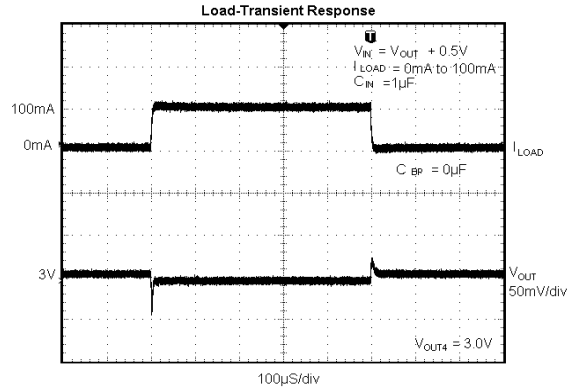
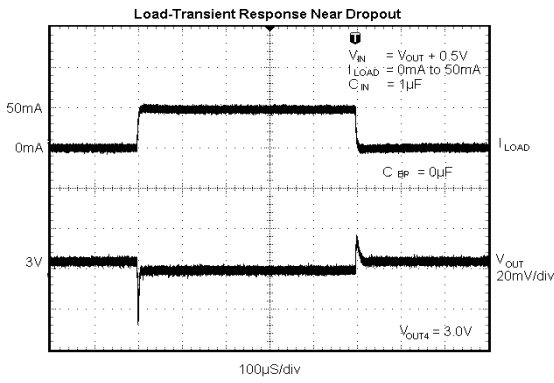
TYPICAL OPERATING CHARACTERISTICS

$V_{IN} = V_{OUT(NOMINAL)} + 0.5V$  or  $2.5V$  (whichever is greater),  $C_{IN} = 1\mu F$ ,  $C_{OUT} = 1\mu F$ ,  $C_{BP} = 0.01\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



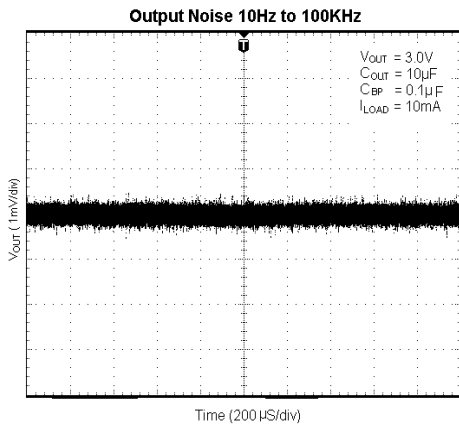
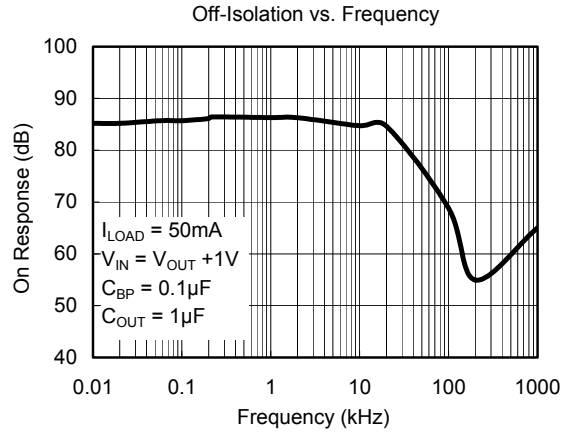
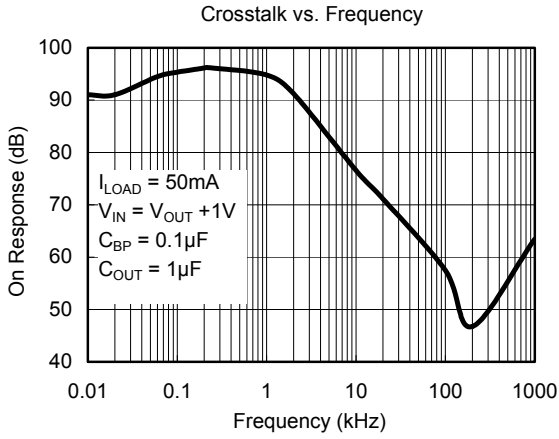
TYPICAL OPERATING CHARACTERISTICS

$V_{IN} = V_{OUT(NOMINAL)} + 0.5V$  or  $2.5V$  (whichever is greater),  $C_{IN} = 1\mu F$ ,  $C_{OUT} = 1\mu F$ ,  $C_{BP} = 0.01\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



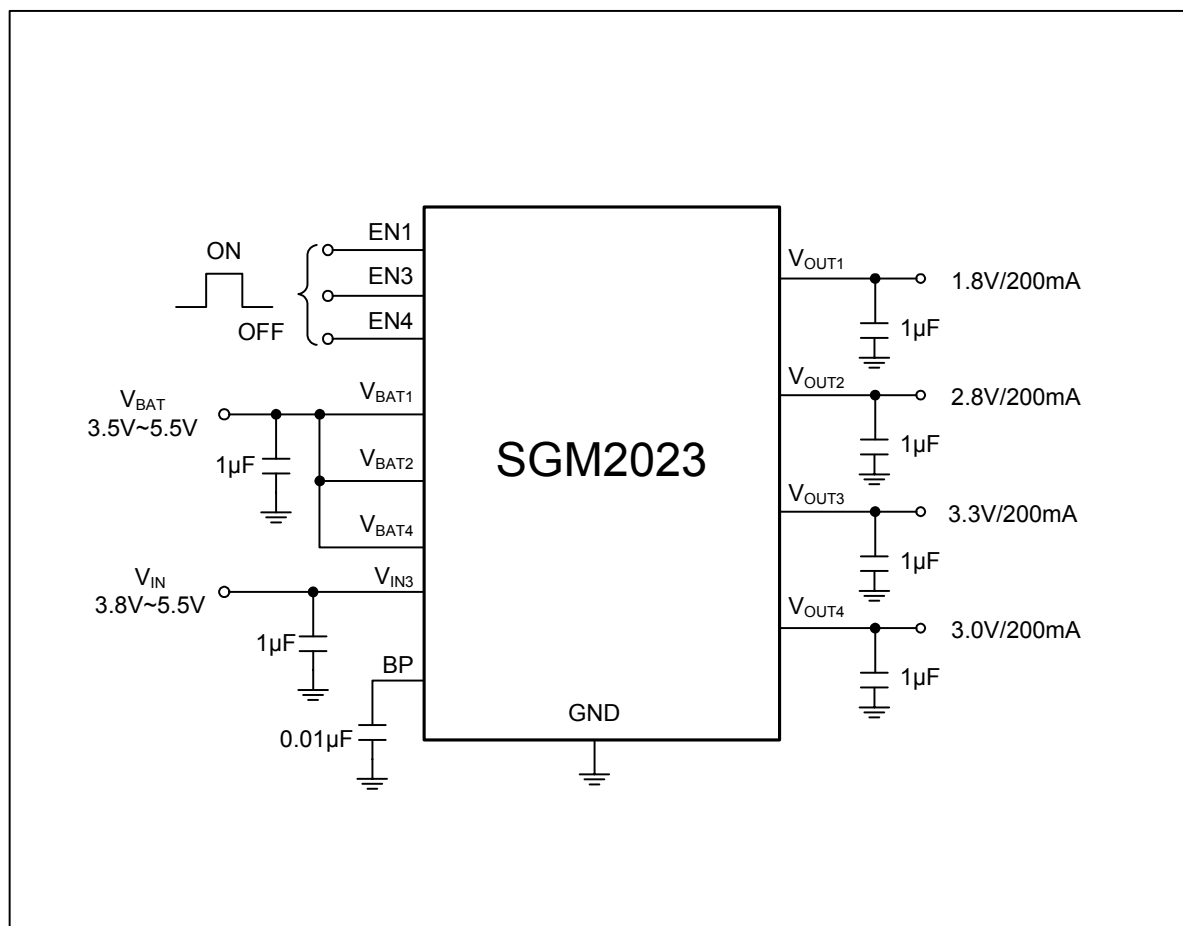
TYPICAL OPERATING CHARACTERISTICS

$V_{IN} = V_{OUT(NOMINAL)} + 0.5V$  or  $2.5V$  (whichever is greater),  $C_{IN} = 1\mu F$ ,  $C_{OUT} = 1\mu F$ ,  $C_{BP} = 0.01\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.





TYPICAL APPLICATION CIRCUIT

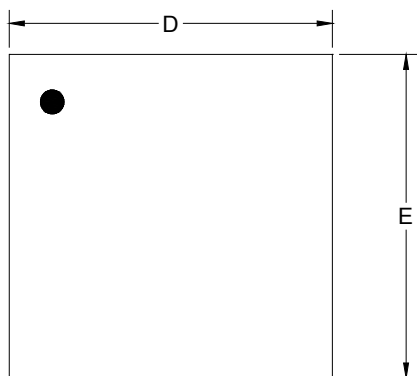


Note:

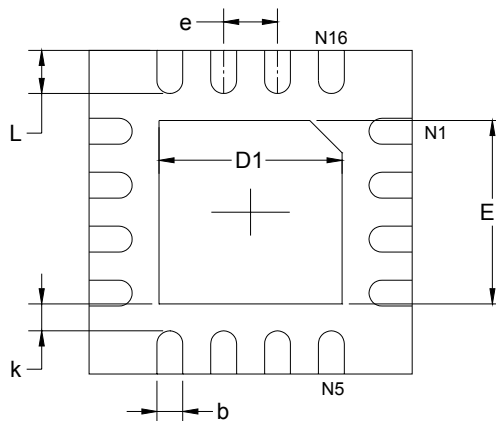
1.  $V_{BAT1}$ ,  $V_{BAT2}$  and  $V_{BAT4}$  should be connected together and input voltage should not be less than 2.5V.
2. Since channel2 enable signal is gained from channel1's output, only after channel1 starts up normally, channel2 starts to output 1.8V.
3. The input voltage of channel2 required to maintain voltage ranging from 3.3V to 5.5V.
4. To ensure stability, LDO's input and output terminals need to have a capacitor (no less than 1µF) respectively.
5. BP pin must be decoupled by a low-leakage 0.01µF ceramic capacitor in order to reduce output noise.

PACKAGE OUTLINE DIMENSIONS

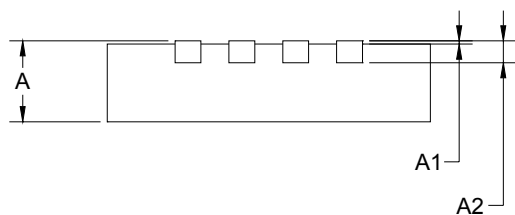
TQFN-16 (3mm × 3mm)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

09/2009 REV. A

SGMICRO is dedicated to provide high quality and high performance analog IC products to customers. All SGMICRO products meet the highest industry standards with strict and comprehensive test and quality control systems to achieve world-class consistency and reliability.

For information regarding SGMICRO Corporation and its products, see [www.sg-micro.com](http://www.sg-micro.com)