



SGM8531/2/4

500kHz, 18 μ A, Rail-to-Rail I/O

CMOS Operational Amplifiers

PRODUCT DESCRIPTION

The SGM8531(single), SGM8532(dual) and SGM8534 (quad) are rail-to-rail input and output voltage feedback amplifiers offering low cost. They have a wide input common-mode voltage range and output voltage swing, and take the minimum operating supply voltage down to 2.1V and the maximum recommended supply voltage is 5.5V. All are specified over the extended -40°C to +125°C temperature range.

The SGM8531/2/4 provide 500kHz bandwidth at a low current consumption of 18 μ A per amplifier. Very low input bias currents of 0.5pA enable the SGM8531/2/4 to be used for integrators, photodiode amplifiers, and piezoelectric sensors. Rail-to-Rail inputs and outputs are useful to designers buffering ASIC in single-supply systems.

Applications for these amplifiers include safety monitoring, portable equipment, battery and power supply control, and signal conditioning and interfacing for transducers in very low power systems.

The SGM8531 is available in the tiny SOT23-5 and SO-8 packages. The SGM8532 comes in the miniature SO-8 and MSOP-8 packages. The SGM8534 is offered in TSSOP-14 and SO-14 packages.

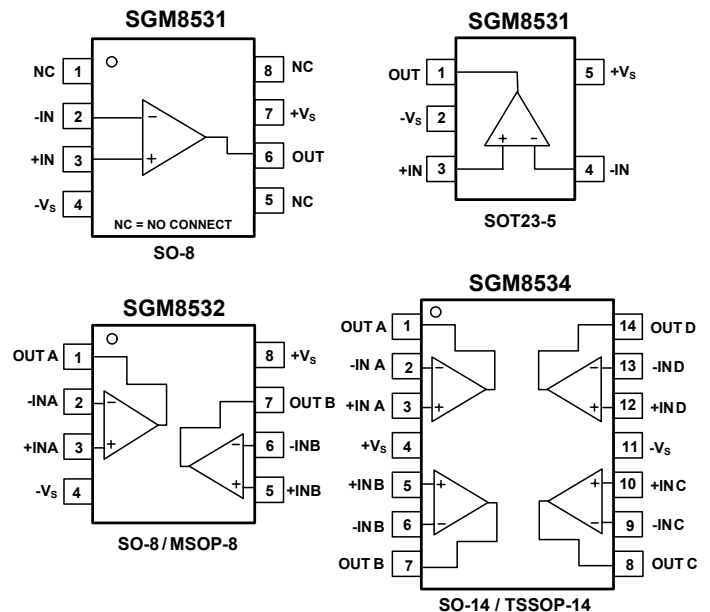
APPLICATIONS

- ASIC Input or Output Amplifier
- Sensor Interface
- Piezo Electric Transducer Amplifier
- Medical Instrumentation
- Mobile Communication
- Audio Output
- Portable Systems
- Smoke Detectors
- Mobile Telephone
- Notebook PC
- PCMCIA Cards
- Battery-Powered Equipment

FEATURES

- Low Cost
- Rail-to-Rail Input and Output
0.8mV Typical V_{OS}
- Unity Gain Stable
- Gain Bandwidth Product : 500kHz
- Very Low Input Bias Currents : 0.5pA
- Operates on 2.1V to 5.5V Supplies
- Input Voltage Range = -0.1V to +5.6V with $V_S = 5.5V$
- Low Supply Current: 18 μ A/Amplifier
- Small Packaging
SGM8531 Available in SO-8 and SOT23-5
SGM8532 Available in SO-8 and MSOP-8
SGM8534 Available in SO-14 and TSSOP-14

PIN CONFIGURATIONS (Top View)



PACKAGE/ORDERING INFORMATION

MODEL	ORDER NUMBER	PACKAGE DESCRIPTION	PACKAGE OPTION	MARKING INFORMATION
SGM8531	SGM8531XN5/TR	SOT23-5	Tape and Reel, 3000	8531
	SGM8531XS/TR	SO-8	Tape and Reel, 2500	SGM8531XS
SGM8532	SGM8532XS/TR	SO-8	Tape and Reel, 2500	SGM8532XS
	SGM8532XMS/TR	MSOP-8	Tape and Reel, 3000	SGM8532XMS
SGM8534	SGM8534XS14/TR	SO-14	Tape and Reel, 2500	SGM8534XS14
	SGM8534XTS14/TR	TSSOP-14	Tape and Reel, 3000	SGM8534XTS14

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V+ to V-	7.5V	SO-8, θ_{JA}	125°C/W
Common-Mode Input Voltage.....	(-V _S) - 0.5V to (+V _S) +0.5V	MSOP-8, θ_{JA}	216°C/W
Storage Temperature Range.....	-65°C to +150°C	Lead Temperature Range (Soldering 10 sec).....	260°C
Junction Temperature	160°C	ESD Susceptibility	
Operating Temperature Range	-55°C to +150°C	HBM.....	4000V
Package Thermal Resistance @ T _A = 25°C		MM.....	400V
SOT23-5, θ_{JA}	190°C/W		

NOTES:

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

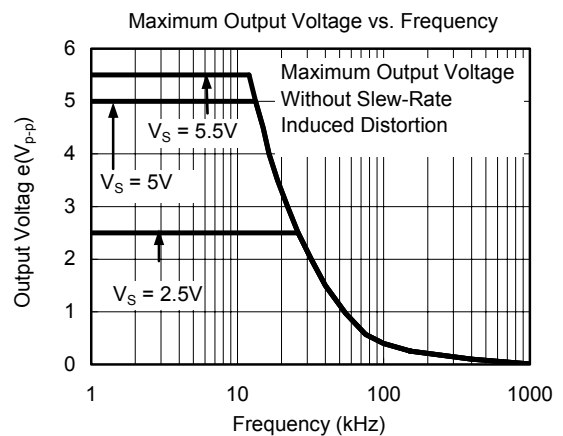
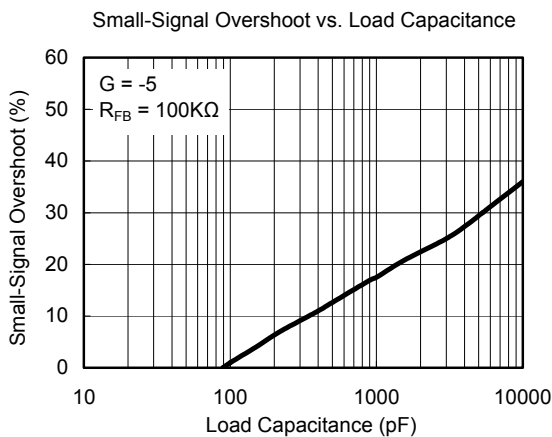
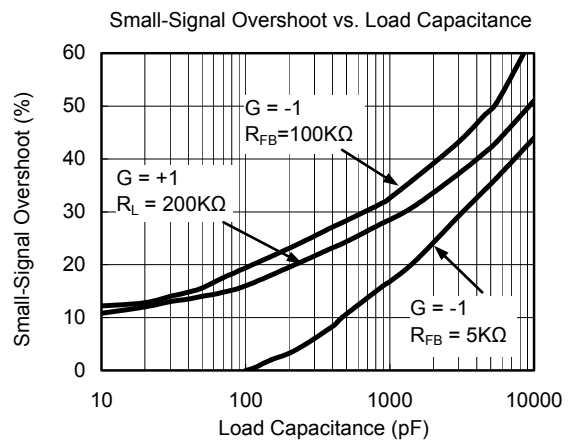
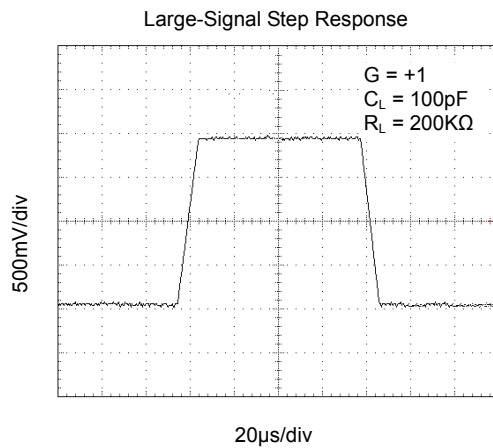
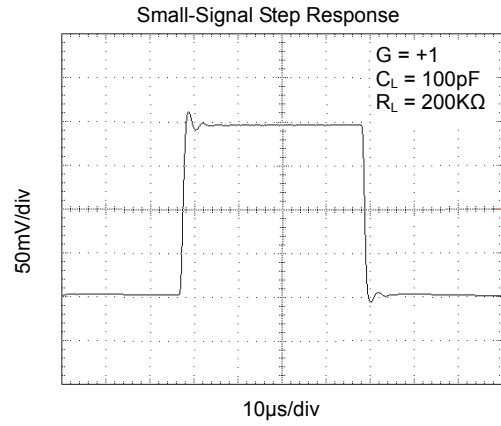
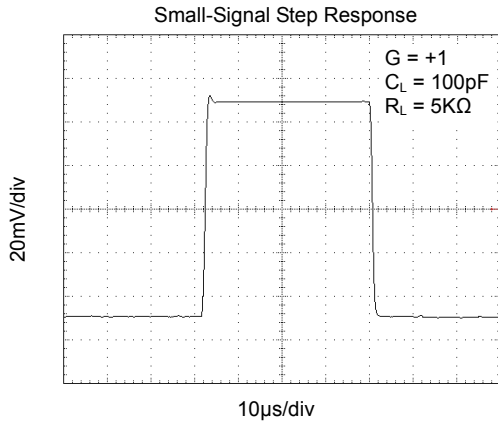
ELECTRICAL CHARACTERISTICS: $V_S = +5V$ (At $R_L = 200K\Omega$ connected to $V_S/2$ and $V_{OUT} = V_S/2$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	SGM8531/2/4							
			TYP	MIN/MAX OVER TEMPERATURE					UNITS	MIN/MAX
			+25°C	+25°C	0°C to +70°C	-40°C to +85°C	-40°C to +125°C			
INPUT CHARACTERISTICS										
Input Offset Voltage	V_{OS}		± 0.8	± 3.5	± 3.7	± 4.1	± 5.4	mV	MAX	
Input Bias Current	I_B		0.5					pA	TYP	
Input Offset Current	I_{OS}		0.5					pA	TYP	
Common-Mode Voltage Range	V_{CM}	$V_S = 5.5V$	-0.1 to +5.6					V	TYP	
Common-Mode Rejection Ratio	CMRR	$V_S = 5.5V, V_{CM} = -0.1V$ to 4V	92	72	72	71	71	dB	MIN	
		$V_S = 5.5V, V_{CM} = -0.1V$ to 5.6V	83	63	62	61	61	dB	MIN	
Open-Loop Voltage Gain	A_{OL}	$R_L = 5K\Omega, V_o = 0.1V$ to 4.9V	100	84	84	84	82	dB	MIN	
		$R_L = 100K\Omega, V_o = 0.035V$ to 4.965V	104	90	90	90	89	dB	MIN	
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$		1.7					$\mu V/^\circ C$	TYP	
OUTPUT CHARACTERISTICS										
Output Voltage Swing from Rail		$R_L = 100K\Omega$	0.008					V	MAX	
Output Current	I_{OUT}		22	20	19.1	18.8	18	mA	MIN	
POWER SUPPLY										
Operating Voltage Range				2.1	2.5	2.5	2.5	V	MIN	
				5.5	5.5	5.5	5.5	V	MAX	
Power Supply Rejection Ratio	PSRR	$V_S = +2.5V$ to + 5.5V $V_{CM} = (-V_S) + 0.5$	90	76	73	71	71	dB	MIN	
Quiescent Current / Amplifier	I_Q	$I_{OUT} = 0$	18	24	26.6	27.4	29.7	μA	MAX	
DYNAMIC PERFORMANCE										
Gain-Bandwidth Product	GBP	$C_L = 100pF$	500					kHz	TYP	
Slew Rate	SR	$G = +1, 2V$ Output Step	0.2					V/ μs	TYP	
Settling Time to 0.1%	t_s	$G = +1, 2V$ Output Step	18					μs	TYP	
Overload Recovery Time		$V_{IN} \cdot Gain = V_S$	16					μs	TYP	
NOISE PERFORMANCE										
Voltage Noise Density	e_n	$f = 1kHz$	37					nV/\sqrt{Hz}	TYP	
		$f = 10kHz$	28					nV/\sqrt{Hz}	TYP	

Specifications subject to change without notice.

TYPICAL PERFORMANCE CHARACTERISTICS

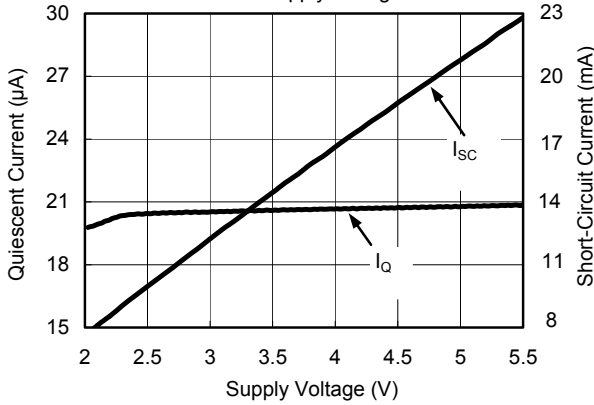
At $T_A = +25^\circ\text{C}$, $V_S = +5\text{V}$, and $R_L = 200\text{K}\Omega$ connected to $V_S/2$, unless otherwise noted.



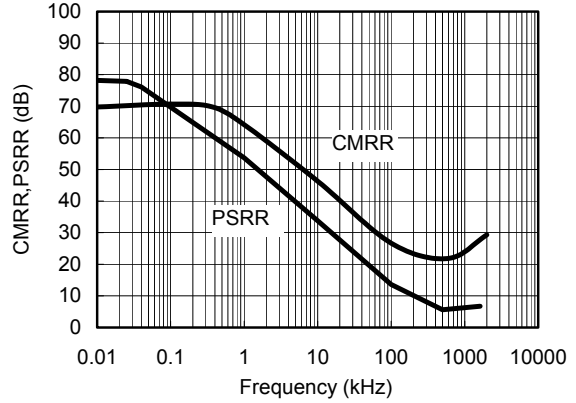
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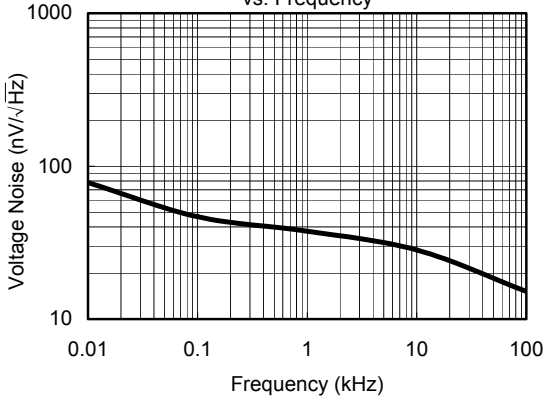
Quiescent and Short-Circuit Current vs. Supply Voltage



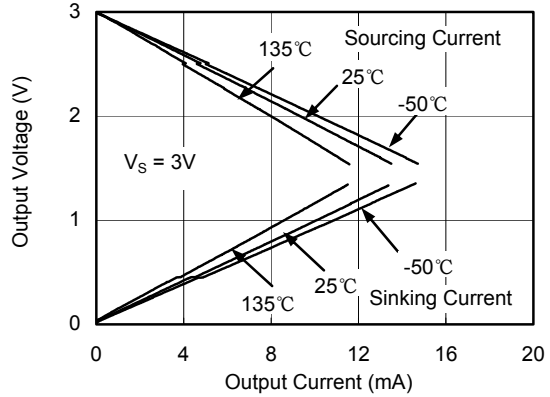
CMRR and PSRR vs. Frequency



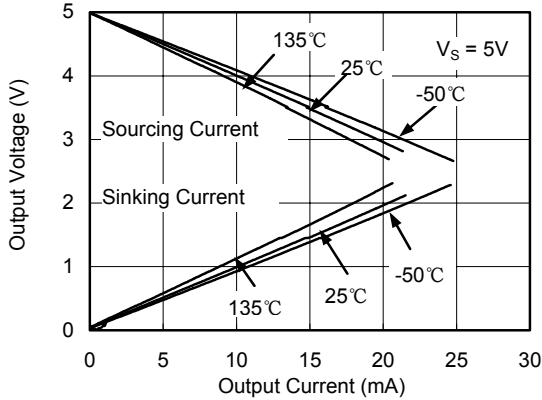
Input Voltage Noise Spectral Density vs. Frequency



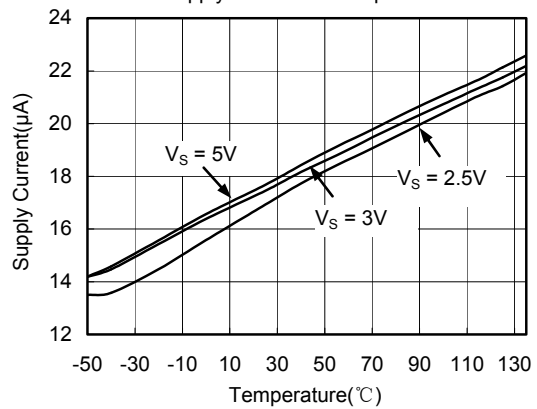
Output Voltage Swing vs. Output Current



Output Voltage Swing vs. Output Current



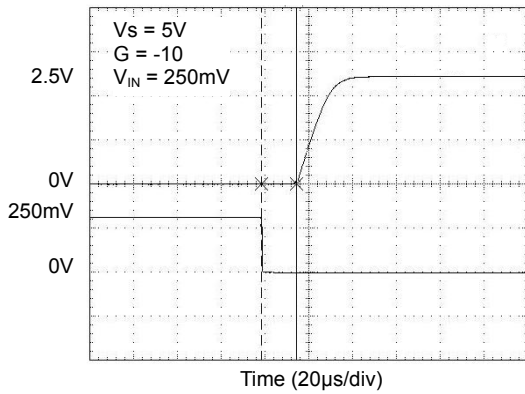
Supply Current vs. Temperature



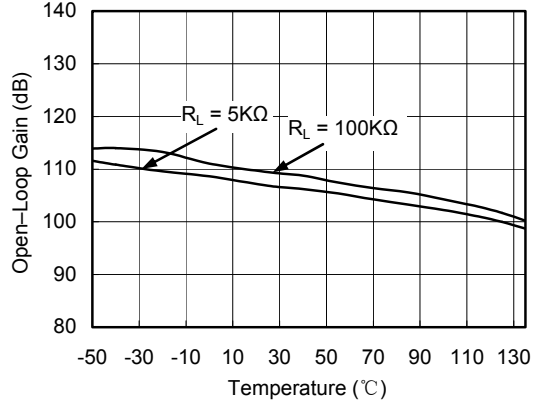
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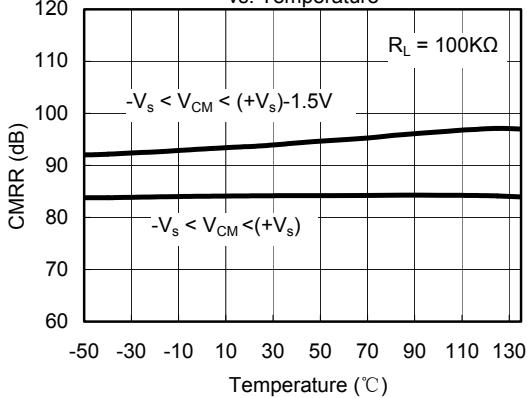
Overload Recovery Time



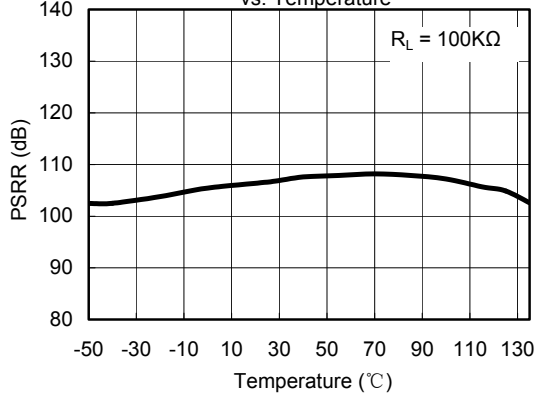
Open-Loop Gain vs. Temperature



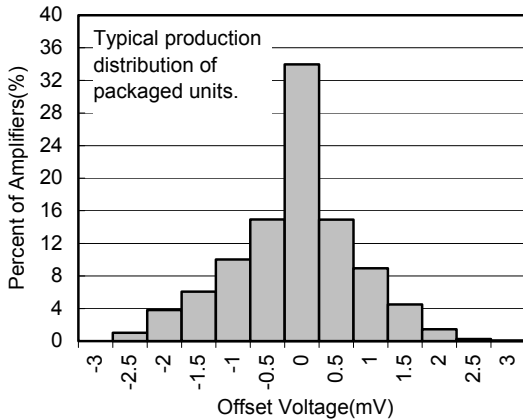
Common-Mode Rejection Ratio vs. Temperature



Power-Supply Rejection Ratio vs. Temperature



Offset Voltage Production Distribution



APPLICATION NOTES

Driving Capacitive Loads

The SGM853X can directly drive 250pF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 1. The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD} .

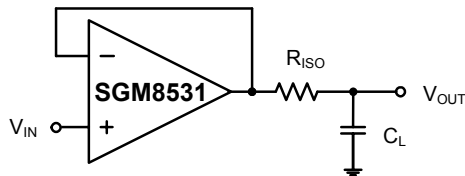


Figure 1. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 2, It provides DC accuracy as well as AC stability. R_F provides the DC accuracy by connecting the inverting signal with the output, C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

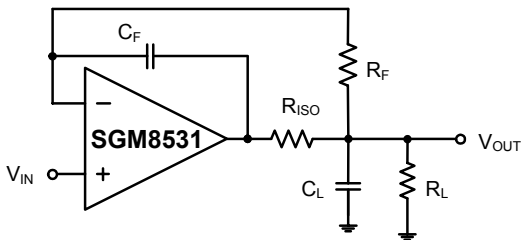


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

Power-Supply Bypassing and Layout

The SGM853X family operates from either a single +2.5V to +5.5V supply or dual $\pm 1.25V$ to $\pm 2.75V$ supplies. For single-supply operation, bypass the power supply V_{DD} with a 0.1µF ceramic capacitor which should be placed close to the V_{DD} pin. For dual-supply operation, both the V_{DD} and the V_{SS} supplies should be bypassed to ground with separate 0.1µF ceramic capacitors. 2.2µF tantalum capacitor can be added for better performance.

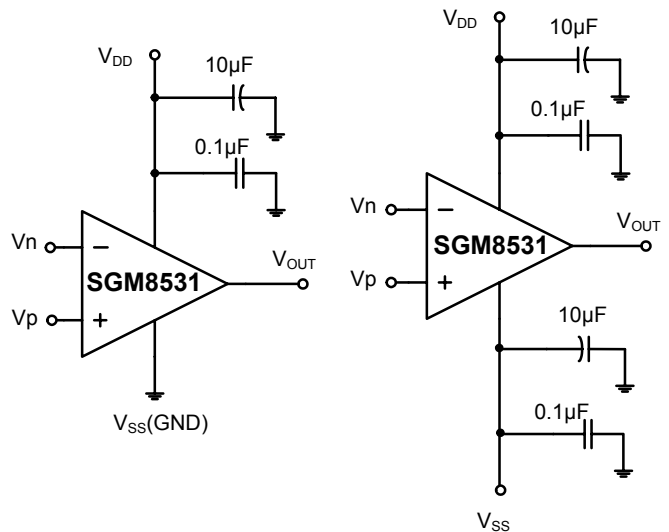


Figure 3. Amplifier with Bypass Capacitors

TYPICAL APPLICATION CIRCUITS

Differential Amplifier

The circuit shown in Figure 4 performs the difference function. If the resistors ratios are equal ($R_4 / R_3 = R_2 / R_1$), then $V_{OUT} = (V_p - V_n) \times R_2 / R_1 + V_{REF}$.

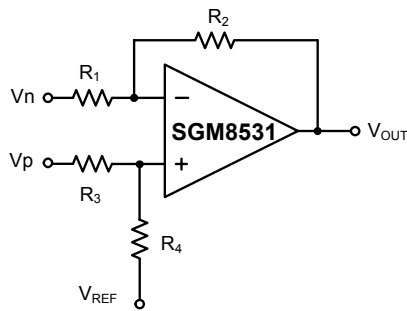


Figure 4. Differential Amplifier

Instrumentation Amplifier

The circuit in Figure 5 performs the same function as that in Figure 4 but with the high input impedance.

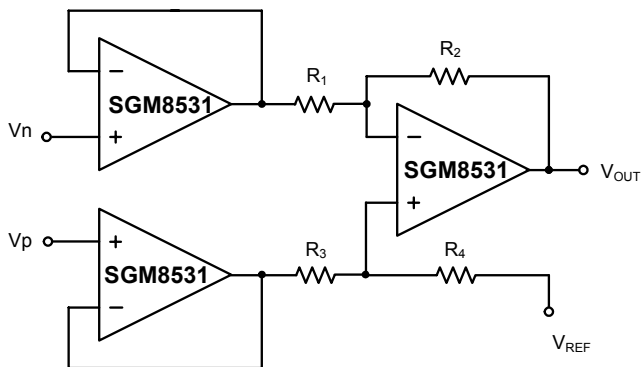


Figure 5. Instrumentation Amplifier

Low Pass Active Filter

The low pass filter shown in Figure 6 has a DC gain of $(- R_2 / R_1)$ and the -3dB corner frequency is $1/2\pi R_2 C$. Make sure the filter is within the bandwidth of the amplifier. The Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high-speed amplifiers. Keep resistors value as low as possible and consistent with output loading consideration.

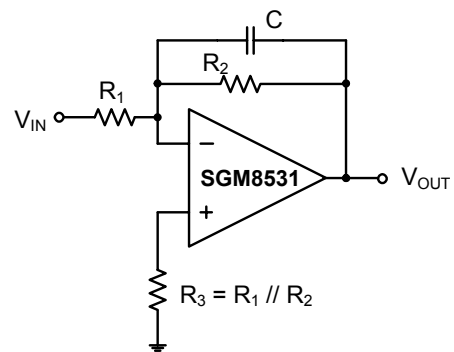
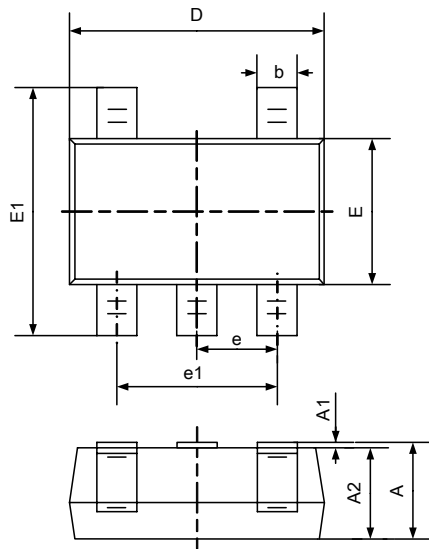


Figure 6. Low Pass Active Filter

PACKAGE OUTLINE DIMENSIONS

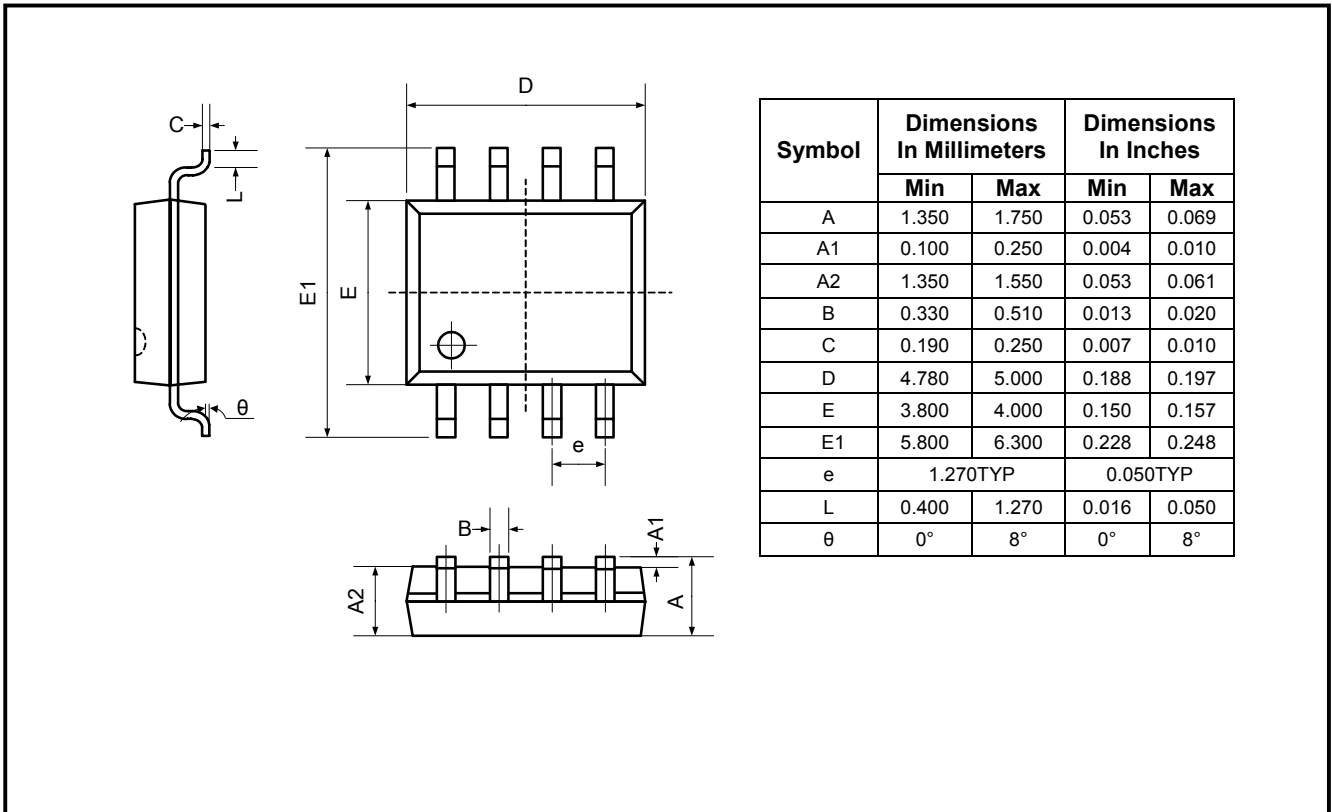
SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
C	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

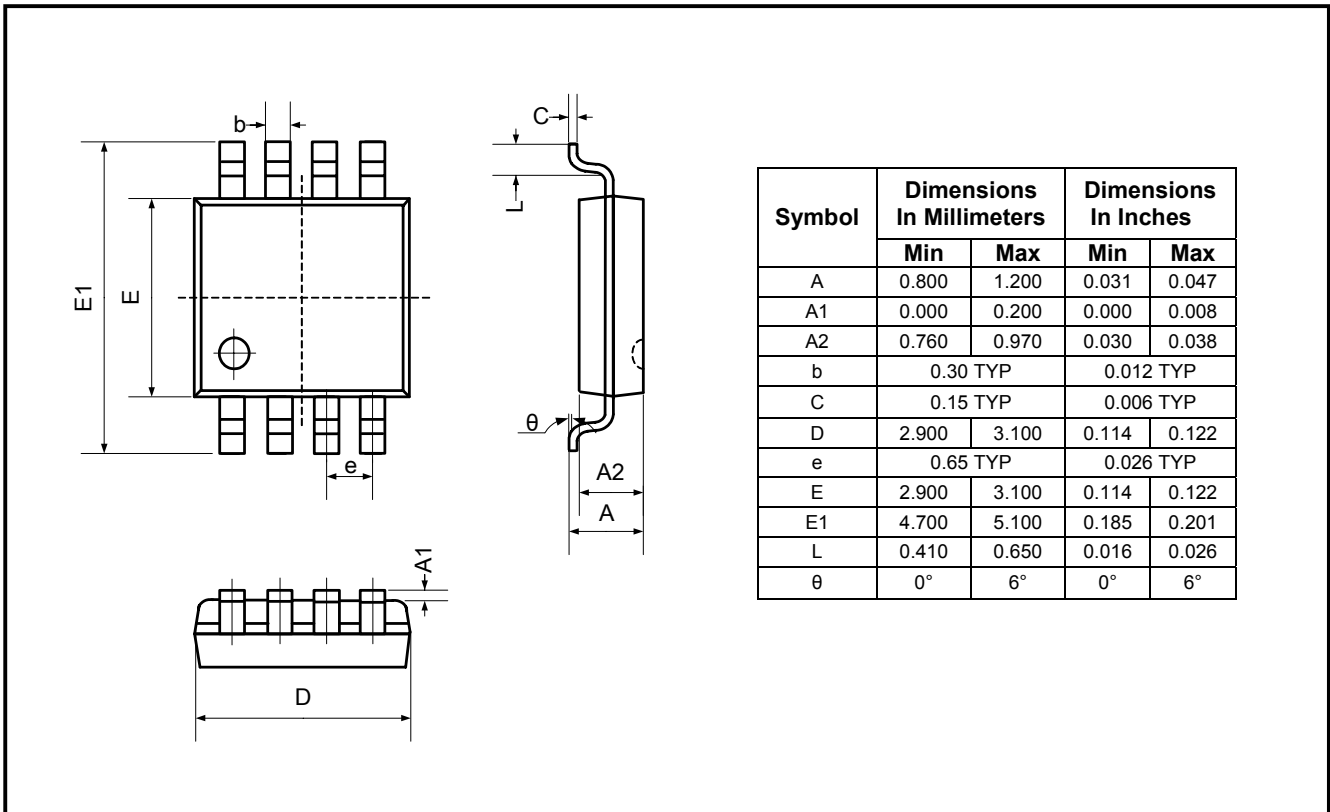
PACKAGE OUTLINE DIMENSIONS

SO-8



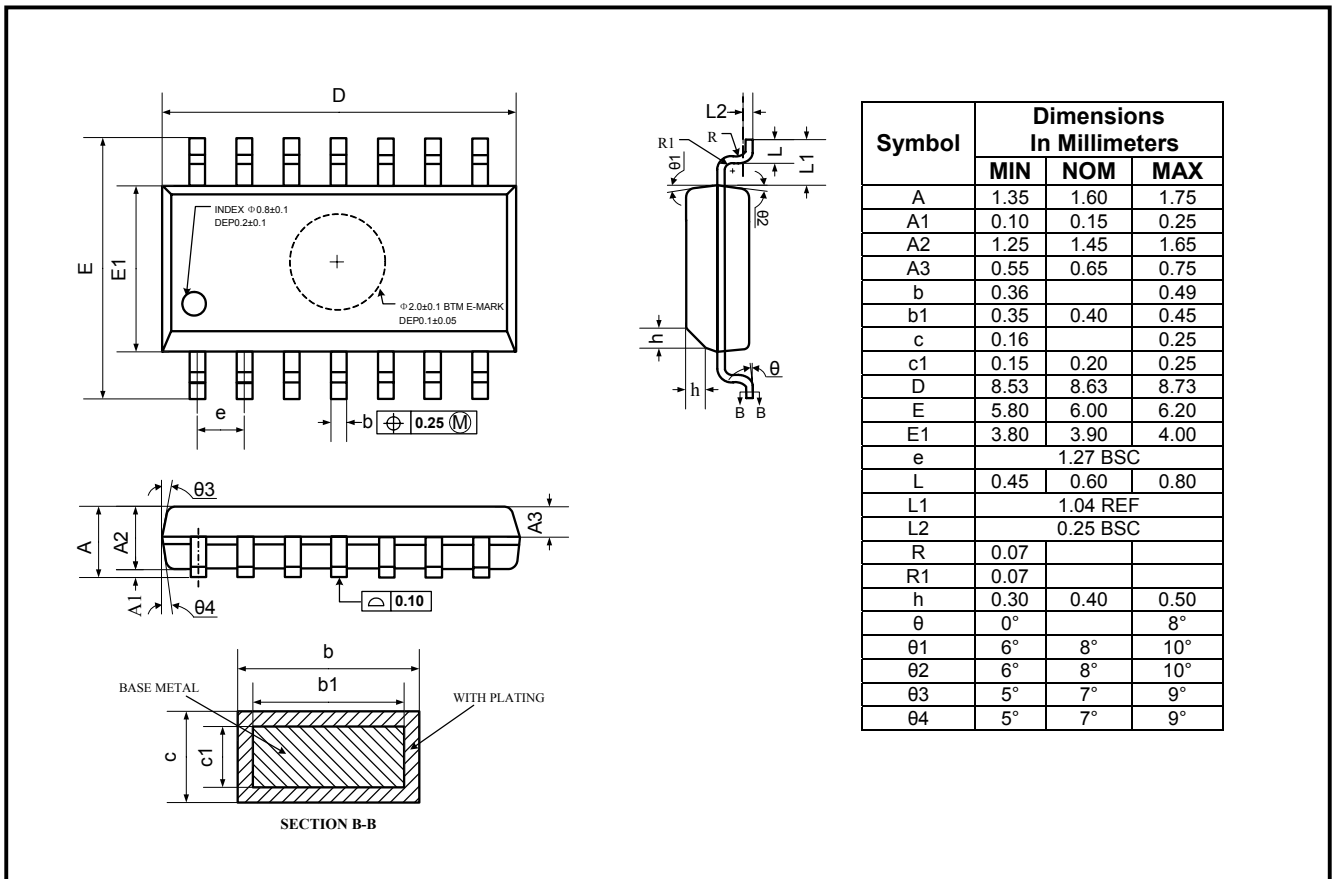
PACKAGE OUTLINE DIMENSIONS

MSOP-8



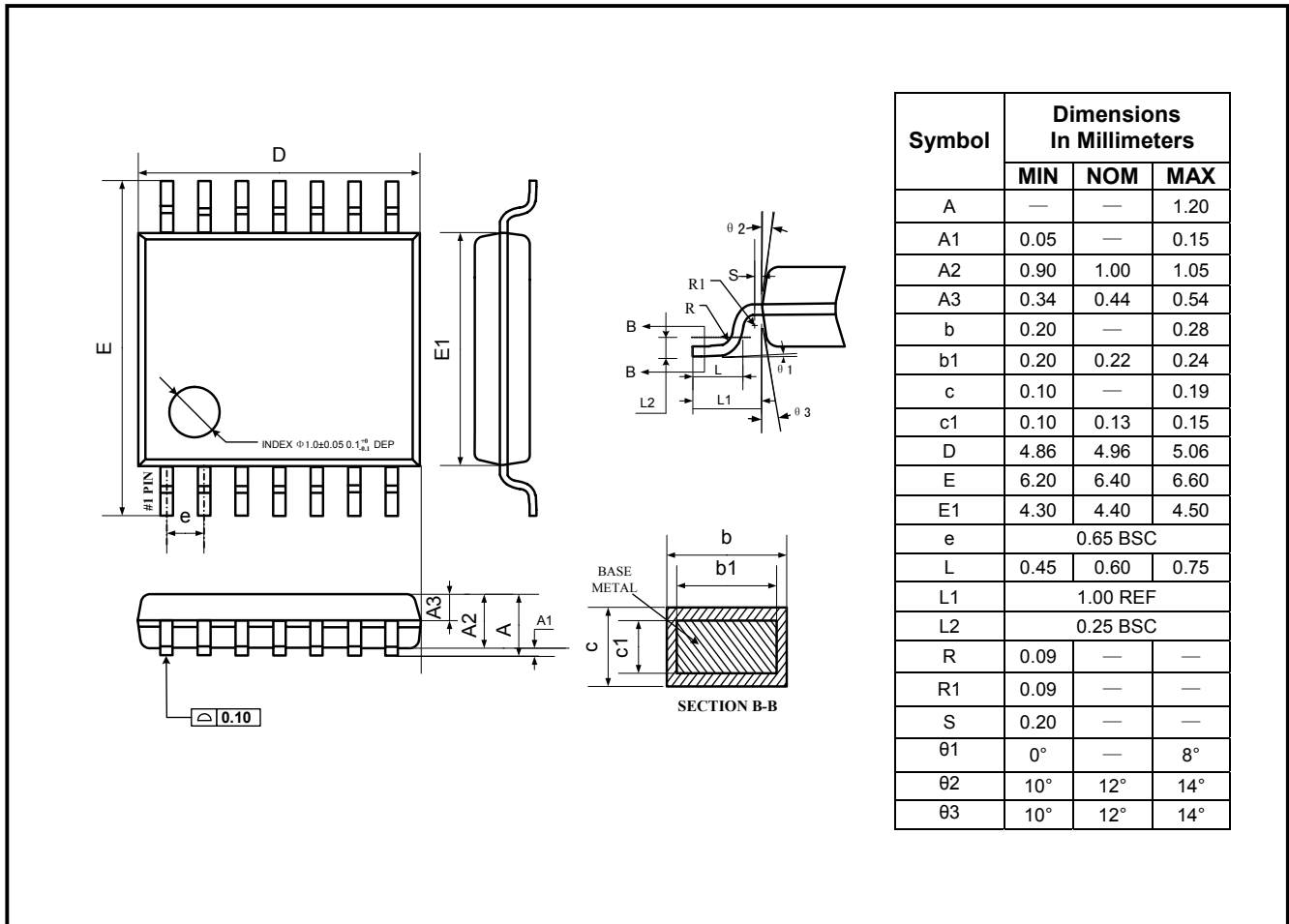
PACKAGE OUTLINE DIMENSIONS

SO-14



PACKAGE OUTLINE DIMENSIONS

TSSOP-14



02/2009 REV. C. 1

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