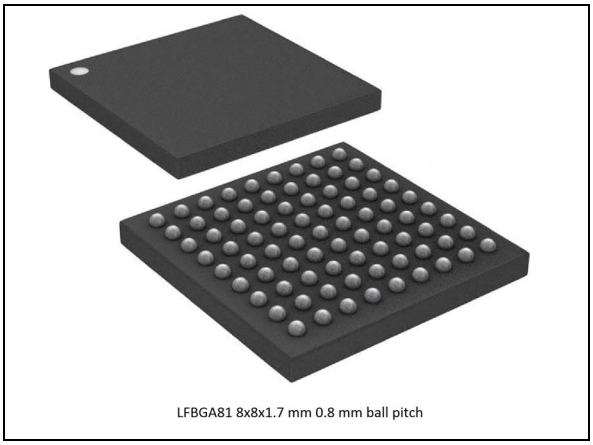
STA8100GA

Teseo V family automotive multi-band multi-constellation GNSS precise engine receiver

Datasheet - production data



LFBGA81 8x8x1.7 mm 0.8 mm ball pitch

Features

- AEC-Q100 qualified
- STMicroelectronics 5th generation positioning receiver with 80 tracking channels and 4 fast acquisition channels compatible with 6 constellations: GPS, Galileo, GLONASS, BeiDou, QZSS, NAVIC (former IRNSS)
- Dual band L1 and L5 single chip solution
- Triple band capability with external RF STA5635A
- ST-DRAW (Dead Reckoning Automotive Way) is supported on STA8100GAD and STA8100GADS only
- SBAS systems: WAAS, EGNOS, MSAS, GAGAN, BeiDou
- Code phase, carrier phase, doppler frequency measurement
- Antenna sensing
- PPS output
- Notch filter for anti-jamming
- ARM® Cortex® M7 core:
  - Maximum clock frequency 314 MHz
  - 16 KB I-cache and 16 KB D-cache
  - 64 KB I-TCM and 384 KB D-TCM, core clock speed
  - Nested vector interrupt controller
  - JTAG debugging capability
  - 256 Kbyte system RAM
- Hardware Security Module (HSM) with HW cryptographic co-processor is enabled for STA8100GAS only
- 32 channels DMA
- Memory interfaces:
  - SFC (Octal/Quad serial flash controller, SDR)
  - SD multimedia card
- Serial interfaces:
  - 3 x UART
  - Synchronous serial port (SPI supported)
  - I^2C
  - 2 x multi mode serial interfaces
  - 2 x CAN controllers
- Core peripherals:
  - 2 x multi timer units
  - Watchdog timer
  - 1 x extended function timers
  - 32 kHz oscillator real time clock
  - AES decipher hardware accelerator
- Power management unit, with separate power supply domain and on-chip LDO and high voltage/low voltage monitors:
  - Backup voltage domain 1.7 to 3.6 V with LDO for always-on core supply and HV/LV detectors, and dedicated IO-ring0
  - Main voltage domain 1.7 to 3.6 V with LDO for switchable logic domain and HV/LV detectors for 85 °C maximum ambient temperature operations or 1.2 V +/ - 5 % external voltage supply for 105 °C maximum ambient temperature operations
  - Separate RF domain with dedicated LDO

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  - IO-ring1 1.8 or 3.3 V capable, and dedicated 1.8 V LDO
  - IO-ring2 3.3 V +/ -10 % capable
  - Fail safe GPIOs available
- USB2.0 full speed (12 Mb/s) with integrated physical layer transceiver
- ESD: 2 kV (HBM) and 500 V (CDM)
- Automotive grade 105 °C option

Description

STA8100GA is part of the Teseo V family.

STA8100GA is a multi-band multi-constellation positioning receiver IC able to manage all the GNSS constellations such as GPS, Galileo, Glonass, BeiDou, NAVIC (former IRNSS) and QZSS, in L1, L2, L5 and E6 frequency bands. Security feature (enabled only for STA8100GAS) is implemented in a dedicated sub-system, embedding cryptographic HW accelerator with protected access.

STA8100GAD and STA8100GADS are offered with STMicroelectronics dead reckoning firmware called TESEO-DRAW.

Contents

1 Overview

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STA8100GA is a multi-band multi-constellation positioning receiver IC able to manage all the GNSS constellations such as GPS, Galileo, Glonass, BeiDou, NAVIC (former IRNSS) and QZSS, in L1, L2, L5 and E6 frequency bands.

STA8100GA is able to receive GPS, Galileo plus Beidou on L1 and L5 bands simultaneously without the need of an external RF front-end.

A dedicated interface allows receiving GNSS data from the external RF front-end STA5635A in order to manage the other GNSS bands (L2, L5, E6 bands) simultaneously with the L1 band signals, allowing also a triple frequency mode L1/L2/L5 or L1/L5/E6.

STA8100GA provides to the main host via serial interface the precise raw measurements of all the visible GNSS satellites to let run any possible precise position algorithm. STA8100GA provides also an autonomous precision positioning calculation to main host using all the satellites constellations.

STA8100GA is compliant with ST Automotive Grade qualification which includes in addition to AEC-Q100 requirements a set of production flow methodologies targeting zero defect per million. STA8100GAD and STA8100GADS are offered with STMicroelectronics dead reckoning firmware called TESEO-DRAW.

With the help of HSM, STA8100GAS supports a secure boot and secure firmware upgrade procedures which allow only properly signed binaries to run on STA8100GAS. STA8100GA is fulfilling high quality and service level requirements of the Automotive market, is the ideal solution for in-dash navigation, smart antenna, car to car, V2X, OEM telematics, marine, drone, lawnmower and many other applications requiring a precise position.

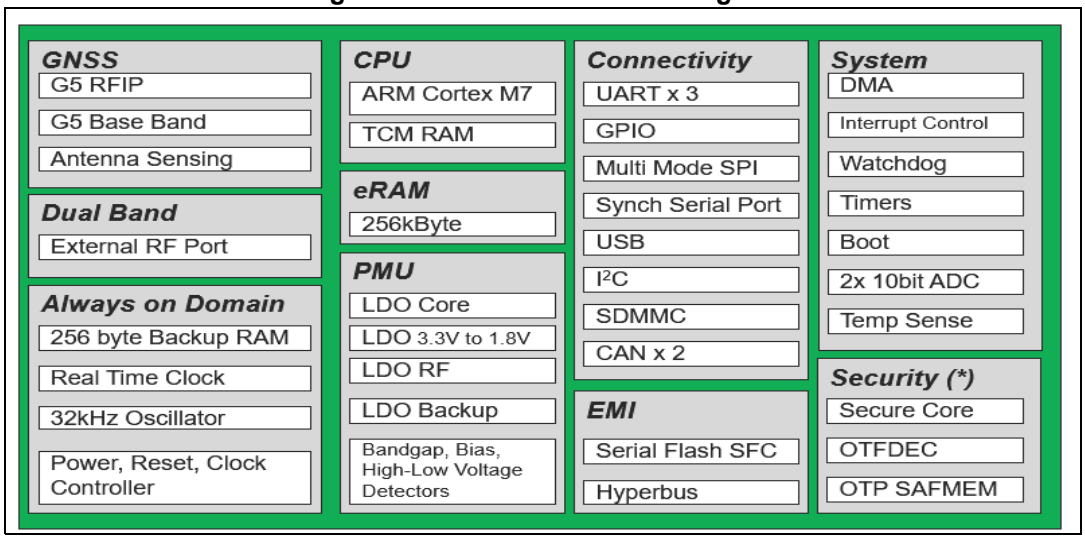
STA8100GA embeds separated LDOs to supply, the analog parts, the digital core and the IO ring of the device facilitating requirements to external power supply.

The chip is manufactured in CMOS technology and housed in a LFBGA package 81 balls 8x8 mm body size 0.8 mm pitch.

2 Pin description

2.1 Block diagram

Figure 1. STA8100GAS block diagram



Note: (*) Security modules are only available for STA8100GAS version.

2.2 Package

LFBGA 81 balls with 8 x 8 x 1.7 mm body size and 0.8 mm ball pitch.

2.3 Ball list

Figure 2. Device ballout

	1	2	3	4	5	6	7	8	9
A	GND	SFC_CSN	VIO1_EXT	Q-mag1	Q-sign2	GPIO6	GPIO5	EXT_REG_SEL	GND
B	SFC_CLK	SFC_SIO5	SFC_SIO2	I-mag1	I-mag2	VDD_EXT_REG	VDD_EXT_REG	VDD_EXT_REG	UART2 RX
C	VIO1_EXT	SFC_SIO6	SFC_SIO3	SFC_SIO1	Q-mag2	I-sign1	TEST	UART2 TX	MAIN_PMU_AGND
D	RTC_XTI	SFC_SIO7	SFC_SIO4	SFC_SIO0	I-sign2	Q-sign1	VCORE_IN	VIO2_IN	STAND_BY_OUT
E	RTC_XTO	RESETn	WAKEUP	BKP_PMU_AGND	GND	GND	JTAG-TMS	JTAG-TDI	JTAG-TDO
F	TCXO_IN	VBK_OUT	VBK_IN	STANDBY_IN	GND	GND	V2V5_OUT	JTAG-TRSTn	JTAG-TCK
G	VCC_PLL	GND_RF	GND_RF	GND_RF	GND_RF	VDD_EXT_REG	MSP1_Dout	GPIO67	TSENS_AGND
H	LNA_IN	GND_RF	GND_RF	TP_IF_N/ ANTSens1/ AIN0	TP_IF_P/ ANTSens2/ AIN1	VIO2_IN	VIO2_IN	PPS_OUT	MSP1_CS
J	VCC_LNA	LNA_OUT	RFA_IN	VRF_OUT	VRF_IN	UART1_TX	UART1_RX	MSP1_clk_out	MSP1_Din

Note: Balls all have alternate functionalities, which can be selected by relevant registers.

Table 1. Power supply pins

Symbol	I/O voltage(1)	I/O	Description	Ball
VRF_IN	1.70 to 3.6 V	PWR	LDO RF power input - IO ring RF	J5
VRF_OUT	1.2 V	PWR	LDO RF power output	J4
VCC_LNA	1.2 V	PWR	LNA power input	J1
VCC_PLL	1.2 V	PWR	RF VCC power input	G1
VBK_IN(2)	1.62 to 3.6 V	PWR	LDO Backup power input - IO ring0	F3
VBK_OUT	1.2 V	PWR	LDO Backup power output	F2
VCORE_IN	1.70 to 3.6 V	PWR	LDO Core power input	D7
VDD_EXT_REG	1.2 V	PWR	LDO Core power output	B6, B7, B8, G6
VIO2_IN	3 to 3.6 V	PWR	LDO IO ring2 power input - IO ring2	D8, H6, H7
VIO1_EXT	1.70 or 3.6 V	PWR	LDO IO ring1 power output - IO ring1 input	A3, C1
V2V5_OUT	2.5 V	PWR	LDO Core 2.5 V output	F7
GND_PMU	GND	GND	Main voltage regulator ground	C9
GND_BKP_PMU	GND	GND	Backup voltage regulator ground	E4
GND_TSENS	GND	GND	Temperature sense block ground	G9
GND_RF	GND	GND	RF ground	G2, G3, G4, G5, H2, H3
GND	GND	GND	Ground	A1, A9, E5, E6, F5, F6

1. Refer to *Section 4: Electrical specifications*.
2. Backup power shall be applied at the same time or before VCORE_IN, not after.

Table 2. Main function pins

Symbol	I/O voltage(1)	I/O	Description	Ball	Reset state
EXT_REG_SEL	VCORE_IN	I	LDO Core Disable. When High the LDO CORE is off. Core is supplied by an external power source.	A8	NA
TEST	IO ring2	I	TEST - JTAG enable. In mission/application mode this pin must be connected to GND.	C7	Hi-Z/PD
RTC_XTI	VBK_IN / IO ring0	I	If 32 kHz oscillator enabled then input of the 32 kHz oscillator amplifier circuit. Else CMOS input as electrical characteristic table. Both cases, it is the reference for real time clock counter circuitry.	D1	NA
RTC_XTO	VBK_IN / IO ring0	O	Output of the oscillator amplifier circuit.	E1	NA
RESETn	VBK_IN / IO ring0	I	Reset input with Schmitt-Trigger characteristics and noise.	E2	Hi-Z/ PD
WAKEUP	VBK_IN / IO ring0	I	When high, the device will wakeup and exit from Standby mode. It has higher priority compared to Standby_in pin. Wakeup from Standby mode.	E3	Hi-Z

Table 2. Main function pins (continued)

Symbol	I/O voltage(1)	I/O	Description	Ball	Reset state
STANDBY_IN(2)	VBK_IN / IO ring0	I	When low, the chip is forced in Standby mode.	F4	Hi-Z
STANDBY_OUT	VBK_IN	O	When low, it indicates device is in Standby mode.	D9	Hi-Z

1. In Standby mode, if VIO1 and VIO2 are powered, GPIOs have no driving capabilities and no PD/PU is active.
2. If VCORE_IN is removed before STANDBY_IN has switched from high to low, STANDBY_OUT remains high level, even if device enters in Standby mode.

Table 3. RF front-end pins

Symbol	I/O voltage	I/O	Description	Ball
ANTSens2/ AIN1	IO ring RF	I	Antenna sensing – TPIF_P	H5
ANTSens1/ AIN0	IO ring RF	I	Antenna sensing – TPIF_N	H4
LNA_IN	LNA VCC	I	LNA input	H1
LNA_OUT	LNA VCC	O	LNA output	J2
RFA_IN	VRFOUT	I	RFA input	J3
TCXO_IN	PLL VCC	I	TCXO input	F1

Table 4. Memory interface (power fail safe IOs)

Symbol	I/O voltage	I/O	Description	Ball	Reset state
SFC_CLK	IO ring1	O	Serial flash controller clock	B1	Hi-Z/ PD
SFC_CSN	IO ring1	O	Serial flash controller chip select	A2	Hi-Z/ PD
SFC_SIO0	IO ring1	I/O	Serial flash controller data IO 0	D4	Hi-Z/ PD
SFC_SIO1	IO ring1	I/O	Serial flash controller data IO 1	C4	Hi-Z/ PD
SFC_SIO2	IO ring1	I/O	Serial flash controller data IO 2	B3	Hi-Z/ PD
SFC_SIO3	IO ring1	I/O	Serial flash controller data IO 3	C3	Hi-Z/ PD
SFC_SIO4	IO ring1	I/O	Serial flash controller data IO 4	D3	Hi-Z/ PD
SFC_SIO5	IO ring1	I/O	Serial flash controller data IO 5	B2	Hi-Z/ PD
SFC_SIO6	IO ring1	I/O	Serial flash controller data IO 6	C2	Hi-Z/ PD
SFC_SIO7	IO ring1	I/O	Serial flash controller data IO 7	D2	Hi-Z/ PD

Table 5. External RF interface (power fail safe IOs)

Symbol	I/O voltage(1)	I/O	Description	Ball
ISIG1	IO ring1 (FS)	I	Ex RF interface I-Sign1	C6
IMAG1	IO ring1 (FS)	I	Ex RF interface I-Mag1	B4
QSIG1	IO ring1 (FS)	I	Ex RF interface Q-Sign1	D6
QMAG1	IO ring1 (FS)	I	Ex RF interface Q-Mag1	A4
ISIG2	IO ring1 (FS)	I	Ex RF interface I-Sign2	D5

Table 5. External RF interface (power fail safe IOs) (continued)

Symbol	I/O voltage[1]	I/O	Description	Ball
IMAG2	IO ring1 (FS)	I	Ex RF interface I-Mag2	B5
QSIG2	IO ring1 (FS)	I	Ex RF interface Q-Sign2	A5
QMAG2	IO ring1 (FS)	I	Ex RF interface Q-Mag2	C5

1. (FS) Fail Safe IO

Table 6. Communication interface pins

Symbol after bootstrap	I/O voltage[1]	I/O	AF	Function	Description	Ball	Reset
GPIO6	IO ring2 (FS)	I/O	Default	GPIO6	—	A6	PD
		I	ALT A	CAN0_RX	CAN Receiver		—
		I	ALT B	—	—		—
		I/O	ALT C	I2C_SDA	I2C Data		—
GPIO5	IO ring2 (FS)	I/O	Default	GPIO5	—	A7	PD
		O	ALT A	CAN0_TX	CAN Transmitter		—
		I	ALT B	SFC_DQS	Serial Flash Controller DQS		—
		I/O	ALT C	I2C_CLK	I2C Cock		—
PPS_OUT	IO ring2 (FS)	I/O	Default	GPIO32	—	H8	PD
		I	ALT A	—	—		—
		O	ALT B	UART0_TX	UART0 Transmitter		—
		O	ALT C	PPS_OUT	—		—
MSP1_clk_out	IO ring1 (FS)	I/O	Default	GPIO91	—	J8	PD
		I/O	ALT A	MSP1_clk	MSP1 Clock		—
		I/O	ALT B	SSPCLK	SSP Clock		—
		O	ALT C	CLKOUT	Clock Output		—
MSP1_CS	IO ring1 (FS)	I/O	Default	GPIO90	—	H9	PD
		I/O	ALT A	MSP1_CS	MSP1 Chip Select		—
		I/O	ALT B	SSPFRM	SSP Chip Select		—
		I	ALT C	UART2_RX	UART2 Receiver		—
MSP1_Din	IO ring1 (FS)	I/O	Default	GPIO94	—	J9	PD
		I	ALT A	MSP1_Din	MSP1 Data Input		—
		I	ALT B	SSPRXD	SSP Data Receive		—
		O	ALT C	OCTOSPI_CLKn	OctoSPI Clock Inverted		—

Table 6. Communication interface pins (continued)

Symbol after bootstrap	I/O voltage[1]	I/O	AF	Function	Description	Ball	Reset
MSP1_Dout	IO ring1 (FS)	I/O	Default	GPIO95	—	G7	PD
		O	ALT A	MSP1_Dout	MSP1 Data Output		—
		O	ALT B	SSPTXD	SSP Data Transmit		—
		O	ALT C	UART2 TX	UART2 Transmitter		—
JTAG-TRSTn[2]	IO ring2 (FS)	I/O	Default	JTAG-TRSTn	JTAG Reset	F8	PD
		O	ALT A	PPS_OUT	—		—
		I	ALT B	—	—		—
		I	ALT C	Timer_OCMPA	Timer A Input		—
JTAG-TCK[2]	IO ring2 (FS)	I/O	Default	JTAG-TCK	JTAG Clock	F9	PD
		I/O	ALT A	SSPCLK	SSP Clock		—
		I/O	ALT B	MSP0_clk	MSP0 Clock		—
		I	ALT C	Timer_ICAPA1	Timer A Input		—
JTAG-TMS[2]	IO ring2 (FS)	I/O	Default	JTAG-TMS	JTAG TMS	E7	PU
		I/O	ALT A	SSPFRM	SSP Chip Select		—
		I	ALT B	MSP0_Din	MSP0 Data Input		—
		O	ALT C	UART0_RTS	UART0 RTS		—
JTAG-TDI[2]	IO ring2 (FS)	I/O	Default	JTAG-TDI	JTAG Data Input	E8	PU
		I	ALT A	SSPRXD	SSP Data Receive		—
		O	ALT B	MSP0_Dout	MSP0 Data Output		—
		O	ALT C	UART0_CTS	UART0 CLR		—
JTAG-TDO[2]	IO ring2 (FS)	I/O	Default	JTAG-TDO	JTAG Data Output	E9	PD
		O	ALT A	SSPTXD	SSP Data Transmit		—
		I/O	ALT B	MSP0_CS	MSP0 Chip Select		—
		I	ALT C	PPS_IN	PPS Input		—
UART1_RX	IO ring2	I/O	Default	USB_DM	USB Minus	J7	PD
		I	ALT A	UART1_RX	UART1 Receiver		—
		I/O	ALT B	I2C_SDA	I2C Data		—
		I	ALT C	CAN1_RX	CAN1 Receiver		—
UART1_TX	IO ring2	I/O	Default	USB_DP	USB Positive	J6	PD
		O	ALT A	UART1_TX	UART1 Transmitter		—
		I/O	ALT B	I2C_CLK	I2C Clock		—
		O	ALT C	CAN1_TX	CAN1 Transmitter		—

Table 6. Communication interface pins (continued)

Symbol after bootstrap	I/O voltage[1]	I/O	AF	Function	Description	Ball	Reset
UART2_RX	IO ring2 (FS)	I/O	Default	GPIO89	—	B9	PD
		I	ALT A	UART2_RX	UART2 Receiver		—
		I/O	ALT B	—	—		—
		O	ALT C	—	—		—
UART2_TX	IO ring2 (FS)	I/O	Default	GPIO88	—	C8	PD
		O	ALT A	UART2_TX	UART2 Transmitter		—
		I/O	ALT B	—	—		—
		O	ALT C	—	—		—
GPIO67	IO ring2	I/O	Default	GPIO67	—	G8	PD
		O	ALT A	—	—		—
		I/O	ALT B	UART0_RX	—		—
		I	ALT C	PPS_IN	—		—

1. (FS) Fail Safe IO

2. JTAG pins can be configured as GPIO in a dedicated alternate function mode as: TRSTn=GPIO0, TCK=GPIO1, TMS=GPIO2, TDI=GPIO3, TDO=GPIO4

3 General description

3.1 Multi-constellation and multi-band

The constellations that STA8100GA supports are the following ones:

- GPS (L1 C/A, L2C, and L5)
- GLONASS (L1OF, L2OF)
- BeiDou (B1C, B1I, B2a, B2I)
- GALILEO (E1, E5a, E5b, E6)
- QZSS (L1 C/A, L2C, L5)
- NAVIC - former IRNSS (L5)

Carrier phase raw measurements are also provided.

STA8100GA supports the simultaneous usage of all constellations in parallel on L1 band: GPS, GLONASS, GALILEO, BeiDou, and QZSS in addition to SBAS. STA8100GA also supports all the other bands in combination with the external STA5635A radio frequency front end. The most important GNSS user cases that can be supported by STA8100GA and STA5635A are listed in the below table. Each of those cases would require a dedicated firmware:

Table 7. GNSS user cases

Constellation	GPS/ QZSS			Glonass		BeiDou			Galileo				NAVIC	SBAS
Frequency	**L1 C/A**	**L2C**	**L5**	**L1OF**	**L2OF**	**B1I**	**B2I**	**B2A**	**E1**	**E5b**	**E5A**	**E6**	**L5**	**L1 C/A**
Case 0	I	E	—	I	E	I	—	—	I	—	—	—	—	I
Case 1	I	E	—	I	—	I	E	—	I	—	—	—	—	I
Case 2	I	E	—	I	—	I	—	—	I	E	—	—	—	I
Case 3	I	—	E	I	—	I	—	E	I	—	—	—	—	I
Case 4	I	—	E	I	—	I	—	—	I	—	E	—	—	I
Case 5	I	—	E	I	—	I	—	—	I	—	—	—	E	I
Case 6	I	—	I	—	—	—	—	—	I	—	I	E	—	I
Case 7	I	—	I	—	—	I	—	I	I	—	—	—	I	I
Case 8	I	—	I	—	—	I	—	—	I	—	I	—	—	I
Case 9	I	E	I	—	—	I	E	I	—	—	—	—	—	I
Case 10	I	E	I	—	—	—	—	—	I	E	I	—	—	I

Note: Maximum 64 satellites tracked simultaneously.

I= Internal STA8100GA RF Section

E= External STA5635A RF Receiver

3.2 RF front end (G5RF)

The integrated RF front-end is able to support different bands (L1, L2, L5, and E6) thanks to a programmable and flexible RF-IF chain driven by a fractional PLL.

The RF_IF chain is followed by a 3-bit ADC able to convert the IF signal to Sign (SIGN) and Magnitude (MAG1, MAG0) bit. The MAG bit is internally integrated in order to control the variable gain amplifiers.

The embedded fractional PLL allows supporting a wide range of reference clocks (10 to 55 MHz).

3.3 Multi-band multi-constellation base band (G5BB) processor

STA8100GA integrates G5BB proprietary IP, which is the STMicroelectronics latest generation high-sensitivity baseband processor fully compliant with all different constellations and bands: GPS, Galileo, Glonass, BeiDou, NAVIC (former IRNSS) and QZSS systems.

3.4 MCU sub system

The Cortex® M7 core masters the system resources (memories, registers, and external memory controllers) through the AXI, AHB and APB interconnections present in the SOC.

3.4.1 Caches

The size of the instruction and data cache used for ARM® sub-system in STA8100GA is 16 KB each.

3.4.2 TCM

ARM® Cortex® M7 has a TCM Control Unit (TCU) with TCM interfaces and an AHB slave (AHBS) interface for system access to TCMs. These TCM memories are integrated outside the ARM® sub-system. STA8100GA has a 64 KB ITCM memory and 384 KB of DTCM memory.

In the DTCM memory 160 KB is dedicated for ARM® usage and the remaining 224 KB DTCM is shared between the ARM® sub-system and the G5BB module.

ARM® provides access to the TCM memories through an AHB slave interface. This AHBS interface is connected to the AMBA infrastructure in STA8100GA so that DMA present on the bus can access the TCM memories MCU.

3.4.3 Nested Vector Interrupt Controller (NVIC)

This Nested Vectored Interrupt Controller (NVIC) allows the operative system interrupt handler to quickly dispatch interrupt service routines in response to peripheral interrupts. It provides a software interface to the interrupt system. ARM® Cortex® M7 has an NVIC module for handling the interrupts. The NVIC supports 128 interrupts with 16 levels of priority, which can be changed dynamically. The software can control each request line to generate software interrupts.

3.4.4 AXI bus

AXI Bus matrix handles major high bandwidth transactions for STA8100GA. It connects the SRAM, boot ROM and external memory controllers, which provide access to the external Flash. ARM® acts as a master on this bus with the highest priority.

3.5 APB peripherals

3.5.1 APB bridge 2 peripherals

AHB to APB Bridge 2 sits on AHB bus matrix 0 as a slave and is used to connect peripherals. These slaves will be accessed by AHB masters connected to AHB bus matrix 0.

The peripherals connected to APB 2 are:

UART2, MSP1, GPIO PORT 2, MTU1.

3.5.2 APB bridge 1 peripherals

AHB to APB bridge 1 sits on AHB bus matrix 0 as a slave and is used to connect peripherals. These slaves will be accessed by AHB masters connected to AHB bus matrix0.

The peripherals connected to APB 1 are UART1, EFT0, EFT1, GPIO PORT 0 and 1, MTU0, OTP, SSP, Thermal sensor, Watchdog timer.

3.5.3 APB bridge 0 peripherals

AHB to APB bridge 0 sits on AHB bus matrix 0 as a slave and is used to connect peripherals. These slaves will be accessed by AHB masters connected to AHB bus matrix0.

The peripherals connected to APB 0 are the ones on the always on domain:

PRCC always ON, RTC.

3.5.4 AHB slave devices

There are some AHB slave devices which are connected to AHB bus matrix 0.

3.6 eSRAM

256 KB of embedded RAM are available on top of the TCM RAM.

The eSRAM is directly connected to the MCU through the AXI bus. It can be used for data and instruction.

3.7 Serial Flash Memory Controller (SFC)

The Serial Flash Memory Controller supports single, quad and octal memories. It can be used for in place execution thanks to direct memory mapping.

3.8 SSP

STA8100GA has one Synchronous Serial Ports (SSPs). The SSP is a master or slave interface that enables synchronous serial communication with slave or master peripherals having one of the following:

- Serial peripheral interface bus standards
- Synchronous serial protocol bus standards
- Micro-wire interface bus standards
- Unidirectional interface

In both master and slave configurations, the SSP has the following features:

- Parallel-to-serial conversion on data written to an internal 32-bit wide, 32-location deep transmit FIFO
- Serial-to-parallel conversion on received data, buffering it in a 32-bit wide, 32-location deep receive FIFO
- Programmable data frame size from 4 to 32 bits
- Programmable clock bit rate and pre-scaler
- Programmable clock phase and polarity in SPI mode
- Support for direct memory access (DMA)

3.9 UART

The UARTx performs serial-to-parallel conversion on data asynchronously received from a peripheral device on UARTx_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on UARTx_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) for receive. FIFOs may be burst-loaded or emptied by the system processor or DMA, from one to sixteen words per transfer.

3.10 Watchdog Timer (WDT)

Watchdog Timer (WDT) provides a way of recovering from software crashes. The watchdog clock is used to generate a regular interrupt (Irq_wdt), depending on a programmed value.

The watchdog monitors the interrupt and asserts a HW reset signal (WDOGRES) if the interrupt remains unserviced for the entire programmed period. The WDT is counting down at a fixed frequency of 32.768 kHz.

The watchdog timer peripheral can be used as free-running timer or as watchdog to resolve processor malfunctions due to hardware or software failures.

Feature set overview:

- 16-bit down counter
- 8-bit clock pre-scaler
- Safe reload sequence
- Free-running timer mode
- End of counting interrupt generation

3.11 GPIO

There are 34 GPIOs in this device.

The GPIO block provides programmable inputs or outputs. Each input or output can be controlled in two modes:

- Software mode through an APB bus interface
- Alternate function mode, where GPIO becomes a peripheral input or output line

Any GPIO input can be independently enabled or disabled (masked) for interrupt generation. User can select for each GPIO which edge (rising, falling, both) will trigger an interrupt.

A de-bouncing logic can be enabled for each GPIO to filter glitches on IOs before going to the Interrupt generation and CPU read value.

All GPIOs are fail safe to avoid leakage consumption in any condition even when the ring is off and the external line is logic level high.

3.12 Multi Timer Unit (MTU)

Multi Timer Unit consists of eight timers. Each timer is clocked by MXTAL frequency divided by 8 (which means 2.4 MHz with a 19.2 MHz crystal) or REFCLK (32.768 kHz) inputs.

3.12.1 MTU feature overview

- The Multi Timer Unit provides access to four interrupt generating programmable 32-bit Free-Running decrementing Counters (FRCs) allowing up to four counts to be performed in parallel.
- The FRCs have their own clock input, allowing the counters to run from a much slower clock than the system clock.
- In each FRC the 32-bit counter is split up into two 16-bit counters.

3.13 RTC

This is an always-on power domain dedicated to RTC logic (backup system) with 256 bytes SRAM and supplied with a dedicated voltage regulator.

The RTC provides a high resolution clock which can be used for GPS. It keeps the time when the system is inactive and can be used to wake the system up when a programmed alarm time is reached. It has a clock trimming feature to compensate for the accuracy of the 32.768 kHz crystal and a secured time update.

RTC features:

- 47-bit counter clocked by 32.768 kHz clock
- 32-bit for the integer part (seconds) and 15-bit for the fractional part
- The integer part and the fractional part are readable independently
- The counter, once enabled, can be stopped
- Integer part load register (32-bit)
- Fractional part load register (15-bit)
- Load bit to transfer the content of the entire load register (integer + fractional part) to the 47-bit counter

Once set by the MCU, this bit is cleared by the hardware to signal to the MCU that the RTC has been updated.

3.14 MSP

STA8100GA has one Multi mode Serial Port (MSP).

The following section describes the functionalities of the MSP unit.

The Multi mode Serial Port (MSP) is a synchronous transmitter serial interface.

The MSP provides:

- Element (data) sizes of 8, 10, 12, 14, 16, 20, 24, and 32 bits, LSB or MSB first
- Programmable frequency shift clock for data transfer
- Direct interface to SPI compliant devices
- Transmit first-in, first-out memory buffers (FIFOs), 32 bits wide, 8 locations deep

3.15 Direct Memory Access (DMA)

The DMAC is an Advanced Microcontroller Bus Architecture (AMBA) compliant System-on-Chip (SoC) peripheral. The DMAC is an AMBA AHB module, and connects to the Advanced High-performance Bus (AHB).

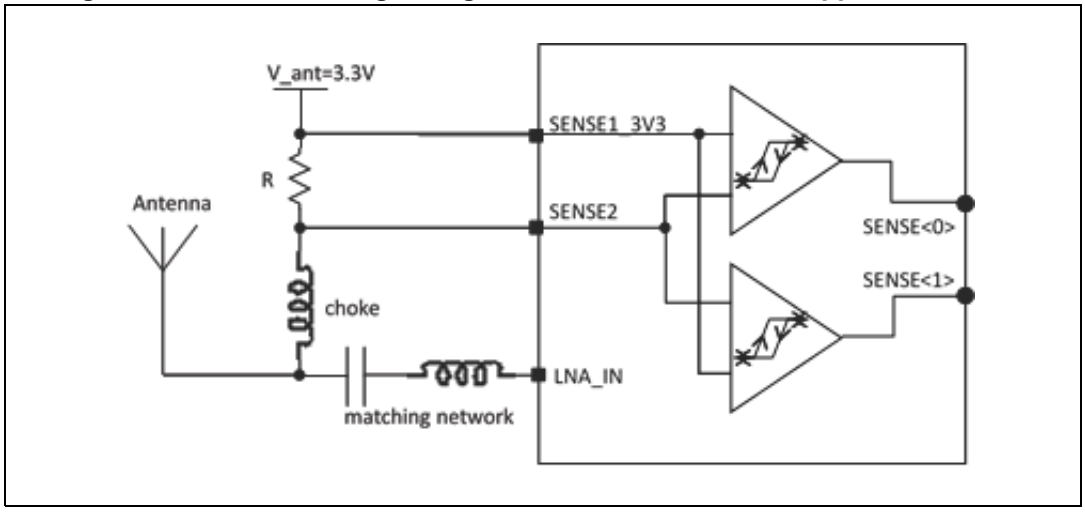
Module key features:

- Eight DMA channels. Each channel can support a unidirectional transfer.
- The DMAC provides 32 peripheral DMA request lines.
- Single DMA and burst DMA request signals.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA support through the use of linked lists.
- Hardware DMA channel priority. DMA channel 0 has the highest priority and channel 31 has the lowest priority.
- If requests from two channels become active at the same time, the channel with the highest priority is serviced first.
- AHB slave DMA programming interface to the DMA control registers.
- Two AHB bus masters for transferring data.
- Programmable DMA burst size.
- Working on AHB clock.

3.16 Antenna sensing

The following figures show how the antenna sensing circuit works. SENSE1 and SENSE2 input voltage range must be between VRF_IN and GND.

Figure 3. Antenna sensing configuration when antenna is supplied with 3.3 V



Antenna sensing detection in STA8100GA uses two comparators with hysteresis. If the antenna is supplied with a voltage of 3.3 V the antenna sensing can be connected as showed in the picture.

The following tables show thresholds when current is rising and when is falling with R = 1.4 Ω and V_ant = 3.3 V.

Table 8. Antenna sensing current - power rising

Current from antenna (when current is rising)	SENSE<1>	SENSE<0>
I < 24 mA	0	0
24 ≤ I ≤ 62 mA	0	1
I > 62 mA	1	1

Table 9. Antenna sensing current - power falling

Current sunk from antenna (when current is falling)	SENSE<1>	SENSE<0>
I > 53 mA	1	1
16 ≤ I ≤ 53 mA	0	1
I < 16 mA	0	0

3.17 Temperature sensor

Thermal sensor provides digital measurement of junction temperature. Temperature measurement range is -40 to 125 °C. It uses integrated bandgap reference and 8-bit ADC.

The temperature sensor provides two threshold registers. Writing in these registers and enabling the threshold mode compare the temperature recorded with the threshold value. If the temperature is higher than the upper threshold register or lower than the lower threshold register, it generates an interrupt if enabled.

Table 10. Temperature sensor

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Tsens	Sensitivity	—	—	—	1	°C
Tacc(1)	Accuracy	Calibration performed at 125°C	+/-3(2)	—	+/-10	°C

1. Best accuracy is at calibrated temperature.
2. Limited by manufacturing calibration environment.

3.18 Serial boot pins

UART2-TX (Boot0) pin is used to select the boot configuration of Cortex® M7. The ROM code starts the boot process which then reads the PRCC register (UART2-TX) which has already latched the UART2-TX pin (C8 ball) status after latch reset.

Based on this register value, the code is loaded from one of the two options as given in the table below:

Table 11. Boot peripheral selection

Pin	ROM action
UART2-TX = 0	Boot from flash memory - SFC controller
UART2-TX = 1	Boot from peripheral - UART

3.19 Reset

After a reset, the Cortex® M7 is woken-up by the ROM code.

The PRCC module is used to sequence through all the steps needed to properly reset the device and prepare it to fetch the first instruction of the user application code.

STA8100GA has the following reset options:

1. Pad reset: SoC will have active low chip reset (RESET) pad. Low (zero) status on this pad will keep device in the reset. Assertion of this pin low should be minimum of 5 ms.
2. Power on reset: The power on reset circuitry is embedded in the main voltage regulator built on HV supply (VCORE_IN) of regulator. It ensures all voltage monitors are under reset state until VCORE_IN (or VDD_EXT_REG) minimum voltage is reached.
3. Hardware resets: The internal voltage regulator embeds multiple LVD (Low Voltage Detector) and HVD (High Voltage Detector) which are used in the reset sequence.
4. Soft reset: Different peripherals present on STA8100GA can be reset independently through registers present inside PRCC module.

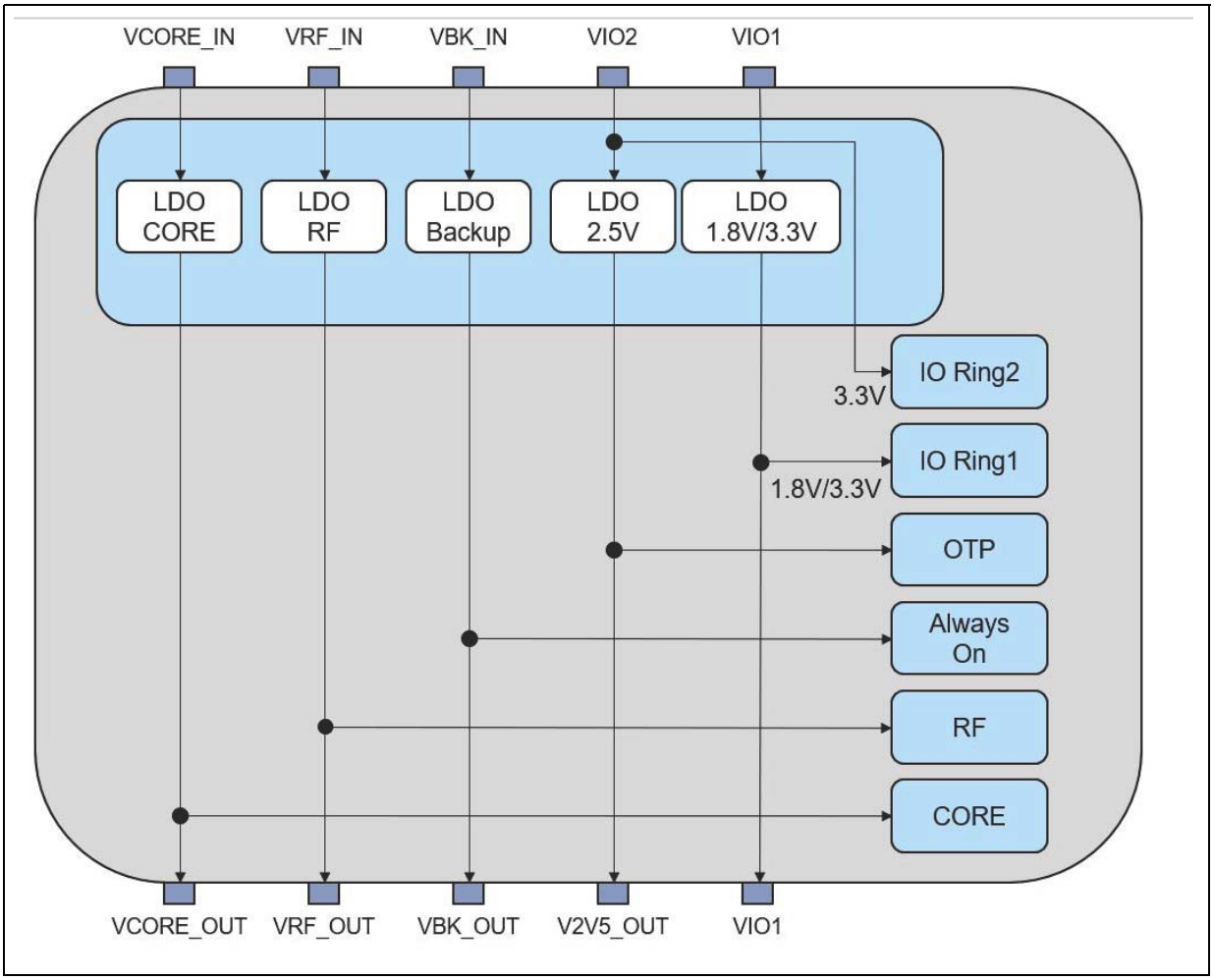
3.20 Power Management Unit (PMU)

STA8100GA embeds five voltage regulators (LDO):

Table 12. LDO on-chip regulators

LDO	Supply regions	Input voltage	Typical output voltage at 25°C
CORE LDO	Core	VCORE_IN = 1.62 – 3.6 V	1.2 V
LDO2v5	Safmem, temp sensor	VIO_IN = 3.3 V	2.5 V
IO LDO	IO ring 1	VIO_IN = 3.3 V	1.8 V
BACKUP LDO	Always on	VBK_IN = 1.62 – 3.6 V	1.2 V
RFLDO	RF	VRF_IN = 1.62 – 3.6 V	1.1 V

Figure 4. LDO on-chip regulators dependencies



3.20.1 Power regions

STA8100GA has six major power regions. The modules present inside each power region are given below.

1. Always on backup region: 1.2 V
   - prcc_backup
   - RTC
   - Backup RAM 256 bytes
2. Switchable region: 1.2 V
   - ARM® core
   - Other digital IPs
3. RF: 1.1 V
4. OTP: 2.5 V
5. IO ring1: 1.8 V or 3.3 V
6. IO ring2: 3.3 V

By default IO ring1 is at 1.8 V supplied by internal LDO IO. If IO ring1 has to be at 3.3 V then external supply must be applied on VIO1 at 3.3 V.

The switchable power region can be supplied by an external voltage regulator directly at pin VDD_EXT_REG. The integrated LDO CORE has to be switched off by forcing EXT_REG_SEL to high voltage.

The usage of the external regulator to supply the switchable power region is mandatory in applications that require to sustain 105 °C.

3.21 CAN interface

CAN sub-system comprises two fully independent FD-CAN controllers: CAN0 and CAN1. Both controllers conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015. Maximum data bit rate supported is 1Mbit/s.

3.22 I2C high speed controller

One I2C high speed controller interface is capable of master/slave modes in multi-master environment. It is DMA capable and multiple baud rates are supported: 100/ 400/ 1000/ 3400 Kbits/s.

3.23 Full speed USB 2.0

It supports 12 Mbps (full speed) and 1.5 Mbps (low speed) serial data transmission according to USB 2.0 OTG controller specification.

4 Electrical specifications

4.1 Absolute maximum ratings

Table 13. Absolute maximum ratings with on chip LDO voltage regulation

Symbol	Parameter	Value		Unit
		Min.	Max.	
VRF_IN	Supply voltages	-0.3	3.9	V
VCORE_IN	Supply voltages	-0.3	3.9	V
VBK_IN	Supply voltages	-0.3	3.9	V
VIO_IN	Supply voltages	-0.3	3.9	V
VDD_EXT_REG(1)	Supply voltages	-0.3	1.4	V
T_J	Junction operating temperature	-40	125	°C
TS	Storage temperature	-55	150	°C
ESDHBM	Electro static discharge – Human Body Model	—	+/-2	kV
ESDCDM(2)	Electro static discharge – Charge Device Model	—	+/-500	V
LU	Latch Up	-100	+100	mA

1. EXT_REG_SEL = high
2. RFA_IN ESDCDM Max is +/-150V. LNA_IN ESDCDM Max is +/-250V

4.2 Thermal data

Table 14. Thermal data

Symbol	Parameter	Value	Unit
T_{AMB}	Ambient operating temperature	- 40 to 105	°C
θ_{JA}(1)	Thermal resistance junction-ambient	33	°C/ W
Ψ_{JC}(2)	Thermal characterization parameter junction-case	3	°C/ W

1. Multilayer 2s2p as per JEDEC JESD51-2
2. JESD51-8

4.3 Electrical characteristics

Table 15. Operating junction temperature range

Parameter	Min.	Typ.	Max.	Units
Junction temperature	-40	27	125	°C

Table 16. VDD_EXT_REG - external core power supply

Parameter	Min.	Typ.	Max.	Units	Comment
External core power supply (VDD_EXT_REG)	1.18	1.25	1.32	V	EXT_SEL_REG = High

Table 17. PMU11 - Functional specifications

Specification	Min.	Typ.	Max.	Units	Comment
LDO_BK					
Input voltage (VBK_IN)	1.7	3.3	3.6	V	—
Output voltage (VBK_OUT)	1.10	1.2	1.26	V	—
Load current at normal mode	—	—	2	mA	—
Load current at deep standby mode	—	—	50	uA	Tamb<27 °C, VBK_IN=1.8 V
LDO power consumption at normal mode (specified by design)	—	—	20	uA	—
LDO power consumption at deep standby mode (specified by design)	—	1	—	uA	Tamb<27 °C, VBK_IN=1.8 V
LDO power down consumption (specified by design)	—	—	1	uA	—
External capacitance (VBK_OUT) (specified by design)	0.5	1	1.2	uF	—
Line regulation	—	—	10	mV	—
Load regulation VO = 1.2 V max at Iout = 0 mA VO = 1.1 V max at Iout = 2 mA	—	—	100	mV	—
Start-up time (specified by design)	—	—	600	µs	—
VBK_IN slew rate	0.04	—	400	ms	In case of VBK_IN slew rate < Min., a 10 Ohm serial resistance is recommended on VBK_IN line

Table 18. PMU12 - Functional specifications

Specification	Min.	Typ.	Max.	Units	Comment
LDO_CORE					
Input voltage (VCORE_IN)	1.71	3.3	3.6	V	—
Output voltage (VCORE_OUT available at balls VDD_EXT_REG)	1.14	1.25	1.30	V	EXT_REG_SEL = low (VDD_EXT_REG)
Load current (mA)	—	—	450	mA	—
LDO power consumption (specified by design)	—	—	200	uA	—
LDO power down consumption (specified by design)	—	—	4	uA	—
External capacitance (VCORE_OUT) (specified by design)	2.35	4.7	6.35	uF	EXT_REG_SEL = low (VDD_EXT_REG)
Line regulation	—	—	10	mV	—
Load regulation	—	—	70	mV	—
Load current transient (specified by design)	—	—	150/100	mA/nS	—
Start-up time (specified by design)	—	15	—	us	—
LDO IO					
Input voltage (VIO2_IN)	3	3.3	3.6	V	—
Output voltage (VIO1_EXT)	1.72	1.80	1.90	V	—
Load current	—	—	90	mA	—
LDO power consumption	—	—	200	uA	—
LDO power down consumption	—	—	4	uA	—
External capacitance (specified by design)	1.1	2.2	3	uF	—
Line regulation	—	—	10	mV	—
Load regulation	—	—	100	mV	—
Load current transient (specified by design)	—	—	90/100	mA/ns	—
Start-up time (specified by design)	—	25	—	us	—
LDO_RF					
VRF_IN	1.62	—	3.6	V	—
VRF_OUT	1	1.15	1.25	V	—
Load Current on VRF_OUT	—	27	—	mA	—

Table 19. Current consumption (T_j = 125 °C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
IBK_Normal	Current consumption at VBK_IN in normal mode	VBK_IN=3.3 V	—	—	1	mA
IBK_DeepStandby	Current consumption at VBK_IN Deep Standby mode	VBK_IN=1.8V Tamb<27 °C	—	—	50	uA
ICORE_Functional_85	Current consumption at VCORE_IN with ST reference application design running	VCORE_IN=3.3 V EXT_REG_SEL=Low Max. ambient temperature=85 °C	—	—	300(1)	mA
ICORE_Functional_105	Current consumption at VDD_EXT_REG with ST reference application design running	VCORE_IN=3.3 V EXT_REG_SEL=High VDD_EXT_REG=1.25 V Max. ambient temperature=105 °C	—	—	400	mA
ICC_VRFIN	Current consumption at VRF_IN	VRF_IN=3.3 V All RF block ON, with VCC_LNA and VCC_PLL connected to VBK_OUT on PCB. Tamb=25 °C	—	28	—	mA
ICC_VRFIN_off	Current consumption at VRF_IN with G5RF in standby (off)	VRF_IN=3.3 V All RF block OFF, with VCC_LNA and VCC_PLL connected to VBK_OUT on PCB. Tamb=25 °C	—	150	—	uA

1. Maximum current at VCORE is limited by maximum junction temperature at 125 °C and θ_{JA} 33 °C/W (which depends on application printed circuit board).

Table 20. RF Electrical characteristics (T_j = 125 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
LNA						
Gp	Power gain	L1 band	—	15	—	dB
		L2- L5 band	—	15	—	
NF	Noise figure(1)	L1 band	—	2.5	—	dB
		L2- L5 band	—	2.5	—	
LNA $P_{\_1dB}$	Input compression point	—	—	-16	—	dBm
RFA − MIXER − IF FILTER – VGA						
GpRFA	RFA voltage gain	Max gain	—	15	—	dB
		Min gain	—	5	—	dB
GC	Conversion gain (from RFA in to ADC input)	VGA & RFA at max gain	—	90	—	dB
		VGA & RFA at min gain	—	40	—	
Δ_{VGA}	VGA dynamic range	—	—	50	—	dB

Table 20. RF Electrical characteristics (T_j = 125 °C) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$P_{\_1dB}$	RF-IF-VGA input compression Point	In band RFA max VGA max	—	-100	—	dBm
		In band RFA max VGA min	—	-50	—	
NF_{RF-IF}	RF-IF-VGA noise figure(1)	VGA & RFA at max gain in L1-L2-L5-L band	—	5	—	dB
BW	-1 dB high freq. corner IF filter	Set corner #1	—	13	—	MHz
		Set corner #2	—	8	—	
ATT	Aliasing frequency rejection	F = 51 MHz (corner #1)	20	—	—	dB
		F = 58 MHz (corner #2)	20	—	—	
Fractional synthesizer – VCO						
TCXO in	TCXO frequency	—	10	26	55	MHz
R_{DIV}	Reference divider range	—	1	—	63	—
N_{DIV}	Loop divider range	—	56	—	2047	—
Frac	PLL fractionality	—	—	18	—	bit
F_{LO}	LO operating frequency	—	2300	—	3300	MHz

1. Specified by design.

Table 21. Electrical characteristics of digital input and output buffers

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Input and output buffers						
V_{IH_1V8}	CMOS input high level	—	$0.65 \times V_{18\_IO}$	—	$0.3 + V_{18\_IO}$	V
V_{IL_1V8}	CMOS input high level	—	- 0.3	—	$0.35 \times V_{18\_IO}$	V
V_{IH_3V3}	CMOS input high level	—	2.0	—	$0.3 + V_{33\_IO}$	V
V_{IL_3V3}	CMOS input high level	—	- 0.3	—	0.8	V
C_{IN}	CMOS input capacitance	—		—	3	pF
V_{OH}	CMOS output high level	at max. IOH	V_{IO} - 0.4	—	—	V
V_{OL}	CMOS output low level	at max. IOL	—	—	0.4	V
I_{OL}/I_{OH} IO ring1 and PPS_OUT	Driving current to sustain VOL/VOH	V_{OL}/V_{OH}	0	—	4	mA
I_{OL}/I_{OH} IO ring2 but PPS_OUT	Driving current to sustain V_{OL}/V_{OH}	V_{OL}/V_{OH}	0	—	2	mA
t_{RISE}(1)	CMOS output rise time with CL = 15 pF, from 10 to 90 %; 3.3 V	2 mA max. current drive	—	3	—	ns
		4 mA max. current drive	—	2	—	

Table 21. Electrical characteristics of digital input and output buffers (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{FALL}(1)	CMOS output fall time with CL = 15 pF, from 10 to 90 %; 3.3 V	2 mA max. current drive	—	3	—	ns
		4 mA max. current drive	—	2	—	

1. Specified by design

4.4 RTC 32.768 kHz oscillator specifications

The 32.768 kHz OSCI32 oscillator is connected between RTC_XTI (oscillator amplifier input) and RTC_XTO (oscillator amplifier output). It also requires two external capacitors of 18 pF (a) as shown in *Figure 5*.

OSCI32 is disabled by default and must be enabled by setting bit28-OSCI_EN of PRCC_BACKUP_REG0 to have 32.768 KHz oscillation when an XTAL pi-network is connected to RTC_XTI/RTC_XTO pins.

The recommended oscillator specifications are shown in the table below:

Table 22. Crystal recommended specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SXTAL}	Crystal frequency	—	32.768	—	kHz
LM_{SXTAL}	Motion inductance	3500	5	6500	kH
CM_{SXTAL}	Motional capacitance	4.0	5.0	6.0	fF
CO_{SXTAL}	Shunt capacitance	1.0	1.3	1.6	pF
ESR	Resonance resistance	—	—	80	kOhm
CL	External load capacitance	—	18 + / - 2 %	—	pF
	External load capacitance (frequency variation < 80 ppm)		18 + / - 2 %		

The oscillator amplifier specifications are shown in the following table:

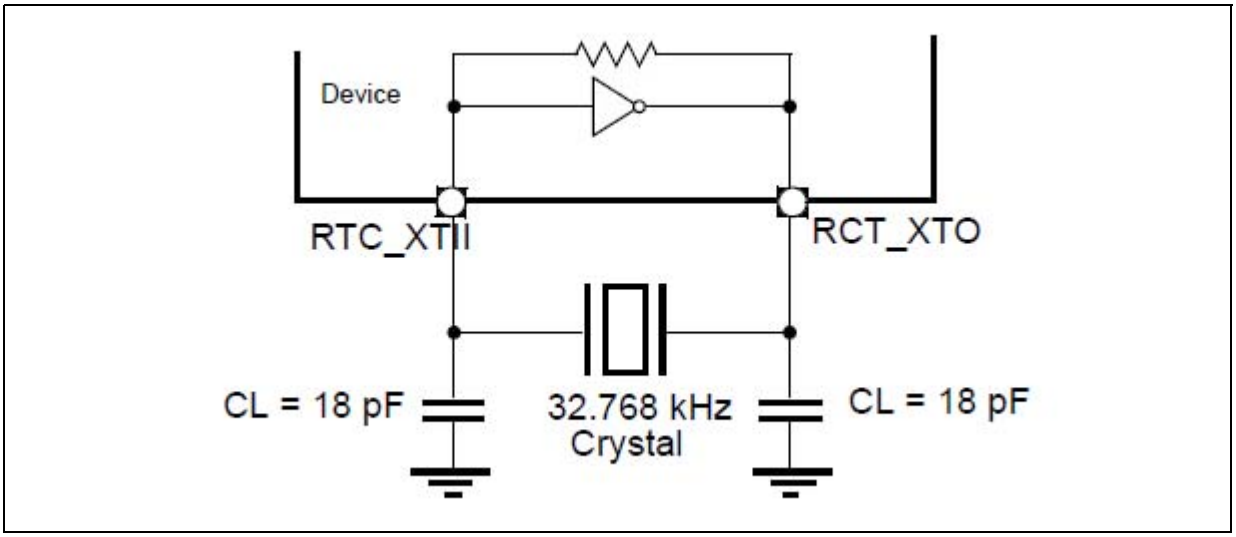
Table 23. Oscillator amplifier specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_S	Startup time(1)	—	0.3	0.6	s
DL	Drive level(1)	—	—	< 0.1	uW
RLC	Required load capacitance(1)	—	12.5	—	pF
GO	Startup conductance	22.5	33.6	60	uA/V

1. Not tested in production.

a. Using crystal with recommended characteristics as per *Table 22*.

Figure 5. 32.768 kHz crystal connection



To drive the 32.768 kHz crystal pins from an external clock source:

- Disable the oscillator (bit28-OSCI_EN = 0b in PRCC_BACKUP_REG0 register). This disables the internal inverter, thus reducing the power consumption to minimum.
- Drive the RTC_XTI pin with a square signal or a sine wave.

Table 24. Characteristics of external slow clock input

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{JIT} (CC)	Cycle-to-cycle jitter	-70	—	70	ps
T_{JIT} (per)	Period jitter	-70	—	70	ps
—	Variation	-500	—	500	ppm
T_{DUTY}	Duty cycle	45	—	55	%

4.5 Power up timing sequence

Figure 6. Power up timing diagram

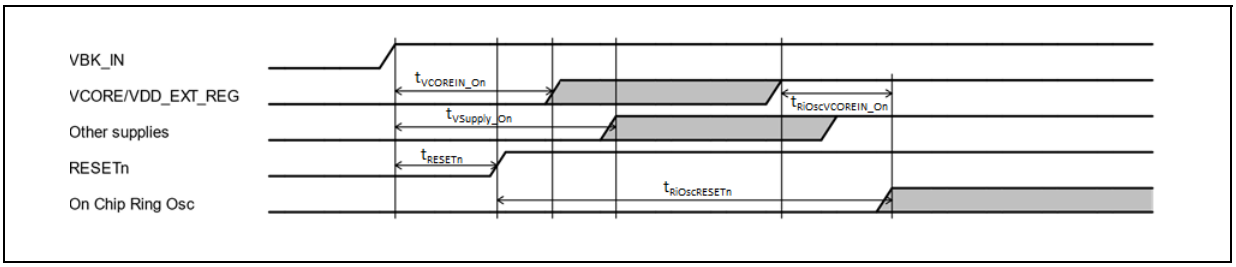


Table 25. Power up timing data

Symbol	Condition	Min.	Max.	Unit	Comment
$t_{VCORE\_IN\_On}$	VBK_IN>1.7 V	0		ms	Simultaneous power on of VBKIN and VCORE_IN/VDD_EXT_REG
$t_{VSupply\_On}$	VBK_IN>1.7 V	0		ms	Simultaneous power on of VBKIN and other supplies is allowed
t_{RESETn}	VBK_IN>1.7 V	4		ms	—
$t_{RiOscRESETn}$	VCORE_IN>1.7 V or VDD_EXT_REG>1.15 V	0.5	—	ms	—
$t_{RiOscVCOREIN\_On}$	RESETn = high	0.5	—	ms	—

4.6 Digital interface AC timing characteristics (specified by design)

Figure 7. Clock block diagram

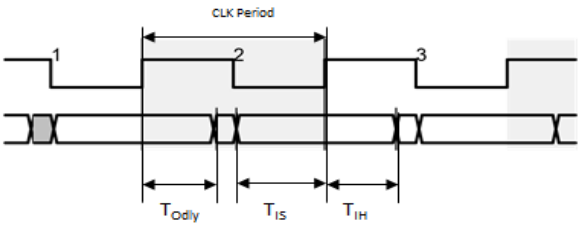


Table 26. Clock data

Symbol	Comment
CLK period	Clock time period
t_{Odly}	Output data delay from rising clock edge, unless differently specified
t_{IS}	Input data setup time to rising clock edge, unless differently specified
t_{IH}	Input data hold time from rising clock edge, unless differently specified

4.6.1 SQIO

Table 27. SQIO SDR mode (feedback mode)

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	—	78.5	MHz	25 pF	—
	CLK period	12.74	—	ns	—	—
	CLK duty cycle	40	60	%	—	—

Table 27. SQIO SDR mode (feedback mode) (continued)

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Input	TIS	0.5	—	ns	—	—
	TIH	2.5	—	ns	—	—
Output	Todly	-2.5	2.4	ns	25 pF	—

Table 28. SQIO DTR mode (DQS mode for flash read)

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	—	65	MHz	25 pF	65 MHz is the flash write frequency
	CLK period	15.38	—	ns	—	—
	CLK duty cycle	40	60	%	—	—
Input	TIS	0	—	ns	—	—
	TIH	0	—	ns	—	
Output	Todly	-1.25	1.8	ns	25 pF	—

4.6.2 SPI

Table 29. SPI (master mode)

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	—	19.625	MHz	25 pF	—
	CLK period	50.95	—	ns	—	—
	CLK duty cycle	40	60	%	—	—
Input	TIS	10	—	ns	—	—
	TIH	2	—	ns	—	—
Output	Todly	2	10	ns	25 pF	—

4.6.3 MSP master mode

Table 30. MSP0 master mode

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	—	9.8125	MHz	25 pF	—
	CLK period	101.9	—	ns	—	—
	CLK duty cycle	40	60	%	—	—
Input	TIS	10	—	ns	—	—
	TIH	4	—	ns	—	—
Output	Todly	0	10	ns	25 pF	—

Table 31. MSP0 slave mode

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	—	9.8125	MHz	25 pF	—
	CLK period	101.9	—	ns	—	—
	CLK duty cycle	40	60	%	—	—
Input	TIS	10	—	ns	—	—
	TIH	4	—	ns	—	—
Output	Todly	0	14.5	ns	25 pF	—

Table 32. MSP1 slave mode

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	—	9.8125	MHz	25 pF	—
	CLK period	101.9	—	ns	—	—
	CLK duty cycle	40	60	%	—	—
Input	TIS	7	—	ns	—	—
	TIH	4	—	ns	—	—
Output	Todly	0	14	ns	25 pF	—

4.6.4 JTAG

Table 33. Default JTAG mode

Type	Symbol	Min.	Max.	Unit	C_{load}	Notes
Clock	CLK freq.	—	26	MHz	25 pF	—
	CLK period	38.4	—	ns	—	—
	CLK duty cycle	40	60	%	—	—
Input	TIS	5	—	ns	—	—
	TIH	5.5	—	ns	—	—
Output	Todly	-3	15	ns	25 pF	—

4.6.5 USB - low speed and full speed mode

Table 34. Low speed and full speed mode

Symbol	Parameter	Condition	Values		Unit
			Min.	Max.	
Full-speed mode					
TR	Output rise time	50 pF differential cap load specified by design	4	20	ns
TF	Output fall time		4	20	ns
TRFM	Rise time and fall time mismatch		90	115	%
VCRS	Output signal crossover voltage		1.3	2	V
Low-speed mode					
TR	Output	50 pF differential cap load specified by design	75	300	ns
TF	Output		75	300	ns
TRFM	Rise		80	125	%
VCRS	Output		1.3	2	V

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.1 LFBGA81 package information

Figure 8. LFBGA81 package outline

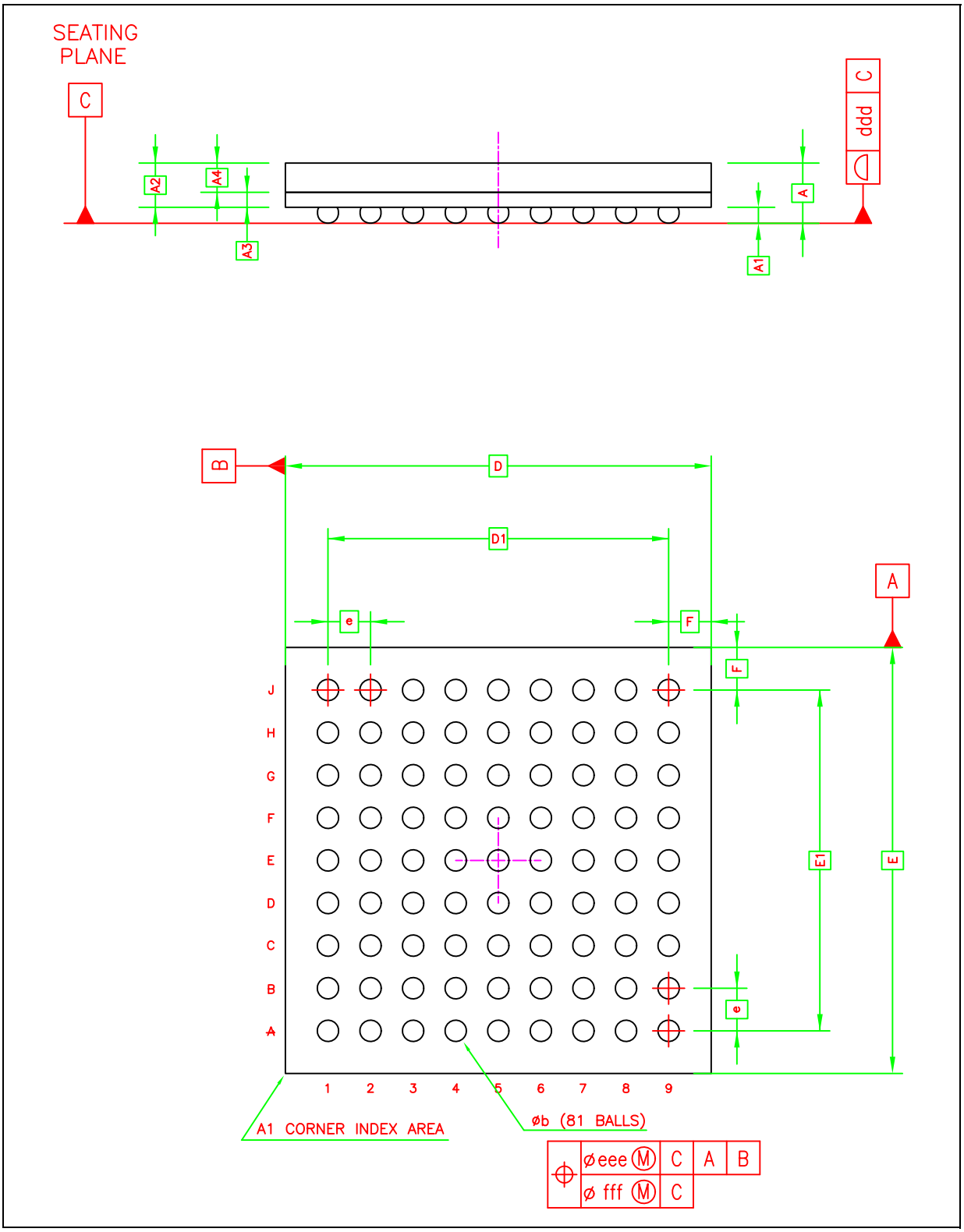


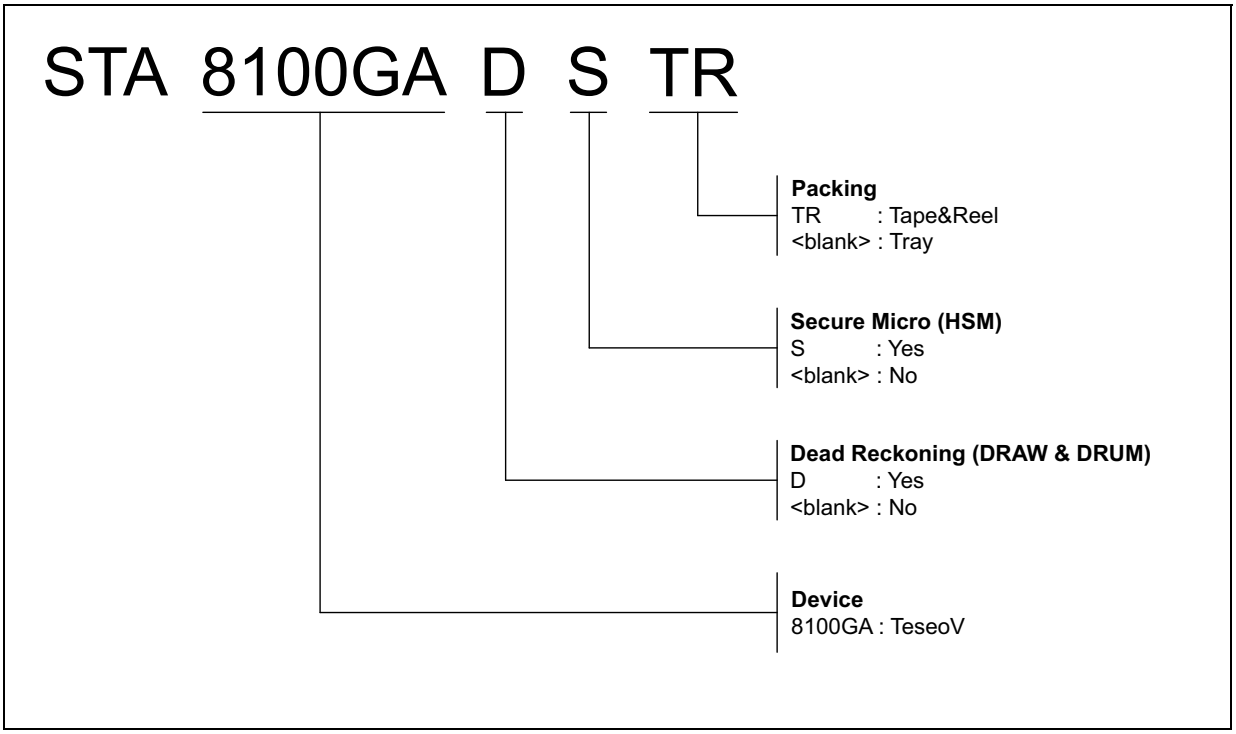
Table 35. LFBGA81 package mechanical data

Ref	Dimensions (mm)		
	Min.	Typ.	Max.
A(1)	—	—	1.70
A1	0.25	—	—
A2	—	0.86	—
A3	—	0.27	—
A4	—	—	0.62
b(2)	0.35	0.40	0.45
D	7.85	8.00	8.15
D1	—	6.40	—
E	7.85	8.00	8.15
E1	—	6.40	—
e	—	0.80	—
F	—	0.80	—
ddd	—	—	0.10
eee(3)	—	—	0.15
fff(4)	—	—	0.08

1. LFBGA stands for Thin profile Fine Pitch Ball Grid Array:
   Thin profile: 1.2 mm < A Max≤ 1.7 mm / Fine pitch: e < 1.00 mm.
   The total profile height (Dim A) is measured from the seating plane “C” to the top of the component.
   The maximum total package height is calculated by the RSS (Root Sum Square) methodology:
   A Max = A1 Typ + A3 Typ + A4 Typ + $\sqrt{(A1^2 + A3^2 + A4^2}$ tolerance values).
2. The typical ball diameter before mounting is 0.40 mm.
3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
4. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

6 Ordering information

Figure 9. Ordering information scheme



7 Revision history

Table 36. Document revision history

Date	Revision	Changes
13-May-2019	1	Initial release
29-Oct-2020	2	Cover page – Changed datasheet classification to Production data – Changed AEC-Q100 qualification to Qualified. – Removed the R in a circle superscript symbol that was inserted after “STMicroelectronics” – Added “for 85 °C maximum ambient temperature operations or 1.2V +/-5 % external voltage supply for 105 °C maximum ambient temperature operations” to bullet starting with “Main voltage domain 1.7 V to 3.6 V with LDO...” – Updated the IO-Ring 2 bullet with +/-10 % after the 3.3 V value – Removed “Hyper SPI Flash and RAM controller” – ESD voltage updated to 500V and other minor editorial changes. – Serial interface / UART updated to 3 – Removed “2x On the Fly decryptor engines” – Removed “Embedded hardware security micro enhanced” – USB2.0 full speed updated to 12 Mb/s *Table 1: Power supply pins*: Updated the from “Backup power may....after.” to “Backup p ower shall....after”. *Table 2: Main function pins*: – Updated EXT_REG_SEL, RTC_XTI and RTC_XTO’s IO voltage data – Updated footnote – Updated the text from “Input..... clock circuit.” to “If 32 kHz.....then input of.....amplifier circuit..... clock counter circuitry.” – Added a note, “If VCORE_IN is.....HIGH level,..... enter Standby mode.” *Table 3: RF front-end pins*: Updated Symbol name for ANTSens1 and ANTSens2 and change IO voltage for LNA_IN,LNA_OUT,RFA_IN and TCXO_IN. *Table 6: Communication interface pins*: Extensive update

Table 36. Document revision history (continued)

Date	Revision	Changes
29-Oct-2020 (contd.)	2	*Table 7: GNSS user cases*: – Updated table. – Updated note “Maximum 72 satellites tracked simultaneously.” to “Maximum 64 satellites tracked simultaneously.” *Table 10: Temperature sensor*: Updated Min. value and added a second footnote. *Table 12: LDO on-chip regulators*: updated Typ.output voltage @25C column *Table 13: Absolute maximum ratings with on chip LDO voltage regulation*: Updated TS max. value *Table 14: Thermal data*: – Updated θ_{JA} parameter and value – Updated Ψ_{JC} parameter *Table 16: VDD_EXT_REG - external core power supply*: updated min, typ and max values. *Table 17: PMU11 - Functional specifications*: Extensive update *Table 18: PMU12 - Functional specifications*: Extensive update *Table 19: Current consumption (T_j = 125 °C)*: – Removed the ICORE_Dynamic row, ICC_VLNA, ICC_VPLL. – Updated test condition and Typ. value for ICC_VRFIN – Added a row for ICC_VRFIN_off – Removed IVIO1_EXT and IVIO2_IN *Table 20: RF Electrical characteristics (T_j = 125 °C)*: Extensive update *Table 21: Electrical characteristics of digital input and output buffers*: Added. *Table 26: Clock data*: Updated the symbol from “T_{IS} and T_{IH}” to “T_{JS} and T_{JH}” respectively. *Table 34: Low speed and full speed mode*: Replaced “high” with “full”. *Table 48: Order codes* Replaced “tray” with “tape” *Figure 1: STA8100GAS block diagram*: Updated

Table 36. Document revision history (continued)

Date	Revision	Changes
29-Oct-2020 (contd.)	2	*Figure 2: Device ballout*: – Replaced CAN0_RX and CAN0_TX with GPIO6 and GPIO5 respectively. – Replaced SPI_CS, SPI_SI, and SPI_SO with JTAG-TMS, JTAG-TDI, and JTAG-TDO respectively. – Replaced PPS_OUT, and SPI_CK with JTAG-TRSTn, and JTAG-TCK respectively. – Replaced SFC_ECS with GPIO67. – Updated TP_IF_N, TP_IF_P, and EOUT0 with TP_IF_N/ ANTSens1/ AIN0, P_IF_P/ ANTSens2/ AIN1, and PPS_OUT respectively. – Updated footnote from “Balls all have alternate..... functions A.” to “Balls all have.....registers”. *Figure 4: LDO on-chip regulators dependencies*: updated *Figure 7: Clock block diagram*: added *Section 3.2: RF front end (G5RF)*: Updated the text from “The RF_IF chain..... 2-bit ADC.....(MAG) bit.” to “The RF_IF..... 3-bit ADC.....(MAG1, MAG0) bit”. *Section 3.5.2: APB bridge 1 peripherals*: Removed mail box and OTFDEC peripherals. *Section 3.16: Antenna sensing*: Updated section introduction paragraph. *Section 3.19: Reset*: Extensive update *Section 4.4: RTC 32.768 kHz oscillator specifications*: – Added section *Section 4.6: Digital interface AC timing characteristics (specified by design)*: Updated the section title from “Interface AC timing characteristics” to “Interface AC timing characteristics (guaranteed by design).” *Section 4.6.5: USB - low speed and full speed mode*: Replaced “high” with “full”. Removed sections related to Safety requirement, Hyperbus, HSM, OTP and OTFDEC.
23-Nov-2020	3	Public version on STMicroelectronics site. Updated *Table 7: GNSS user cases*.

Table 36. Document revision history (continued)

Date	Revision	Changes
7-Oct-2021	4	Following are the changes in this revision of the Datasheet: Updated all occurrences of “guaranteed by design” to “specified by design” in the document. Removed information related to SDMMC. *Section : Features*: – Added a bullet for Hardware Security Module (HSM). – Added a bullet for ST-DRAW. – Removed bullet for SDMMC (Secure Digital Multi Media Card Controller). *Section : Description*: Added a statement for security feature and TESEO-DRAW. *Section 1: Overview*: Updated to add statements related to HSM feature. *Figure 1: STA8100GAS block diagram*: Updated the block diagram and added a note. *Table 6: Communication interface pins*: Extensive update in the values of the table. Added footnote. *Section 3.10: Watchdog Timer (WDT)*: Updated to add HW reset in the description. *Figure 4: LDO on-chip regulators dependencies*: Updated the block diagram. *Table 16: VDD_EXT_REG - external core power supply*: Updated Min. and Max. voltage values. *Table 17: PMU11 - Functional specifications*: Removed rows for ILVDBK, ILVDCORE_BK, OLVDBK, OHVDBK, OLVDCORE_BK. Added “specified by design” for some parameters in Specification column. *Table 18: PMU12 - Functional specifications*: Removed rows for IVLDCORE, OLVDCORE, OHVDCORE, OLVDBK_CORE, OLVDRF, ILVDIO2, OLVDIO1 and OHVDIO1. Added “specified by design” for some parameters in Specification column. *Table 19: Current consumption (T_j = 125 °C)*: Added a row for ICORE_functional_105. Updated information related to ICORE_Functional_85. Added a footnote. *Table 22: Crystal recommended specifications*: Removed footnote. *Table 28: SQIO DTR mode (DQS mode for flash read)*: Added table. *Section 6: Ordering information*: Removed the table for order codes. *Figure 9: Ordering information scheme*: Added the diagram.

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