7mΩ, 100V, N-Channel Power MOSFET SRT10N070L

General Description

The Sanrise SRT10N070L is a low voltage power MOSFET, fabricated using advanced split gate trench technology. The resulting device has extremely low on resistance, low gate charge and fast switching time, making it especially suitable for applications which require superior power density and synchronous rectification.

The SRT10N070L break down voltage is 100V and it has a high rugged avalanche characteristics. The SRT10N070L is available in PDFN5*6 package.

Features

- Ultra Low $R_{DS(ON)\_TYP}$ = 5.2mΩ@V_{GS} = 10V.
- Ultra Low Gate Charge, Qg=38.9nC typ.
- Fast switching capability
- Robust design with better EAS performance
- Non-automotive Qualified

Application

- Charger / Adapter
- PD
- High Power Supply
- E-Tools

Symbol

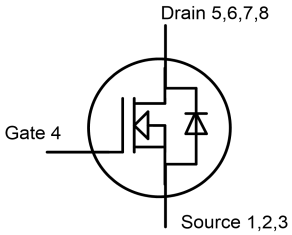
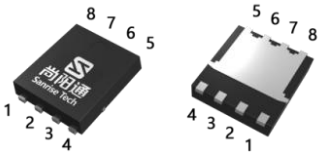


Figure 1 Symbol of SRT10N070L

Package Type



DFN5*6

Figure 2 Package Type of SRT10N070L

Ordering Information

SRT10N070L□□–□

Circuit Type

Package
D56: PDFN5*6

E: Lead Free
G: Green

Blank: Tube
TR: Tape & Reel

Package	Part Number	Marking ID	Packing Type
PDFN5*6	SRT10N070LD56TR-G	SRT10N070LD56G	Tape & Reel

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Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_C=25ºC	I_D	84	A
	T_C=100ºC		53	
Pulsed Drain Current (Note 2)		I_{DM}	336	A
Power Dissipation (T_C = 25°C)		P_D	96	W
Avalanche Energy, Single Pulse (Note 3)		E_{AS}	36	mJ
Avalanche Destructive Energy, Single Pulse (Note 4)		E_{AS_Limit}	256	mJ
Avalanche Energy, Repetitive (Note 2)		E_{AR}	0.04	mJ
Avalanche Current, Repetitive (Note 2)		I_{AR}	18	A
Continuous Diode Forward Current		I_S	84	A
Diode Pulse Current		$I_{S.PULSE}$	320	A
Max Power Dissipation		P_D	96.1	W
Operating Junction Temperature		T_J	150	ºC
Storage Temperature		T_{STG}	-55 to 150	ºC
Lead Temperature (Soldering, 10 sec)		T_{LEAD}	260	ºC

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. I_{AS}= 12.0A, V_{DD}= 50V, R_G= 25Ω, Starting T_J= 25°C
4. I_{AS_Limit}= 32A, V_{DD}= 50V, R_G= 25Ω, Starting T_J= 25°C

Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance，Junction-to-Case	R_{thJC}			1.3	ºC/W
Thermal Resistance，Junction-to-Ambient	R_{thJA}			50	ºC/W

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Electrical Characteristics

T_J = 25℃, unless otherwise specified.

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics							
Drain-Source Breakdown Voltage		BV_{DSS}	V_{GS}=0V, I_D=250uA	100			V
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS}=100V, V_{GS}=0V			1	uA
Gate-Body Leakage Current	Forward	I_{GSSF}	V_{GS}=20V, V_{DS}=0V			100	nA
	Reverse	I_{GSSR}	V_{GS}=-20V, V_{DS}=0V			-100	
Gate Threshold Voltage		$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=0.25mA	1.2	1.8	2.4	V
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS}=4.5V, I_D=20A		7.0	10.0	mΩ
Static Drain-Source On-Resistance		$R_{DS(ON)}$	V_{GS}=10V, I_D=30A		5.2	7.0	mΩ
Gate Resistance		R_G	f=1MHz, Open Drain		1.4		Ω
Dynamic Characteristics							
Input Capacitance		C_{ISS}	V_{DS}=50V, V_{GS}=0V, f=1MHz		2.5		nF
Output Capacitance		C_{OSS}			720		pF
Reverse Transfer Capacitance		C_{RSS}			13		pF
Effective output capacitance, energy related NOTE5		$C_{O(er)}$	V_{GS}=0V, V_{DS}=0…80V		690		pF
Effective output capacitance, time related NOTE6		$C_{O(tr)}$			920		
Turn-on Delay Time		$t_{d(on)}$	V_{DD}=50V, I_D=30A R_G=3.0Ω, V_{GS}=10V		6.5		nS
Rise Time		t_r			4.8		
Turn-off Delay Time		$t_{d(off)}$			22.7		
Fall Time		t_f			7.0		
Gate Charge Characteristics							
Gate to Source Charge		Q_{gs}	V_{DD}=50V, I_D=30A V_{GS}=0 to 4.5V		8.4		nC
Gate to Drain Charge		Q_{gd}			6.8		
Gate Charge Total		Q_g			19.3		
Gate Charge Total		Q_g	V_{DD}=50V, I_D=30A V_{GS}=0 to 10V		38.9		nC
Gate Charge Total, sync FET		Q_g	V_{DD}=0.1V, V_{GS}=0 to 10V		34.6		nC
Reverse Diode Characteristics							
Drain-Source Diode Forward Voltage		V_{SD}	V_{GS}=0V, I_{SD}=30A		0.85	1.1	V
Reverse Recovery Time		t_{rr}	V_R=50V, I_F=30A dI$_F$/dt=100A/us		26		nS
Reverse Recovery Charge		Q_{rr}			21		nC
Peak Reverse Recovery Current		I_{rrm}			1.6		A

Note:

5. $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 80V
6. $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80 V

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Sanrise Technology Limited Company

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