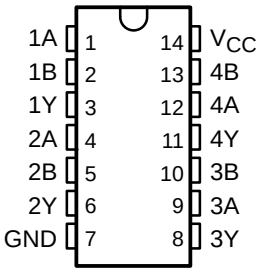
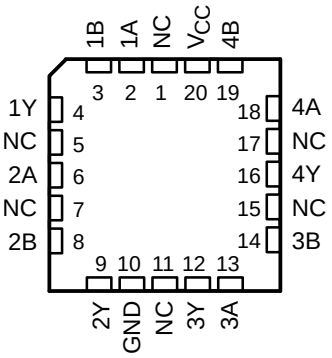
SCLS247A – OCTOBER 1995 – REVISED MARCH 1996

- **Operating Range 2-V to 5.5-V V_{CC}**
- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) Process**
- **High Latch-Up Immunity Exceeds 250 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54AHC32 . . . J OR W PACKAGE
SN74AHC32 . . . D, DB, N, OR PW PACKAGE
(TOP VIEW)



SN54AHC32 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The ’AHC32 are quadruple 2-input positive-OR gates. These devices perform the Boolean function $Y = \overline{\overline{A} \bullet \overline{B}}$ or $Y = A + B$ in positive logic.

The SN54AHC32 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AHC32 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	**B**	**Y**
H	X	H
X	H	H
L	L	L

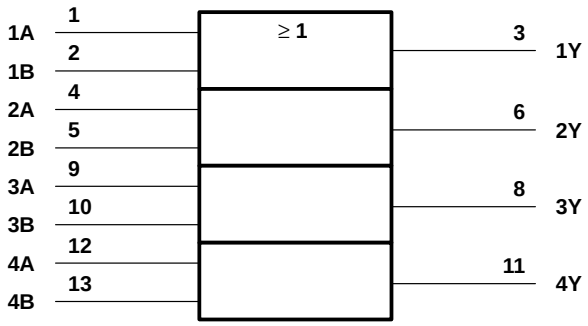
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1996, Texas Instruments Incorporated

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, DB, J, N, PW, and W packages.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): D package . . . . . 1.25 W
DB or PW package . . . . . 0.5 W
N package . . . . . 1.1 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

recommended operating conditions (see Note 3)

			SN54AHC32		SN74AHC32		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		–50		–50	μA
		V_{CC} = 3.3 V ± 0.3 V		–4		–4	mA
		V_{CC} = 5 V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC32		SN74AHC32		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		I_{OH} = –50 μA	2 V	1.9	2		1.9		1.9		V
			3 V	2.9	3		2.9		2.9		
			4.5 V	4.4	4.5		4.4		4.4		
		I_{OH} = –4 mA	3 V	2.58			2.48		2.48		
		I_{OH} = –8 mA	4.5 V	3.94			3.8		3.8		
V_{OL}		I_{OL} = 50 μA	2 V			0.1		0.1		0.1	V
			3 V			0.1		0.1		0.1	
			4.5 V			0.1		0.1		0.1	
		I_{OL} = 4 mA	3 V			0.36		0.5		0.44	
		I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44	
I_I	A or B inputs	V_I = V_{CC} or GND	5.5 V			±0.1		±1		±1	μA
I_{CC}		V_I = V_{CC} or GND, I_O = 0	5.5 V			2		20		20	μA
C_i		V_I = V_{CC} or GND	5 V		2	10				10	pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC32					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}*					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC32					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		5.5	7.9	1	9.5	ns
t_{PHL}					5.5	7.9	1	9.5	
t_{PLH}	A or B	Y	C_L = 50 pF		8	11.4	1	13	ns
t_{PHL}					8	11.4	1	13	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN54AHC32					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}*	A or B	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}*					3.8	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

* On products compliant to MIL-PRF-38535, this parameter is ensured but not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	SN74AHC32					UNIT
				T_A = 25°C			MIN	MAX	
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 15 pF		3.8	5.5	1	6.5	ns
t_{PHL}					3.8	5.5	1	6.5	
t_{PLH}	A or B	Y	C_L = 50 pF		5.3	7.5	1	8.5	ns
t_{PHL}					5.3	7.5	1	8.5	

noise characteristics, V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (see Note 4)

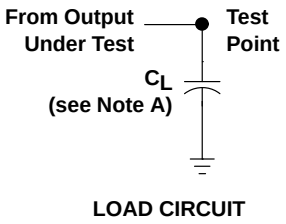
PARAMETER		SN74AHC32			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.3	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.3	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are determined during product characterization and ensured by design for surface-mount packages only.

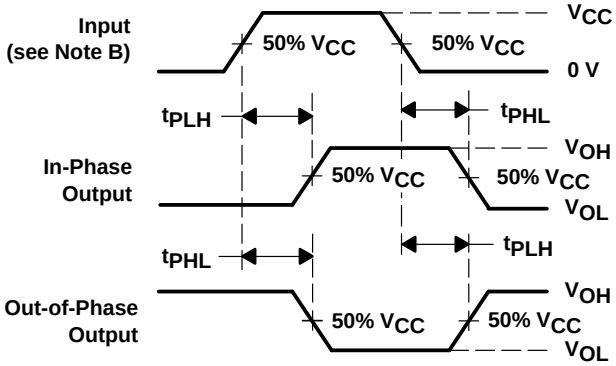
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	14	pF

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated