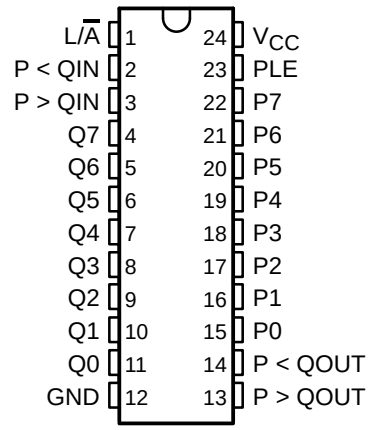
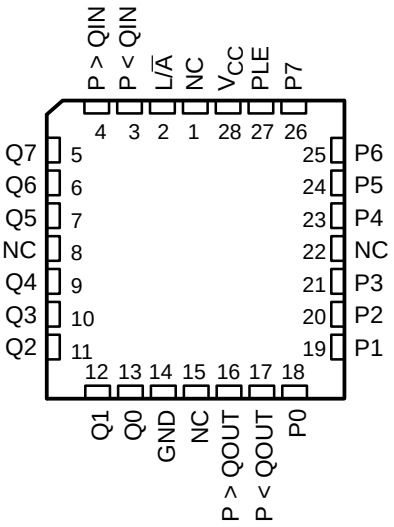
- **Latchable P-Input Ports With Power-Up Clear**
- **Choice of Logical or Arithmetic (Two's Complement) Comparison**
- **Data and PLE Inputs Utilize pnp Input Transistors to Reduce dc Loading Effects**
- **Approximately 35% Improvement in ac Performance Over Schottky TTL While Performing More Functions**
- **Cascadable to n Bits While Maintaining High Performance**
- **10% Less Power Than STTL for an 8-Bit Comparison**
- **Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs**

SN54AS885 . . . JT PACKAGE
SN74AS885 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS885 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These advanced Schottky devices are capable of performing high-speed arithmetic or logic comparisons on two 8-bit binary or two's complement words. Two fully decoded decisions about words P and Q are externally available at two outputs. These devices are fully expandable to any number of bits without external gates. To compare words of longer lengths, the P > QOUT and P < QOUT outputs of a stage handling less significant bits can be connected to the P > QIN and P < QIN inputs of the next stage handling more significant bits. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words. Two alternative methods of cascading are shown in *application information*.

The latch is transparent when P latch-enable (PLE) input is high; the P-input port is latched when PLE is low. This provides the designer with temporary storage for the P-data word. The enable circuitry is implemented with minimal delay times to enhance performance when cascaded for longer words. The PLE, P, and Q data inputs utilize pnp input transistors to reduce the low-level current input requirement to typically –0.25 mA, which minimizes dc loading effects.

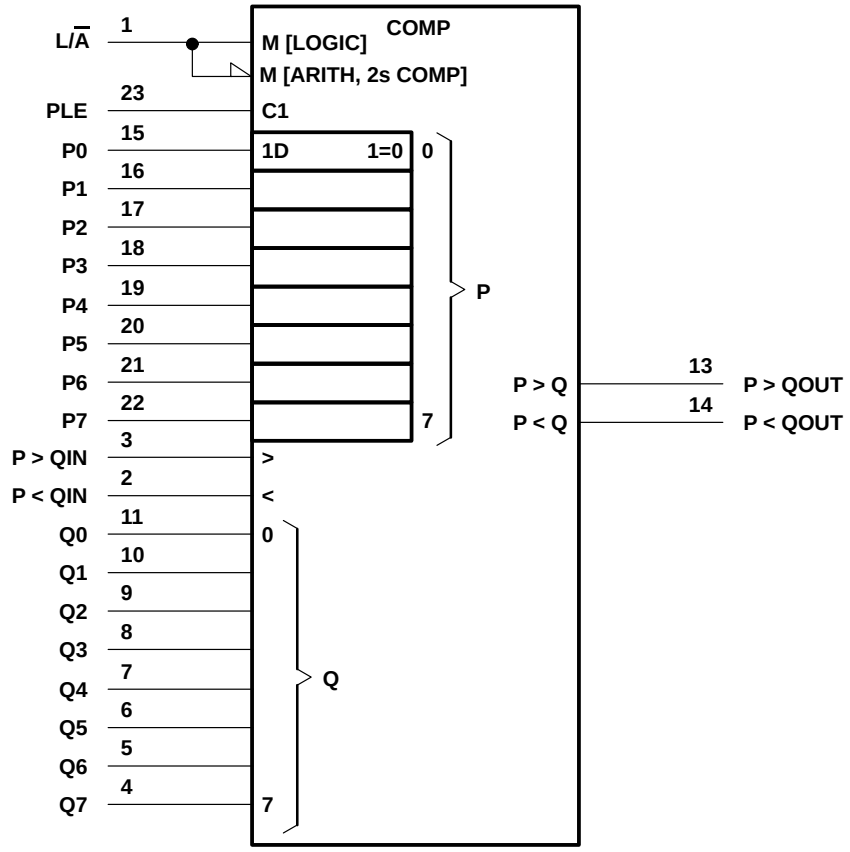
The SN54AS885 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74AS885 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

COMPARISON	INPUTS				OUTPUTS	
	L/$\overline{A}$	DATA P0–P7, Q0–Q7	P > QIN	P < QIN	P > QOUT	P < QOUT
Logical	H	P > Q	X	X	H	L
Logical	H	P < Q	X	X	L	H
Logical†	H	P = Q	H or L	H or L	H or L	H or L
Arithmetic	L	P AG Q	X	X	H	L
Arithmetic	L	Q AG P	X	X	L	H
Arithmetic†	L	P = Q	H or L	H or L	H or L	H or L

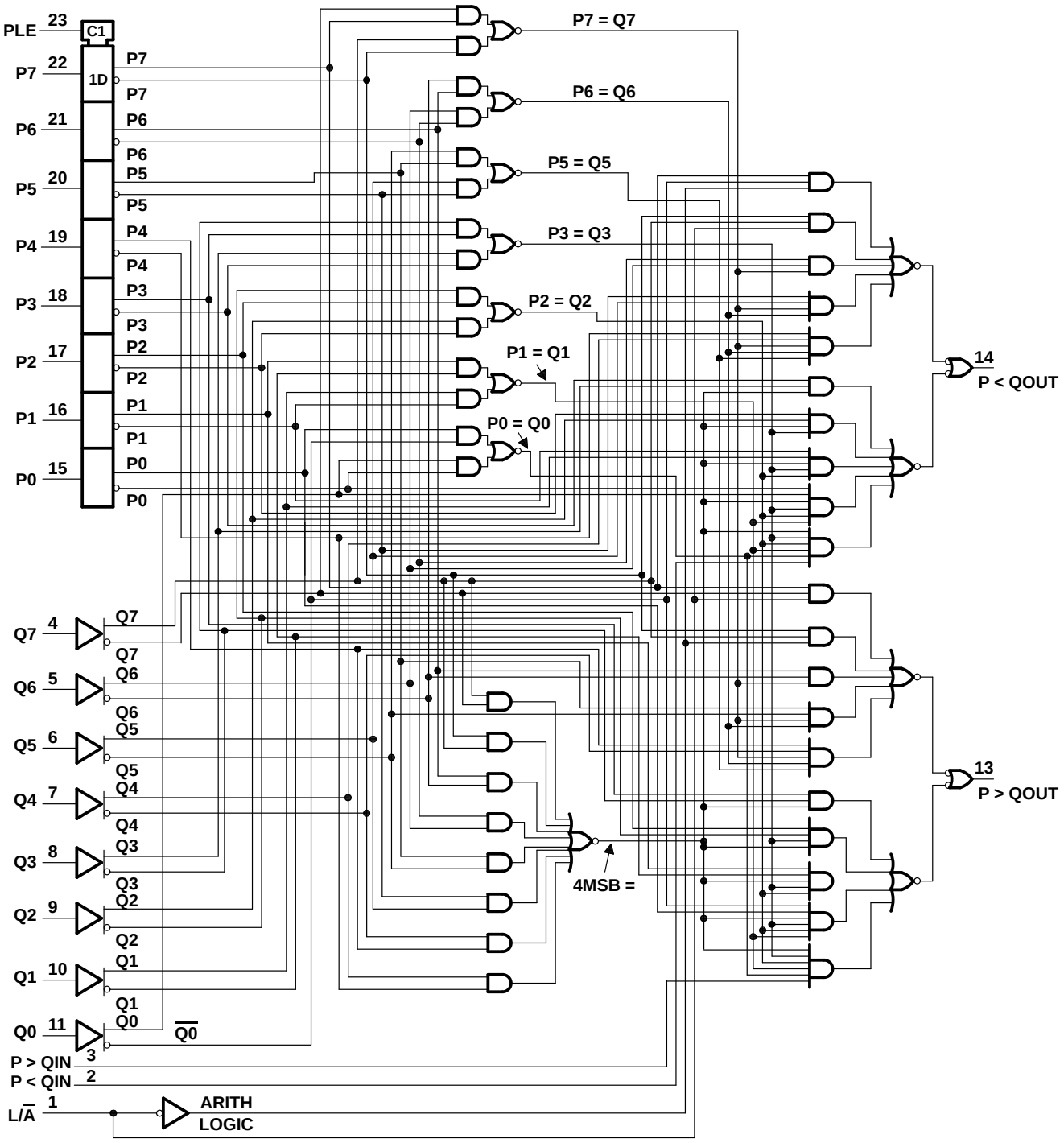
† In these cases, P > QOUT follows P > QIN and P < QOUT follows P < QIN.
AG = arithmetically greater than

logic symbol‡



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DW, JT, and NT packages.

logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A: SN54AS885 . . . . . –55°C to 125°C
SN74AS885 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS885			SN74AS885			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–2			–2	mA
I_{OL}	Low-level output current			20			20	mA
t_{su}*	Setup time, data before PLE↓	2			2			ns
t_h*	Hold time, data after PLE↓	4.5			4			ns
T_A	Operating free-air temperature	–55		125	0		70	°C

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS885			SN74AS885			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC} –2			V_{CC} –2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	L/$\overline{A}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	µA
	Others					20			20	
I_{IL}	L/$\overline{A}$	V_{CC} = 5.5 V,	V_I = 0.4 V			–4			–4	mA
	P > QIN, P < QIN					–2			–2	
	P, Q, PLE					–1			–1	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–20		–112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		130	210		130	210	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with all inputs high except L/$\overline{A}$, which is low.

switching characteristics (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS885			SN74AS885			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	L/$\overline{A}$	P < QOUT, P > QOUT	2	8.5	14	1	8.5	13	ns
t_{PHL}			2	7.5	14	1	7.5	13	
t_{PLH}	P < QIN, P > QIN	P < QOUT, P > QOUT	2	5	10	1	5	8	ns
t_{PHL}			2	5.5	10	1	5.5	8	
t_{PLH}	Any P or Q data input	P < QOUT, P > QOUT	2	13.5	21	1	13.5	17.5	ns
t_{PHL}			2	10	17	1	10	15	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

APPLICATION INFORMATION

The ′AS885 can be cascaded to compare words longer than eight bits. Figure 1 shows the comparison of two 32-bit words; however, the design is expandable to n bits. Figure 1 shows the optimum cascading arrangement for comparing words of 32 bits or greater. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C and use the standard advanced Schottky load of R_L = 500 Ω, C_L = 50 pF.

Figure 2 shows the fastest cascading arrangement for comparing 16-bit or 24-bit words. Typical delay times shown are at V_{CC} = 5 V, T_A = 25°C and use the standard advanced Schottky load of R_L = 500 Ω, C_L= 50 pF.

APPLICATION INFORMATION

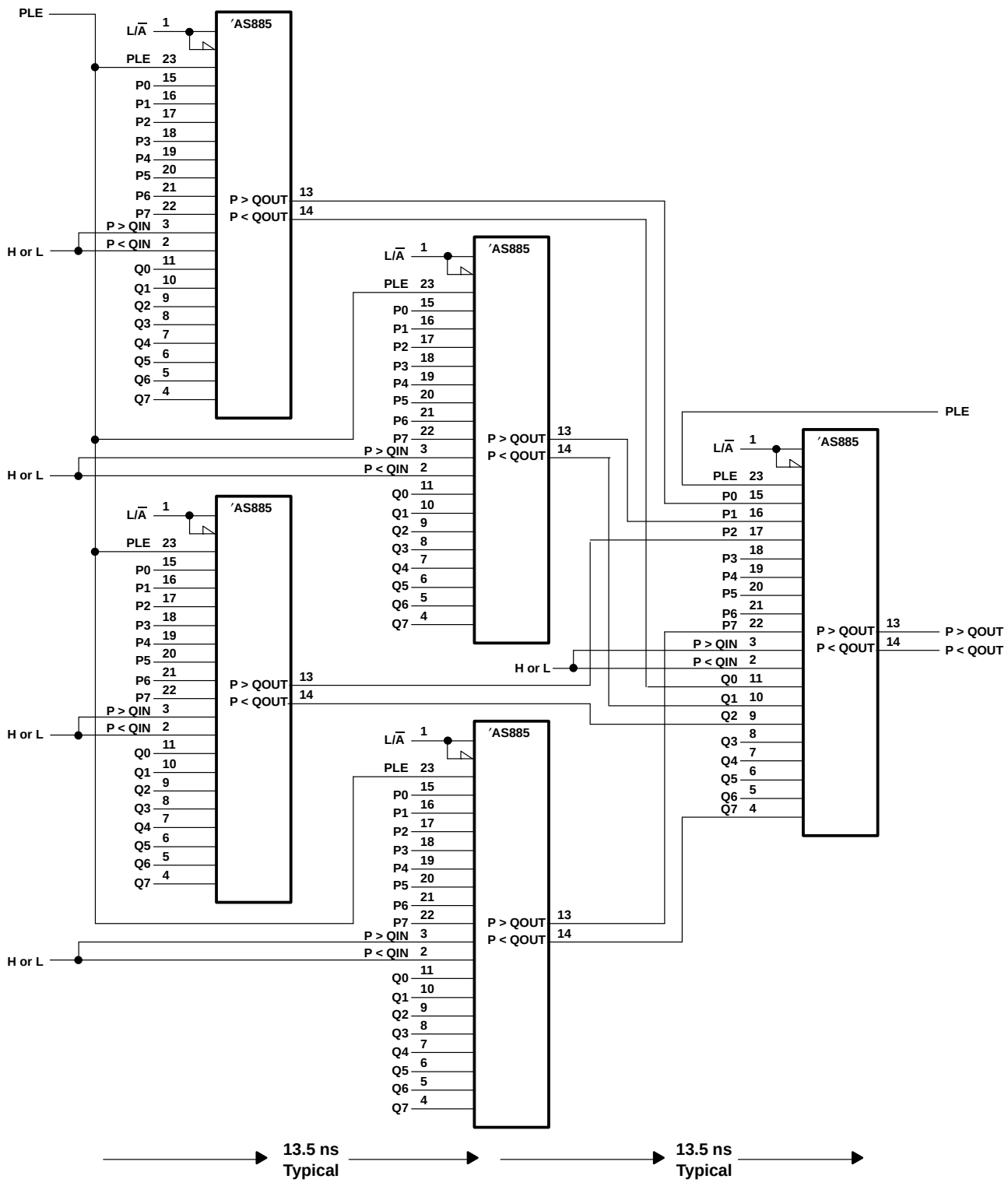


Figure 1. 32-Bit to 72 (n)-Bit Magnitude Comparator

APPLICATION INFORMATION

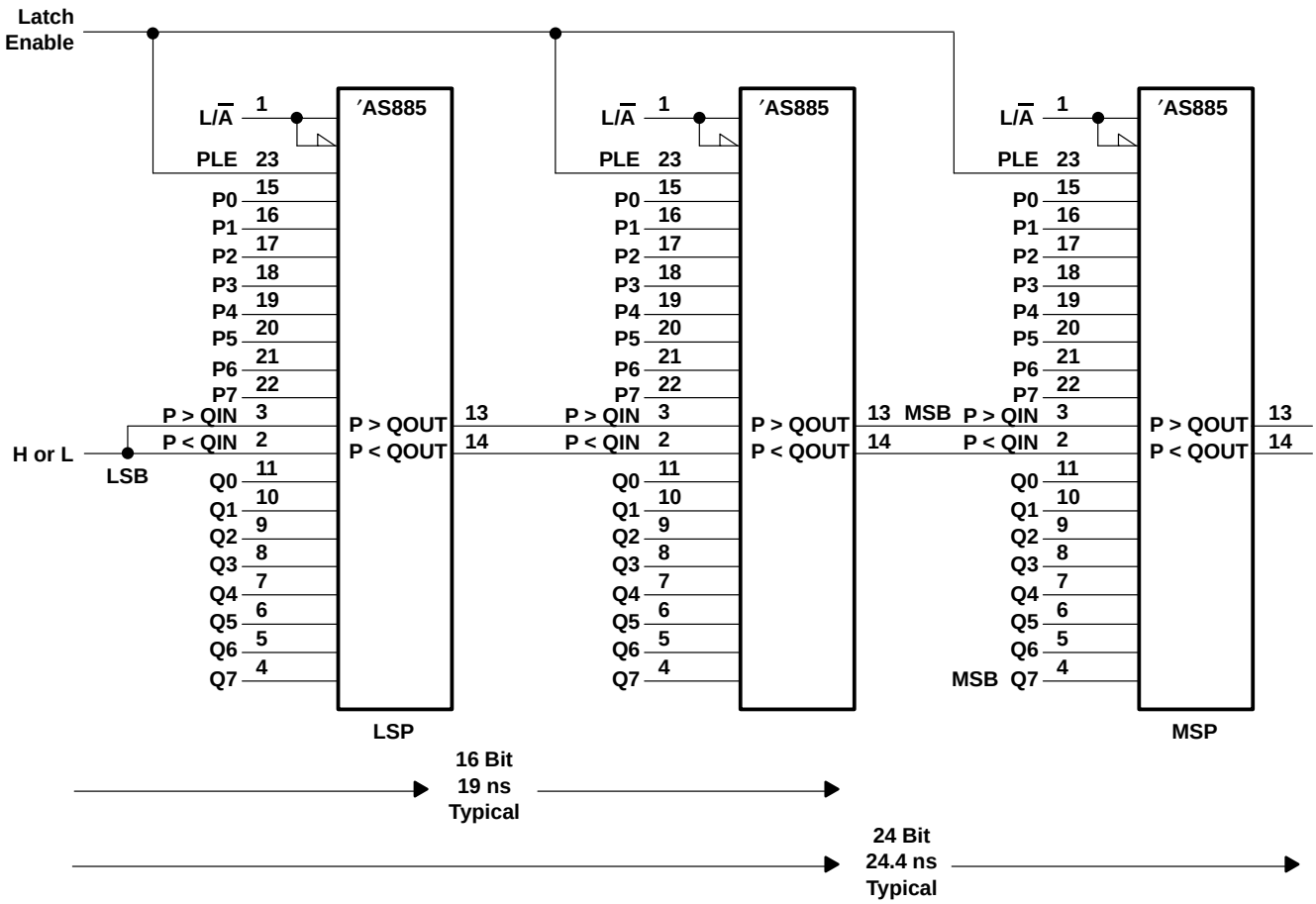
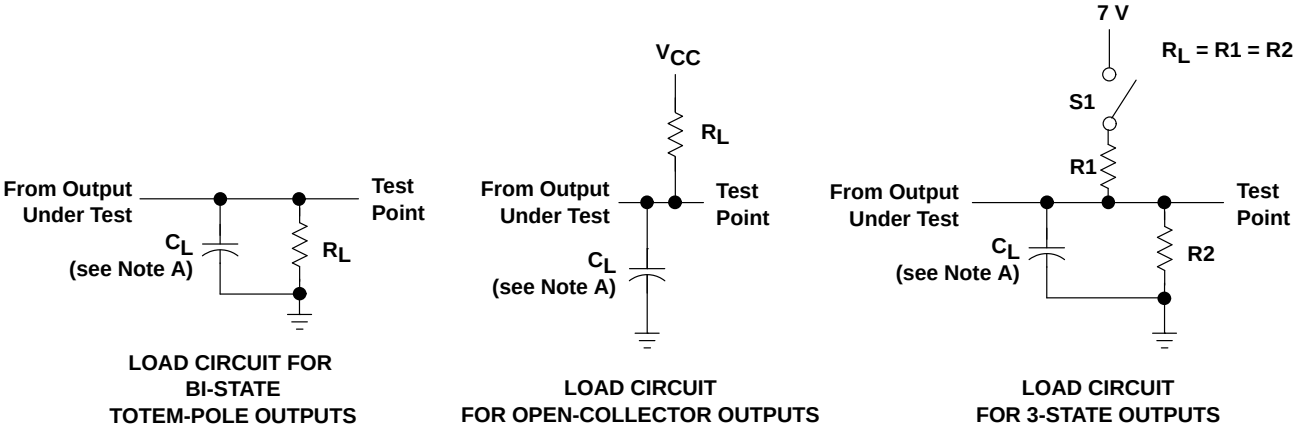


Figure 2. Fastest Cascading Arrangement for Comparing 16-Bit or 24-Bit Words

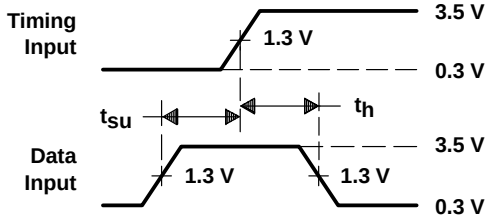
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



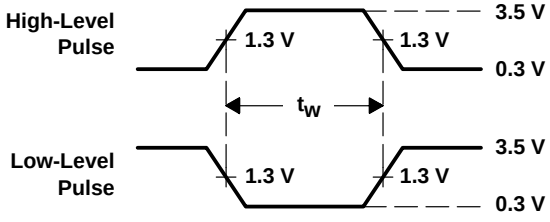
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

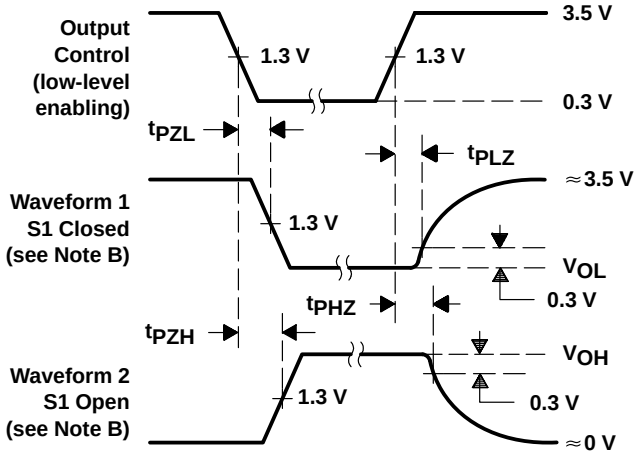
LOAD CIRCUIT FOR 3-STATE OUTPUTS



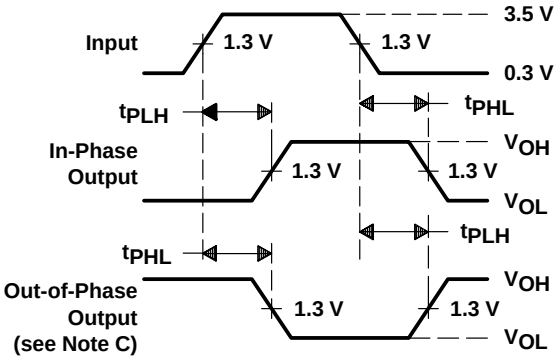
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

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