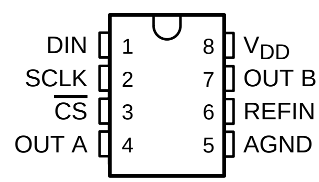
- **Programmable Settling Time to 0.5 LSB 2.5 μs or 12.5 μs Typ**
- **Two 10-Bit CMOS Voltage Output DACs in an 8 Pin Package**
- **Simultaneous Updates for DAC A and DAC B**
- **Single Supply Operation**
- **3-Wire Serial Interface**
- **High-Impedance Reference Inputs**
- **Voltage Output Range . . . 2 Times the Reference Input Voltage**
- **Software Power Down Mode**
- **Internal Power-On Reset**
- **Low Power Consumption:**
  3 mW Typ in Slow Mode
  8 mW Typ in Fast Mode
- **Input Data Update Rate of 1.21 MHz**
- **Monotonic Over Temperature**

applications

- **Battery Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Battery Operated/Remote Industrial Controls**
- **Machine and Motion Control Devices**
- **Cellular Telephones**

D OR P PACKAGE
(TOP VIEW)



description

The TLC5617 is a dual 10-bit voltage output digital-to-analog converter (DAC) with buffered reference inputs (high impedance). The DACs have an output voltage range that is two times the reference voltage, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5617 is over a 3-wire CMOS compatible serial bus. The device receives a 16-bit word for programming and to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The TLC5617C is characterized for operation from 0°C to 70°C. The TLC5617I is characterized for operation from –40°C to 85°C.

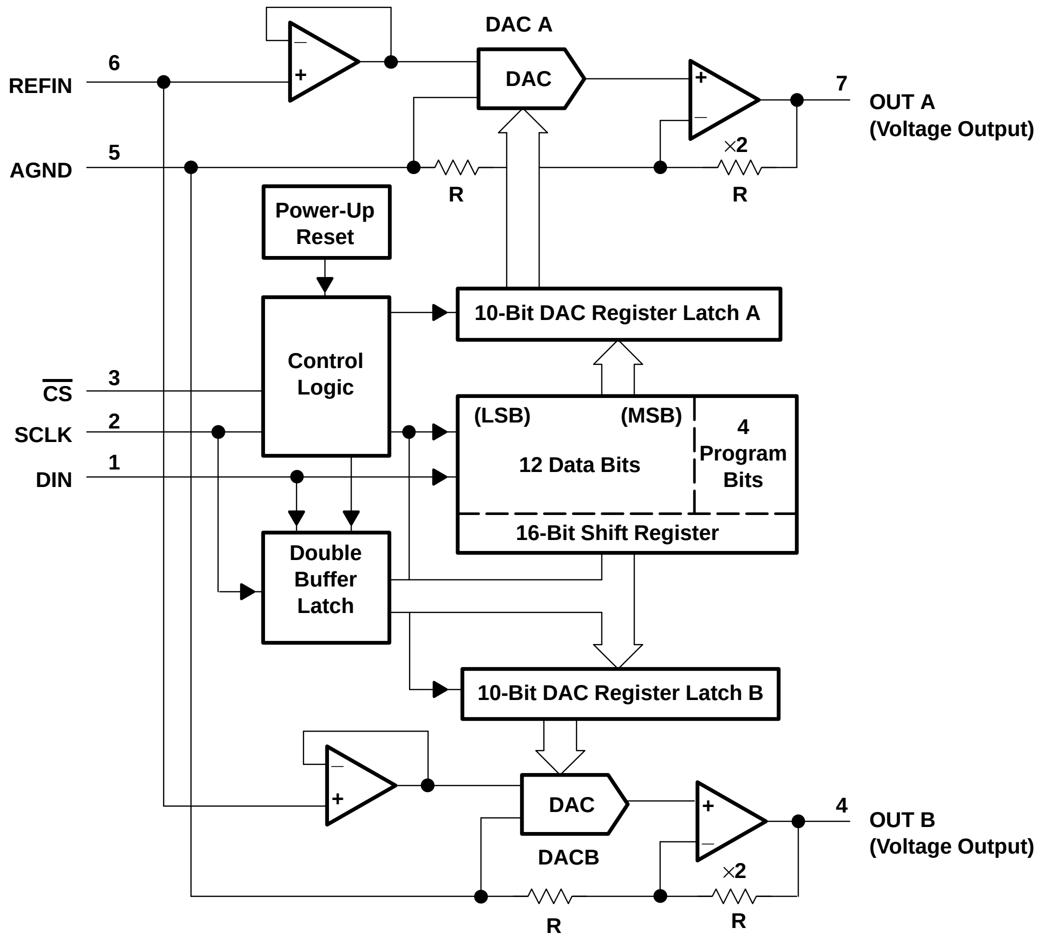
AVAILABLE OPTIONS

T_A	PACKAGE SMALL OUTLINE† (D)	PACKAGE PLASTIC DIP (P)
0°C to 70°C	TLC5617CD	TLC5617CP
–40°C to 85°C	TLC5617ID	TLC5617IP

† Available in tape and reel as the TLC5617CDR and the TLC5617IDR

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corporation.

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
$\overline{CS}$	3	I	Chip select, active low
OUT B	4	O	DAC B analog output
AGND	5		Analog ground
REFIN	6	I	Reference voltage input
OUT A	7	O	DAC A analog output
V_{DD}	8		Positive power supply

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to AGND) . . . . 7 V
Digital input voltage range to AGND . . . . – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range to AGND . . . . – 0.3 V to V_{DD} + 0.3 V
Output voltage at OUT from external source . . . . V_{DD} + 0.3 V
Continuous current at any terminal . . . . ±20 mA
Operating free-air temperature range, T_A: TLC5617C . . . . 0°C to 70°C
TLC5617I . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}	V_{DD} = 5 V	0.7 V_{DD}			V
Low-level digital input voltage, V_{IL}	V_{DD} = 5 V			0.3 V_{DD}	V
Reference voltage, V_{ref} to REFIN terminal		1	2.048	V_{DD} – 1.1	V
Load resistance, R_L		2			kΩ
Operating free-air temperature, T_A	TLC5617C	0		70	°C
	TLC5617I	–40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} (REFIN)= 2.048 V (unless otherwise noted)

static DAC specifications

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution				10			bits
	Integral nonlinearity (INL), end point adjusted		$V_{ref(REFIN)}$ = 2.048 V,	See Note 1			±1	LSB
	Differential nonlinearity (DNL)		$V_{ref(REFIN)}$ = 2.048 V,	See Note 2		±0.1	± 0.5	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)		$V_{ref(REFIN)}$ = 2.048 V,	See Note 3			±3	LSB
	Zero-scale-error temperature coefficient		$V_{ref(REFIN)}$ = 2.048 V,	See Note 4		3		ppm/°C
E_G	Gain error		$V_{ref(REFIN)}$ = 2.048 V,	See Note 5			±3	LSB
	Gain error temperature coefficient		$V_{ref(REFIN)}$ = 2.048 V,	See Note 6		1		ppm/°C
PSRR	Power-supply rejection ratio	Zero scale	See Notes 7 and 8	Slow		80		dB
		Gain		Slow		80		dB
		Zero scale		Fast		80		dB
		Gain		Fast		80		dB

NOTES: 1. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
2. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale-error temperature coefficient is given by: E_{ZS} TC = [E_{ZS} (T_{max}) – E_{ZS} (T_{min})]/V_{ref} × 10^6/(T_{max} – T_{min}).
5. Gain error is the deviation from the ideal output (V_{ref} – 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
6. Gain temperature coefficient is given by: E_G TC = [E_G(T_{max}) – E_G (T_{min})]/V_{ref} × 10^6/(T_{max} – T_{min}).
7. Zero-scale-error rejection ratio (EZS-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Gain-error rejection ratio (EG-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

A OUT and B OUT output specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L = 10 kΩ		0		V_{DD}–0.4	V
	Output load regulation accuracy	$V_{O(OUT)}$ = 2V,	R_L from 10 kΩ to 2 kΩ			0.5	LSB
I_{OSC}	Output short circuit current	$V_{O(A\ OUT)}$ or $V_{O(B\ OUT)}$ to V_{DD} or AGND			20		mA
$I_{O(sink)}$	Output sink current	$V_{O(OUT)}$ > 0.25 V			5		mA
$I_{O(source)}$	Output source current	$V_{O(OUT)}$ < 4.75 V			5		mA

reference input (REFIN)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range			0		V_{DD}–2	V
R_i	Input resistance			10			MΩ
C_i	Input capacitance				5		pF
	Reference feedthrough	REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 9)			–80		dB
	Reference input bandwidth (f–3dB)	REFIN = 0.2 V_{pp} + 1.024 V dc	Slow		0.5		MHz
			Fast		1		MHz

NOTE 9: Reference feedthrough is measured at the DAC output with an input code = 00 hex and a $V_{ref(REFIN)}$ input = 1.024 V dc + 1 V_{pp} at 1 kHz.

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, V_{ref} (REFIN)= 2.048 V (unless otherwise noted) (continued)

digital inputs (DIN, SCLK, $\overline{CS}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±1	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±1	µA
C_i	Input capacitance			8		pF

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Supply voltage, V_{DD}			4.5	5	5.5	V
I_{DD}	Power supply current	V_{DD} = 5.5 V, No load, All inputs = 0 V or V_{DD}	Slow		0.6	1	mA
			Fast		1.6	2.5	
	Power down supply current	D13 = 0 (see Table 3)			1		µA

operating characteristics over recommended operating free-air temperature range, V_{DD} = 5 V ± 5%, $V_{ref(REFIN)}$ = 2.048 V (unless otherwise noted)

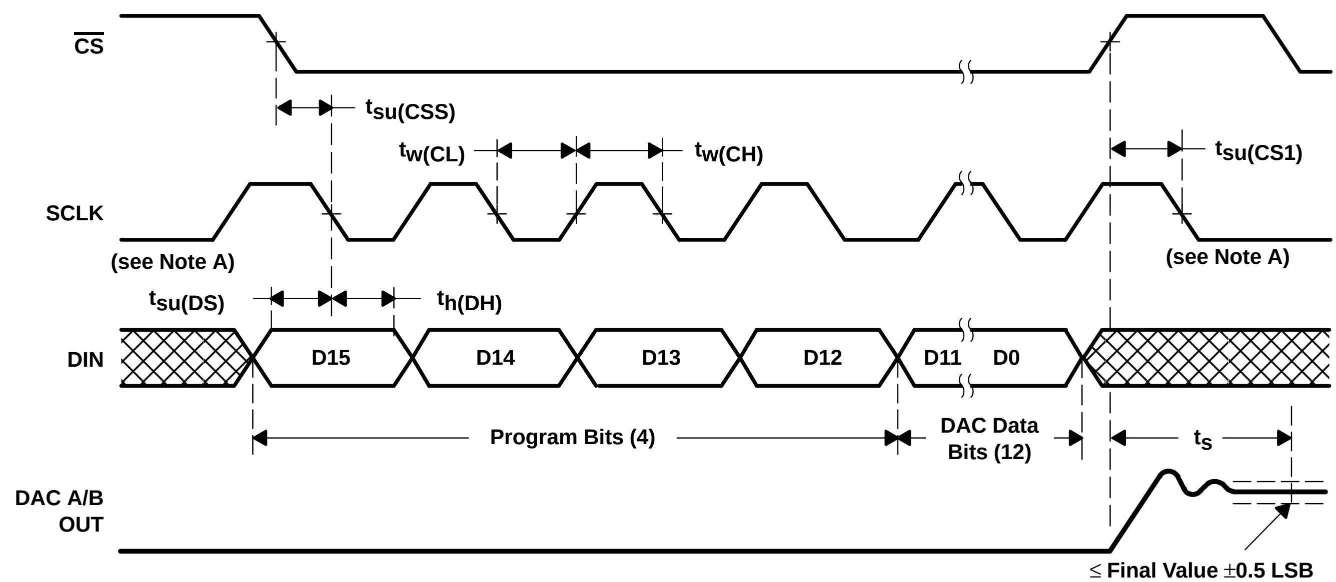
analog output dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Output slew rate	C_L = 100 pF, R_L = 10 kΩ, Code 32 to Code 1024,	$V_{ref(REFIN)}$ = 2.048 V, T_A = 25°C, V_O from 10% to 90%	Slow	0.3	0.5		V/µs
				Fast	2.4	3		
t_s	Output settling time	To ±0.5 LSB, R_L = 10 kΩ,	C_L = 100 pF, See Note 10	Slow		12.5		µs
				Fast		2.5		
$t_{s(c)}$	Output settling time, code to code	To ±0.5 LSB, R_L = 10 kΩ,	C_L = 100 pF, See Note 11	Slow		2		µs
				Fast		2		
	Glitch energy	DIN = All 0s to all 1s, $f_{(SCLK)}$ = 100 kHz	$\overline{CS} = V_{DD}$,			5		nV–s
S/(N+D)	Signal to noise + distortion	$V_{ref(REFIN)}$ = 1 V_{pp} at 1 kHz and 10 kHz + 1.024 V dc, Input code = 10 0000 0000		Slow		78		dB
				Fast		81		

NOTES: 10. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 020 hex to 3FF hex or 3FF hex to 020 hex.
11. Setting time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of one count.

digital input timing requirements

		MIN	NOM	MAX	UNIT
$t_{su(DS)}$	Setup time, DIN before SCLK low	5			ns
$t_{h(DH)}$	Hold time, DIN valid after SCLK low	5			ns
$t_{su(CSS)}$	Setup time, $\overline{CS}$ low to SCLK low	5			ns
$t_{su(CS1)}$	Setup time, $\overline{CS}$ high to SCLK low	5			ns
$t_{w(CL)}$	Pulse duration, SCLK low	25			ns
$t_{w(CH)}$	Pulse duration, SCLK high	25			ns



NOTE A: The input clock, applied at the SCLK terminal, should be inhibited low when $\overline{CS}$ is high to minimize clock feedthrough.

Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

OUTPUT SINK CURRENT (FAST MODE)
vs
OUTPUT LOAD VOLTAGE

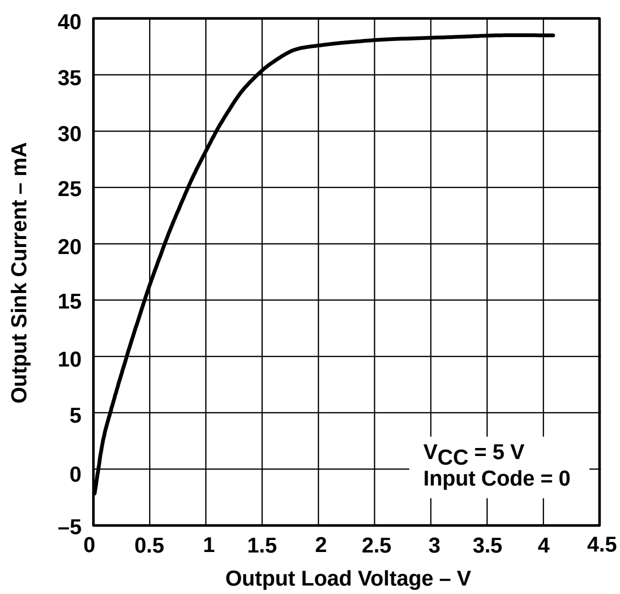


Figure 2

OUTPUT SOURCE CURRENT (FAST MODE)
vs
OUTPUT LOAD VOLTAGE

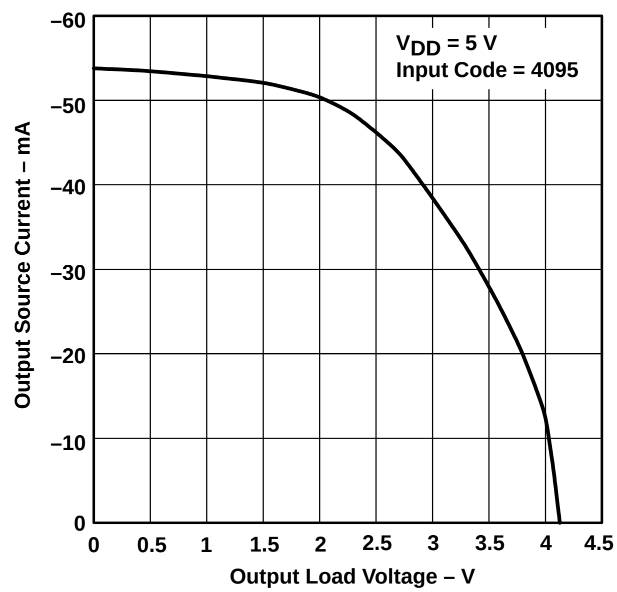


Figure 3

TYPICAL CHARACTERISTICS

OUTPUT SINK CURRENT (SLOW MODE) vs OUTPUT LOAD VOLTAGE

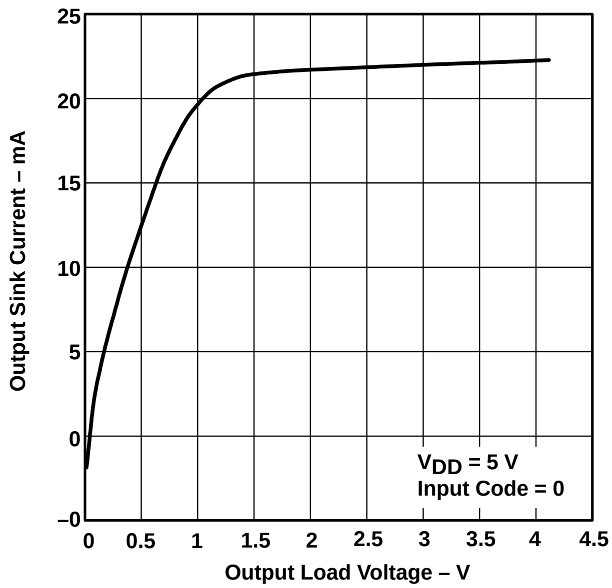


Figure 4

OUTPUT SOURCE CURRENT (SLOW MODE) vs OUTPUT LOAD VOLTAGE

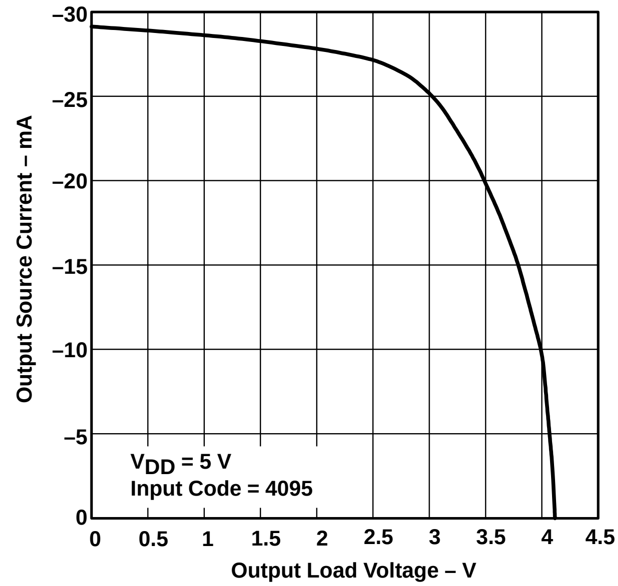


Figure 5

SUPPLY CURRENT vs TEMPERATURE

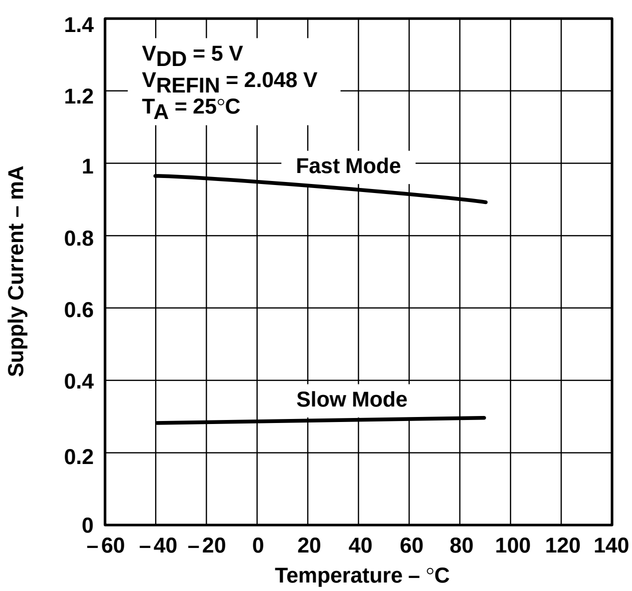


Figure 6

RELATIVE GAIN (FAST MODE) vs FREQUENCY

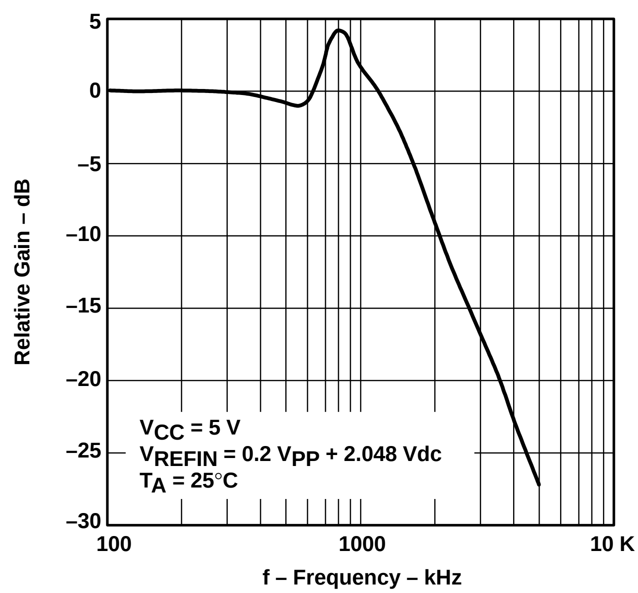


Figure 7

TYPICAL CHARACTERISTICS

RELATIVE GAIN (SLOW MODE) vs FREQUENCY

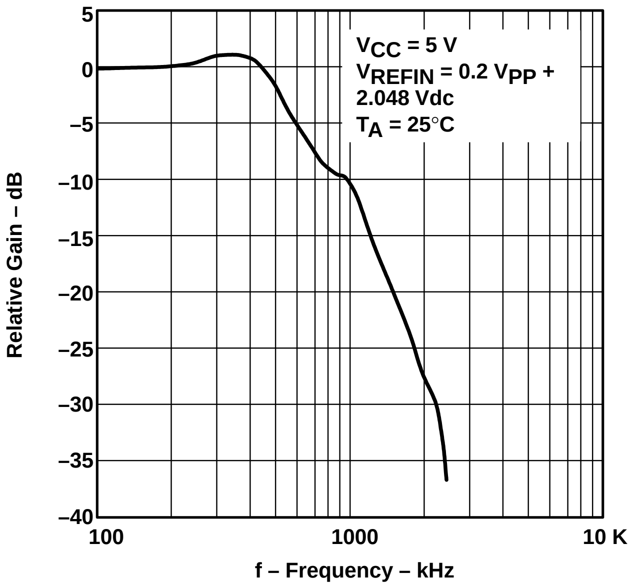


Figure 8

TOTAL HARMONIC DISTORTION (SLOW MODE) vs FREQUENCY

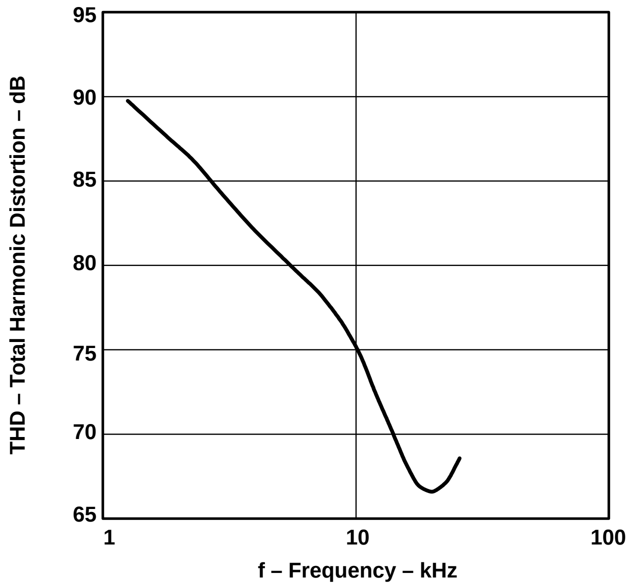


Figure 9

TOTAL HARMONIC DISTORTION + NOISE (SLOW MODE) vs FREQUENCY

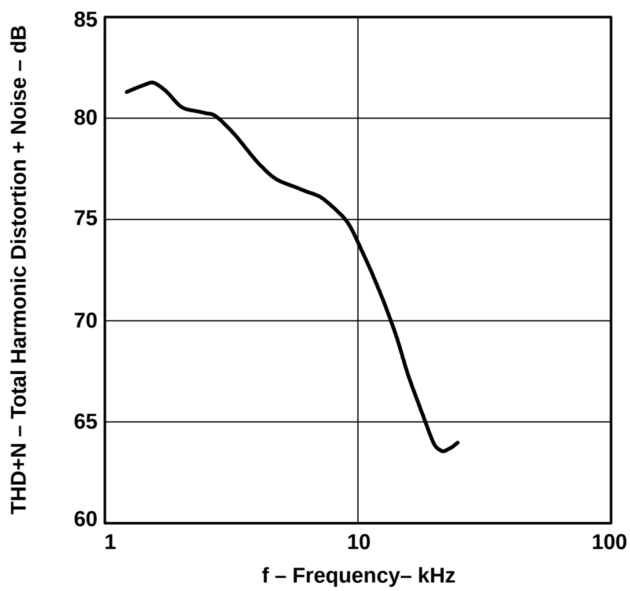


Figure 10

SIGNAL-TO-NOISE RATIO (SLOW MODE) vs FREQUENCY

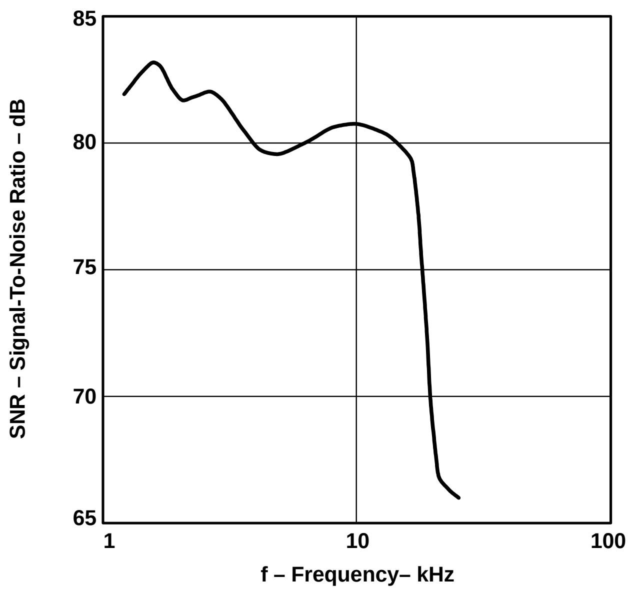


Figure 11

TYPICAL CHARACTERISTICS

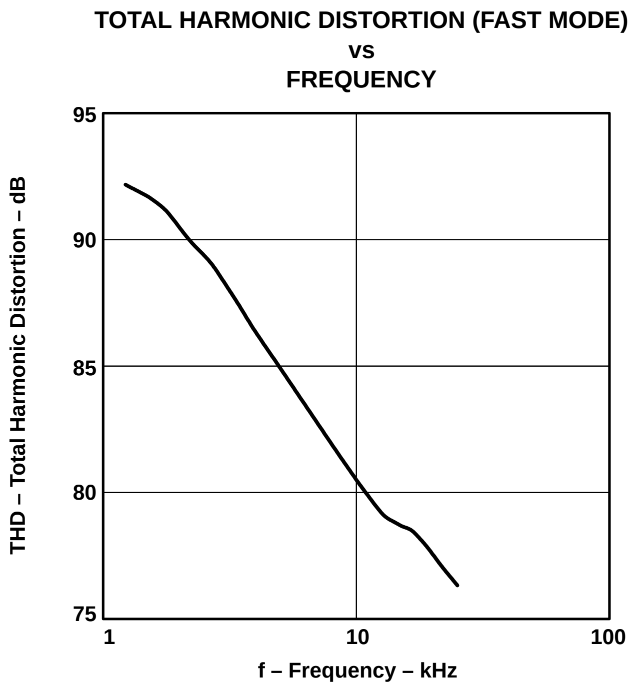


Figure 12

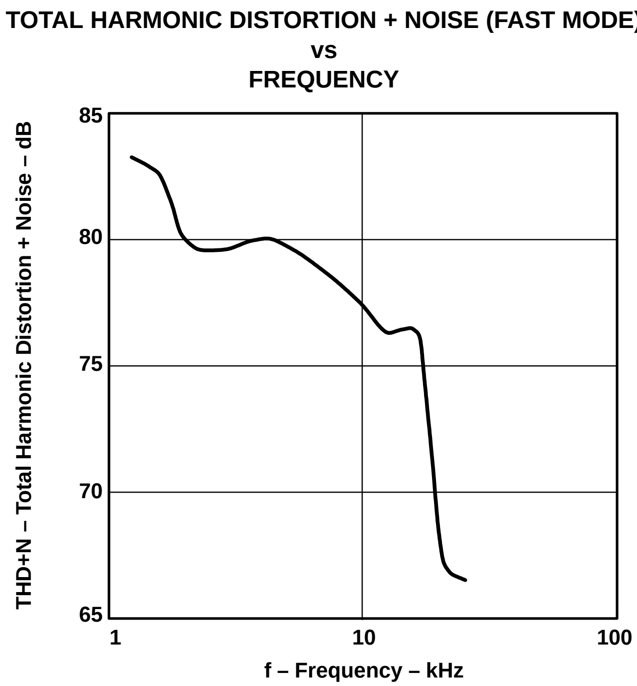


Figure 13

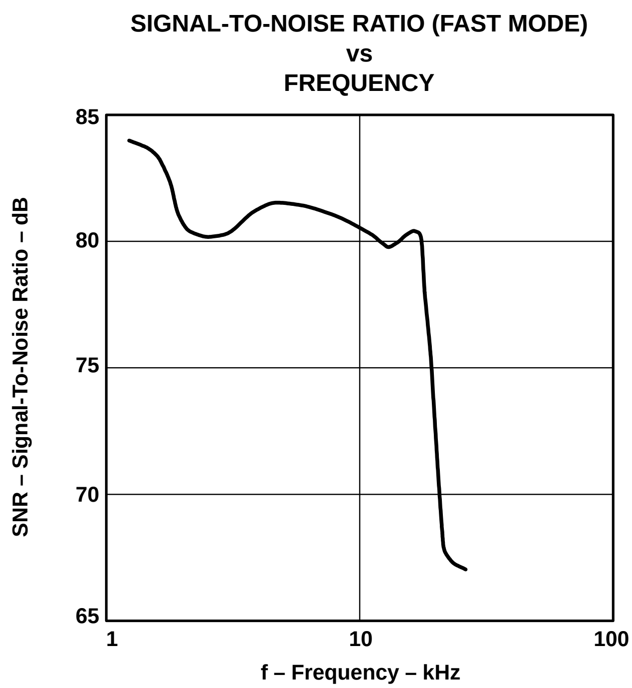


Figure 14

TYPICAL CHARACTERISTICS

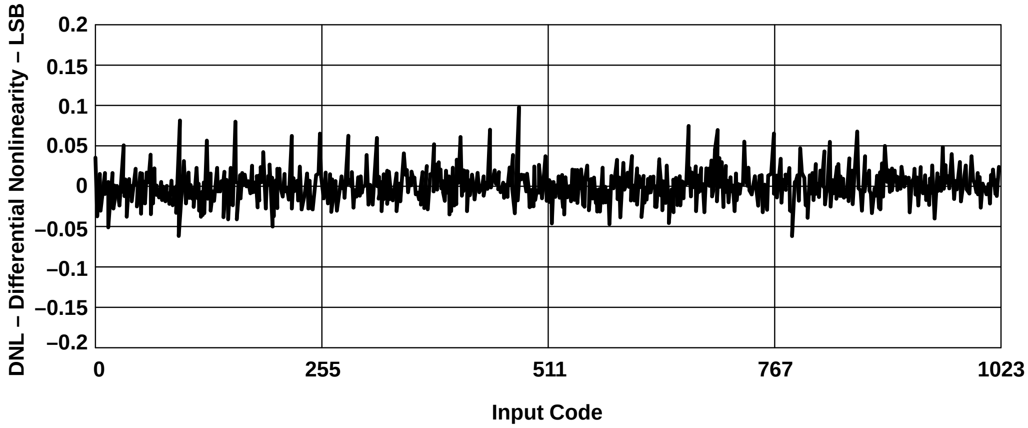


Figure 15. Differential Nonlinearity With Input Code

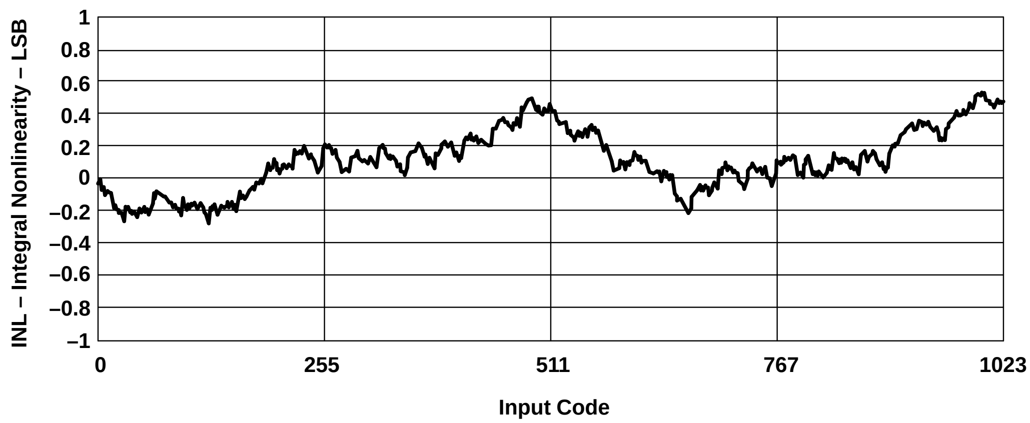


Figure 16. Integral Nonlinearity With Input Code

APPLICATION INFORMATION

general function

The TLC5617 uses a resistor string network buffered with an op amp to convert 10-bit digital data to analog voltage levels (see functional block diagram and Figure 17). The output of the TLC5617 is the same polarity as the reference input (see Table 1).

The output code is given by: $2\left(V_{REFIN}\right)\frac{CODE}{1024}$

An internal circuit resets the DAC register to all 0s on power-up.

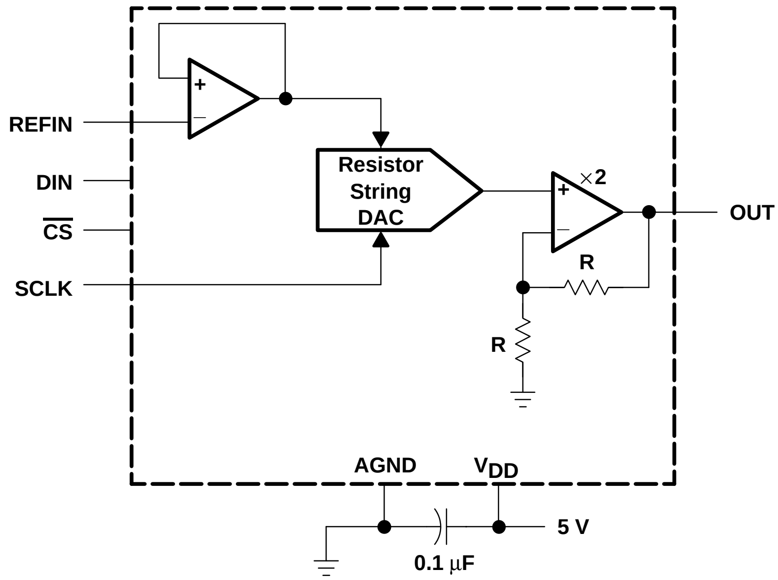


Figure 17. TLC5617 Typical Operating Circuit

Table 1. Binary Code Table (0 V to 2 V_{REFIN} Output), Gain = 2

INPUT†			OUTPUT
1111	1111	11(00)	$2\left(V_{REFIN}\right)\frac{1023}{1024}$
	:		:
1000	0000	01(00)	$2\left(V_{REFIN}\right)\frac{513}{1024}$
1000	0000	00(00)	$2\left(V_{REFIN}\right)\frac{512}{1024} = V_{REFIN}$
0111	1111	11(00)	$2\left(V_{REFIN}\right)\frac{511}{1024}$
	:		:
0000	0000	01(00)	$2\left(V_{REFIN}\right)\frac{1}{1024}$
0000	0000	00(00)	0 V

† A 10-bit data word with two sub-LSB 0s must be written since the DAC input latch is 12 bits wide.

APPLICATION INFORMATION

buffer amplifier

The output buffer has a rail-to-rail output with short circuit protection and can drive a 2-kΩ load with a 100 pF load capacitance. Settling time is a software selectable 12.5 µs or 2.5 µs typical to within ±0.5 LSB of final value.

external reference

The reference voltage input is buffered which makes the DAC input resistance not code dependent. Therefore, the REFIN input resistance is 10 MΩ and the REFIN input capacitance is typically 5 pF, independent of input code. The reference voltage determines the DAC full-scale output.

logic interface

The logic inputs function with CMOS logic levels. Most of the standard high-speed CMOS logic families may be used.

serial clock and update rate

Figure 1 shows the TLC5617 timing. The maximum serial clock rate is

$$f_{(SCLK)max} = \frac{1}{t_{w(CH)min} + t_{w(CL)min}} = 20\ \text{MHz}$$

The digital update rate is limited by the chip-select period, which is

$$t_{p(CS)} = 16 \times \left(t_{w(CH)} + t_{w(CL)}\right) + t_{su(CS1)}$$

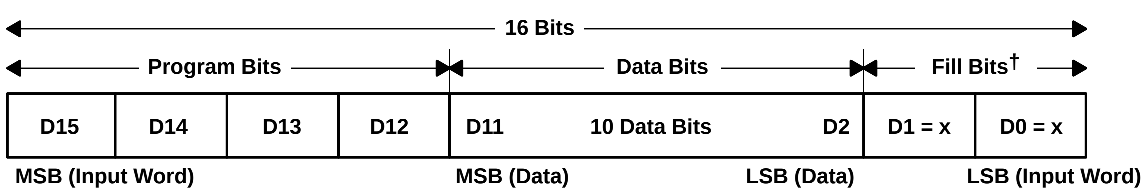
This equals an 820-ns or 1.21-MHz update rate. However, the DAC settling time to 10 bits limits the update rate for full-scale input step transitions.

serial interface

When chip select ($\overline{CS}$) is low, the input data is read into a 16-bit shift register with the input data clocked in most significant bit first. The falling edge of the SCLK input shifts the data into the input register.

The rising edge of $\overline{CS}$ then transfers the data to the DAC register. All $\overline{CS}$ transitions should occur when the SCLK input is low.

The 16 bits of data can be transferred with the sequence shown in Figure 18.



† Two extra (sub-LSB) bits (can be don't care)

Figure 18. Input Data Word Format

APPLICATION INFORMATION

Table 2 shows the function of program bits D15 – D12.

Table 2. Program Bits D15 – D12 Function

PROGRAM BIT				DEVICE FUNCTION
D15	D14	D13	D12	
1	X	X	X	Write to latch A with serial interface register data and latch B updated with buffer latch data
0	X	X	0	Write to latch B and double buffer latch
0	X	X	1	Write to double buffer latch only
X	1	X	X	12.5 µs settling time
X	0	X	X	2.5 µs settling time
X	X	0	X	Powered-up operation
X	X	1	X	Powered-down mode

function of the latch control bits (D15 and D12)

Three data transfers are possible. All transfers occur immediatly after $\overline{CS}$ goes high and are described in the following sections.

latch A write, latch B update (D15 = high, D12 = X)

The serial interface register (SIR) data are written to latch A and the double buffer latch contents are written to latch B. The double buffer contents are unaffected. This control bit condition allows simultaneous output updates of both DACs.

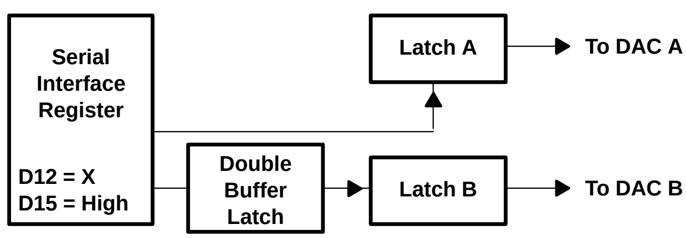


Figure 19. Latch A Write, Latch B Update

latch B and double-buffer 1 write (D15 = low, D12 = low)

The SIR data are written to both latch B and the double buffer. Latch A is unaffected.

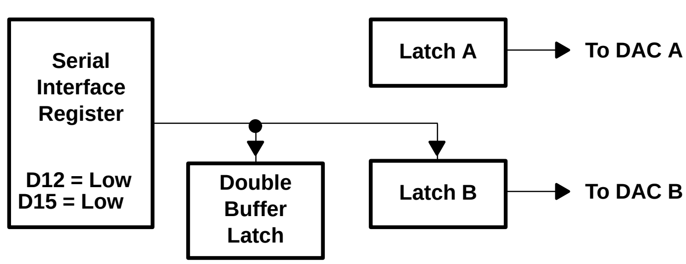


Figure 20. Latch B and Double-Buffer Write

double-buffer-only write (D15 = low, D12 = high)

The SIR data are written to the double buffer only. Latch A and B contents are unaffected.

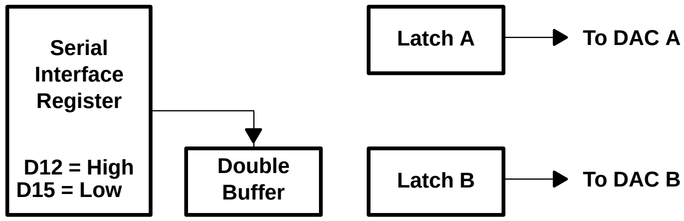


Figure 21. Double-Buffer-Only Write

purpose and use of the buffer

Normally only one DAC output can change after a write. The double buffer allows both DAC outputs to change after a single write. This is achieved by the two following steps.

1. A double-buffer-only write is executed to store the new DAC B data without changing the DAC A and B outputs.
2. Following the previous step a write to latch A is executed. This writes the SIR data to latch A and also writes the double-buffer contents to latch B. Thus both DACs receive their new data at the same time and so both DAC outputs begin to change at the same time.

Unless a double-buffer-only write is issued, the latch B and double-buffer contents are identical. Thus, following a write to latch A or B with another write to latch A does not change the latch B contents.

operational examples

changing the latch A data from zero to full code

Assuming that latch A starts at zero code (e.g., after power-up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right)

1X0X 1111 1111 11XX

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other Xs can be zero or one (don’t care).

The latch B contents and the DAC B output are not changed by this write unless the double-buffer contents are different from the latch B contents. This can only be true if the last write was a double-buffer-only write.

changing the latch B data from zero to full code

Assuming that latch B starts at zero code (e.g., after power-up), the latch can be filled with 1s by writing (bit D15 on the left, D0 on the right).

0X00 1111 1111 11XX

to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other Xs can be zero or one (don’t care). The data (bits D0 to D11) are written to both the double buffer and latch B.

The latch A contents and the DAC A output are not changed by this write.

double-buffered change of both DAC outputs

Assuming that DACs A and B start at zero code (e.g., after power-up), if DAC A is to be driven to mid-scale and DAC B to full-scale, and if the outputs are to begin rising at the same time, this can be achieved as follows:

First,

0d01 1111 1111 11XX

is written (bit D15 on the left, D0 on the right) to the serial interface. This loads the full-scale code into the double buffer latch but does not change the latch B contents and the DAC B output voltage. The latch A contents and the DAC A output are also unaffected by this write operation.

Changing from fast to slow mode or slow to fast mode changes the supply current which can glitch the outputs, and so D14 (designated by d in the data word) should be set to maintain the speed made set by the previous write. The other Xs can be ones or zeros (don’t care).

Next,

1X0X 1000 0000 00XX

is written (bit D15 on the left, D0 on the right) to the serial interface. Bit D14 can be zero to select slow mode or one to select fast mode. The other Xs can be zero or one (don’t care). This writes the mid-scale code (1000000000XX) to latch A and also copies the full-scale code from the double buffer to latch B. Both DAC outputs thus begin to rise after the second write.

general serial interface

The TLC5617 three-wire interface is compatible with the SPI, QSPI, and Microwire serial standards. The hardware connections are shown in Figure 22 and Figure 23.

The SPI and Microwire interfaces transfer data in 8-bit bytes, therefore, two write cycles are required to input data to the DAC. The QSPI interface, which has a variable input data length from 8 to 16 bits, can load the DAC input register in one write cycle.

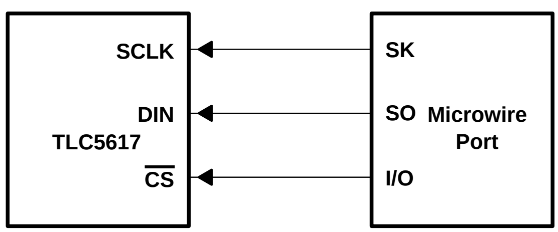


Figure 22. Microwire Connection

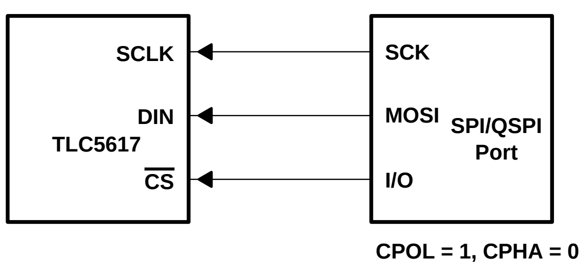


Figure 23. SPI/QSPI Connection

APPLICATION INFORMATION

linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 24.

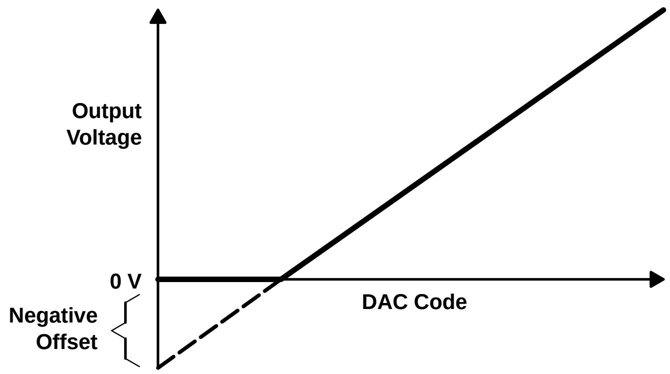


Figure 24. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full scale code and the lowest code that produces a positive output voltage. For the TLC5617, the zero-scale (offset) error is plus or minus 3 LSB maximum. The code is calculated from the maximum specification for the negative offset.

APPLICATION INFORMATION

power-supply bypassing and ground management

Printed circuit boards that use separate analog and digital ground planes offer the best system performance. Wire-wrap boards do not perform well and should not be used. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analog ground plane making sure that analog ground currents are well managed.

A 0.1 μF ceramic bypass capacitor should be connected between V_{DD} and AGND and mounted with short leads as close as possible to the device. Use of ferrite beads may further isolate the system analog and digital power supplies.

Figures 25 shows the ground plane layout and bypassing technique.

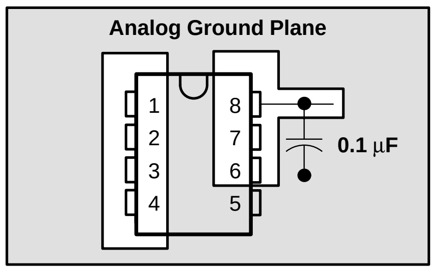


Figure 25. Power-Supply Bypassing

saving power

Setting the DAC register to all 0s minimizes power consumption by the reference resistor array and the output load when the system is not using the DAC.

ac considerations/analog feedthrough

Higher frequency analog input signals may couple to the output through internal stray capacitance. Analog feedthrough is tested by holding $\overline{CS}$ high, setting the DAC code to all 0s, sweeping the frequency applied to REFIN, and monitoring the DAC output.