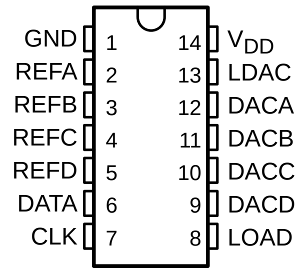
TLV5620C, TLV5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

- **Four 8-Bit Voltage Output DACs**
- **3-V Single-Supply Operation**
- **Serial Interface**
- **High-Impedance Reference Inputs**
- **Programmable for 1 or 2 Times Output Range**
- **Simultaneous-Update Facility**
- **Internal Power-On Reset**
- **Low Power Consumption**
- **Half-Buffered Output**

D OR N PACKAGE
(TOP VIEW)



applications

- **Programmable Voltage Sources**
- **Digitally-Controlled Amplifiers/Attenuators**
- **Mobile Communications**
- **Automatic Test Equipment**
- **Process Monitoring and Control**
- **Signal Synthesis**

description

The TLV5620C and TLV5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND; and, the DACs are monotonic. The device is simple to use, because it runs from a single supply of 3 V to 3.6 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

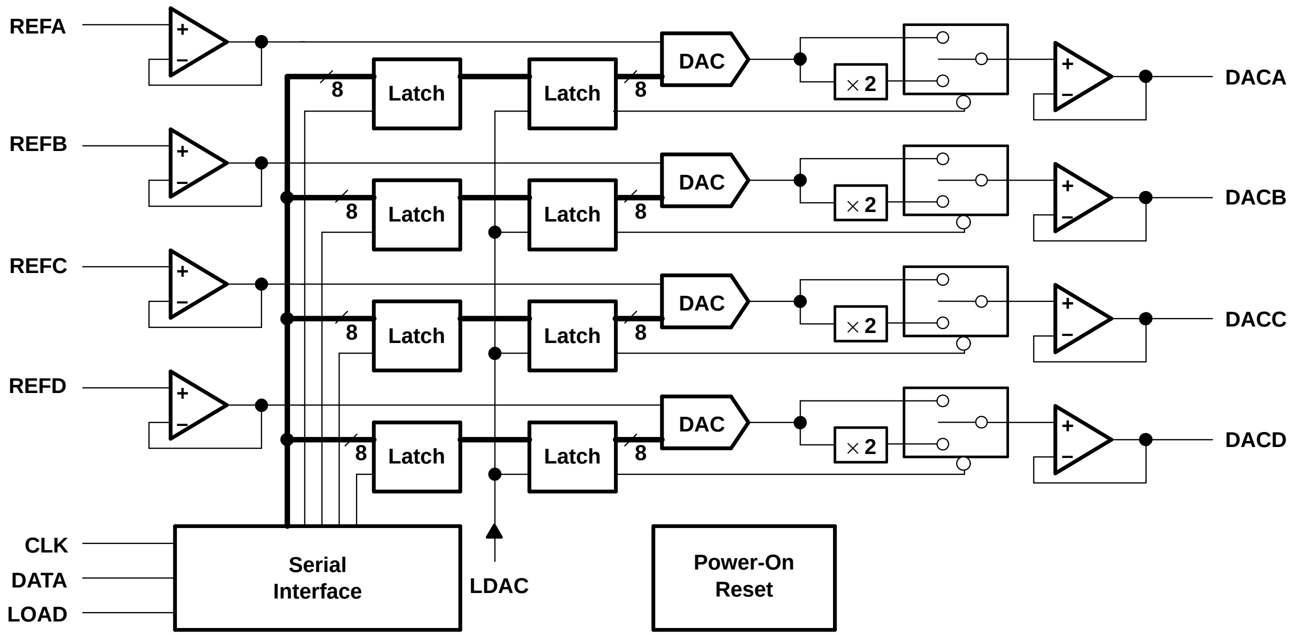
Digital control of the TLV5620C and TLV5620I is over a simple 3-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises 8 bits of data, 2 DAC select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs update simultaneously through control of the LDAC terminal. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-terminal small-outline (SO) package allows digital control of analog functions in space-critical applications. The TLV5620C is characterized for operation from 0°C to 70°C. The TLV5620I is characterized for operation from –40°C to 85°C. The TLV5620C and TLV5620I do not require external trimming.

AVAILABLE OPTIONS

	PACKAGE	
T_A	**SMALL OUTLINE (D)**	**PLASTIC DIP (N)**
0°C to 70°C	TLV5620CD	TLV5620CN
–40°C to 85°C	TLV5620ID	TLV5620IN

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLK	7	I	Serial-interface clock, data enters on the negative edge
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial-interface digital-data input
GND	1	I	Ground return and reference terminal
LDAC	13	I	DAC-update latch control
LOAD	8	I	Serial-interface load control
REFA	2	I	Reference voltage input to DACA
REFB	3	I	Reference voltage input to DACB
REFC	4	I	Reference voltage input to DACC
REFD	5	I	Reference voltage input to DACD
V_{DD}	14	I	Positive supply voltage

detailed description

The TLV5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Because the inputs are buffered, the DACs always presents a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier, which can be programmed to times 1 or times 2 gain.

On power-up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(DACA|B|C|D) = REF \times \frac{CODE}{256} \times (1 + RNG\ bit\ value)$$

where CODE is in the range 0 to 255 and the range (RNG) bit is a 0 or 1 within the serial-control word.

data interface

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial-input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated and LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered MSB first. Data transfers using two 8 clock cycle periods are shown in Figures 3 and 4.

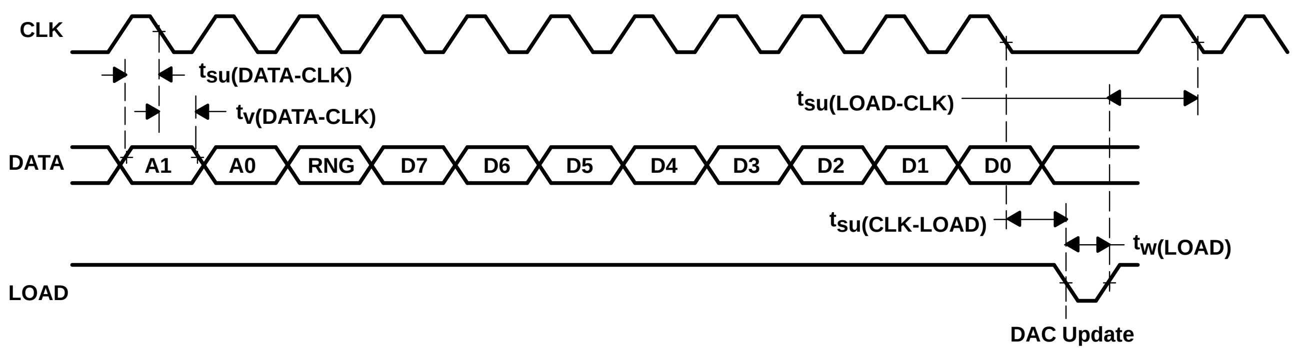


Figure 1. LOAD-Controlled Update (LDAC = Low)

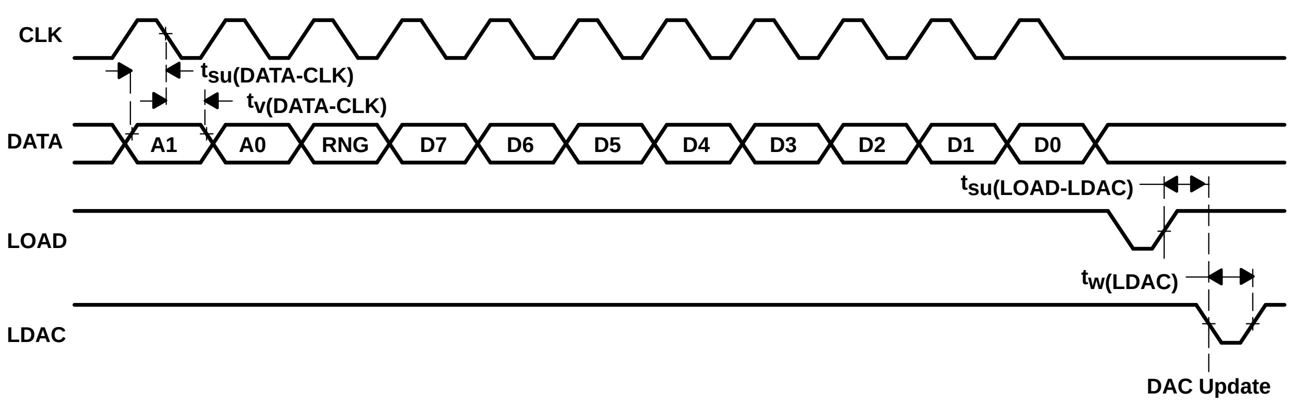


Figure 2. LDAC-Controlled Update

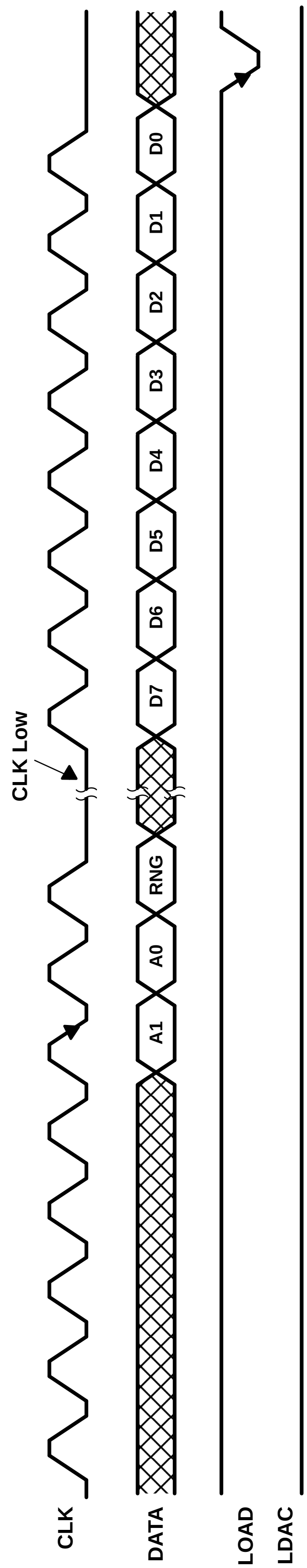


Figure 3. Load Controlled Update Using 8-Bit Serial Word (LDAC = Low)

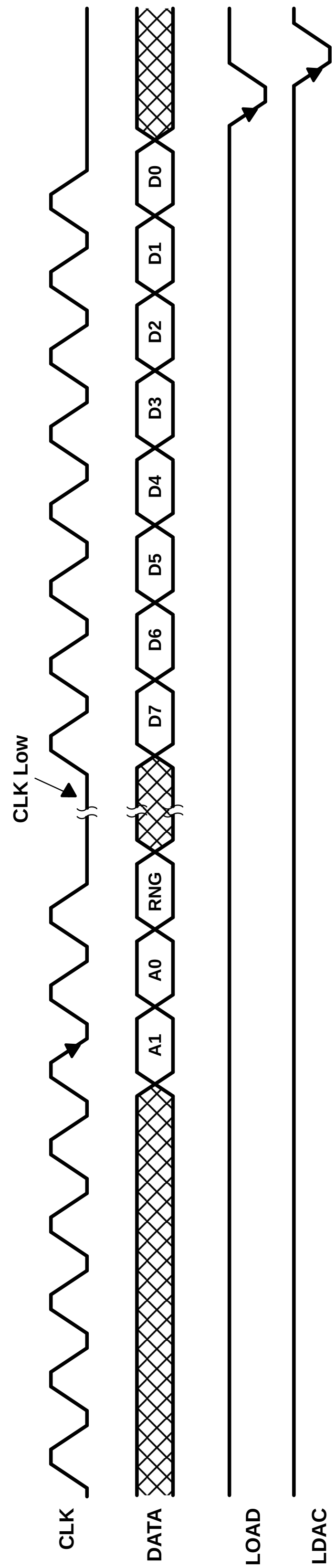


Figure 4. LDAC Controlled Update Using 8-Bit Serial Word

data interface (continued)

Table 2 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 1. Ideal-Output Transfer

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	(1/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	(127/256) × REF (1+RNG)
1	0	0	0	0	0	0	0	(128/256) × REF (1+RNG)
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	(255/256) × REF (1+RNG)

Table 2. Serial-Input Decode

A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, with a negative voltage offset, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive to a negative voltage.

So when the output offset voltage is negative, the output voltage remains at zero volts until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in the transfer function shown in Figure 5.

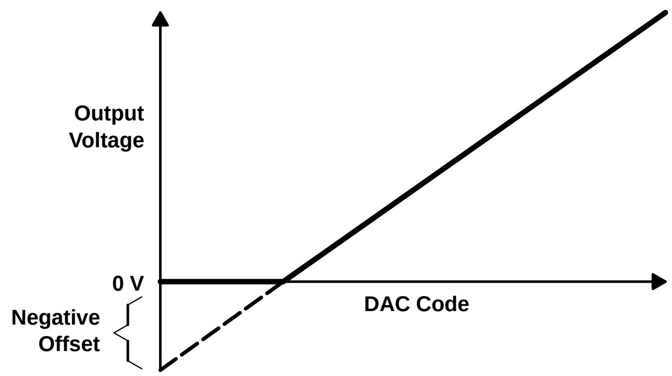


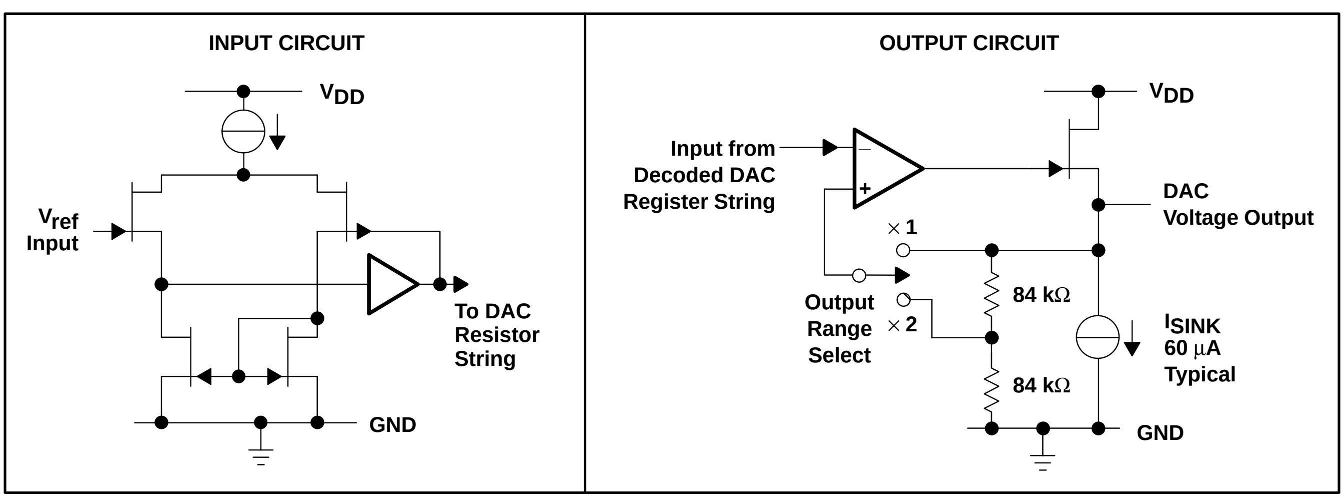
Figure 5. Effect of Negative Offset (Single Supply)

This negative offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive to a negative voltage.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full scale code and the lowest code which produces a positive output voltage.

The code is calculated from the maximum specification for the negative offset.

equivalent inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} – GND) . . . . 7 V
Digital input voltage range . . . . GND – 0.3 V to V_{DD} + 0.3 V
Reference input voltage range, V_{ID} . . . . GND – 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5620C . . . . 0°C to 70°C
TLV5620I . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –50°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 230°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		2.7	3.3	5.25	V
High-level digital input voltage, V_{IH}		0.8 V_{DD}			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} [A|B|C|D], x1 gain				V_{DD} −1.5	V
Load resistance, R_L		10			kΩ
Setup time, data input, $t_{su(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Valid time, data input valid after CLK↓, $t_{v(DATA-CLK)}$ (see Figures 1 and 2)		50			ns
Setup time, CLK eleventh falling edge to LOAD, $t_{su(CLK-LOAD)}$ (see Figure 1)		50			ns
Setup time, LOAD↑ to CLK↓, $t_{su(LOAD-CLK)}$ (see Figure 1)		50			ns
Pulse duration, LOAD, $t_{w(LOAD)}$ (see Figure 1)		250			ns
Pulse duration, LDAC, $t_{w(LDAC)}$ (see Figure 2)		250			ns
Setup time, LOAD↑ to LDAC↓, $t_{su(LOAD-LDAC)}$ (see Figure 2)		0			ns
CLK frequency				1	MHz
Operating free-air temperature, T_A	TLV5620C	0		70	°C
	TLV5620I	−40		85	°C

electrical characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			±10	µA
I_{IL}	Low-level digital input current	V_I = 0 V			±10	µA
$I_{O(sink)}$	Output sink current	Each DAC output	20			µA
$I_{O(source)}$	Output source current	Each DAC output	1			mA
C_i	Input capacitance			15		pF
C_i	Reference input capacitance			15		pF
I_{DD}	Supply current	V_{DD} = 3.3 V			2	mA
I_{ref}	Reference input current	V_{DD} = 3.3 V, V_{ref} = 1.5 V			±10	µA
E_L	Linearity error (end point corrected)	V_{ref} = 1.25 V, × 2 gain (see Note 1)			±1	LSB
E_D	Differential linearity error	V_{ref} = 1.25 V, × 2 gain (see Note 2)			±0.9	LSB
E_{ZS}	Zero-scale error	V_{ref} = 1.25 V, × 2 gain (see Note 3)	0		30	mV
	Zero-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain (see Note 4)		10		µV/°C
E_{FS}	Full-scale error	V_{ref} = 1.25 V, × 2 gain (see Note 5)			±60	mV
	Full-scale error temperature coefficient	V_{ref} = 1.25 V, × 2 gain (see Note 6)		±25		µV/°C
PSRR	Power-supply sensitivity	See Notes 7 and 8		0.5		mV/V

NOTES: 1. Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
2. Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
4. Zero-scale error temperature coefficient is given by: ZSETC = [ZSE(T_{max}) – ZSE(T_{min})]/V_{ref} × 10^6/(T_{max} – T_{min}).
5. Full-scale error is the deviation from the ideal full-scale output (V_{ref} – 1 LSB) with an output load of 10 kΩ.
6. Full-scale temperature coefficient is given by: FSETC = [FSE(T_{max}) – FSE (T_{min})]/V_{ref} × 10^6/(T_{max} – T_{min}).
7. Zero-scale error rejection ratio (ZSE-RR) is measured by varying the V_{DD} voltage from 4.5 V to 5.5 V dc and measuring the effect of this signal on the zero-code output voltage.
8. Full-scale error rejection ratio (FSE-RR) is measured by varing the V_{DD} voltage from 3 V to 3.6 V dc and measuring the effect of this signal on the full-scale output voltage.

operating characteristics over recommended operating free-air temperature range, V_{DD} = 3 V to 3.6 V, V_{ref} = 2 V, × 1 gain output range (unless otherwise noted)

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	C_L = 100 pF, R_L = 10 kΩ		1		V/µs
Output settling time	To 0.5 LSB, C_L = 100 pF, R_L = 10 kΩ, See Note 9		10		µs
Large-signal bandwidth	Measured at –3 dB point		100		kHz
Digital crosstalk	CLK = 1-MHz square wave measured at DACA-DACD		–50		dB
Reference feedthrough	See Note 10		–60		dB
Channel-to-channel isolation	See Note 11		–60		dB
Reference input bandwidth	See Note 12		100		kHz

NOTES: 9. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 00 hex to FF hex or FF hex to 00 hex. For TLV5620C: V_{DD} = 5 V, V_{ref} = 2 V and range = ×2. For TLV5620I: V_{DD} = 3 V, V_{ref} = 1.25 V and range ×2.
10. Reference feedthrough is measured at any DAC output with an input code = 00 hex with a V_{ref} input = 1 V dc + 1 V_{PP} at 10 kHz.
11. Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with V_{ref} input = 1 V dc + 1 V_{PP} at 10 kHz.
12. Reference bandwidth is the –3 dB bandwidth with an input at V_{ref} = 1.25 V dc + 2 V_{PP} and with a digital input code of full-scale.

PARAMETER MEASUREMENT INFORMATION

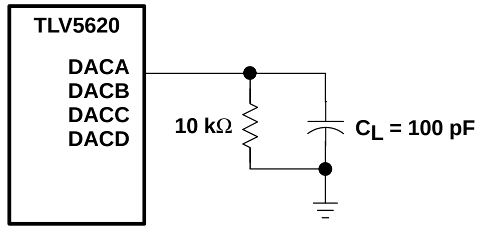
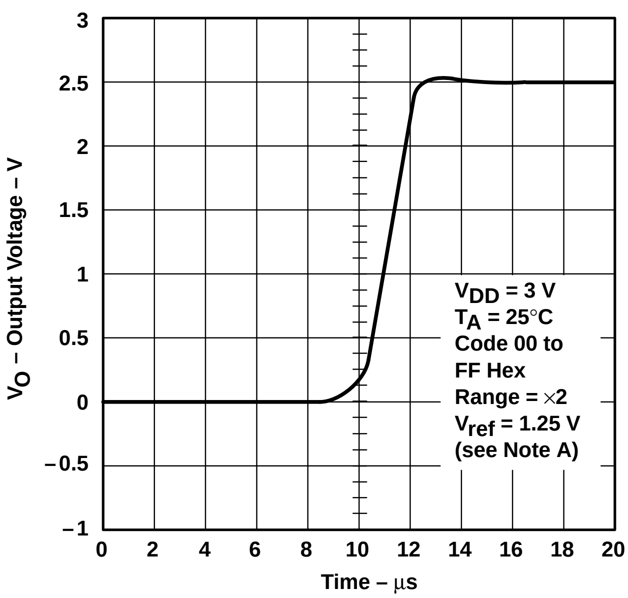


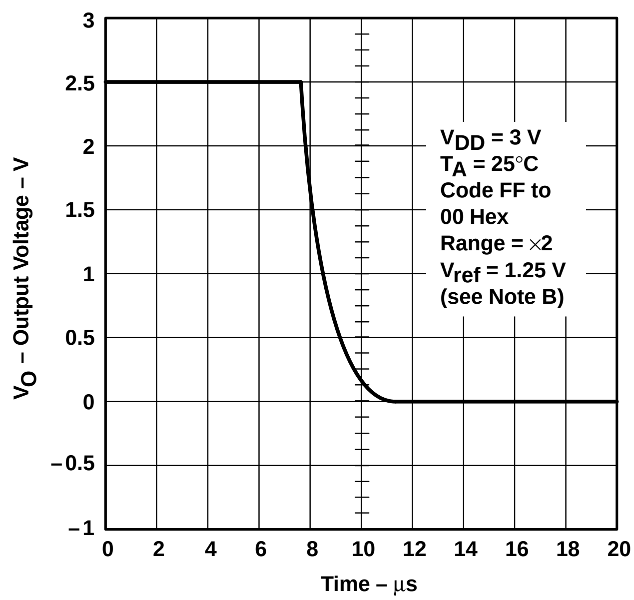
Figure 6. Slewing Settling Time and Linearity Measurements

TYPICAL CHARACTERISTICS

POSITIVE RISE TIME AND SETTLING TIME



NEGATIVE FALL TIME AND SETTLING TIME



NOTES: A. Rise time = 2.05 µs, positive slew rate = 0.96 V/µs, settling time = 4.5 µs.
B. Fall time = 4.25 µs, negative slew rate = 0.46 V/µs, settling time = 8.5 µs.

Figure 7

Figure 8

TYPICAL CHARACTERISTICS

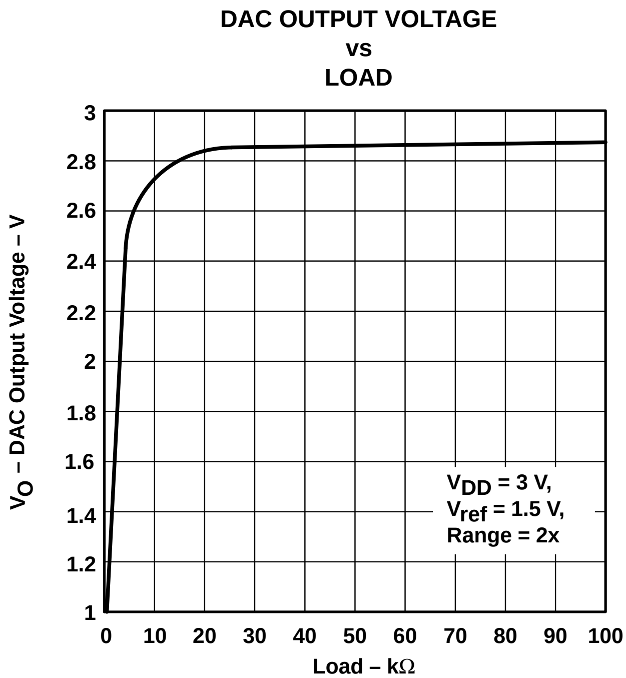


Figure 9

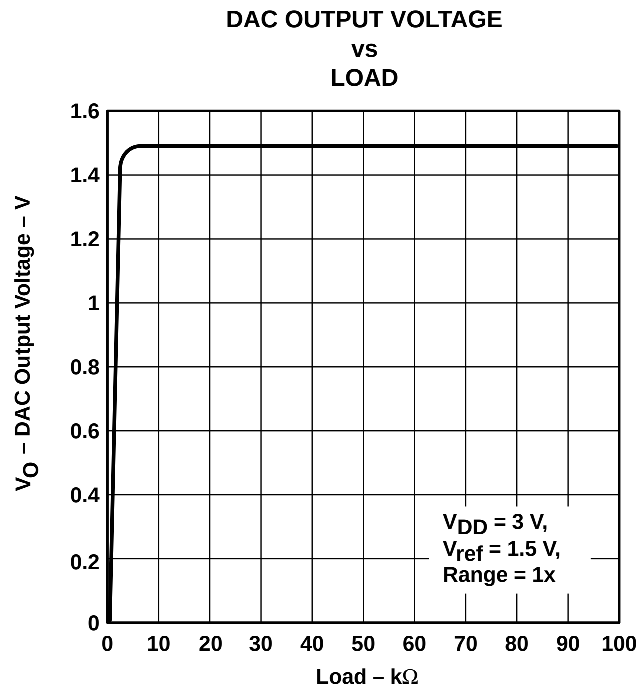


Figure 10

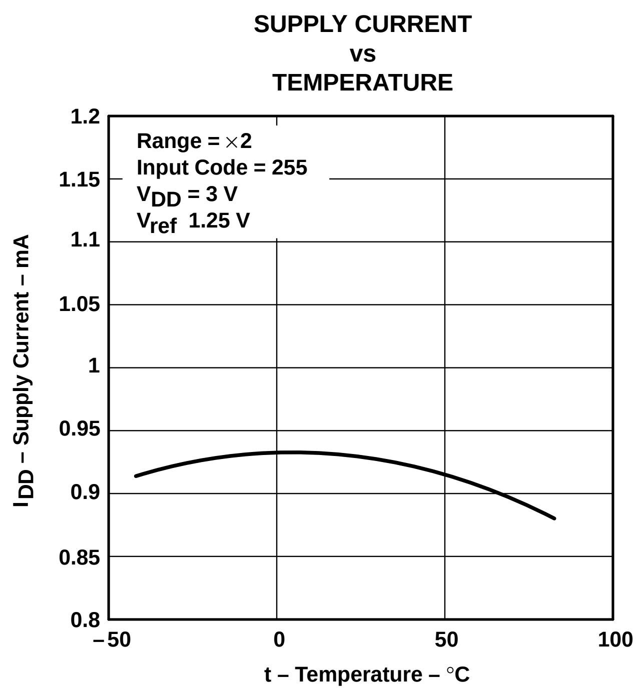
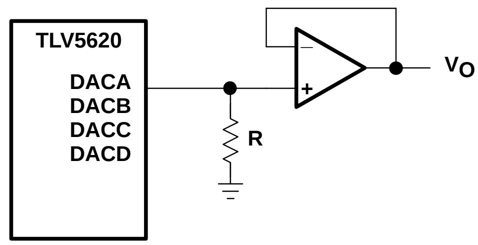


Figure 11

APPLICATION INFORMATION



NOTE A: Resistor R $\geq$ 10 kΩ

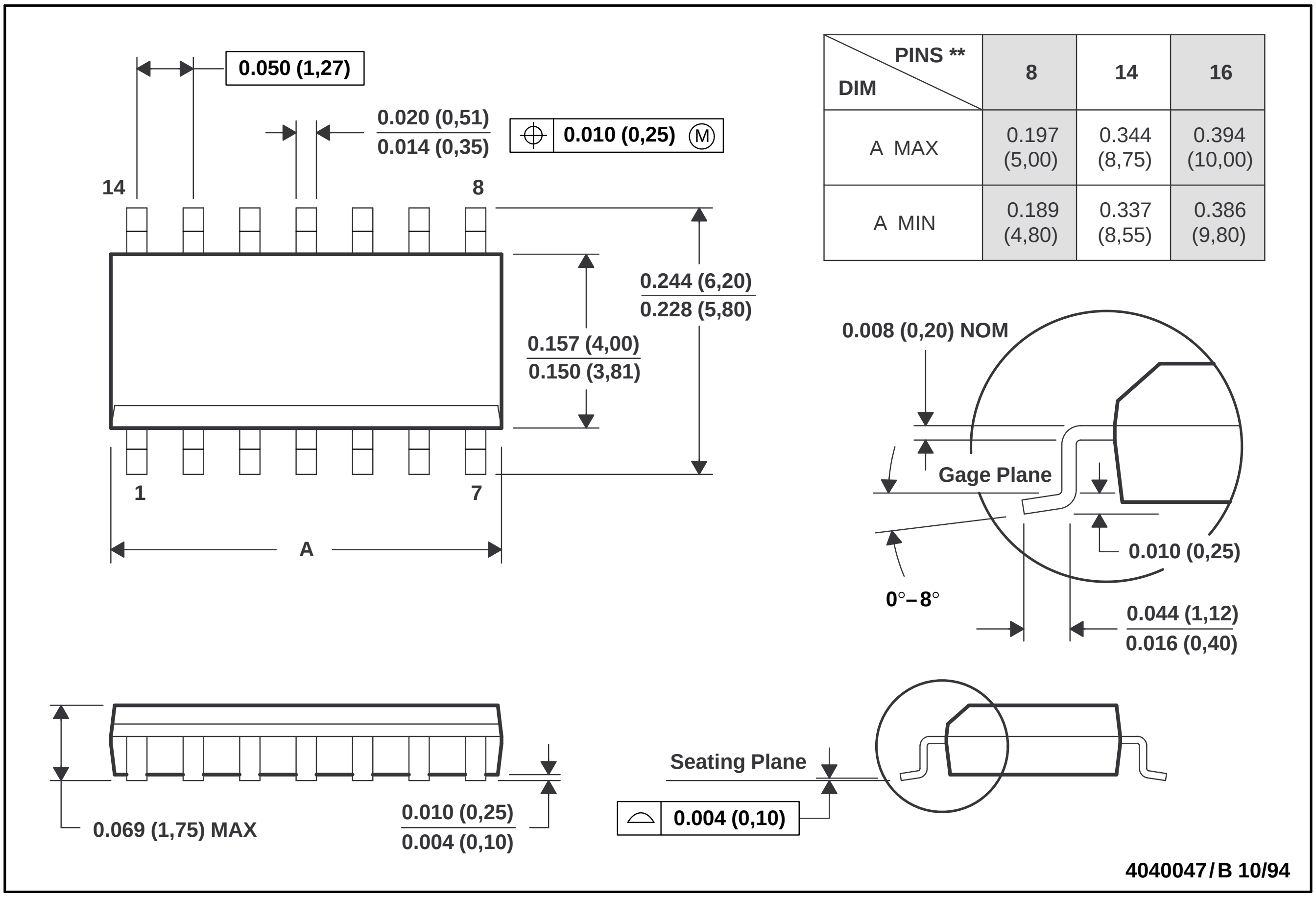
Figure 12. Output Buffering Scheme

MECHANICAL DATA

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN

DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

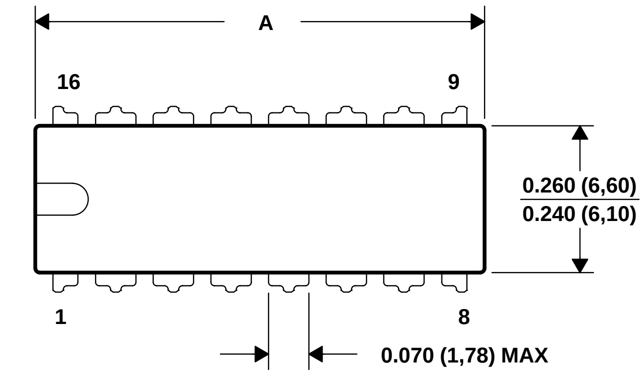


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Four center pins are connected to die mount pad
E. Falls within JEDEC MS-012

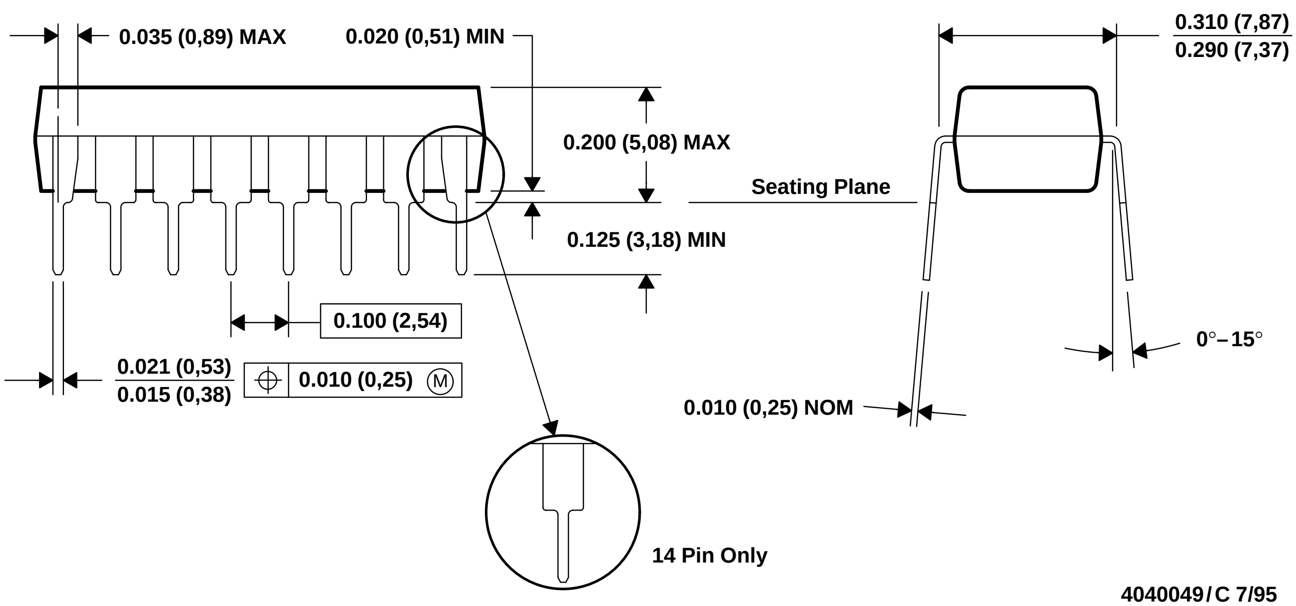
MECHANICAL DATA

N (R-PDIP-T)** **PLASTIC DUAL-IN-LINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23.37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21.59)	0.940 (23,88)



4040049/C 7/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

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