- **Low Supply-Voltage Range, 1.8 V . . . 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 225 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.8 μA**
  - **Off Mode (RAM Retention): 0.1 μA**
- **Five Power-Saving Modes**
- **Wake Up From Standby Mode in 6 μs**
- **Frequency-Locked Loop, FLL+**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **Integrated LCD Driver for 96 Segments**
- **On-Chip Comparator**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader in Flash Devices**
- **Family Members Include:**
  - **MSP430C412: 4KB ROM, 256B RAM†**
  - **MSP430C413: 8KB ROM, 256B RAM†**
  - **MSP430F412: 4KB + 256B Flash Memory, 256B RAM**
  - **MSP430F413: 8KB + 256B Flash Memory, 256B RAM**
- **Available in 64-Pin Quad Flat Pack (QFP)**

† ADVANCE INFORMATION

description

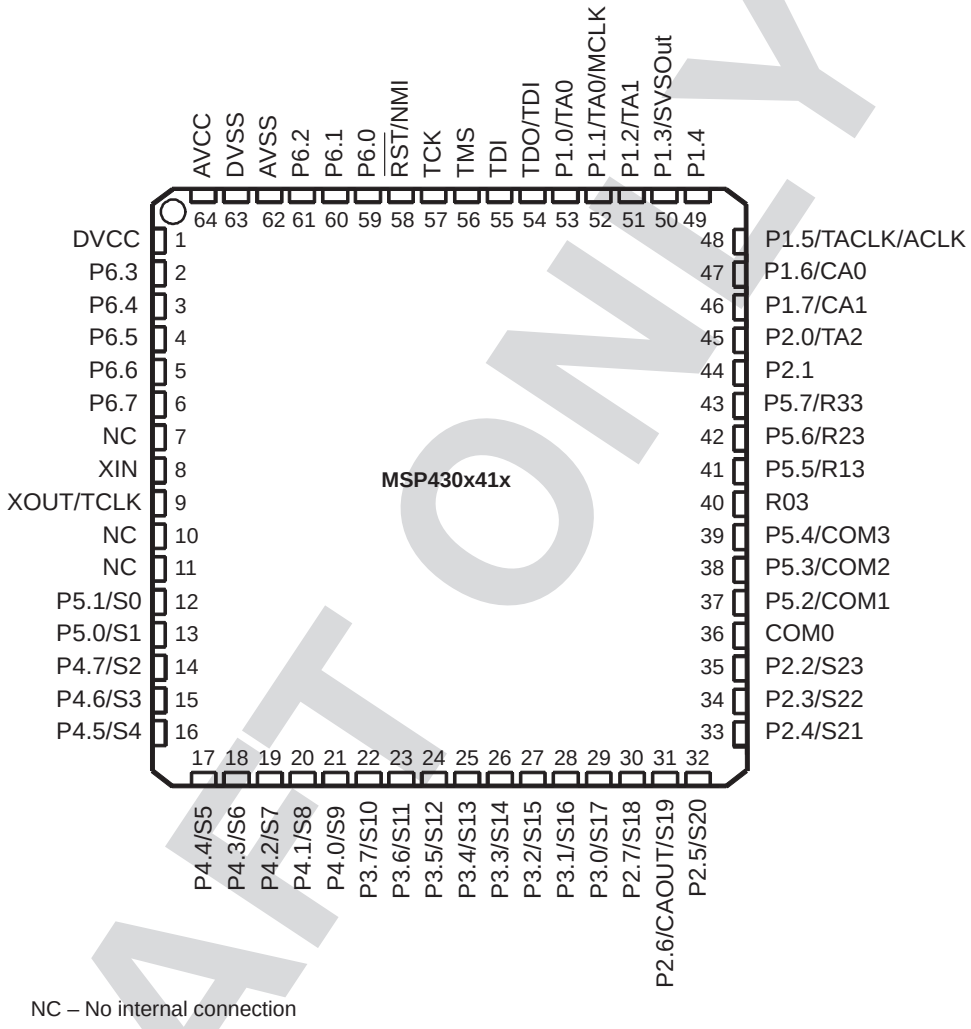
The Texas Instruments MSP430 series is an ultralow-power microcontroller family consisting of several devices featuring different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for use in extended-time applications. With 16-bit RISC architecture, 16-bit integrated registers on the CPU, and the *constant generator*, the MSP430 achieves maximum code efficiency. The digitally-controlled oscillator provides wake up from low-power mode to active mode in less than 6 μs. The MSP430x41x series are microcontroller configurations with one built-in 16-bit timer, a comparator, 96 segment drive capability, and 48 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process the data and transmit them to a host system. The comparator and timer make the configurations ideal for industrial meters, counter applications, handheld meters, etc.

AVAILABLE OPTIONS

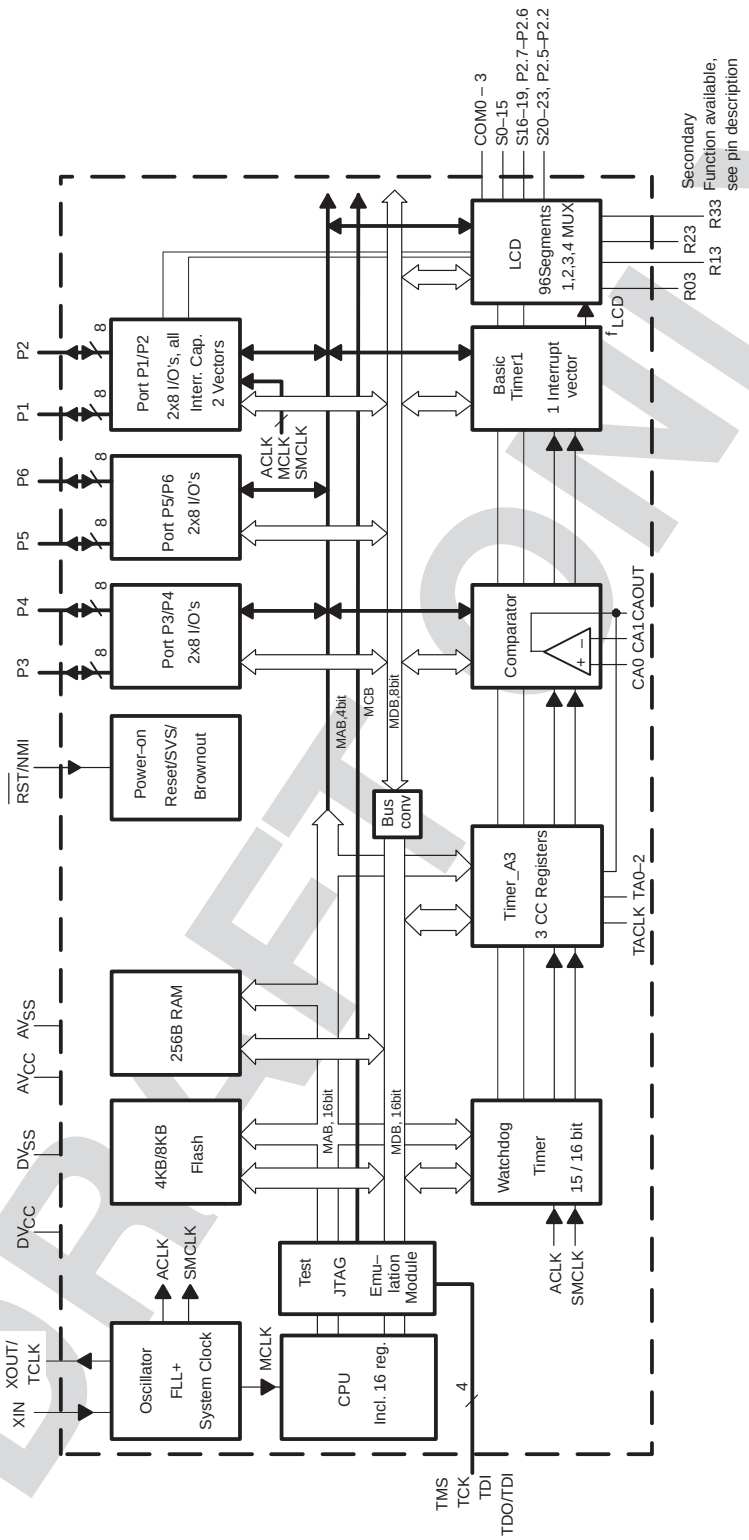
T_A	PACKAGED DEVICES
	PLASTIC 64-PIN QFP (PM)
–40°C to 85°C	MSP430C412IPM MSP430C413IPM MSP430F412IPM MSP430F413IPM

pin designation, MSP430x41x



NC – No internal connection

functional block diagrams



Terminal Functions

MSP430x41x

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AVCC	64		Positive terminal that supplies SVS, brownout, oscillator, FLL+, comparator_A, port 1, and LCD resistive divider circuitry; must not power up prior to DVCC.
AVSS	62		Internally connected to DVSS
DVCC	1		Digital supply voltage, positive terminal. Supplies all parts, except those which are supplied via AVCC.
DVSS	63		Digital supply voltage, negative terminal. Supplies all digital parts, except those which are supplied via AVCC/AVSS.
NC	7, 10, 11		No connection
P1.0/TA0	53	I/O	General-purpose digital I/O/Timer_A. Capture: CCI0A input, compare: Out0 output
P1.1/TA0/MCLK	52	I/O	General-purpose digital I/O/Timer_A. Capture: CCI0B input/MCLK output. Note: TA0 is only an input on this pin.
P1.2/TA1	51	I/O	General-purpose digital I/O/Timer_A, capture: CCI1A input, Compare: Out1 output
P1.3/SVSOut	50	I/O	General-purpose digital I/O/SVS: output of SVS comparator
P1.4	49	I/O	General-purpose digital I/O
P1.5/TACLK/ ACLK	48	I/O	General-purpose digital I/O/input of Timer_A clock/output of ACLK
P1.6/CA0	47	I/O	General-purpose digital I/O/Comparator_A input
P1.7/CA1	46	I/O	General-purpose digital I/O/Comparator_A input
P2.0/TA2	45	I/O	General-purpose digital I/O/ Timer_A capture: CCI2A input, compare: Out2 output
P2.1	44	I/O	General-purpose digital I/O
P2.2/S23	35	I/O	General-purpose digital I/O/LCD segment output 23 (see Note 1)
P2.3/S22	34	I/O	General-purpose digital I/O/LCD segment output 22 (see Note 1)
P2.4/S21	33	I/O	General-purpose digital I/O/LCD segment output 21 (see Note 1)
P2.5/S20	32	I/O	General-purpose digital I/O/LCD segment output 20 (see Note 1)
P2.6/CAOUT/S19	31	I/O	General-purpose digital I/O/Comparator_A output/LCD segment output 19 (see Note 1)
P2.7/S18	30	I/O	General-purpose digital I/O/LCD segment output 18 (see Note 1)
P3.0/S17	29	I/O	General-purpose digital I/O/ LCD segment output 17 (see Note 1)
P3.1/S16	28	I/O	General-purpose digital I/O/ LCD segment output 16 (see Note 1)
P3.2/S15	27	I/O	General-purpose digital I/O/ LCD segment output 15 (see Note 1)
P3.3/S14	26	I/O	General-purpose digital I/O/ LCD segment output 14 (see Note 1)
P3.4/S13	25	I/O	General-purpose digital I/O/LCD segment output 13 (see Note 1)
P3.5/S12	24	I/O	General-purpose digital I/O/LCD segment output 12 (see Note 1)
P3.6/S11	23	I/O	General-purpose digital I/O/LCD segment output 11 (see Note 1)
P3.7/S10	22	I/O	General-purpose digital I/O/LCD segment output 10 (see Note 1)

NOTE 1: LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

Terminal Functions (Continued)

MSP430x41x

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
P4.0/S9	21	I/O	General-purpose digital I/O/LCD segment output 9 (see Note 1)
P4.1/S8	20	I/O	General-purpose digital I/O/LCD segment output 8 (see Note 1)
P4.2/S7	19	I/O	General-purpose digital I/O/LCD segment output 7 (see Note 1)
P4.3/S6	18	I/O	General-purpose digital I/O/LCD segment output 6 (see Note 1)
P4.4/S5	17	I/O	General-purpose digital I/O/LCD segment output 5 (see Note 1)
P4.5/S4	16	I/O	General-purpose digital I/O/LCD segment output 4 (see Note 1)
P4.6/S3	15	I/O	General-purpose digital I/O/LCD segment output 3 (see Note 1)
P4.7/S2	14	I/O	General-purpose digital I/O/LCD segment output 2 (see Note 1)
P5.0/S1	13	I/O	General-purpose digital I/O/LCD segment output 1 (see Note 1)
P5.1/S0	12	I/O	General-purpose digital I/O/LCD segment output 0 (see Note 1)
COM0	36	O	Common output. COM0–3 are used for LCD backplanes
P5.2/COM1	37	I/O	General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes
P5.3/COM2	38	I/O	General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes
P5.4/COM3	39	I/O	General-purpose digital I/O/common output. COM0–3 are used for LCD backplanes
R03	40	I	Input port of fourth positive (lowest) analog LCD level (V5)
P5.5/R13	41	I/O	General-purpose digital I/O/input port of third most positive analog LCD level (V4 or V3)
P5.6/R23	42	I/O	General-purpose digital I/O/input port of second most positive analog LCD level (V2)
P5.7/R33	43	I/O	General-purpose digital I/O/output port of most positive analog LCD level (V1)
P6.0	59	I/O	General-purpose digital I/O
P6.1	60	I/O	General-purpose digital I/O
P6.2	61	I/O	General-purpose digital I/O
P6.3	2	I/O	General-purpose digital I/O
P6.4	3	I/O	General-purpose digital I/O
P6.5	4	I/O	General-purpose digital I/O
P6.6	5	I/O	General-purpose digital I/O
P6.7	6	I/O	General-purpose digital I/O
$\overline{\text{RST}}$/NMI	58	I	Reset input or nonmaskable interrupt input port
TCK	57	I	Test clock. TCK is the clock input port for device programming and test.
TDI	55	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT/TCLK	9	I/O	Output terminal of crystal oscillator XT1 or test clock input

NOTE 1. LCD function selected automatically when applicable LCD module control bits are set, not with PxSEL bits.

short-form description

processing unit

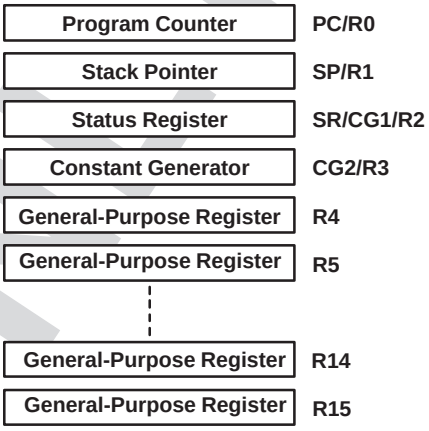
The processing unit is based on a consistent and orthogonal CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and is notable for its ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

CPU

Sixteen registers are located inside the CPU, providing reduced instruction execution time. This reduces the register-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as a program counter, a stack pointer, a status register and a constant generator. The remaining registers are available as general-purpose registers.

Peripherals are connected to the CPU using a data address and control bus and can be handled easily with all memory manipulation instructions.



instruction set

The instruction set for this register-register architecture provides a powerful and easy-to-use assembler language. The instruction set consists of 51 instructions with three formats and seven address modes. Table 1 provides a summation and example of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 ——> R5
Single operands, destination only	e.g. CALL R8	PC —>(TOS), R8—> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Each instruction operating on word and byte data is identified by the suffix B.

Examples:	Instructions for word operation		Instructions for byte operation	
	MOV	EDE, TONI	MOV.B	EDE,TONI
	ADD	#235h,&MEM	ADD.B	#35h,&MEM
	PUSH	R5	PUSH.B	R5
	SWPB	R5	—	

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 —> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) —> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) —> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) —> M(Tab+R6)
Indirect Autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) —> R11 R10 + 2—> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 —> M(TONI)

NOTE: S = source D = destination

Computed branches (BR) and subroutine call (CALL) instructions use the same address modes as other instructions. These address modes provide *indirect* addressing, which is ideally suited for computed branches and calls. The full use of this programming capability permits a program structure which is different from conventional 8- and 16-bit controllers. For example, numerous routines can be easily designed to deal with pointers and stacks instead of using flag-type programs for flow control.

operating modes

The MSP430 operating modes support various advanced requirements for ultralow power and ultralow energy consumption. The intelligent management of the operations during the different module operation modes and CPU states achieves this. The requirements are fully supported during interrupt event handling. An interrupt event awakens the system from each of the various operating modes and returns with the RETI instruction to the mode that was selected before the interrupt event. The clocks used are ACLK and MCLK.

ACLK is the crystal frequency, MCLK and SMCLK are a multiple of ACLK and are used as the system clock and sub-system clock.

The following six operating modes are supported:

- Active mode (AM). The CPU is enabled with different combinations of active peripheral modules.
- Low-power mode 0 (LPM0). The CPU is disabled, peripheral operation continues, ACLK and SMCLK signals are active, and loop control for MCLK is active.
- Low-power mode 1 (LPM1). The CPU is disabled, peripheral operation continues, ACLK and SMCLK signals are active, and loop control for MCLK is inactive.
- Low-power mode 2 (LMP2). The CPU is disabled, peripheral operation continues, ACLK signal is active, SMCLK and loop control for MCLK are inactive.
- Low-power mode 3 (LMP3). The CPU is disabled, peripheral operation continues, ACLK signal is active, SMCLK and loop control for MCLK are inactive, and the dc generator for the digital controlled oscillator (DCO) is switched off.
- Low-power mode 4 (LMP4). The CPU is disabled, peripheral operation continues (e.g. if external clock is applied), ACLK signal is inactive (crystal oscillator stopped), SMCLK and loop control for MCLK are inactive, and the dc generator for the DCO is switched off.

operating modes (continued)

The various operating modes are controlled by the software through control of the internal clock system operation. This clock system gives a large combination of hardware and software capabilities to run the application with the lowest power consumption and with optimized system costs:

- Use of the internal clock (DCO) generator without any external components
- Selection of an external crystal or ceramic resonator for lowest frequency and cost
- Application of an external clock source

The control bits that most influence the operation of the clock system and support fast turnon from low power operating modes are located in the status register SR. Four bits control the CPU and the system clock generator: SCG1, SCG0, OscOff, and CPUOff.

15 – 9	8	7							0
Reserved for Future Enhancements	V	SCG1	SCG0	OscOff	CPUOff	GIE	N	Z	C
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

CPUOff, SCG1, SCG0, and OscOff are the most important bits in low-power control when the basic function of the system clock generator is established. They are pushed to the stack whenever an interrupt is accepted and saved for returning to the operation before an interrupt request. They can be manipulated via indirect access to the data on the stack during execution of an interrupt handler so that program execution can resume in another power operating mode after return-from-interrupt.

CPUOff:	The CPUOff bit, when set, disables CPU.
SCG0:	The SCG0 bit, when set, disables the FLL+.
SCG1:	The SCG1 bit, when set, disables the MCLK and SMCLK signals.
OscOff:	The OscOff bit, when set, disables the LFXT1 crystal oscillator.
DC generator:	When both SCG0 and SCG1 are set, the dc generator for the DCO is disabled.

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the ROM with an address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG (see Notes 1 & 3) OFIFG (see Notes 1 & 3) ACCVIFG (see Notes 1 & 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
			0FFFAh	13
			0FFF8h	12
Comparator_A	CMPAIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
			0FFF2h	9
			0FFF0h	8
			0FFEEh	7
Timer_A3	CCIFG0 (see Note 2)	Maskable	0FFECh	6
Timer_A3	CCIFG1, CCIFG2, TAIFG (see Notes 1 & 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 (see Notes 1 & 2) To P1IFG.7 (see Notes 1 & 2)	Maskable	0FFE8h	4
			0FFE6h	3
			0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 (see Notes 1 & 2) To P2IFG.7 (see Notes 1 & 2)	Maskable	0FFE2h	1
Basic Timer1	BTIFG	Maskable	0FFE0h	0, lowest

NOTES: 2. Multiple source flags
3. Interrupt flags are located in the module.
4. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt-enable cannot.

special function registers

The special-function registers (SFR) include module-enable bits that stop or enable the operation of the specific peripheral module. All registers of the peripherals may be accessed if the operational function is stopped or enabled. However, some peripheral current-saving functions are accessed through the state of local register bits. An example is the enable/disable of the analog voltage generator in the LCD peripheral, which is turned on or off using one register bit.

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits that are not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

Address	7	6	5	4	3	2	1	0
1h	BTIE							
	rw-0							

WDTIE: Watchdog-timer-interrupt enable signal
OFIE: Oscillator-fault-interrupt enable signal
NMIIE: Nonmaskable-interrupt enable signal
ACCVIE: (Non)maskable-interrupt enable signal, access violation if flash memory/module is busy
BTIE: Basic Timer1 interrupt enable signal

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG			OFIFG	WDTIFG
				rw-0			rw-1	rw-0

Address	7	6	5	4	3	2	1	0
3h	BTIFG							
	rw-0							

WDTIFG: Set on overflow or security key violation or reset on VCC power-on or reset condition at $\overline{\text{RST}}$/NMI pin
OFIFG: Flag set on oscillator fault
NMIIFG: Set via $\overline{\text{RST}}$/NMI pin
BTIFG: Basic Timer1 interrupt flag

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h/05h								

Legend: rw: **Bit Can Be Read and Written**
rw-0: **Bit Can Be Read and Written. It Is Reset by PUC.**
SFR Bit Not Present in Device

memory organization

		MSP430F412	MSP430C412	MSP430F413	MSP430C413
Memory	Size	4kB	4kB	8kB	8kB
Interrupt vector	ROM	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h	0FFFFh – 0FFE0h
Code memory	ROM	0FFFFh – 0F000h	0FFFFh – 0F000h	0FFFFh – 0E000h	0FFFFh – 0E000h
Information memory	Size	256 Byte	NA	256 Byte	NA
		010FFh – 01000h	NA	010FFh – 01000h	NA
Boot memory	Size	1kB	NA	1kB	NA
		0FFFh – 0C00h	NA	0FFFh – 0C00h	NA
RAM	Size	256 Byte	256 Byte	256 Byte	256 Byte
		02FFh – 0200h	02FFh – 0200h	02FFh – 0200h	02FFh – 0200h
Peripherals	16-bit	01FFh – 0100h	01FFh – 0100h	01FFh – 0100h	01FFh – 0100h
	8-bit	0FFh – 010h	0FFh – 010h	0FFh – 010h	0FFh – 010h
	8-bit SFR	0Fh – 00h	0Fh – 00h	0Fh – 00h	0Fh – 00h

boot ROM containing bootstrap loader

The intention of the bootstrap loader is to download data into the flash memory module. Various write, read, and erase operations are needed for a proper download environment.

functions of the bootstrap loader:

Definition of read: Apply data to pin P1.0/TA0 (BSLTX) and transmit peripheral registers or memory data to pin P1.0/TA0.

write: Read data from pin P1.1/TA0/MCLK (BSLRX) and write it to flash memory

unprotected functions

Mass erase, erase of the main memory (segment 0 to segment n)

Access to the MSP430 via the bootstrap loader is protected. It must be enabled before any protected function can be performed. The 256 bits in 0FFE0h to 0FFFFh provide the access key.

protected functions

All protected functions can be executed only if the access is enabled.

- Write/program byte into flash memory. The parameters passed are start address and number of bytes (the flash segment-write feature of the flash memory is not supported and not used with the UART protocol).
- Segment erase of segment 0 to segment n in main memory, and segment erase of segments A and B in the information memory
- Reading of all data in main memory and information memory
- Reading and writing to all peripheral modules and RAM
- Modifying PC and start program execution immediately

NOTE:

Unauthorized readout of code and data is prevented by the user's definition of the data in the interrupt memory locations.

features of the bootstrap loader are:

- UART communication protocol, fixed to 9600 baud
- Port pin P1.0/TA0 for transmit, P1.1/TA0/MCLK for receive
- TI standard serial protocol definition
- Loader implemented in flash memory version only
- Program execution starts with the user vector at 0FFFEh or with the bootstrap loader (address 0C00h)

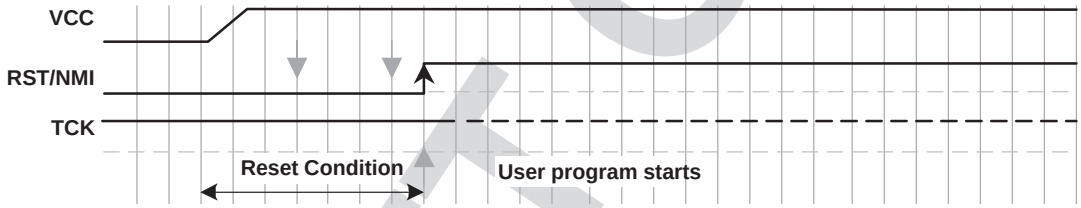
boot ROM containing bootstrap loader (continued)

hardware resources used for serial input/output:

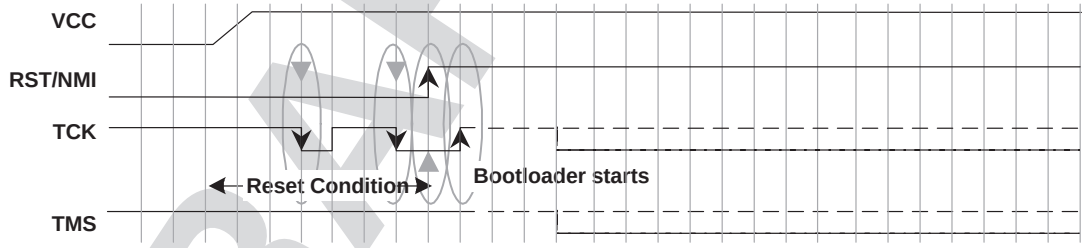
- Pins P1.0/TA0 and P1.1/TA0/MCLK for serial data transmission
- TCK and $\overline{\text{RST}}$/NMI to start program execution at the reset or bootstrap loader vector
- FLL+ module: SCFI0=0, SCFI1=098h, SCG0=1
- Timer_A: Timer_A operates in continuous mode with SMCLK source selected, input divider set to 1, and using CCR0 and polling CCIFG0.
- WDT: Watchdog Timer is halted
- Interrupt: GIE=0, NMIIE=0, OFIFG=0, ACCVIFG=0
- Using the stack depends on the start condition:
  Starting via RST/NMI and TCK pin: 6 bytes used, stack pointer initialized to 220h
  Start via SW (e.g., BR &0C02h): 6 bytes used, on top of the actual stack pointer
- RAM: 20 bytes used, start at address 0200h, last address used: 0219h

NOTE:
When writing RAM data via the bootstrap loader, make sure the stack is outside the range of data to be written.

Program execution begins with the user's reset vector at FFFEh (standard method) if TCK is held high while RST/NMI goes from low to high:



Program execution begins with the bootstrap vector at 0C00h (boot ROM) if TCK has applied a minimum of two negative edges at signal/pin TCK, and if TCK is low while RST/NMI goes from low to high.



The bootstrap loader does not start (via the vector in address 0C00h) if:

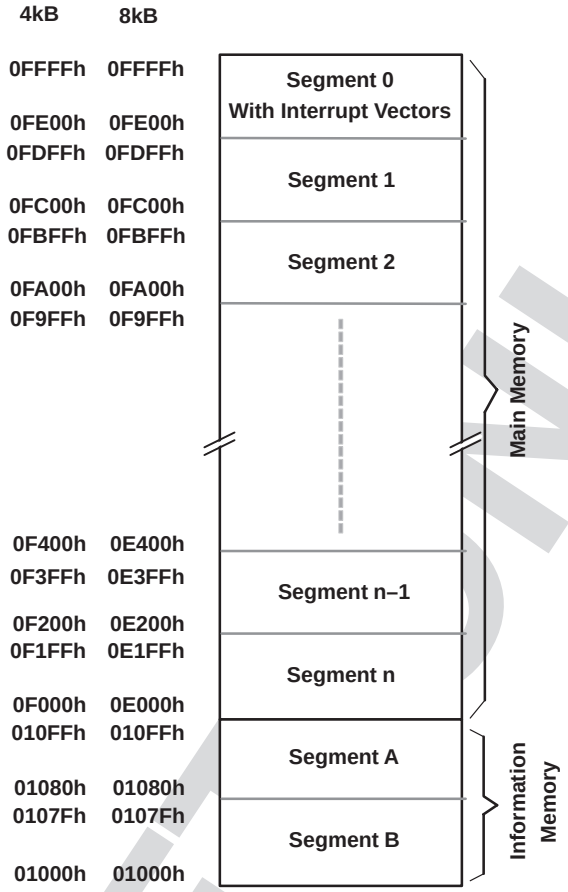
- There are less than two negative edges at TCK while RST/NMI is low
- TCK is high when RST/NMI goes from low to high
- JTAG has control over the MSP430 resources
- The supply voltage V_{CC} drops and a POR is executed
- RST/NMI pin is configured for NMI function (NMI bit is set)

NOTES: 5. The default level of TCK is high. An active low has to be applied to enter the bootstrap loader. Other MSP430s which have a pin function used with a low default level can use an inverted signal.
6. The TMS signal must be high while TCK clocks are applied. This ensures that the JTAG controller function remains in its default mode.

flash memory

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and segment B can be erased individually, or as a group with segments 0–n. Segments A and B are also called *information memory.*
- A security fuse burning is irreversible; no further access to JTAG is possible afterwards
- Internal generation of the programming/erase voltage: no external V_{PP} has to be applied, but V_{CC} increases the supply current requirements.
- Program and erase timing is controlled by hardware in the flash memory—no software intervention is needed.
- The control hardware is called the flash-timing generator. The input frequency of the flash-timing generator should be in the proper range and should be maintained until the write/program or erase operation is completed. No code/program can be executed from the flash memory during programming or erase mode
- During program or erase, no code can be executed from flash memory and all interrupts must be disabled by setting the GIE, NMIIE, ACCVIE, and OFIE bits to zero. If a user program requires execution concurrent with a flash program or erase operation, the program must be executed from memory other than the flash memory (e.g., boot ROM, RAM). In the event that a flash program or erase operation is initiated while the program counter is pointing to the flash memory, the CPU will execute JMP $ instructions until the flash program or erase operation is completed. Normal execution of the previously running software then resumes.
- Unprogrammed, new devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user is recommended to perform an erase of the information memory prior to first use.

flash memory (continued)



flash memory, control register FCTL1, FCTL2, and FCTL3

All control bits are reset during PUC. PUC is active after VCC is applied, a reset condition is applied to the RST/NMI pin or the watchdog timer expires, a watchdog access violation occurs, or an improper flash operation has been performed. Any write to control register FCTL1 during erase, mass erase, or write (programming) ends in an access violation with ACCVIFG=1. In an active segment write mode the control register may be written if wait mode is active (WAIT=1). Read access is possible at any time without restrictions.

The control bits of control register FCTL1 hold all bits that apply write (programming) or erase modes. Writing to the control register requires key word 0A5H in the *high-byte*. Any other data there generates a power-up clear (PUC) which resets the controller.

FCTL1, 0128h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								SEG WRT	WRT	res.	res.	res.	MEras	Erase	res.
								rw-0	rw-0	r0	r0	r0	rw-0	rw-0	r0

FCTL1 Read: ◄— 096h —►
FCTL1 Write: ◄— 0A5h —►

The bits control erase or mass erase of the flash, write (WRT), or programming or segment write (SEGWRT).

The control register FCTL2 determines the operation of the timing generator that generates all the timing signals necessary for write, erase, and mass erase from the selected clock source. One of three different clock sources may be selected. The selected clock source must be divided to meet the frequency requirements specified in the recommended operating conditions.

NOTE:
The mass erase duration generated by the flash timing generator is at least 11.1 ms. The cummulative mass erase time needed is 200 ms. This can be achieved by repeating the mass erase operation until the cumulative mass erase time is met (a minimum of 19 cycles may be

FCTL2, 012Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								SSEL1	SSEL0	FN5	FN4	FN3	FN2	FN1	FN0
								rw-0	rw-1	rw-0	rw-0	rw-0	rw-0	rw-1	rw-0

FCTL2 Read: ◄— 096h —►
FCTL2 Write: ◄— 0A5h —►

Control register FCTL3 determines the access and flags the status and error conditions of the flash operation. There are no restrictions to modify this control register. Control bits are reset or set (WAIT) with PUC but key violation bit KEYV is reset with POR.

FCTL3, 012Ch

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								res.	res.	EMEX	Lock	WAIT	ACCV IFG	KEYV	BUSY
								r0	r0	rw-0	rw-1	r-1	rw-0	rw-(0)	r(w)-0

FCTL3 Read: ◄— 096h —►
FCTL3 Write: ◄— 0A5h —►

flash memory, interrupt and security key violation

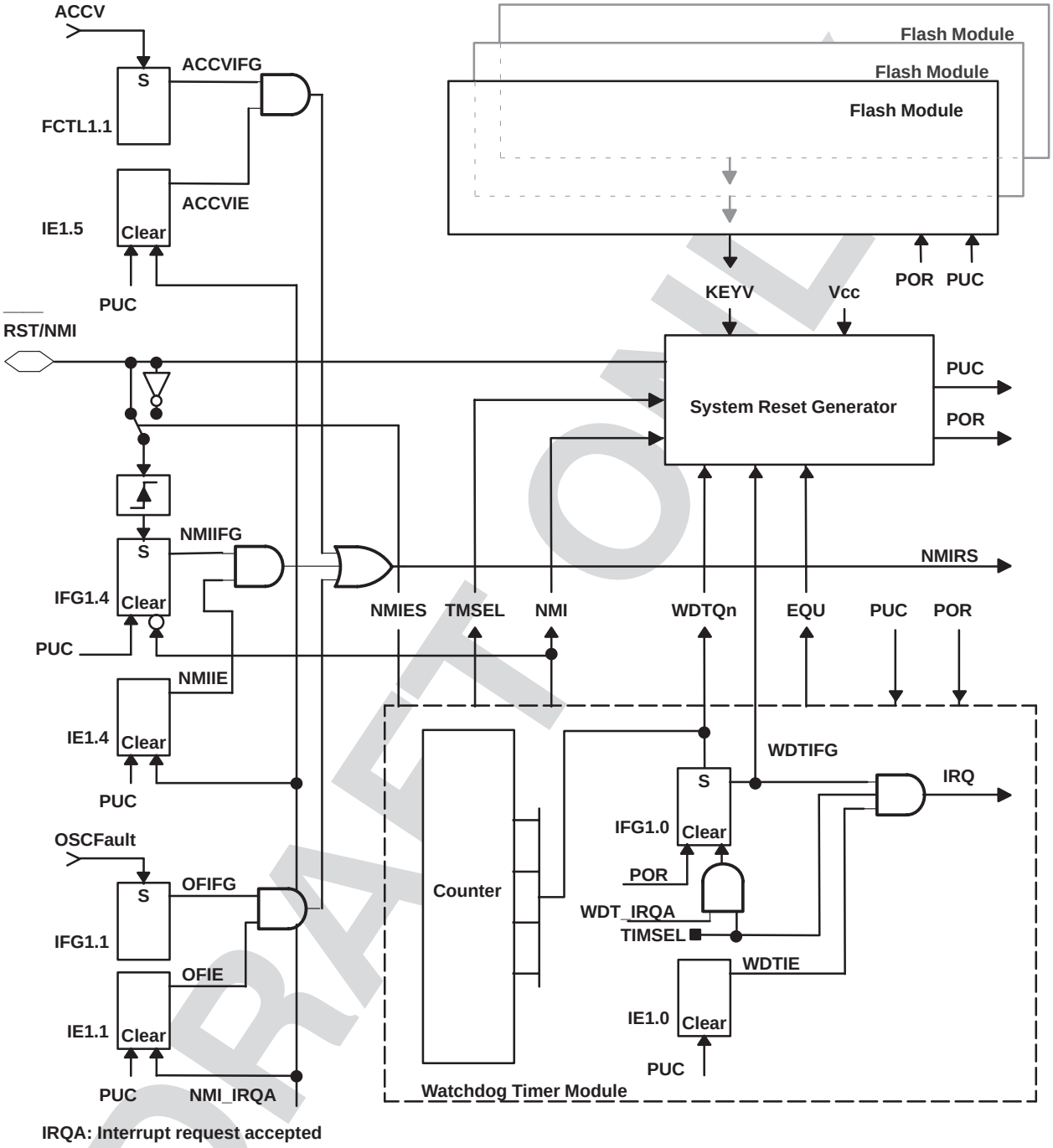


Figure 1. Block Diagram of NMI Interrupt Sources

One NMI vector is used for three NMI events: RST/NMI (NMIIFG), oscillator fault (OFIFG) and flash memory access violation (ACCVIFG). The software can determine the source of the interrupt request since all flags remain set until they are reset by software. The enable flag(s) must be set only within one instruction directly before the return-from-interrupt RETI instruction. This ensures that the stack remains under control. A pending NMI interrupt request does not increase stack demand unnecessarily.

peripherals

Peripherals are connected to the CPU through data, address, and control busses, and can be easily handled using all memory-manipulation instructions.

oscillator and system clock

Three clocks are used in the system:

- Main system (master) clock MCLK, used by the CPU and the system
- Subsystem (master) clock SMCLK, used by the peripheral modules
- Auxiliary clock ACLK, originated by LFXT1CLK (crystal frequency) and used by the peripheral modules

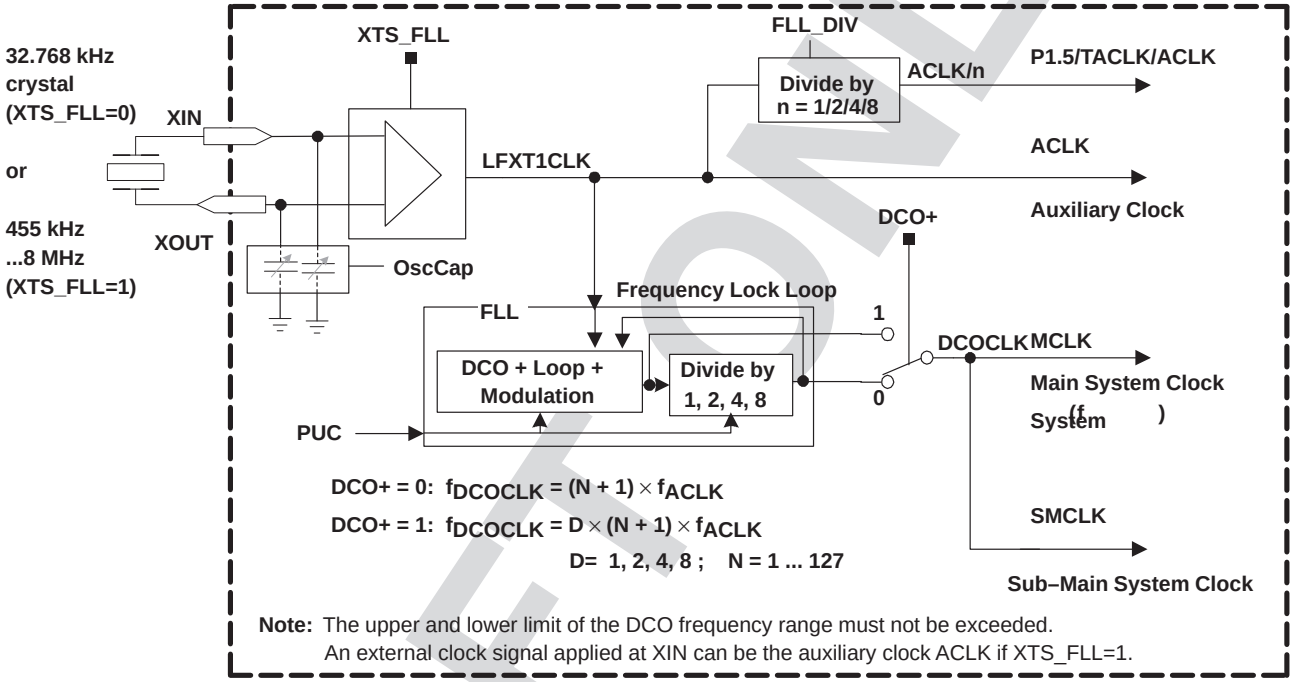


Figure 2. Block Diagram of FLL+ Oscillator and System Clock

The ACLK is defined by connecting a low-power, low-frequency, or high-frequency crystal to the oscillator, or by applying an external clock source (XTS_FLL must be set). The crystal oscillator may be switched off when the ACLK oscillator is not needed for the present operation mode.

The software selects the DCOCLK frequency. The DCOCLK is active if SCG1 is reset and stopped if SCG1 is set. The dc generator can be stopped when SCG0 and SCG1 are reset. The dc generator defines the basic DCO frequency and can be adjusted in five steps using control bits FN_2, FN_3, FN_4, and FN_8.

When the target frequency needs modification of the FN_x bits, increasing D or setting DCO+, the following sequence ensures that the maximum system frequency f_{system} is not exceeded:

1. Save FLL lock bit (SCG0 in status register) and set it; loop control goes off.
2. Load modulation control register SCFQCTL with new data (modulation bit M, multiply factor N).
3. Set DCO control bits and MSB's of modulator: SCFI1 = 0Fh to lowest possible frequency.
4. Select DCO+ control bit to be set or reset.
5. Load control register SCFI0 with new data.
6. Restore or set/reset FLL control bit.

oscillator and system clock (continued)

NOTE:
The system clock generator starts with the DCOCLK for MCLK (CPU clock) and program execution starts quickly. The software defines the ACLK clock generation through control bit manipulation.

The start conditions for MCLK and SMCLK frequency are identical to the FLL in MSP430x3xx devices.

The ACLK, supplied for external use via port P1.5, may be divided by 1, 2, 4, or 8. This ensures clock signal compatibility to the MSP430x3xx and MSP430x1xx families.

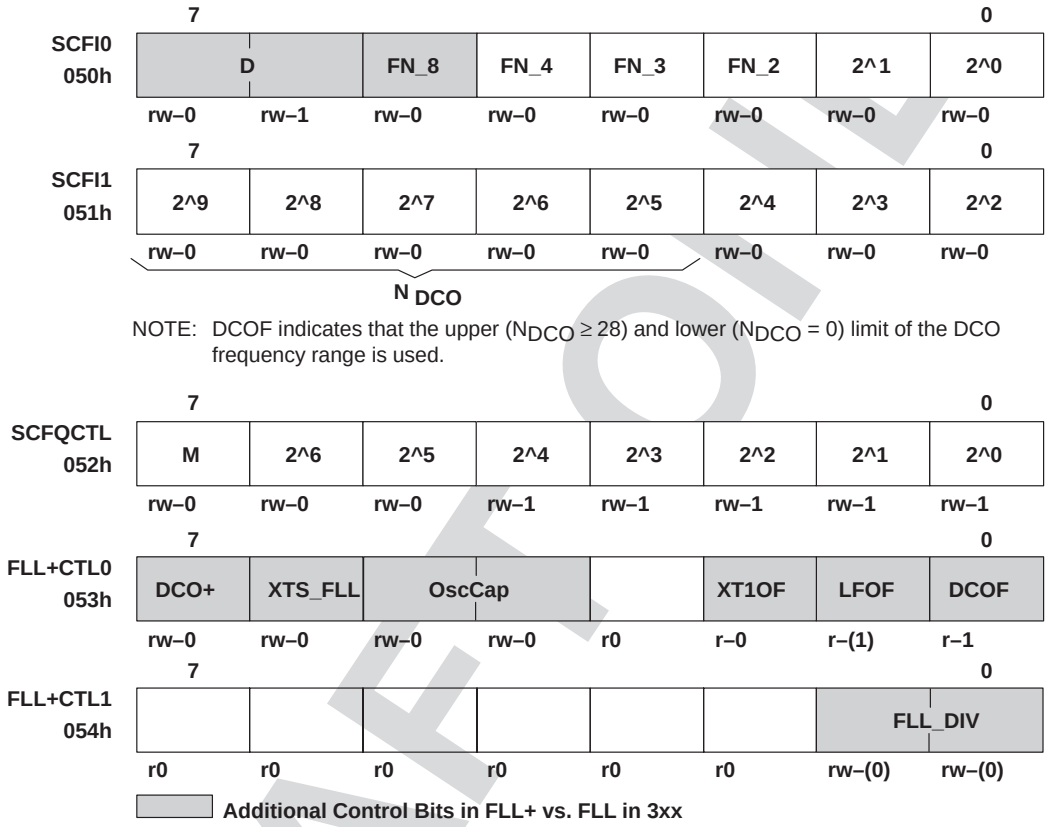


Figure 3. Registers and Control Bits of FLL+ Oscillator and System Clock

Three oscillator-fault bits, DCOF, XT1OF, and LFOF, indicate if the DCO, LFXT1 oscillator-HF mode, and LFXT1 oscillator-LF mode, respectively, are operating properly. The oscillator fault XT1OF is applicable only if XTS_FLL=1, and LFOF is applicable only if XTS_FLL=0. If one of the three oscillator faults occurs, the OSCFault signal set the OFIFG flag. An NMI service is requested if the interrupt enable bit OFIE is set.

WARNING:
The oscillator fault flag is set if the oscillator is inactive. Inactivity can be caused by system failure such as crystal damage, broken leads, etc., but also if the oscillator is switched on or switched from nonselected to selected.

oscillator and system clock (continued)

The clock signals ACLK, MCLK, and SMCLK can be used externally via port pins.

Different application requirements and system conditions dictate different system clock requirements. The FLL+ clock system supports the following conditions:

- High frequency for quick reaction to system hardware requests or events (DCO/FLL+XT1)
- Low frequency to minimize current consumption, EMI, etc. (LF)
- Stable peripheral clock for timer applications, such as real time clock (RTC)
- Enabling of start-stop operation with minimum delay (DCO)

brownout, supply voltage supervisor

The brownout detects if a supply voltage is applied to or removed from the VCC terminal. The supply voltage supervision detects if the supply voltage drops to the minimum recommended operational value. After the supply voltage is applied, the supply voltage supervisor circuitry is switched inactive to have the current consumption at a minimum. The user's software may switch the supervisor on as required. The user's software can also determine if a POR is generated or if only one bit in the control register latches a low-voltage situation.

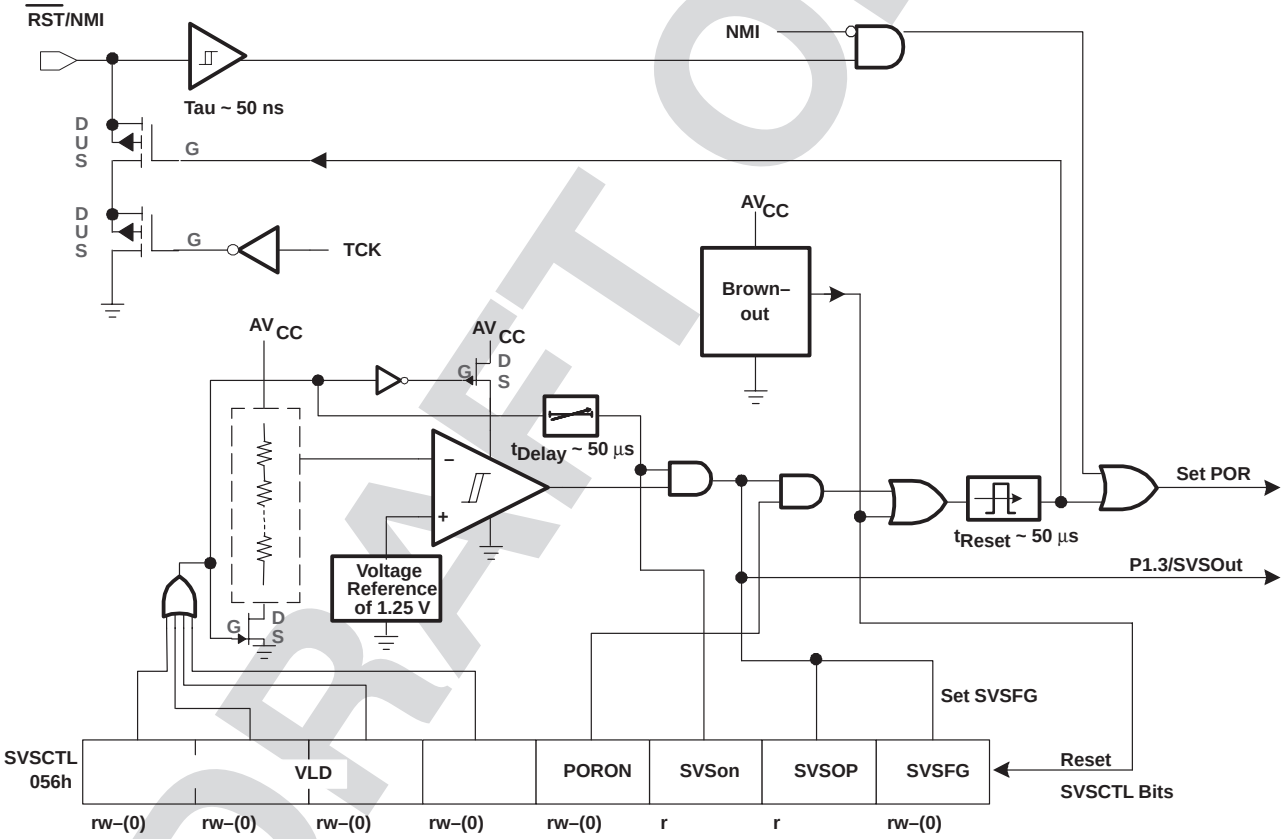


Figure 4. Block Diagram of Brown-Out and Supply Voltage Supervision

The VLD bits control the on/off state of the supply voltage supervisor (SVS) circuitry. The SVS function is off if VLD=0, and on if VLD=1. Bit PORON enables or disables the automatic reset of the MSP430 upon a low-voltage situation. If PORON=1, a low-voltage situation generates a POR signal and resets the MSP430.

The SVSon bit indicates that the SVS circuitry is switched on and operational. Bit SVSOP is used to watch the actual SVS comparator output. Bit SVSFG is set if a low-voltage situation is detected and remains set until software resets it; SVSFG latches such events whereas SVSOP represents the actual output of the comparator.

digital I/O

There are six 8-bit I/O ports—Ports P1 through P6—implemented. Ports P1 and P2 use seven control registers, while ports P3, P4, P5, and P6 use only four of the control registers to provide maximum digital input/output flexibility to the application:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Interrupt processing of external events is fully implemented for all eight bits of ports P1 and P2.
- Read/write access to all registers using all instructions is possible.

The seven control registers are:

- Input register 8 bits @ Ports P1 through P6
- Output register 8 bits @ Ports P1 through P6
- Direction register 8 bits @ Ports P1 through P6
- Interrupt edge select 8 bits @ Ports P1 and P2
- Interrupt flags 8 bits @ Ports P1 and P2
- Interrupt enable 8 bits @ Ports P1 and P2
- Selection (port or module) 8 bits @ Ports P1 through P6

Each one of these registers contains eight bits. Two interrupt vectors are implemented: one commonly used for any interrupt event on Ports P1.0 to P1.7, and another commonly used for any interrupt event on Ports P2.0 to P2.7.

Ports P3, P4, P5, and P6 have no interrupt capability.

LCD drive

The liquid crystal displays (LCDs) for static, 2-MUX, 3-MUX, and 4-MUX operation can be driven directly. The operation of the controller LCD logic is defined by software through memory-bit manipulation. The LCD memory is part of the LCD module, not part of data memory. Eight mode and control bits define the operation and current consumption of the LCD drive. The information for the individual digits can be easily obtained using table programming techniques combined with the proper addressing mode. The segment information is stored into LCD memory using instructions for memory manipulation.

The drive capability is defined by the external resistor divider that supports analog levels for 2-, 3-, and 4-MUX operation. Groups of the digital I/O-LCD segment lines can be selected digital I/O or LCD function. Digital I/Os are selected by default after POR and PUC. The MSP430x41x configuration has four common lines, 24 segment lines, and four terminals for adjusting the analog levels.

LCD mode bits 5,6,7:

0 : Pins P5.1/S0 to P2.2/S23 are digital I/O, not segment lines
1 : Pins P5.1/S0 to P3.2/S15 are segment lines, P3.1/S16 to P2.2/S23 are digital I/O
2 : Pins P5.1/S0 to P2.6CAOUT//S19 are segment lines, P2.5/S20 to P2.2/S23 are digital I/O
3..7 : Pins P5.1/S0 to P2.2/S23 are segment lines

Basic Timer1

The Basic Timer1 (BT1) divides the frequency of SMCLK or ACLK, as selected with the SSEL bit, to provide low-frequency control signals. This is done within the system by one central divider, the Basic Timer1, to support low-current applications. The BTCTL control register contains the flags that control or select the different operational functions. When the supply voltage is applied or when a device is reset (RST/NMI pin), a watchdog overflow or a watchdog security key violation occurs; all bits in the register hold undefined or unchanged status. The user software usually configures the operational conditions on the BT during initialization. The Basic Timer1 has two eight-bit timers which can be cascaded to a sixteen-bit timer. Both timers can be read and written by software. Two bits in the SFR address range handle the system control interaction according to the function implemented in the Basic Timer1. These two bits are the Basic Timer1 interrupt flag (BTIFG) and the Basic Timer1 interrupt enable (BTIE) bit.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after software upset has occurred. A system reset is generated if the selected time interval expires. If an application does not require this watchdog function, the module can work as an interval timer, which generates an interrupt after a selected time interval.

The watchdog timer counter (WDTCNT) is a 15/16-bit up counter not directly accessible by software. The WDTCNT is controlled using the watchdog timer control register (WDTCTL), which is an 8-bit read/write register. Writing to WDTCTL in either operating mode (watchdog or timer) is only possible when using the correct password (05Ah) in the high-byte. If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated. The password is read as 069h to minimize accidental write operations to the WDTCTL register. The low-byte stores data written to the WDTCTL. In addition to the Watchdog Timer control bits, there are two bits included in the WDTCTL that configure the NMI pin.

Timer_A (three capture/compare registers)

The timer module offers one sixteen-bit counter and three capture/compare registers. The timer clock source can be selected from the external source TACLK (noninverted via SSEL=0 or inverted via SSEL=3), or from two internal sources—ACLK (SSEL=1) or SMCLK (SSEL=2)). The clock source can be divided by one, two, four, or eight. The timer can be fully controlled (in word mode)—it can be halted, read, and written. It can be stopped, run continuously, or made to count up or up/down using one compare block to determine the period. The three capture/compare blocks are configured by the application to run in capture or compare mode.

The capture mode is mostly used to individually measure internal or external events from any combination of positive, negative, or positive and negative edges. It can also be stopped by software. Three different external events (TA0, TA1, and TA2) can be selected. In the capture/compare register CCR2, ACLK is the capture signal if CCI2B is selected. Software capture is chosen if CCISx=2 or CCISx=3.

The compare mode is mostly used to generate timing for the software or application hardware, or to generate pulse-width modulated output signals for various purposes such as D/A conversion functions or motor control. An individual output module is assigned to each of the three capture/compare registers. This module can run independently of the compare function or can be triggered in several ways.

Timer_A (three capture/compare registers) (continued)

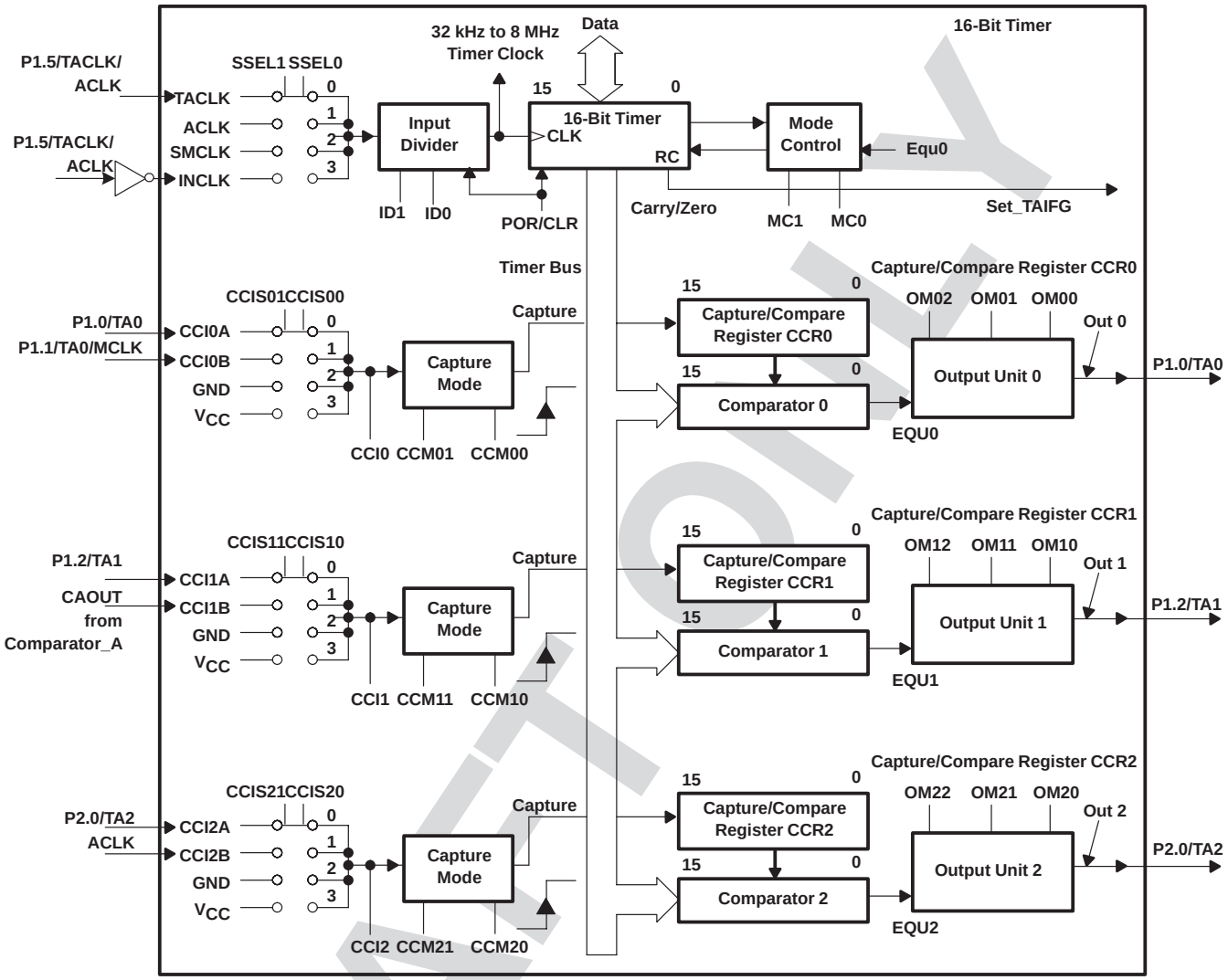


Figure 5. Timer_A Configuration With Three Capture/Compare Registers (CCRs)

The module uses two interrupt vectors. One individual vector is assigned to capture/compare block CCR0 and one common interrupt vector is implemented for the timer and the other two capture/compare blocks. The three interrupt events using the same vector are identified by an individual interrupt vector word. The interrupt vector word is used to add an offset to the program counter to continue the interrupt handler software on the corresponding program location. This simplifies the interrupt handler and gives each interrupt event the same overhead of 5 cycles in the interrupt handler.

Comparator_A

The primary functions of the comparator module are: support of precision slope conversion in A/D applications, battery voltage supervision, and external analog signal monitoring. The comparator is connected to port pins P1.6/CA0 (+ terminal) and to P1.7/CA1 (–terminal). It is controlled via eight control bits in the CACTL register.

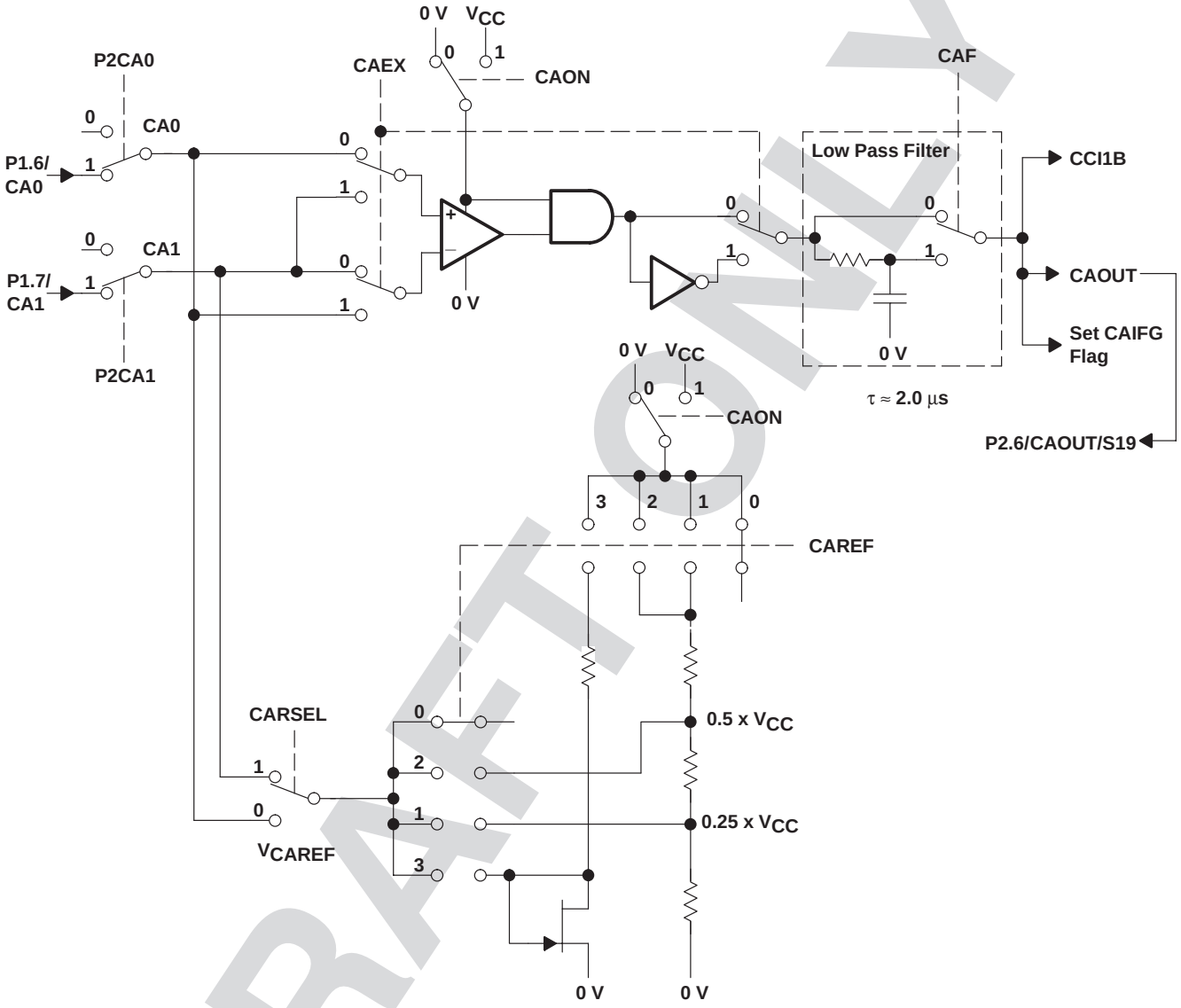


Figure 6. Block Diagram of Comparator_A

The eight control bits are used to connect the comparator to the supply voltage, apply external or internal signals to the +terminal and –terminal, and select to use the comparator output, including a small filter.

Eight additional bits in register CAPD are implemented into the Comparator_A module and enable the SW to switch off the input buffer of Port P1. A CMOS input buffer dissipates supply current when the input is not near V_{SS} or V_{CC}. Control bits CAPI0 to CAPI7 are initially reset and the port input buffer is active. The port input buffer is inactive if the corresponding control bit is set.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog Timer control	WDTCTL	0120h
Timer_A3	Timer_A interrupt vector	TAIV	012Eh
	Timer_A control	TACTL	0160h
	Capture/compare control 0	CCTL0	0162h
	Capture/compare control 1	CCTL1	0164h
	Capture/compare control 2	CCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A register	TAR	0170h
	Capture/compare register 0	CCR0	0172h
	Capture/compare register 1	CCR1	0174h
	Capture/compare register 2	CCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
PERIPHERALS WITH BYTE ACCESS			
LCD	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD Memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDCTL	090h
Comparator_A	Comp._A port disable	CAPD	05Bh
	Comp._A control2	CACTL2	05Ah
	Comp._A control1	CACTL1	059h
BrownOUT, SVS	SVS control register	SVSCTL	056h
System Clock FLL+	FLL+ Control1	FLL+CTL1	054h
	FLL+ Control0	FLL+CTL0	053h
	System clock Frequency control	SCFQCTL	052h
	System clock Frequency integrator	SCFI1	051h
	System clock Frequency integrator	SCFI0	050h
Basic Timer1	BT counter2	BTCNT2	047h
	BT counter1	BTCNT1	046h
	BT control	BTCTL	040h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P6	Port P6 Selection	P6SEL	037h
	Port P6 Direction	P6DIR	036h
	Port P6 Output	P6OUT	035h
	Port P6 Input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings†

Voltage applied at V_{CC} to V_{SS} . . . . . –0.3 V to + 4.1 V
Voltage applied to any pin (referenced to V_{SS}) . . . . . –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . . ±2 mA
Storage temperature (unprogrammed device) . . . . . –55°C to 150°C
Storage temperature (programmed device) . . . . . –40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
All voltages referenced to V_{SS}.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNITS
Supply voltage during program execution, SVS disabled V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430x41x	1.8		3.6	V
Supply voltage during program execution, SVS enabled (see Note 7), V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430x41x	2		3.6	V
Supply voltage during programming flash memory, V_{CC} (AV_{CC} = DV_{CC} = V_{CC})		MSP430F413	2.7		3.6	V
Supply voltage, V_{SS}			0.0		0.0	V
Operating free-air temperature range, T_A		MSP430x41x	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Note 8)	LF selected, XTS_FLL=0	Watch crystal		32768		Hz
	XT1 selected, XTS_FLL=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS_FLL=1	Crystal	450		8000	kHz
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	
Flash-timing-generator frequency, $f_{(FTG)}$		MSP430F413	257		476	kHz
Cumulative program time, $t_{(CPT)}$ (see Note 9)		V_{CC} = 2.7 V/3.6 V MSP430F413			3	ms
Cumulative mass time, $t_{(CMEras)}$ (see Note 10)		V_{CC} = 2.7 V/3.6 V MSP430F413	200			ms
Input levels at Xin and Xout	$V_{IL(Xin, Xout)}$	V_{CC} = 2.2 V/3 V XTS_FLL=1	V_{SS}		$0.2 \times V_{SS}$	V
	$V_{IH(Xin, Xout)}$		$0.8 \times V_{CC}$		V_{CC}	

NOTES: 7. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing supply voltage. POR is going inactive when the supply voltage is raised above minimum supply voltage plus the hysteresis of the SVS circuitry.
8. The LFXT1 oscillator in LF-mode requires a watch crystal.
9. The cumulative program time must not be exceeded during a segment-write operation.
10. The mass-erase duration generated by the flash timing generator is at least 11.1 ms. The cummulative mass-erase time needed is 200 ms. This can be achieved by repeating the mass-erase operation until the cumulative mass-erase time is met (a minimum of 19 cycles may be required).

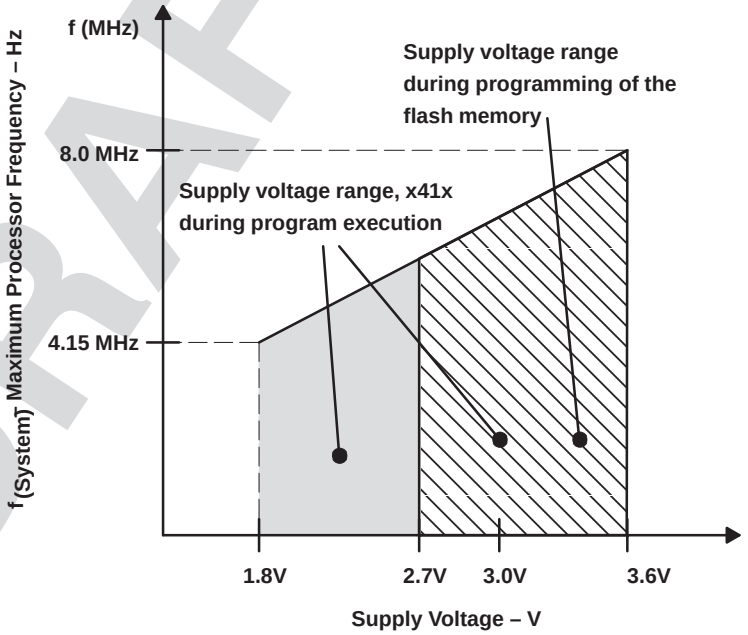


Figure 7. Frequency vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current, $f_{(System)}$ = 1 MHz (see Note 10)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz, XTS_FLL=0	T_A = –40°C to 85°C	V_{CC} = 2.2 V		225	TBD	µA
			V_{CC} = 3 V		340	TBD	
$I_{(LPM0)}$	Low-power mode, (LPM0) FN_8=FN_4=FN_3=FN_2=0	T_A = –40°C to 85°C	V_{CC} = 2.2 V		32	TBD	µA
			V_{CC} = 3 V		55	TBD	
$I_{(LPM2)}$	Low-power mode, (LPM2),	T_A = –40°C to 85°C	V_{CC} = 2.2 V		13	TBD	µA
			V_{CC} = 3 V		20	TBD	
$I_{(LPM3)}$	Low-power mode, (LPM3)	T_A = –40°C	V_{CC} = 2.2 V		0.9	1.8	µA
		T_A = 25°C			0.8	1.5	
		T_A = 85°C			1.5	2.8	
		T_A = –40°C	V_{CC} = 3 V		0.9	1.8	µA
		T_A = 25°C			0.8	1.5	
		T_A = 85°C			1.5	3.9	
$I_{(LPM4)}$	Low-power mode, (LPM4)	T_A = –40°C	V_{CC} = 2.2 V/3 V		0.1	0.5	µA
		T_A = 25°C			0.1	0.5	
		T_A = 85°C			0.8	2.5	

NOTE 11: All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2, LPM3, and LPM4 are measured with active Basic Timer1 and LCD (ACLK selected).
The current consumption of the Comparator_A and the SVS module are specified in the respective sections.

current consumption of active mode versus system frequency, F version

$$I(AM) = I(AM)\ [1\ MHz] \times f(System)\ [MHz]$$

current consumption of active mode versus supply voltage, F version

$$I_{(AM)} = I_{(AM)\ [3\ V]} + xxx\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs – Ports P1, P2, P3, P4, P5, and P6; $\overline{\text{RST}}$/NMI; JTAG: TCK, TMS, TDI, TDO

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.9	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

outputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V,	See Note 11	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V,	See Note 12	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V,	See Note 11	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V,	See Note 12	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 11	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 12	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 11	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 12	V_{SS}		V_{SS}+0.6	

NOTES: 12. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
13. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

input frequency – Ports P1, P2, P3, P4, P5, and P6

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(IN)}$	$t_{(h)} = t_{(L)}$	V_{CC} = 2.2 V			8	MHz
		V_{CC} = 3 V			10	

capture timing _ Timer_A3: TA0, TA1, TA2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(int)}$	TA0 to TA4: External trigger signal for capture flag (see Note 13)	V_{CC} = 2.2 V/3 V	1.5			Cycle
		V_{CC} = 2.2 V	62			ns
		V_{CC} = 3 V	50			

NOTE 14: The external capture signal triggers the capture event every time when the minimum t_{cap} cycles and time parameters are met. A capture may be triggered with capture signals even shorter than t_{cap}. Both the cycle and timing specifications must be met to ensure a correct capture of the 16-bit timer value and to ensure the flag is set.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{Px.y}$	(1 ≤ x ≤ 6, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ± 1.5mA	V_{CC} = 2.2 V	DC		10	MHz
			V_{CC} = 3 V	DC		TBD	
f_{ACLK}, f_{MCLK}, f_{SMCLK}	P1.1/TA0/MCLK, P1.5/TACLK/ ACLK	C_L = 20 pF				f_{System}	MHz
t_{Xdc}	Duty cycle of output frequency	P1.5/TACLK/ACLK, C_L = 20 pF V_{CC} = 2.2 V / 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1/n}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 2.2 V / 3 V	$f_{MCLK} = f_{LFXT1/n}$	50%– 15 ns	50%	50%+ 15 ns	
			$f_{MCLK} = f_{DCOCLK}$	50%– 15 ns	50%	50%+ 15 ns	

external interrupt timing

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(int)}$	Ports P1, P2: External trigger signal for the interrupt flag (see Note 14)	V_{CC} = 2.2 V/3 V	1.5			ns
		V_{CC} = 2.2 V	62			
		V_{CC} = 3 V	50			

NOTE 15: The external signal sets the interrupt flag every time the minimum t_{int} cycle and time parameters are met. It may be set even with trigger signals shorter than t_{int}. Both the cycle and timing specifications must be met to ensure the flag is set. t_{int} is measured in MCLK cycles.

wake-up LPM3 (see Note 15)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(LPM3)}$	Delay time	V_{CC} = 2.2 V/3 V			6	µs

NOTE 16: The delay time $t_{(LPM3)}$ is independent of the system frequency and V_{CC}.

leakage current (see Note 16)

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current	Port P1	Port 1: $V_{(P1.x)}$ (see Note 17)	V_{CC} = 2.2 V/3 V			±50	nA
$I_{lkg(P6.x)}$		Port P6	Port 6: $V_{(P6.x)}$ (see Note 17)				±50	

NOTES: 17. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
18. The port pin must be selected as input and there must be no optional pullup or pulldown resistor.

RAM (see Note 18)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU halted (see Note 18)	1.6			V

NOTE 19: This parameter defines the minimum supply voltage when the data in the program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

LCD

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at P5.7/R33	V_{CC} = 3 V	2.5		V_{CC} +0.2	V
$V_{(23)}$		Voltage at P5.6/R23			$(V_{33}–V_{03}) \times 2/3 + V_{03}$		
$V_{(13)}$		Voltage at P5.5/R13			$(V_{(33)}–V_{(03)}) \times 1/3 + V_{(03)}$		
$V_{(03)}$		Voltage at R03		$V_{(33)}$ – 2.5		V_{CC} +0.2	
$V_{O(HLCD)}$	Output 1	$I_{(HLCD)} \le$ 10 nA	V_{CC} = 3 V	$V_{(RSS)}$ +0.125		V_{CC}	V
$V_{O(LLCD)}$	Output 0	$I_{(LLCD)} \le$ 10 nA		V_{SS}		V_{SS} + 0.125	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V			±20	nA
$I_{(R13)}$		P5.5/R13 = V_{CC}/3				±20	
$I_{(R23)}$		P5.6/R23 = 2 × V_{CC}/3				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{Sxx)}$ = –3 µA,	V_{CC} = 3 V	$V_{(03)}$		$V_{(03)}$ – 0.1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ – 0.1	
$V_{(Sxx2)}$				$V_{(23)}$		$V_{(23)}$ – 0.1	
$V_{(Sxx3)}$				$V_{(33)}$		$V_{(33)}$ + 0.1	

Comparator_A (see Note 19)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(CC)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	µA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=0, CARSEL=0, CAREF=1/2/3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V		30	50	µA
			V_{CC} = 3 V		45	71	
$V_{(Ref025)}$		PCA0=1, CARSEL=1, CAREF=1, No load at P2.3/CA0 and P2.4/CA1	V_{CC} = 2.2 V / 3V	0.23	0.24	0.25	V
$V_{(Ref050)}$		PCA0=1, CARSEL=1, CAREF=2, No load at P2.3/CA0 and P2.4/CA1	V_{CC} = 2.2V / 3V	0.47	0.48	0.50	V
$V_{(RefVT)}$		PCA0=1, CARSEL=1, CAREF=3, No load at P2.3/CA0 and P2.4/CA1; T_A=85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3.0 V	400	490	550	
$V_{(IC)}$	Common-mode input voltage range	CAON=1	V_{CC} = 2.2V/3V	0		VCC–1.0	V
$V_{(offset)}$	Offset voltage	See Note 20	VCC = 2.2 V/3V	–30		+30	mV
V_{hys}	Input hysteresis	CAON = 1	V_{CC} = 2.2V / 3V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2V	160	185	210	ns
			V_{CC} = 3V	90	110	130	
		T_A = 25°C Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2V	1.8	2.6	3.4	µs
			V_{CC} = 3V	1.3	1.8	2.6	
$t_{(response\ HL)}$		T_A = 25°C Overdrive 10 mV, without filter: CAF = 0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, with filter: CAF = 1	V_{CC} = 2.2 V	1.4	1.9	3.4	µs
			V_{CC} = 3.0 V	0.9	1.5	2.6	

NOTES: 20. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
21. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

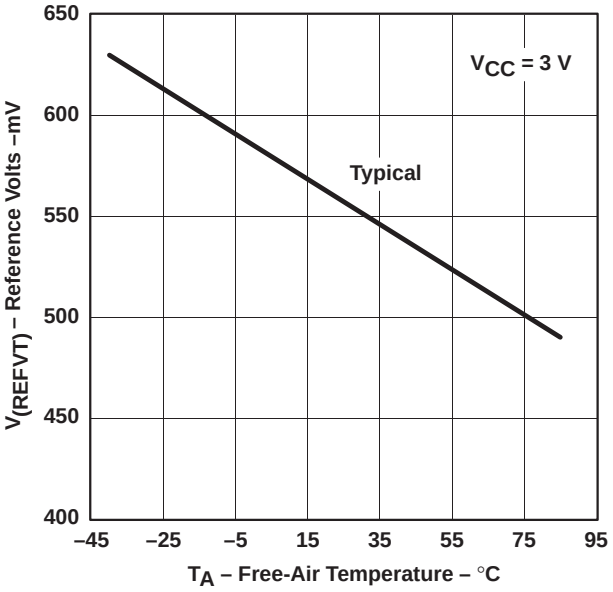


Figure 8. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

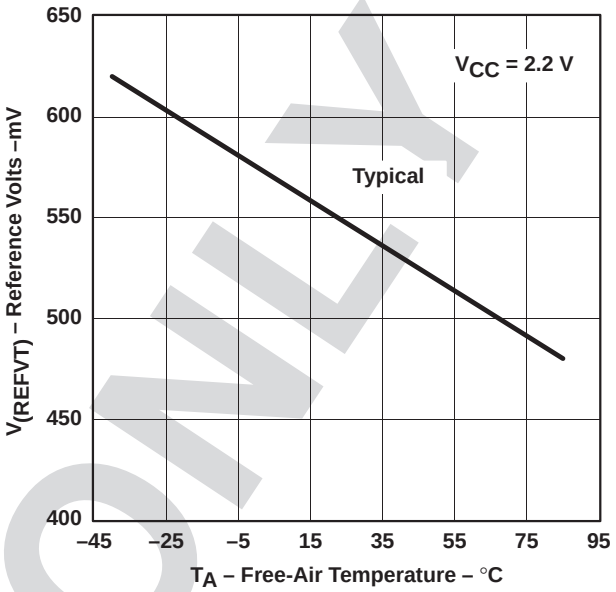


Figure 9. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

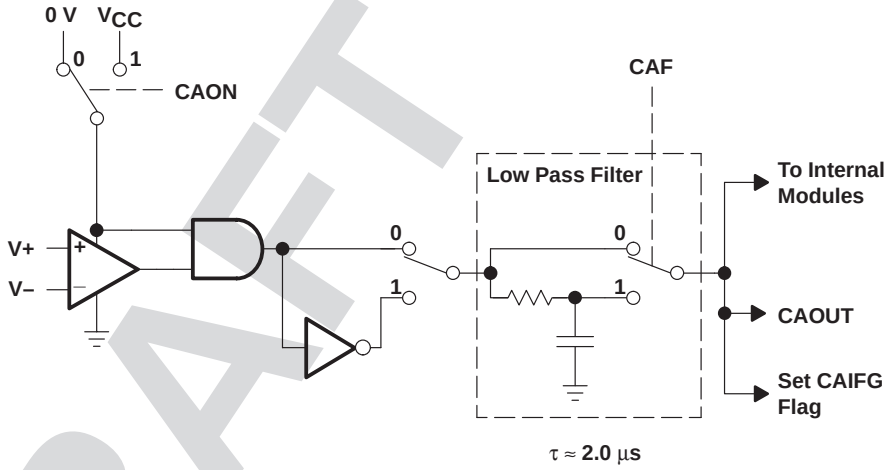


Figure 10. Block Diagram of Comparator_A Module

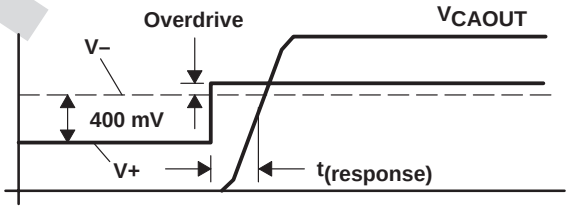


Figure 11. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR brownout, reset (see Note 21)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{BOR(delay)}$	Brownout	$dV_{CC}/dt \geq 30$ V/ms	5		150	µs
		$dV_{CC}/dt \leq 30$ V/ms			2000	
$V_{CC(start)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 12)	$0.7 \times V_{B\_IT-}$			V
$V_{(B,IT-)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 12, 13, 14)	0.9	1.35	1.71	V
$V_{hys(B,IT-)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 12)	70	100	110	mV
$t_{(reset)}$		Pulse length needed at RST/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			µs

NOTE 22: The current consumption of the brown-out module is already included in the I_{CC} current consumption data.

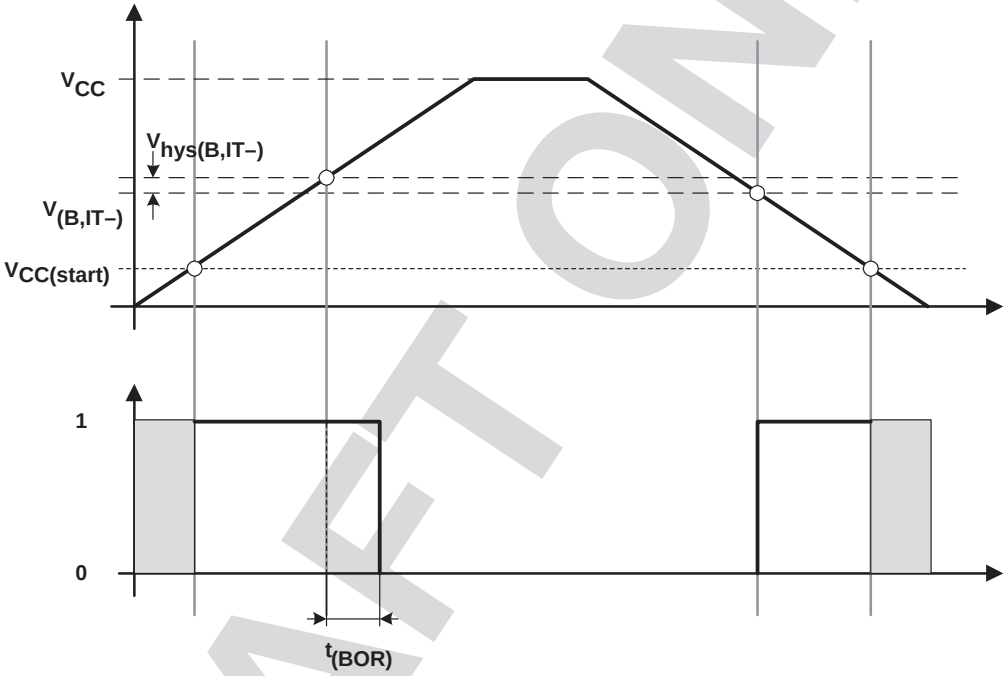


Figure 12. POR/Brownout Reset (BOR) vs Supply Voltage

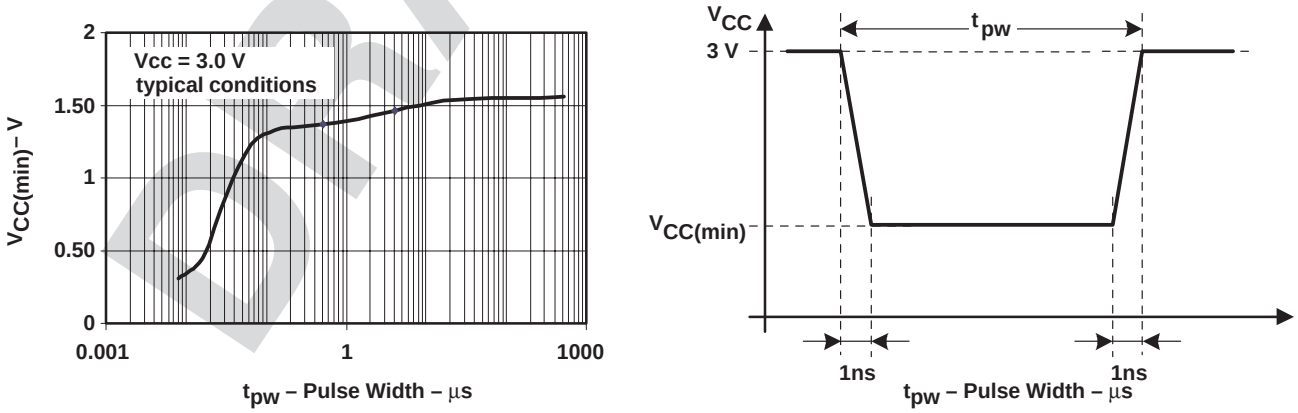


Figure 13. $V_{(CC)min}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

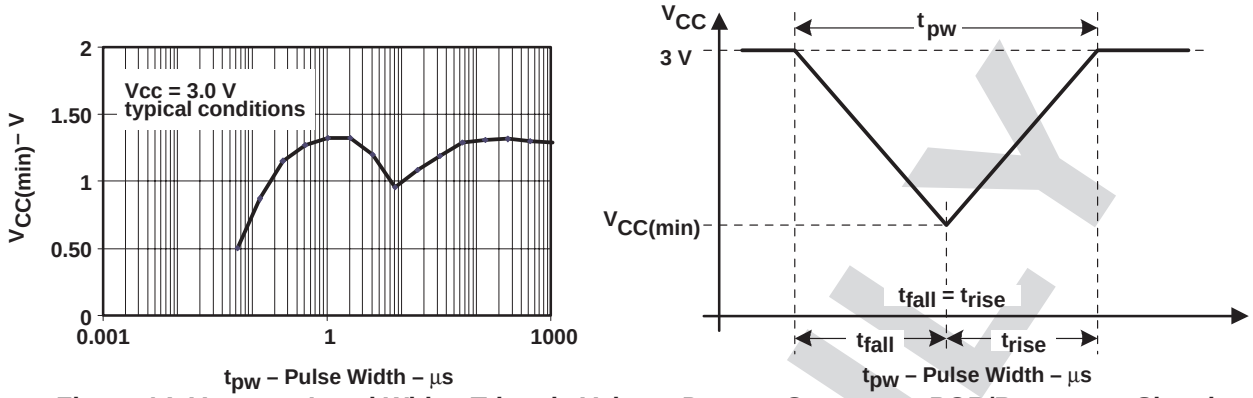


Figure 14. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brown-out Signal

SVS (supply voltage supervisor), reset

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SVSR(delay)}$	SVS	$dV_{CC}/dt \geq 30V/ms$	5		150	µs
		$dV_{CC}/dt \leq 30V/ms$			2000	µs
$t_{SVSon(delay)}$		SVSon, switch from 0 to 1, V_{CC} = 3 V	20		150	µs
$V_{SVS(start)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 15)		1.55	1.7	V
$V_{(SVS,IT–)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 15)	1.8	1.85	1.9	V
$V_{hys(B,IT–)}$		$dV_{CC}/dt \leq 3$ V/s (see Figure 15)	70	100	150	mV
$I_{CC(SVS)}$ (See Note 23)		VLD ≠ 0 (VLD bits are in SVSCTL register), V_{CC} = 2.2V/ 3V		10	15	µA

NOTE 23: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

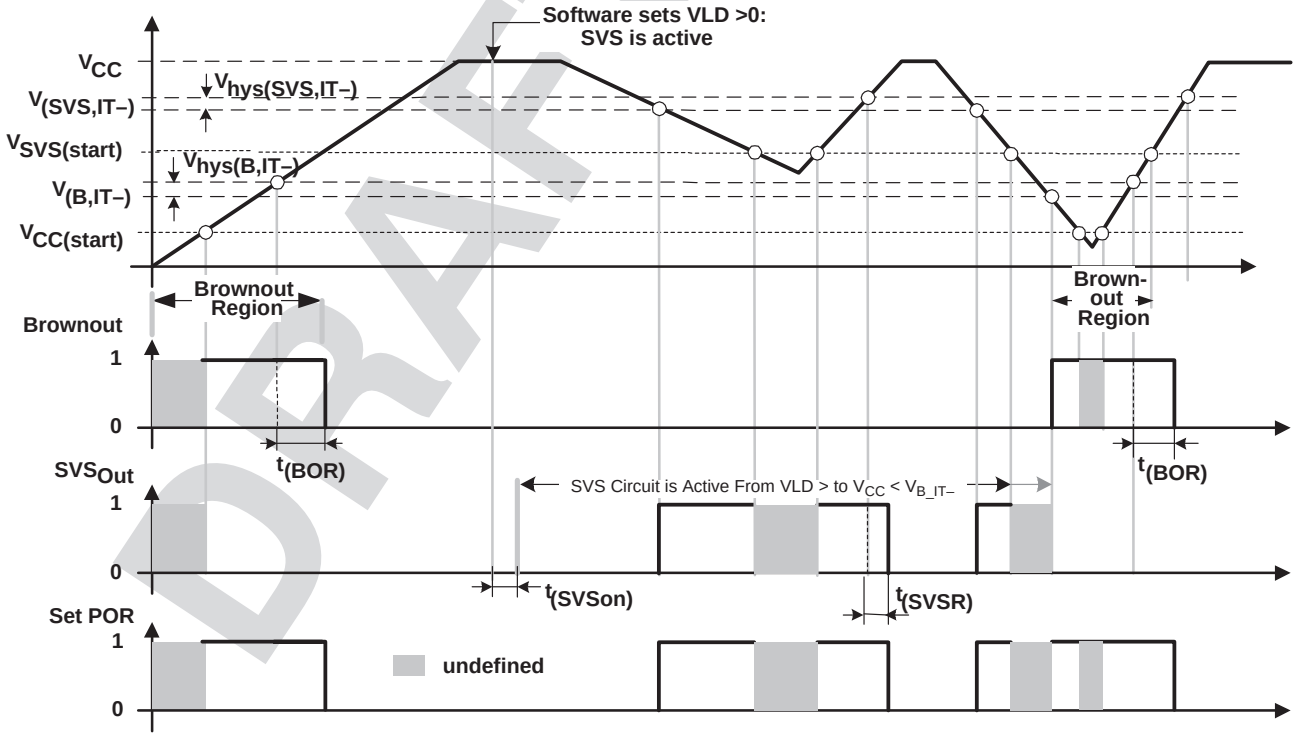


Figure 15. SVS Reset (SVSR) vs Supply Voltage

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

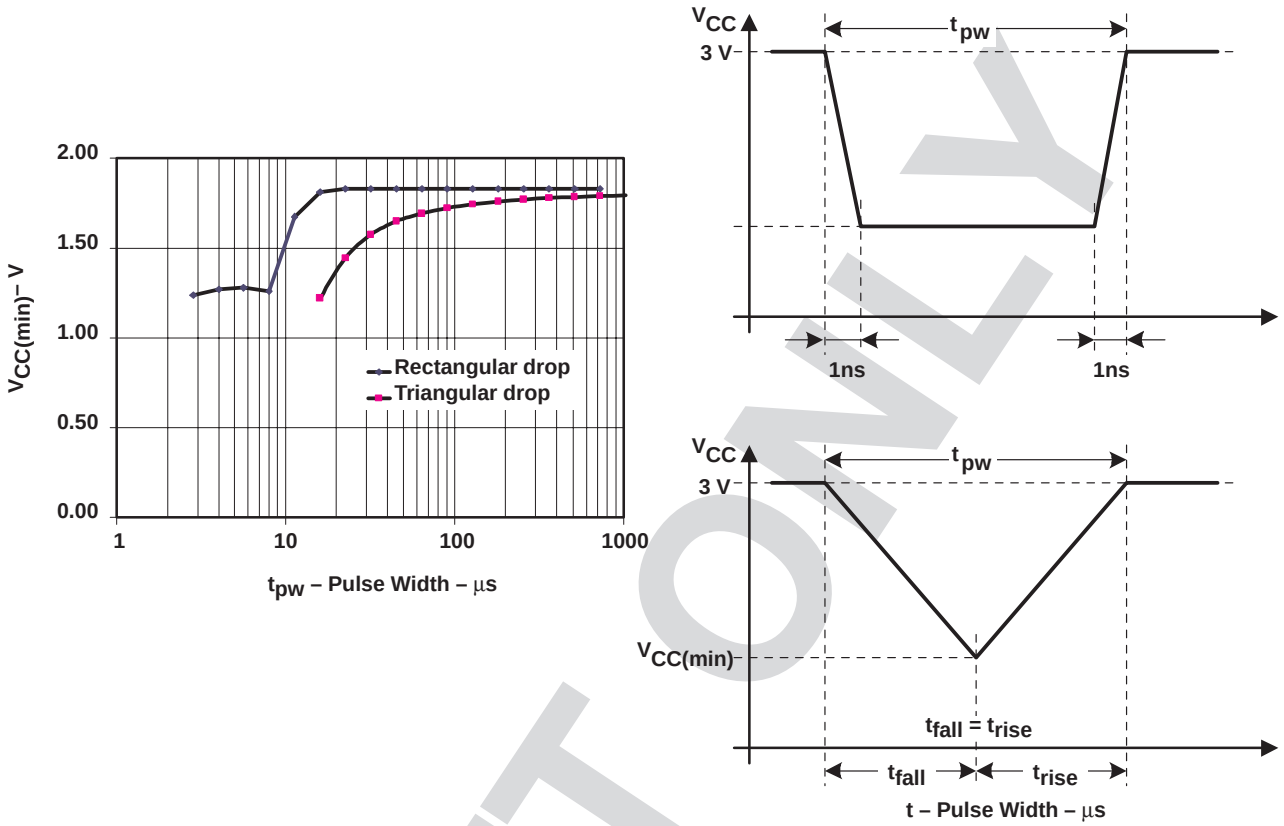


Figure 16. $V_{CC(min)}$ With a Square Voltage Drop and a Triangle Voltage Drop to Generate a SVS Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(DCOCLK)}$	$N_{(DCO)}$=01E0h, FN_8=FN_4=FN_3=FN_2=0, D = 2, DCO+= 0	V_{CC} = 2.2 V/3 V		1		MHz
$f_{(DCO2)}$	FN_8=FN_4=FN_3=FN_2=0 , DCO+ = 1	V_{CC} = 2.2 V	0.23	0.41	0.82	MHz
		V_{CC}= 3 V	0.30	0.57	1.20	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=FN_2=0, DCO+ = 1	V_{CC} = 2.2 V	2.25	4.0	8.0	MHz
		V_{CC} = 3 V	3.0	5.6	11.2	
$f_{(DCO2)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCO+ = 1	V_{CC} = 2.2 V	0.45	0.85	1.75	MHz
		V_{CC} = 3 V	0.60	1.2	2.4	
$f_{(DCO27)}$	FN_8=FN_4=FN_3=0, FN_2=1; DCO+ = 1	V_{CC} = 2.2 V	4.4	8.0	16.5	MHz
		V_{CC} = 3 V	6.0	11.0	22.5	
$f_{(DCO2)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x; DCO+ = 1	V_{CC} = 2.2 V	0.73	1.3	2.7	MHz
		V_{CC} = 3 V	1.0	1.85	3.9	
$f_{(DCO27)}$	FN_8=FN_4=0, FN_3= 1, FN_2=x;, DCO+ = 1	V_{CC} = 2.2 V	6.5	12.0	24.0	MHz
		V_{CC} = 3 V	9.0	16.5	34.0	
$f_{(DCO2)}$	FN_8=0, FN_4= 1, FN_3= FN_2=x; DCO+ = 1	V_{CC} = 2.2 V	1.1	2.1	4.3	MHz
		V_{CC} = 3 V	1.6	2.9	6.0	
$f_{(DCO27)}$	FN_8=0, FN_4=1, FN_3= FN_2=x; DCO+ = 1	V_{CC} = 2.2 V	9.5	18.0	38.0	MHz
		V_{CC} = 3 V	13.0	25.0	52.0	
$f_{(DCO2)}$	FN_8=1, FN_4=FN_3=FN_2=x; DCO+ = 1	V_{CC} = 2.2 V	2.2	4.0	8.2	MHz
		V_{CC} = 3 V	3.0	5.6	12.0	
$f_{(DCO27)}$	FN_8=1,FN_4=FN_3=FN_2=x,DCO+ = 1	V_{CC} = 2.2 V	17.5	32.0	65.0	MHz
		V_{CC} = 3 V	24.0	45.0	94.0	
S	$f_{(NDCO)+1} = f_{(NDCO)}$		1.07		1.13	
D_t	Temperature drift, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2, DCO+ = 0, (see Note 24)	V_{CC} = 2.2 V	–0.31	–0.36	–0.40	%/°C
		V_{CC} = 3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, $N_{(DCO)}$ = 01E0h, FN_8=FN_4=FN_3=FN_2=0 D = 2, DCO+ = 0 (see Note 24)		0	5	10	%/V

NOTE 24: This parameter not production tested.

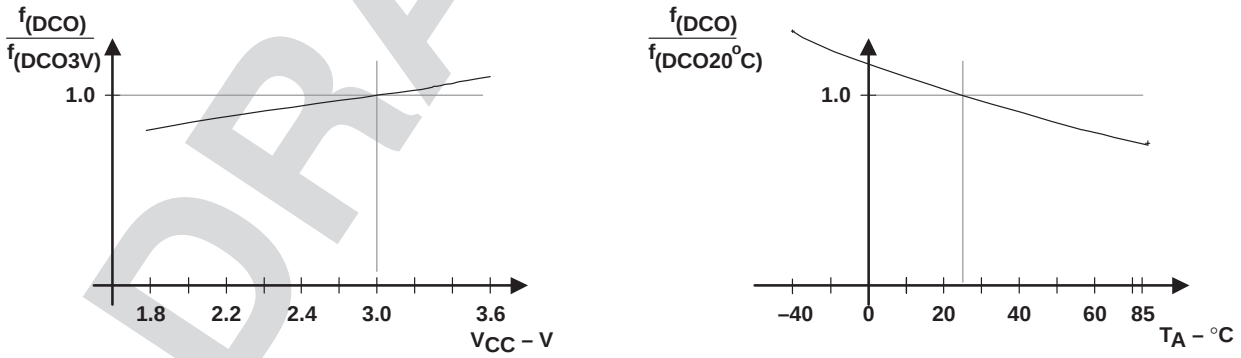


Figure 17. DCO Frequency vs Supply Voltage V_{CC} and vs Ambient Temperature

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

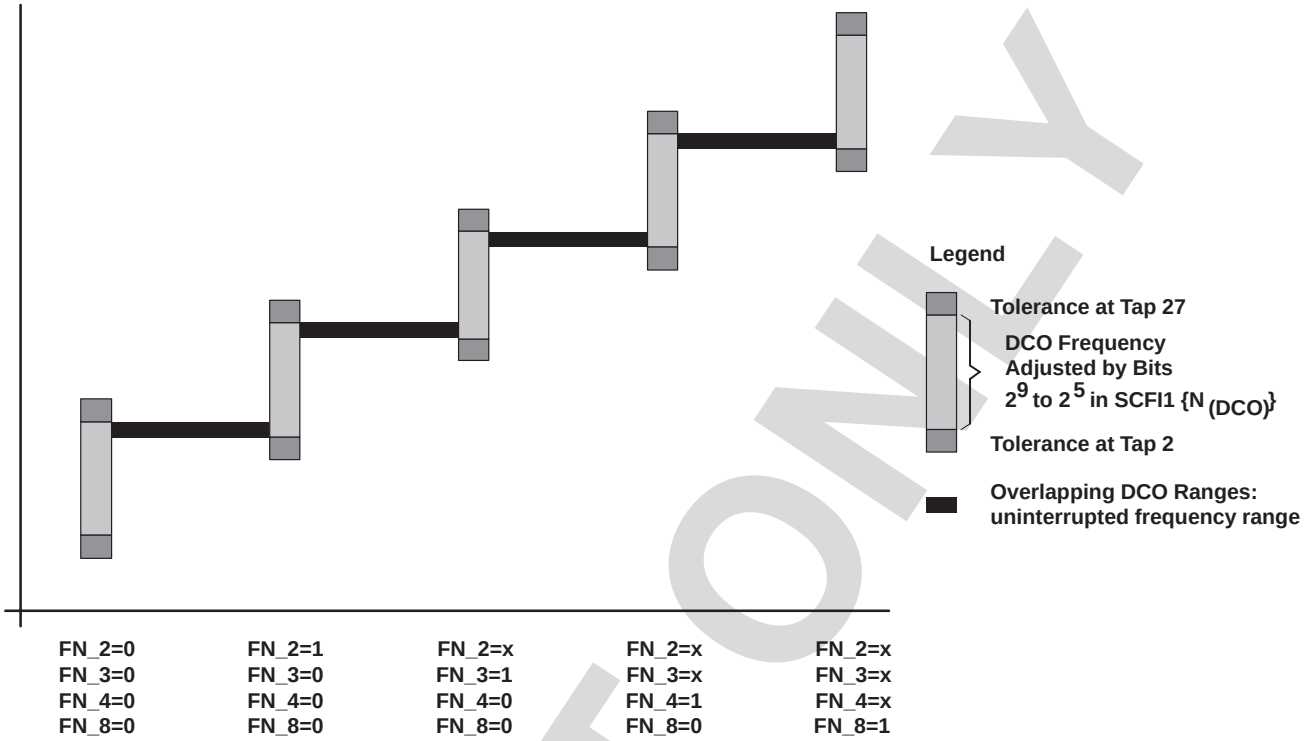


Figure 18. Five Overlapping DCO Ranges Controlled by FN_x Bits

crystal oscillator, LFXT1 oscillator (see Note 25)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{(XIN)}$	Integrated input capacitance	OscCap = 0, V_{CC} = 2.2 V / 3.0		0		pF
		OscCap = 1, V_{CC} = 2.2 V / 3.0		10		
		OscCap = 2, V_{CC} = 2.2 V / 3.0		14		
		OscCap = 3, V_{CC} = 2.2 V / 3.0		18		
$C_{(XOUT)}$	Integrated output capacitance	OscCap = 0, V_{CC} = 2.2 V / 3.0		0		pF
		OscCap = 1, V_{CC} = 2.2 V / 3.0		10		
		OscCap = 2, V_{CC} = 2.2 V / 3.0		14		
		OscCap = 3, V_{CC} = 2.2 V / 3.0		18		

NOTE 25: The parasitic capacitance from the package and board may be estimated to be 2pF. The effective load capacitor for the crystal is (X_{CIN} x X_{COUT}) / (X_{CIN} + X_{COUT}). It is independent of XST_FLL .

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

JTAG, program memory and fuse

PARAMETER		CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{(TCK)}$	JTAG/Test	TCK frequency	2.2V	DC		5	MHz
			3.0V	DC		10	
		Pull-up resistors on TMS, TCK, TDI (see Note 26)	2.2V/ 3.0V	25	60	90	kΩ
V_{FB}	JTAG/Fuse See Note 27	Fuse blow voltage, C versions (see Note 27)	2.2 V/3.0 V	3.5		3.9	V
		Fuse blow voltage, F versions (see Note 28)	2.2 V/3.0 V	6.0		7.0	V
I_{FB}		Supply current on TDI during fuse is blown				100	mA
t_{FB}		Time to blow the fuse				1	ms
$I_{(DD–PGM)}$	F-versions only	Current from programming voltage source (see Note 29)	2.7V/3.6V		3	5	mA
$I_{(DD–Erase)}$	F-versions only	Programming time, single pulse (see Note 298)	2.7V/3.6V		3	5	mA
$t_{(retention)}$	F-versions only	Write/Erase cycles		10^4	10^5		cycles
		Data retention Tj = 25°C		100			years

NOTES: 26. TMS, TDI, and TCK pull-up resistors are implemented in all C- and F-versions.

27. Once the fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block is switched to bypass mode.

28. The supply voltage to blow the fuse is applied to TDI pin.

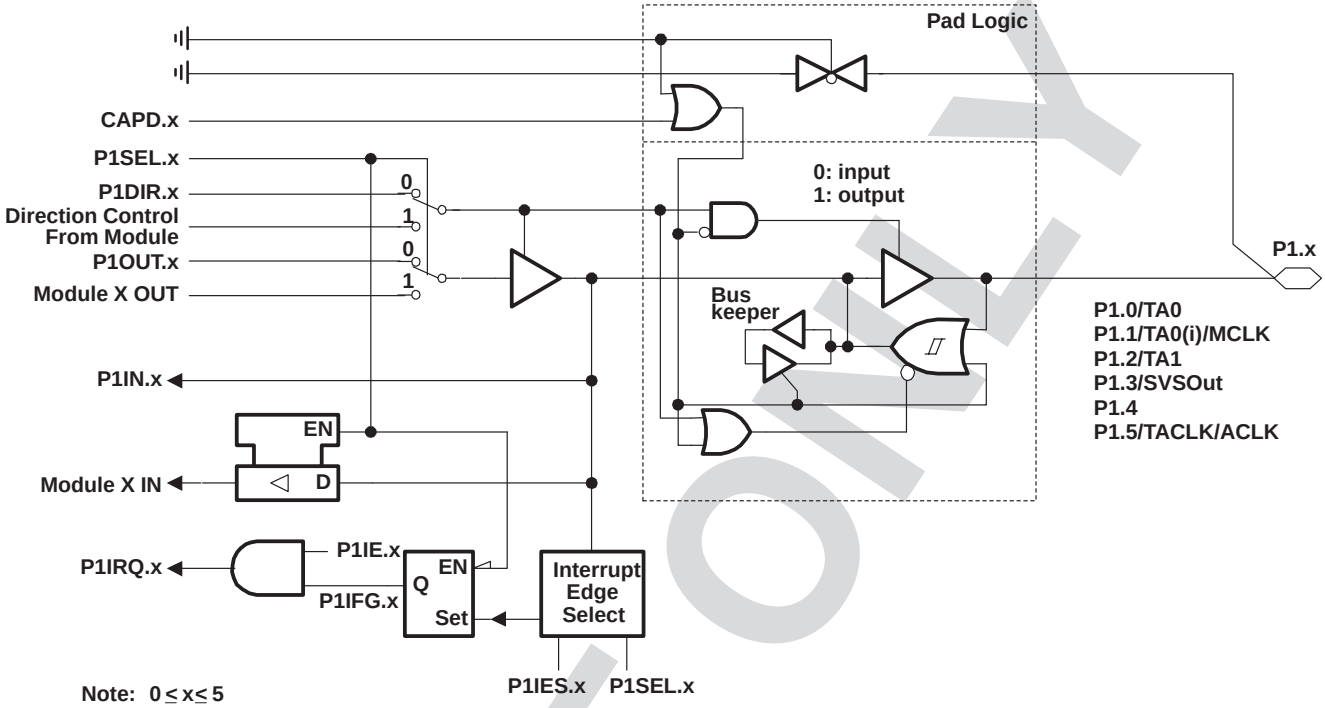
29. $f_{(TCK)}$ may be restricted to meet the timing requirements of the module selected. Duration of the program/erase cycle is determined by $f_{(FTG)}$ applied to the flash timing controller. It can be calculated as follows:

$t_{(word\ write)} = 33 \times 1/f_{(FTG)}$
$t_{(segment\ write,\ byte\ 0)} = 29 \times 1/f_{(FTG)}$
$t_{(segment\ write,\ byte\ 1-63)} = 21 \times 1/f_{(FTG)}$
$t_{(mass\ erase)} = 5296 \times 1/f_{(FTG)}$
$t(page\ erase) = 4817 \times 1/f_{(FTG)}$

The mass-erase cycle needs to be repeated n-times by software to ensure minimum 200 ms mass-erase time.

input/output schematic

Port P1, P1.0 to P1.5, input/output with Schmitt-trigger



Note: $0 \le x \le 5$

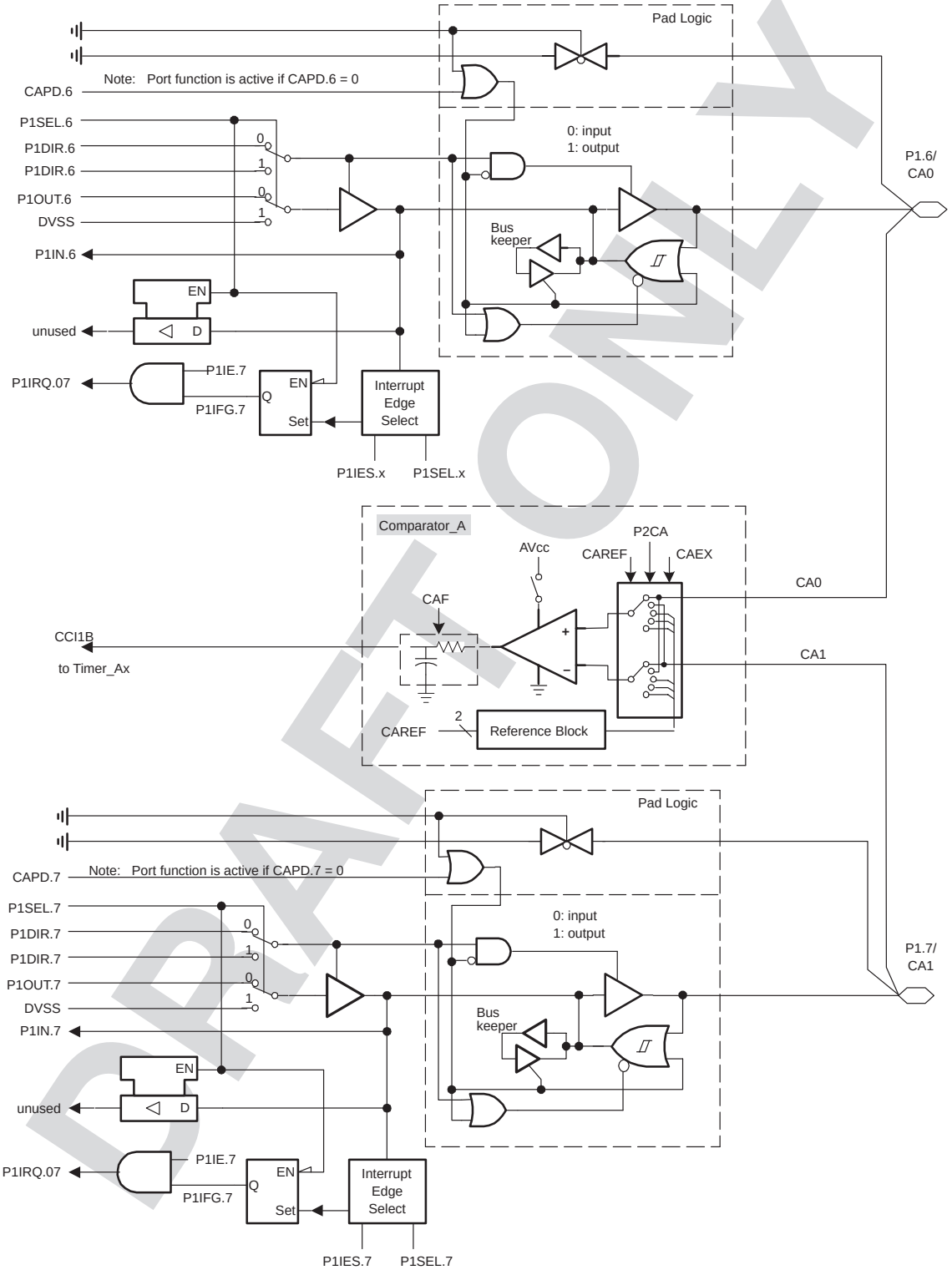
Note: Port function is active if CAPD.x = 0

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	Out0 sig.†	P1IN.0	CCI0A†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	MCLK	P1IN.1	CCI0B†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 sig.†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	SVSOut	P1IN.3	unused	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	DVSS	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	ACLK	P1IN.5	TACLK†	P1IE.5	P1IFG.5	P1IES.5

† Timer_A

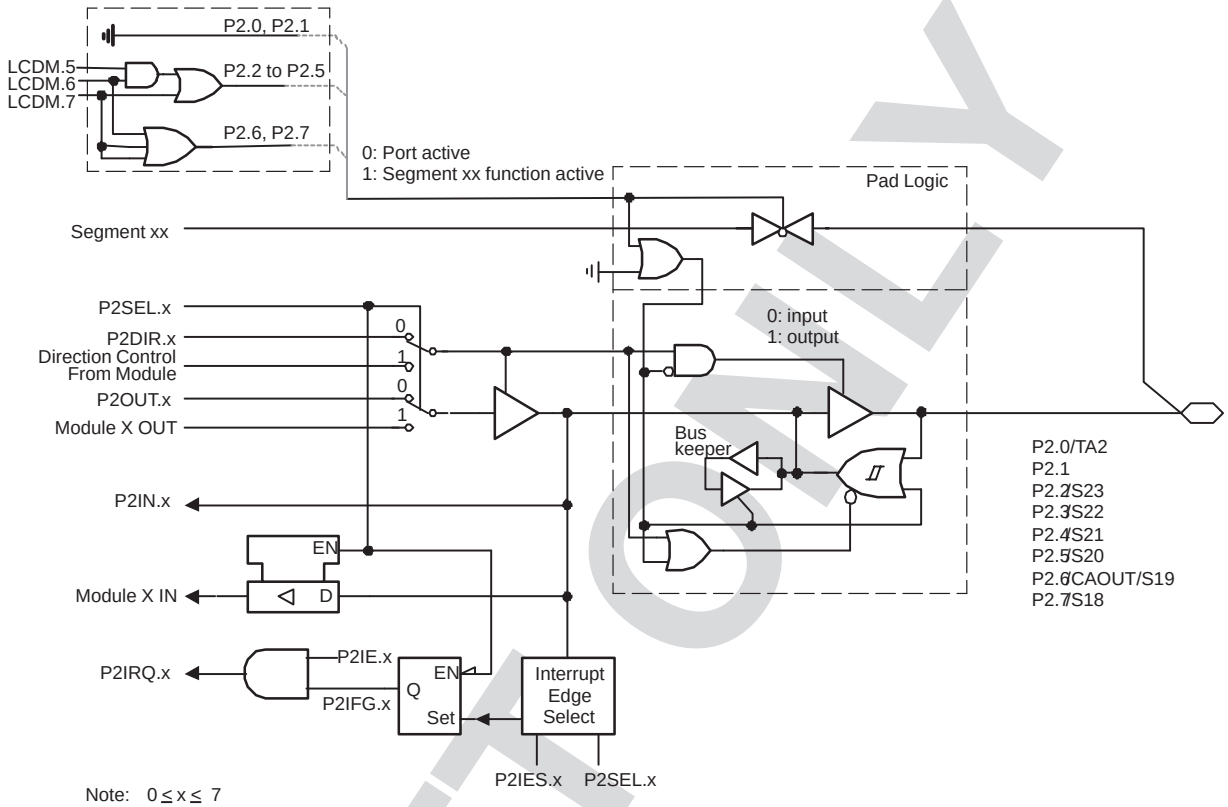
input/output schematic (continued)

Port P1, P1.6, P1.7, input/output with Schmitt-trigger



input/output schematic (continued)

port P2, P2.0 to P2.7, input/output with Schmitt-trigger



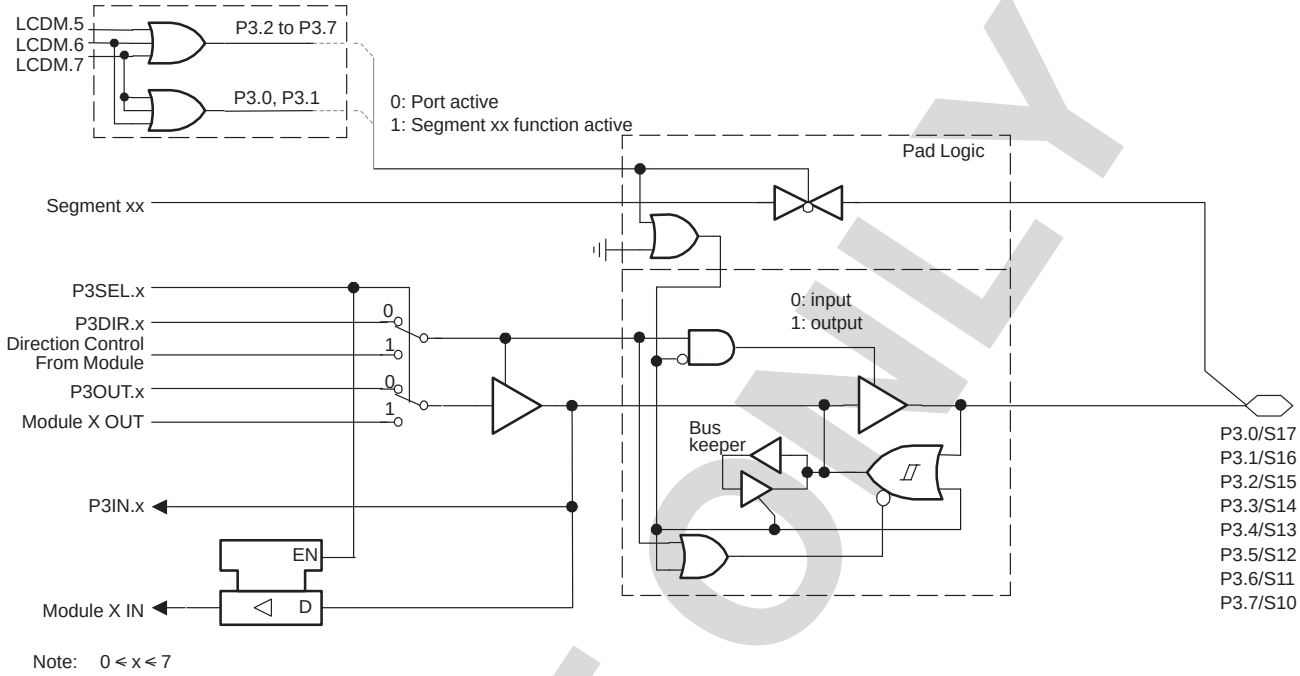
Note: $0 \le x \le 7$

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	Out2 sig.†	P2IN.0	CCI2A†	P2IE.0	P2IFG.0	P2IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	DVSS	P2IN.1	unused	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	DVSS	P2IN.2	unused	P2IE.2	P2IFG.2	P2IES.2
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	DVSS	P2IN.3	unused	P2IE.3	P2IFG.3	P2IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	DVSS	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	DVSS	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5
P2Sel.6	P2DIR.4	P2DIR.6	P2OUT.6	CAOUT	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.5	P2DIR.7	P2OUT.7	DVSS	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

† Timer_A

input/output schematic (continued)

port P3, P3.0, P3.7, input/output with Schmitt-trigger

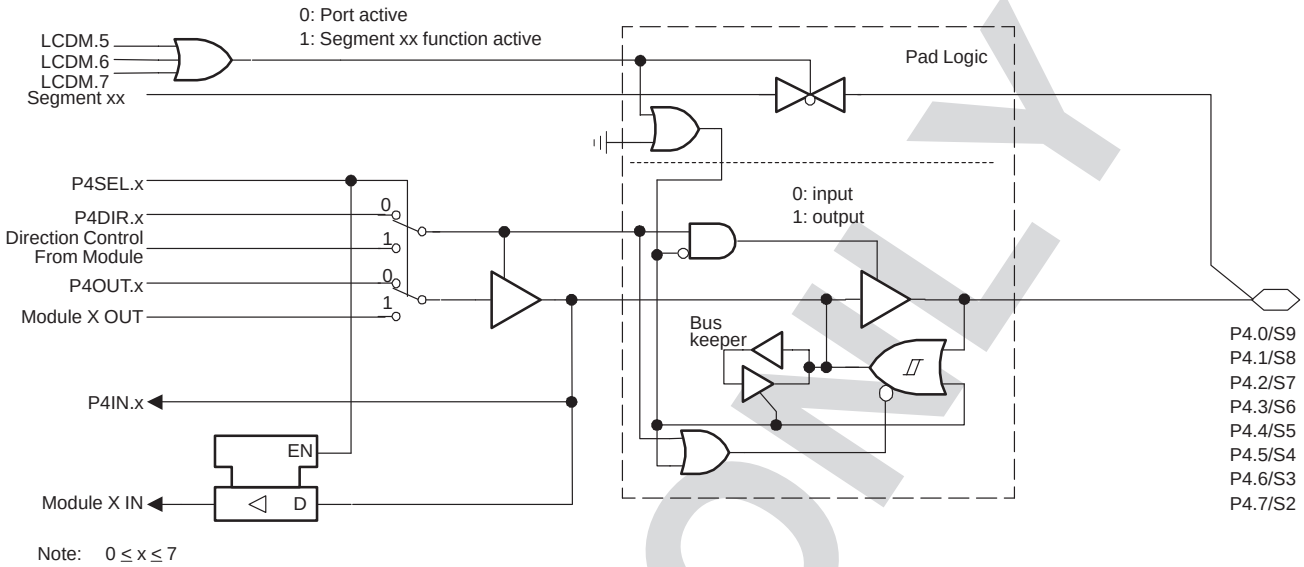


Note: $0 \leq x \leq 7$

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P3Sel.0	P3DIR.0	P3DIR.0	P3OUT.0	DVSS	P3IN.0	unused
P3Sel.1	P3DIR.1	P3DIR.1	P3OUT.1	DVSS	P3IN.1	unused
P3Sel.2	P3DIR.2	P3DIR.2	P3OUT.2	DVSS	P3IN.2	unused
P3Sel.3	P3DIR.3	P3DIR.3	P3OUT.3	DVSS	P3IN.3	unused
P3Sel.4	P3DIR.4	P3DIR.4	P3OUT.4	DVSS	P3IN.4	unused
P3Sel.5	P3DIR.5	P3DIR.5	P3OUT.5	DVSS	P3IN.5	unused
P3Sel.6	P3DIR.4	P3DIR.6	P3OUT.6	DVSS	P3IN.6	unused
P3Sel.7	P3DIR.5	P3DIR.7	P3OUT.7	DVSS	P3IN.7	unused

input/output schematic (continued)

port P4, P4.0 to P4.7, input/output with Schmitt-trigger

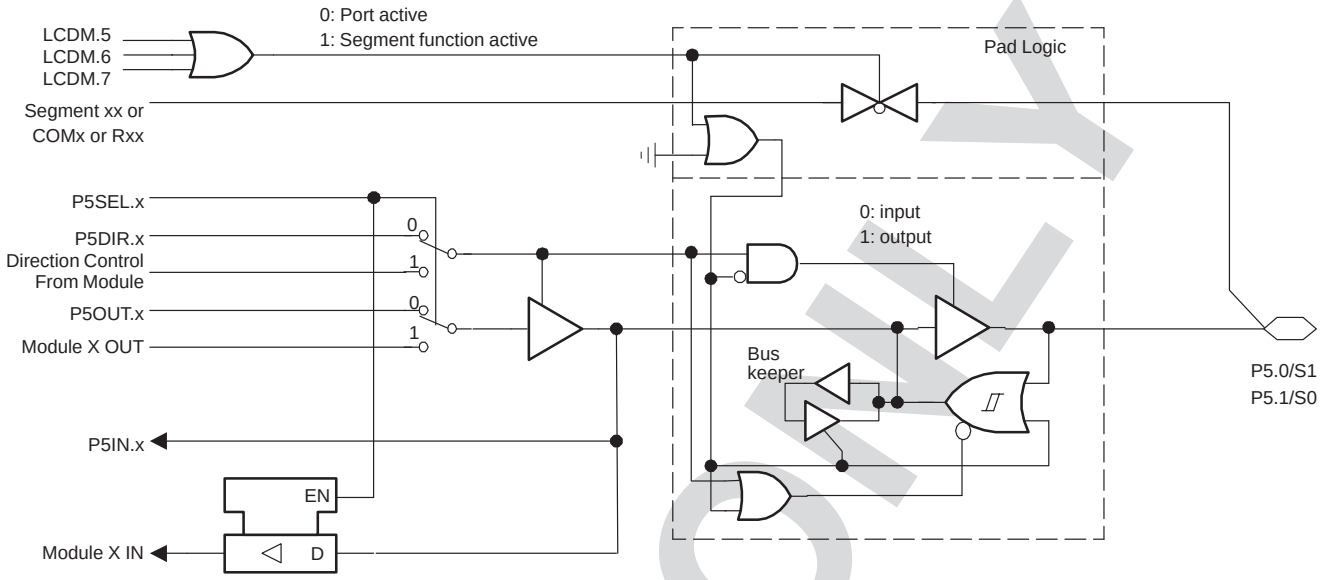


Note: $0 \le x \le 7$

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P4Sel.0	P4DIR.0	P4DIR.0	P4OUT.0	DVSS	P4IN.0	unused
P4Sel.1	P4DIR.1	P4DIR.1	P4OUT.1	DVSS	P4IN.1	unused
P4Sel.2	P4DIR.2	P4DIR.2	P4OUT.2	DVSS	P4IN.2	unused
P4Sel.3	P4DIR.3	P4DIR.3	P4OUT.3	DVSS	P4IN.3	unused
P4Sel.4	P4DIR.4	P4DIR.4	P4OUT.4	DVSS	P4IN.4	unused
P4Sel.5	P4DIR.5	P4DIR.5	P4OUT.5	DVSS	P4IN.5	unused
P4Sel.6	P4DIR.4	P4DIR.6	P4OUT.6	DVSS	P4IN.6	unused
P4Sel.7	P4DIR.5	P4DIR.7	P4OUT.7	DVSS	P4IN.7	unused

input/output schematic (continued)

port P5, P5.0, P5.1, input/output with Schmitt-trigger

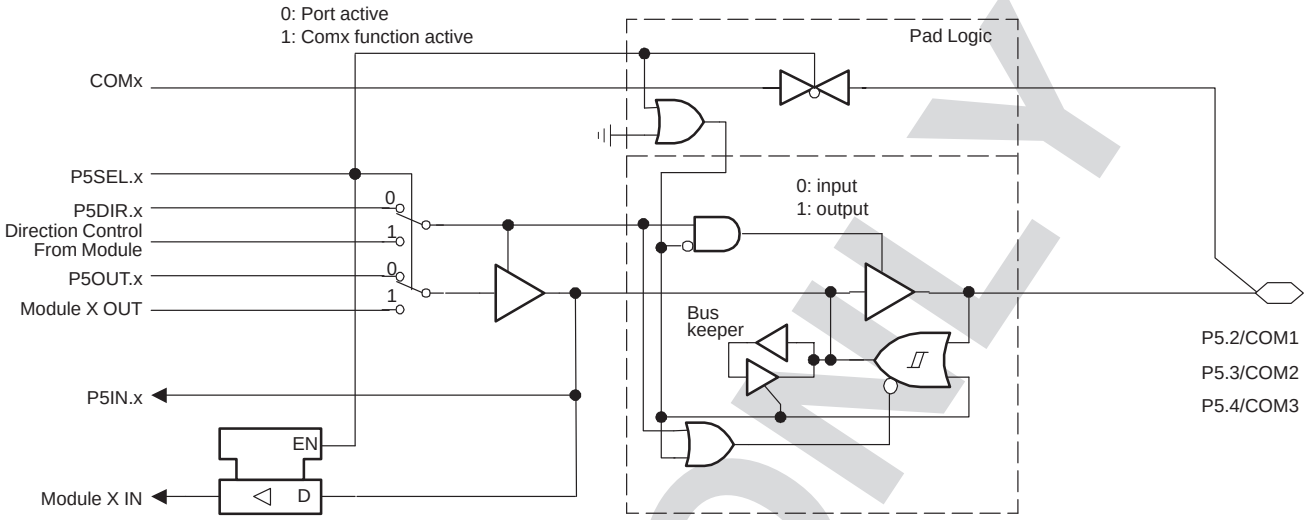


Note: $0 \le x \le 1$

PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Segment
P5Sel.0	P5DIR.0	P5DIR.0	P5OUT.0	DVSS	P5IN.0	unused	S1
P5Sel.1	P5DIR.1	P5DIR.1	P5OUT.1	DVSS	P5IN.1	unused	S0

input/output schematic (continued)

port P5, P5.2, P5.4, input/output with Schmitt-trigger



Note: $2 \leq x \leq 4$

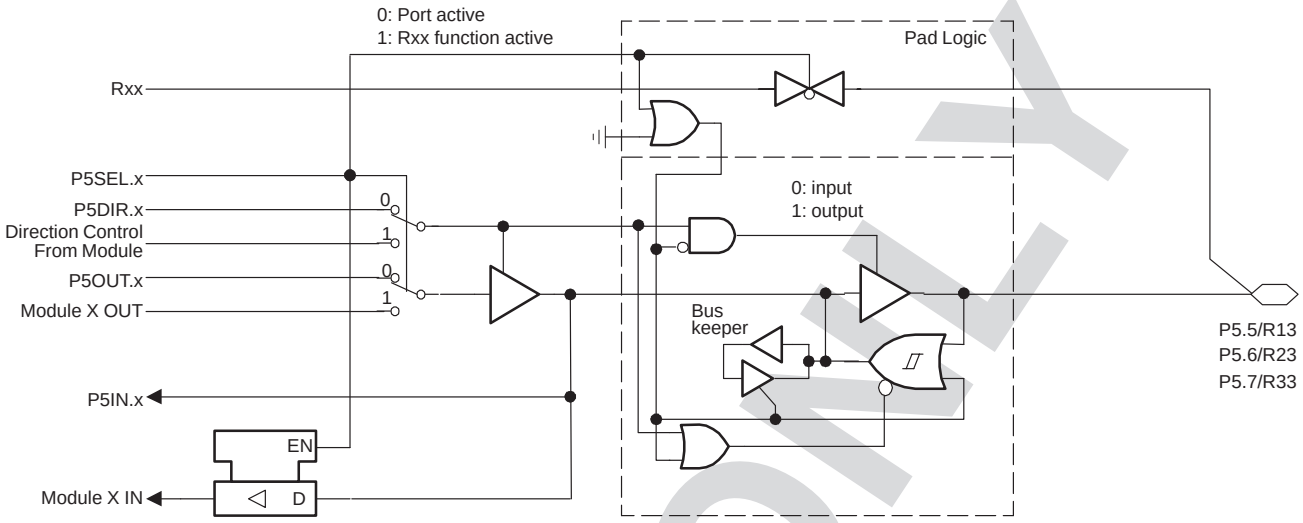
PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	COMx
P5Sel.2	P5DIR.2	P5DIR.2	P5OUT.2	DVSS	P5IN.2	unused	COM1
P5Sel.3	P5DIR.3	P5DIR.3	P5OUT.3	DVSS	P5IN.3	unused	COM2
P5Sel.4	P5DIR.4	P5DIR.4	P5OUT.4	DVSS	P5IN.4	unused	COM3

NOTE:

The direction control bits P5SEL.2, P5SEL.3, and P5SEL.4 are used to distinguish between port and common functions. Note that a 4MUX LCD requires all common signals COM3 to COM0, a 3MUX LCD requires COM2 to COM0, 2MUX LCD requires COM1 to COM0, and a static LCD requires only COM0.

input/output schematic (continued)

port P5, P5.5 to P5.7, input/output with Schmitt-trigger



Note: $5 \le x \le 7$

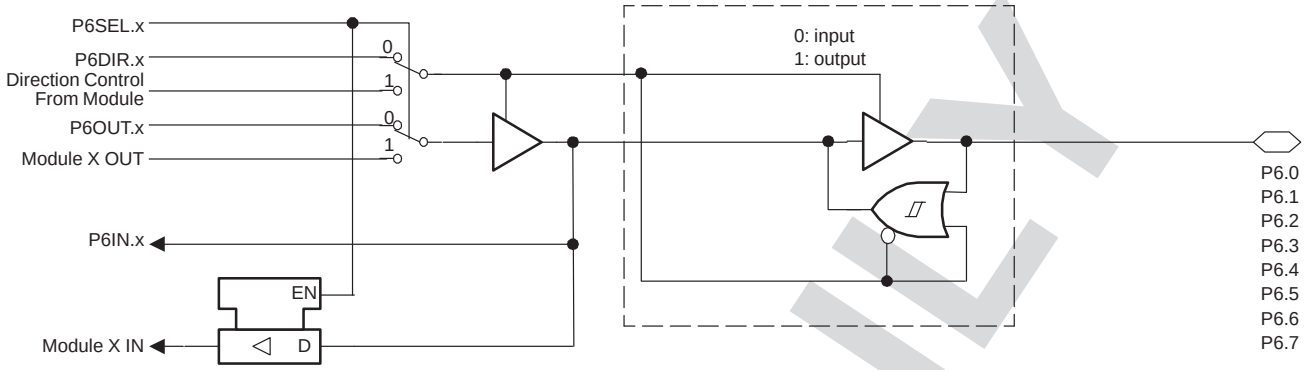
PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	Rxx
P5Sel.5	P5DIR.5	P5DIR.5	P5OUT.5	DVSS	P5IN.5	unused	R13
P5Sel.6	P5DIR.4	P5DIR.6	P5OUT.6	DVSS	P5IN.6	unused	R23
P5Sel.7	P5DIR.5	P5DIR.7	P5OUT.7	DVSS	P5IN.7	unused	R33

NOTE:

The direction control bits P5SEL.5, P5SEL.6, and P5SEL.7 are used to distinguish between port and LCD analog level functions. Note that a 4MUX and 3MUX LCD requires all Rxx signals R33 to R03, 2MUX LCD requires R33, R13, and R03, and a static LCD requires only R33 and R03.

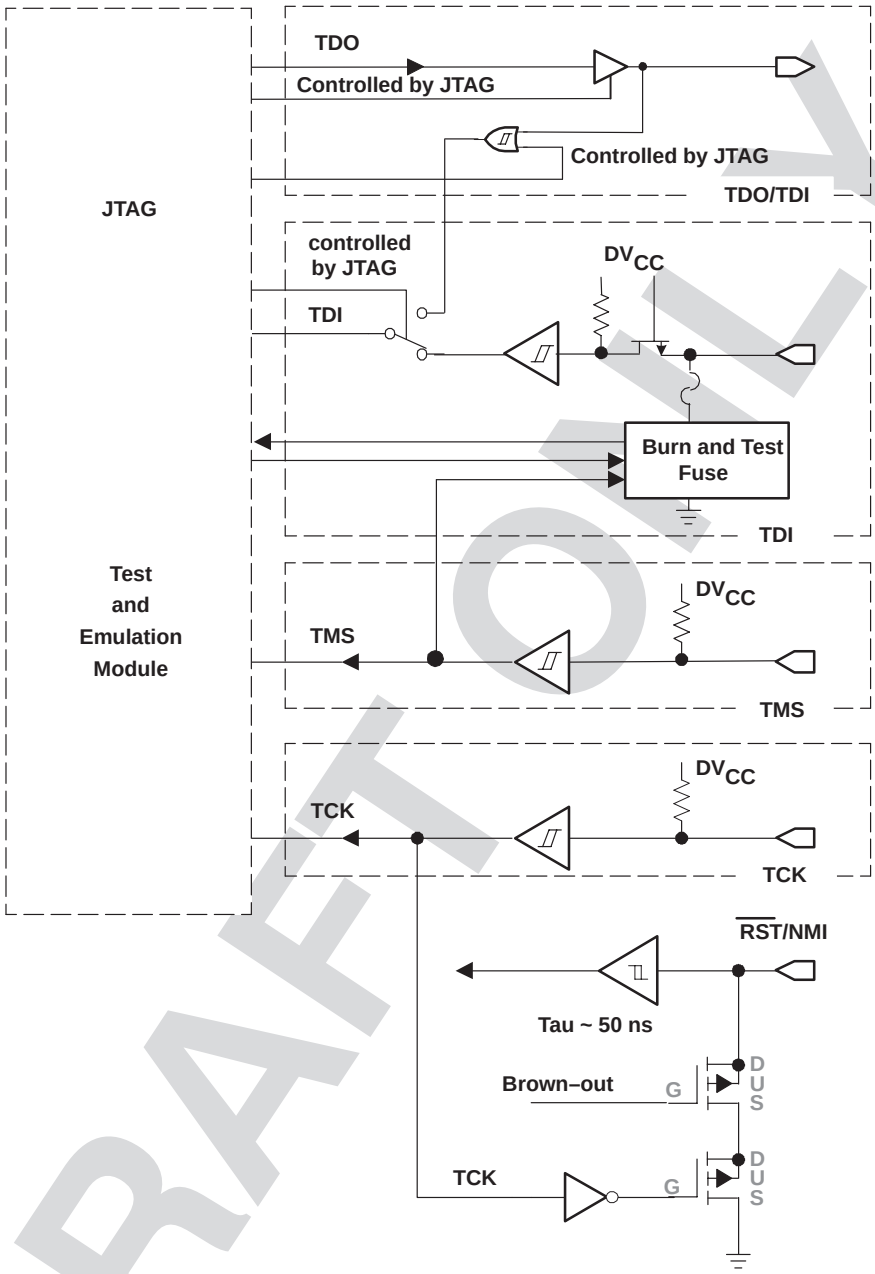
input/output schematic (continued)

port P6, P6.0 to P6.7, input/output with Schmitt-trigger



PnSel.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DVSS	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DVSS	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DVSS	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DVSS	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DVSS	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DVSS	P6IN.5	unused
P6Sel.6	P6DIR.4	P6DIR.6	P6OUT.6	DVSS	P6IN.6	unused
P6Sel.7	P6DIR.5	P6DIR.7	P6OUT.7	DVSS	P6IN.7	unused

JTAG pins TMS, TCK, TDI, TDO/TDI, input/output with Schmitt-trigger or output



JTAG fuse check mode

MSP430 devices that have the fuse on the TDI terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V can flow from the TDI pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current only flows when the fuse check mode is active and the TMS pin is in a low state (see Figure 19). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

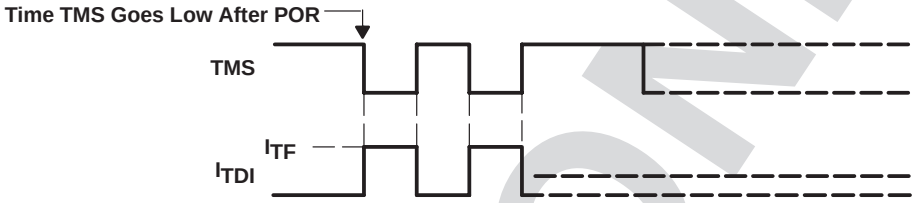
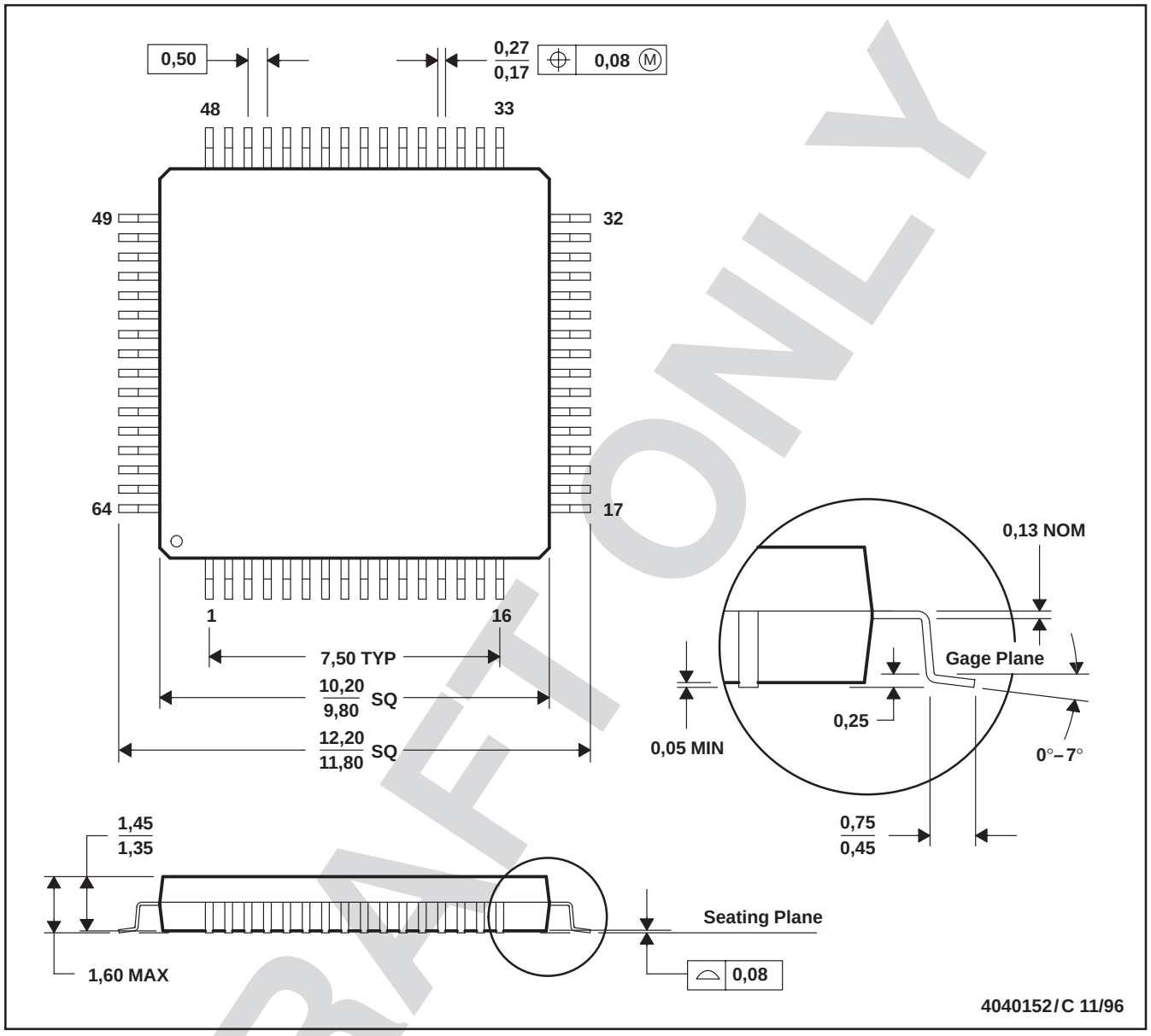


Figure 19. Fuse Check Mode Current, MSP430C41x, MSP430F41x

MECHANICAL DATA

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.