STEREO AUDIO CODEC WITH USB INTERFACE, SINGLE-ENDED ANALOG INPUT/OUTPUT AND S/PDIF

FEATURES

- **PCM2900: Without S/PDIF**
- **PCM2902: With S/PDIF**
- **On-Chip USB Interface:**
  - **With Full-Speed Transceivers**
  - **Fully Compliant With USB 1.1 Specification**
  - **Certified by USB-IF**
  - **Partially Programmable Descriptors(1)**
  - **USB Adaptive Mode for Playback**
  - **USB Asynchronous Mode for Record**
  - **Bus Powered**
- **16-Bit Delta Sigma ADC and DAC**
- **Sampling Rate:**
  - **DAC: 32, 44.1, 48 kHz**
  - **ADC: 8, 11.025, 16, 22.05, 32, 44.1, 48 kHz**
- **On-Chip Clock Generator:**
  - **With Single 12-MHz Clock Source**
- **Single Power Supply: 5 V TYP (V_{BUS})**
- **Stereo ADC Analog Performance at V_{BUS} = 5 V:**
  - **THD+N = 0.01%**
  - **SNR = 89 dB**
  - **Dynamic Range = 89 dB**
  - **Decimation Digital Filter**
  - **Passband Ripple = ±0.05 dB**
  - **Stopband Attenuation = –65 dB**
  - **Single-Ended Voltage Input**
  - **Antialiasing Filter Included**
  - **Digital LCF Included**
- **Stereo DAC Analog Performance at V_{BUS} = 5 V:**
  - **THD+N = 0.005%**
  - **SNR = 96 dB**
  - **Dynamic Range = 93 dB**
  - **Oversampling Digital Filter**
  - **Passband Ripple = ±0.1 dB**
  - **Stopband Attenuation = –43 dB**
  - **Single-Ended Voltage Output**
  - **Analog LPF Included**
- **Multifunctions:**
  - **HID Volume ± Control and Mute Control**
  - **Suspend Flag**
- **Package: 28-Pin SSOP, Lead-Free Product**

APPLICATIONS

- **USB Audio Speaker**
- **USB Headset**
- **USB Monitor**
- **USB Audio Interface Box**

DESCRIPTION

The PCM2900/2902 is Texas Instruments single-chip USB stereo audio codec with USB 1.1 compliant full-speed protocol controller and S/PDIF (only PCM2902). The USB protocol controller works with no software code, but the USB descriptors can be modified in some areas (ex. vendor ID/product ID). The PCM2900/2902 employs a USB data tracking system named sampling period adaptive controlled tracking (SpAct™), which is TI's audio clock recovery architecture. The on-chip analog PLLs with the SpAct enables independent playback and record sampling rates with low clock jitters.

Clocked by SpAct

Input signal is reclocked with the patented sampling period adaptive controlled tracking system for maximum quality.

(1)The descriptor can be modified by changing a mask.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING ORDERING INFORMATION

PCM2900						
PRODUCT	**PACKAGE–LEAD**	**PACKAGE DESIGNATOR**	**SPECIFIED TEMPERATURE RANGE**	**PACKAGE MARKING**	**ORDERING NUMBER(1)**	**TRANSPORT MEDIA**
PCM2900E	SSOP-28	28DB	–25°C to 85°C	PCM2900E	PCM2900E	Rails
					PCM2900E/2K	Tape and reel

(1) Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of PCM2900E/2K gets a single 2000 piece tape and reel.

PCM2902						
PRODUCT	**PACKAGE–LEAD**	**PACKAGE DESIGNATOR**	**SPECIFIED TEMPERATURE RANGE**	**PACKAGE MARKING**	**ORDERING NUMBER(1)**	**TRANSPORT MEDIA**
PCM2902E	SSOP-28	28DB	–25°C to 85°C	PCM2902E	PCM2902E	Rails
					PCM2902E/2K	Tape and reel

(1) Models with a slash (/) are available only in tape and reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of PCM2902E/2K gets a single 2000 piece tape and reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		PCM2900/PCM2902	UNIT
Supply voltage, V_{BUS}		6.5	V
Ground voltage differences, AGNDC, AGNDP, AGNDX, DGND, DGNDU		±0.1	V
Digital input voltage	SEL0, SEL1, DIN	–0.3 to 6.5	V
	D+, D–, HID0, HID1, HID2, XTI, XTO, DOUT, $\overline{SSPND}$	–0.3 to (V_{DDI} + 0.3)	V
Analog input voltage	$V_{IN}L$, $V_{IN}R$, V_{COM}, $V_{OUT}R$, $V_{OUT}L$	–0.3 to (V_{CCCI} + 0.3)	V
	V_{CCCI}, V_{CCP1I}, V_{CCP2I}, V_{CCXI}, V_{DDI}	–0.3 to 4	V
Input current (any pins except supplies)		±10	mA
Ambient temperature under bias		–40 to 125	°C
Storage temperature, T_{stg}		–55 to 150	°C
Junction temperature T_J		150	°C
Lead temperature (soldering)		260	°C, 5 s
Package temperature (IR reflow, peak)		260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input/Output							
	Host interface		Apply USB Revision 1.1, full speed				
	Audio data format		USB isochronous data format				
Input Logic							
V_{IH}	High-level input voltage	D+, D–		2		3.3	VDC
		XTI, HID0, HID1, and HID2		2.52		3.3	
		SEL0, SEL1		2		5.25	
		DIN, PCM2902		2.52		5.25	
V_{IL}	Low-level input voltage	D+, D–				0.8	VDC
		XTI, HID0, HID1, and HID2				0.9	
		SEL0, SEL1				0.8	
		DIN, PCM2902				0.9	
I_{IH}	High-level input current	D+, D–, XTI, SEL0, SEL1	V_{IN} = 3.3 V			±10	µA
		HID0, HID1, and HID2	V_{IN} = 3.3 V		50	80	
		DIN, PCM2902	V_{IN} = 3.3 V		65	100	
I_{IL}	Low-level input current	D+, D–, XTI, SEL0, SEL1	V_{IN} = 0 V			±10	µA
		HID0, HID1, and HID2	V_{IN} = 0 V			±10	
		DIN, PCM2902	V_{IN} = 0 V			±10	
Output Logic							
V_{OH}	High-level output voltage	D+, D–		2.8			VDC
		DOUT, PCM2902	I_{OH} = –4 mA	2.8			
		$\overline{SSPND}$	I_{OH} = –2 mA	2.8			
V_{OL}	Low-level output voltage	D+, D–				0.3	VDC
		DOUT, PCM2902	I_{OL} = 4 mA			0.5	
		$\overline{SSPND}$	I_{OL} = 2 mA			0.5	
Clock Frequency							
	Input clock frequency, XTI			11.994	12	12.006	MHz
ADC Characteristics							
	Resolution				8, 16		bits
	Audio data channel				1, 2		channel

(1) f_{IN} = 1 kHz, using Audio Precision System II, RMS mode with 20-kHz LPF, 400-Hz HPF in calculation.

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency						
f_S	Sampling frequency		8, 11.025, 16, 22.05, 32, 44.1, 48			kHz
DC Accuracy						
	Gain mismatch channel-to-channel			±1	±5	%FSR
	Gain error			±2	±10	%FSR
	Bipolar zero error			±0		%FSR
Dynamic Performance(1)						
THD+N	Total harmonic distortion plus noise	V_{CCCI} = 3.67 V, V_{IN} = –0.5 dB(2)		0.01%	0.02%	
		V_{IN} = –0.5 dB(3)		0.1%		
		V_{IN} = –60 dB		5%		
	Dynamic range	A-weighted	81	89		dB
SNR	Signal-to-noise ratio	A-weighted	81	89		dB
	Channel separation		80	85		dB
Analog Input						
	Input voltage			0.6 V_{CCCI}		$V_{p–p}$
	Center voltage			0.5 V_{CCCI}		V
	Input impedance			30		kΩ
	Antialiasing filter frequency response	–3 dB		150		kHz
		f_{IN} = 20 kHz		–0.08		dB
Digital Filter Performance						
	Passband				0.454 f_S	Hz
	Stopband		0.583 f_S			Hz
	Passband ripple				±0.05	dB
	Stopband attenuation		–65			dB
t_d	Delay time			17.4/f_S		s
	LCF frequency response	–3 dB		0.078f_S		MHz
DAC Characteristics						
	Resolution			8, 16		bits
	Audio data channel			1, 2		channel
Clock Frequency						
f_S	Sampling frequency			32, 44.1, 48		kHz

(1) f_{IN} = 1 kHz, using Audio Precision System II, RMS mode with 20-kHz LPF, 400-Hz HPF in calculation.
(2) Using external voltage regulator for V_{CCCI} (as shown in Figure 7, using with REG103xA-A
(3) Using internal voltage regulator for V_{CCCI} (as shown in Figure 9)

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted(1)

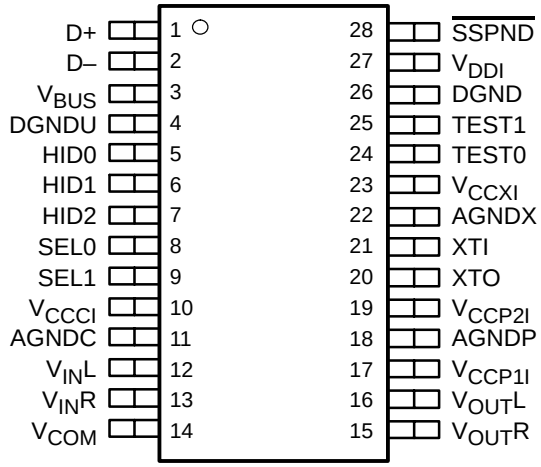
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC Accuracy						
	Gain mismatch channel-to-channel			±1	±5	%FSR
	Gain error			±2	±10	%FSR
	Bipolar zero error			±2		%FSR
Dynamic Performance(1)						
THD+N	Total harmonic distortion plus noise	V_{OUT} = 0 dB		0.005%	0.016%	
		V_{OUT} = –60 dB		3%		
	Dynamic range	EIAJ, A-weighted	87	93		dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted	90	96		dB
	Channel separation		86	92		dB
Analog Output						
V_O	Output voltage			0.6 V_{CCCI}		$V_{p–p}$
	Center voltage			0.5 V_{CCCI}		V
	Load impedance	AC coupling	10			kΩ
	LPF frequency response	–3 dB		250		kHz
		f = 20 kHz		–0.03		dB
	Digital filter performance					
	Passband				0.445 f_S	Hz
	Stopband		0.555 f_S			Hz
	Passband ripple				±0.1	dB
	Stopband attenuation		–43			dB
t_d	Delay time			14.3 f_S		s
Power Supply Requirements						
V_{BUS}	Voltage range		4.35	5	5.25	VDC
	Supply current	ADC, DAC operation		56	67	mA
		Suspend mode(2)		210		µA
P_D	Power dissipation	ADC, DAC operation		280	352	mW
		Suspend mode(2)		1.05		mW
	Internal power supply voltage (V_{CCCI}, V_{CCP1I}, V_{CCP2I}, V_{CCXI}, and VDDI)		3.25	3.35	3.5	VDC
Temperature Range						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance	28-pin SSOP		100		°C/W

(1) f_{OUT} = 1 kHz, using Audio Precision System II, RMS mode with 20-kHz LPF, 400-Hz HPF.

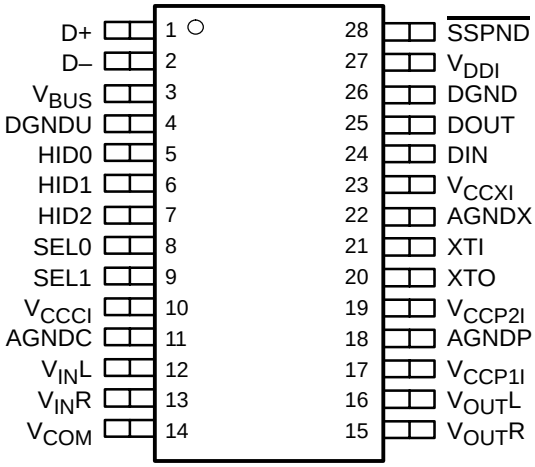
(2) Under USB suspend state

PIN ASSIGNMENTS

PCM2900
(TOP VIEW)



PCM2902
(TOP VIEW)



PCM2900 Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{\text{SSPND}}$	28	O	Suspend flag, active low (Low: suspend, High: operational)
AGNDC	11	–	Analog ground for codec
AGNDP	18	–	Analog ground for PLL
AGNDX	22	–	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	–	Digital ground
DGNDU	4	–	Digital ground for USB transceiver
HID0	5	I	HID key state input (mute), active high(3)
HID1	6	I	HID key state input (volume up), active high(3)
HID2	7	I	HID key state input (volume down), active high(3)
SEL0	8	I	Must be set to high(5)
SEL1	9	I	Must be set to high(5)
TEST0	24	I	Test pin, must be connected to GND
TEST1	25	O	Test pin, must be left open
V_{BUS}	3	I	Connect to USB power (V_{BUS})
V_{CCCI}	10	–	Internal analog power supply for codec(4)
V_{CCP1I}	17	–	Internal analog power supply for PLL(4)
V_{CCP2I}	19	–	Internal analog power supply for PLL(4)
V_{CCXI}	23	–	Internal analog power supply for oscillator(4)
V_{COM}	14	–	Common for ADC/DAC (V_{CCCI}/2) (4)
V_{DDI}	27	–	Internal digital power supply(4)
$V_{IN}L$	12	I	ADC analog input for L-channel
$V_{IN}R$	13	I	ADC analog input for R-channel
$V_{OUT}L$	16	O	DAC analog output for L-channel
$V_{OUT}R$	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input(2)
XTO	20	O	Crystal oscillator output

(1) LV-TTL level

(2) 3.3-V CMOS level input

(3) 3.3-V CMOS level input with internal pulldown. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which has no connection with the internal DAC or ADC directly. See the *volume control* and *mute control* section.

(4) Connect a decouple capacitor to GND

(5) TTL Schmitt trigger, 5 V tolerant

PCM2902 Terminal Functions

TERMINAL NAME	PIN	I/O	DESCRIPTIONS
$\overline{\text{SSPND}}$	28	O	Suspend flag, active low (Low: suspend, High: operational)
AGNDC	11	–	Analog ground for codec
AGNDP	18	–	Analog ground for PLL
AGNDX	22	–	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	–	Digital ground
DGNDU	4	–	Digital ground for USB transceiver
DIN	24	I	S/PDIF input(5)
DOUT	25	O	S/PDIF output
HID0	5	I	HID key state input (mute), active high(3)
HID1	6	I	HID key state input (volume up), active high(3)
HID2	7	I	HID key state input (volume down), active high(3)
SEL0	8	I	Must be set to high(6)
SEL1	9	I	Must be set to high(6)
V_{BUS}	3	I	Connect to USB power (V_{BUS})
V_{CCCI}	10	–	Internal analog power supply for codec(4)
V_{CCP1I}	17	–	Internal analog power supply for PLL(4)
V_{CCP2I}	19	–	Internal analog power supply for PLL(4)
V_{CCXI}	23	–	Internal analog power supply for oscillator(4)
V_{COM}	14	–	Common for ADC/DAC ($V_{CCCI}/2$) (4)
V_{DDI}	27	–	Internal digital power supply(4)
$V_{IN}L$	12	I	ADC analog input for L-channel
$V_{IN}R$	13	I	ADC analog input for R-channel
$V_{OUT}L$	16	O	DAC analog output for L-channel
$V_{OUT}R$	15	O	DAC Analog output for R-channel
XTI	21	I	Crystal oscillator input(2)
XTO	20	O	Crystal oscillator output

(1) LV-TTL level

(2) 3.3-V CMOS level input

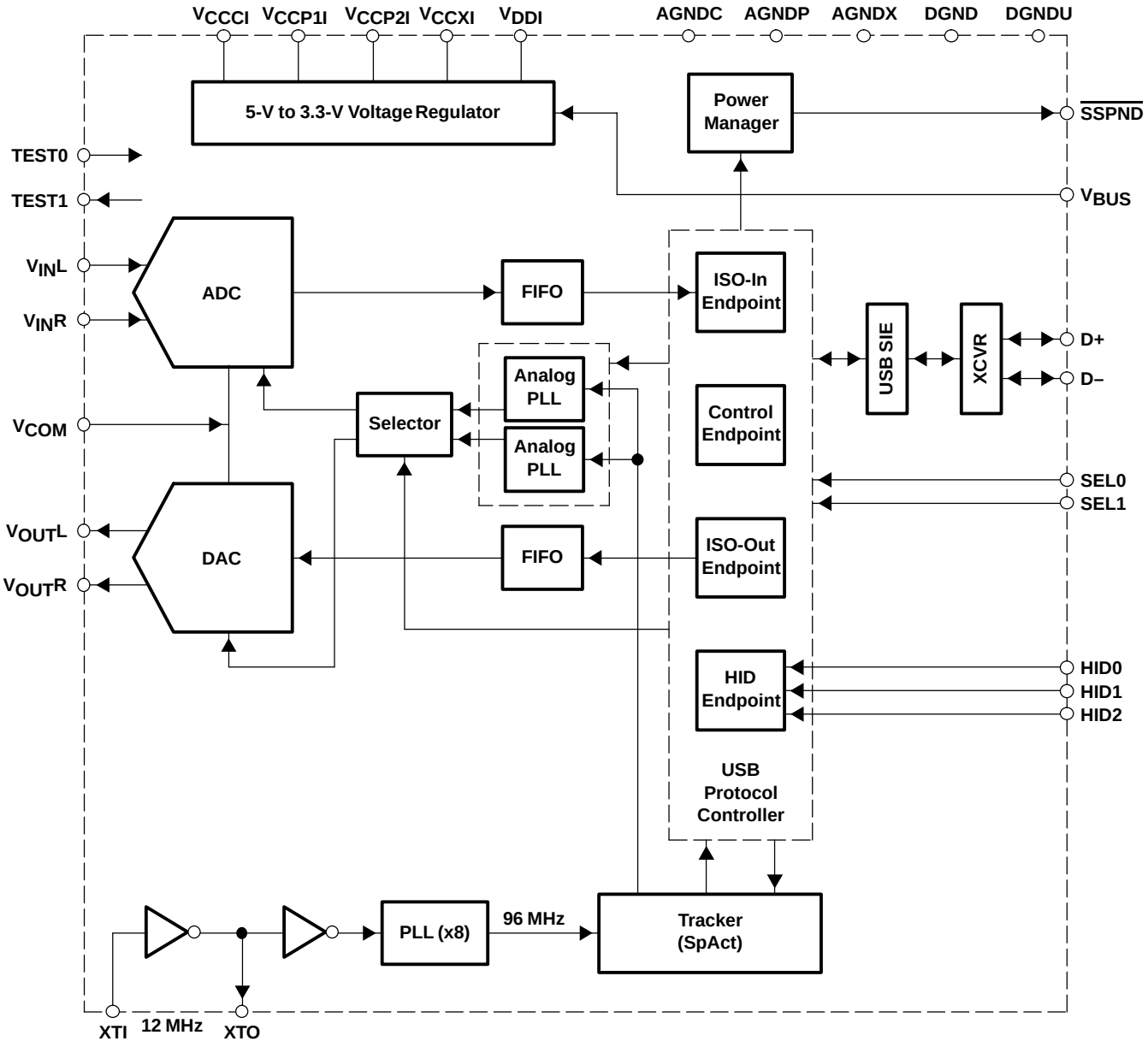
(3) 3.3-V CMOS level input with internal pulldown. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which has no connection with the internal DAC or ADC directly. See the *volume control* and *mute control* section.

(4) Connect a decouple capacitor to GND

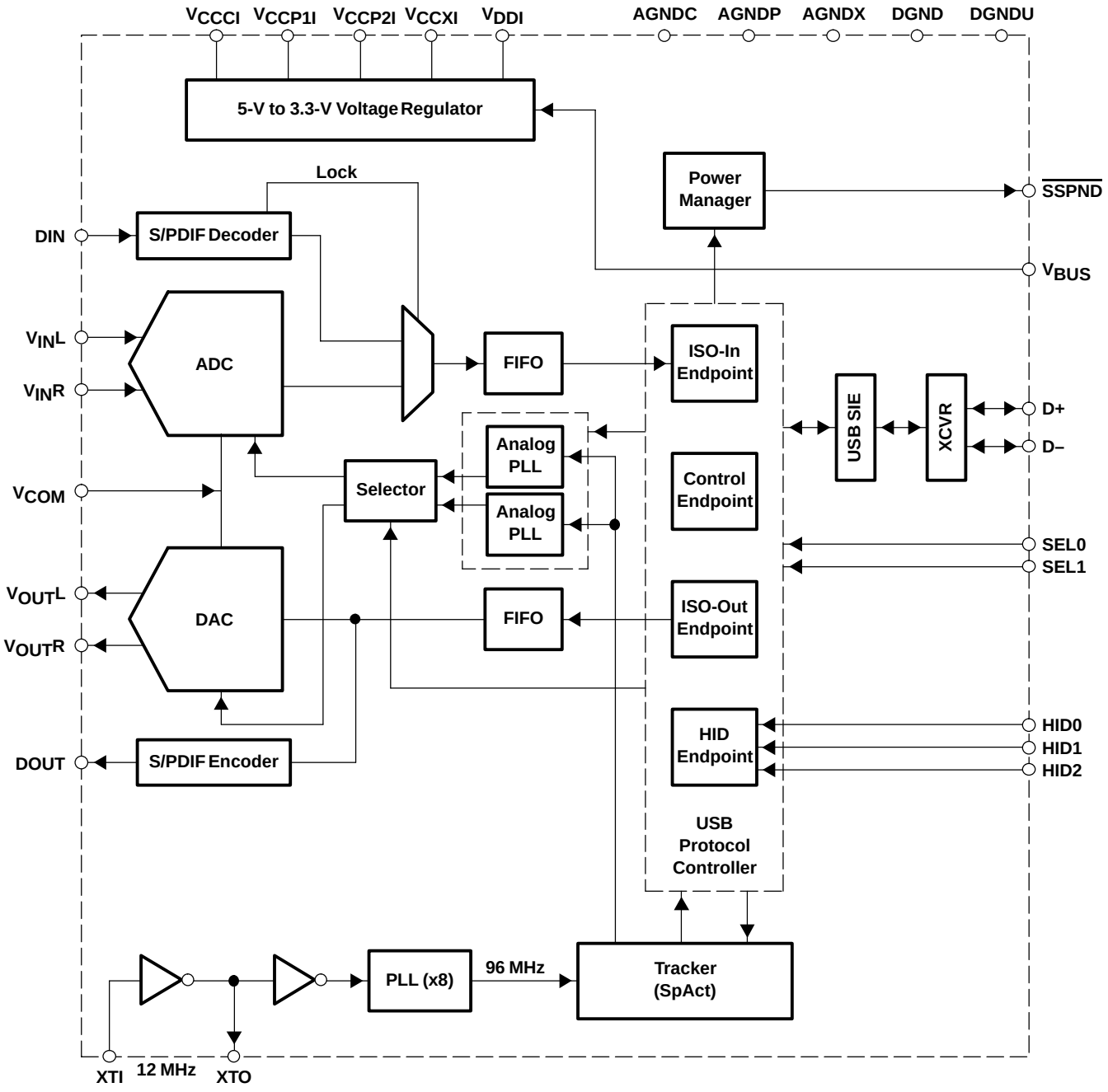
(5) 3.3-V CMOS level input with internal pulldown, 5 V tolerant

(6) TTL Schmitt trigger, 5 V tolerant

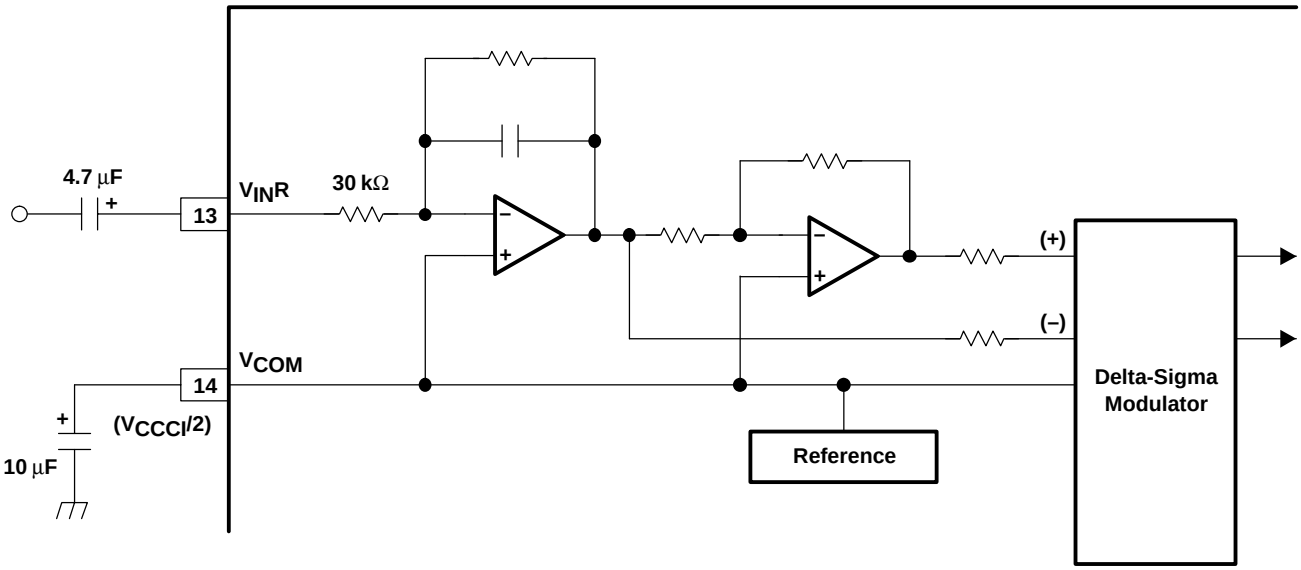
PCM2900 FUNCTIONAL BLOCK DIAGRAM



PCM2902 FUNCTIONAL BLOCK DIAGRAM



PCM2900/2902 BLOCK DIAGRAM OF ANALOG FRONT-END (RIGHT CHANNEL)



TYPICAL CHARACTERISTICS

ADC

TOTAL HARMONIC DISTORTION + NOISE at –0.5 dB vs FREE-AIR TEMPERATURE

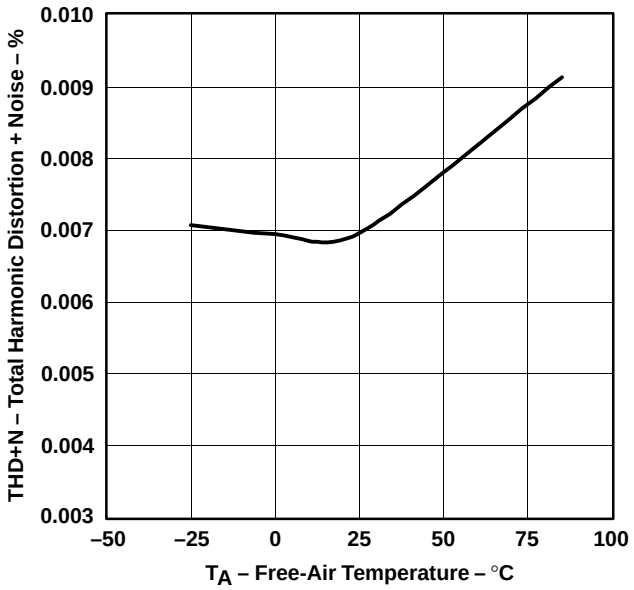


Figure 1

DYNAMIC RANGE and SNR vs FREE-AIR TEMPERATURE

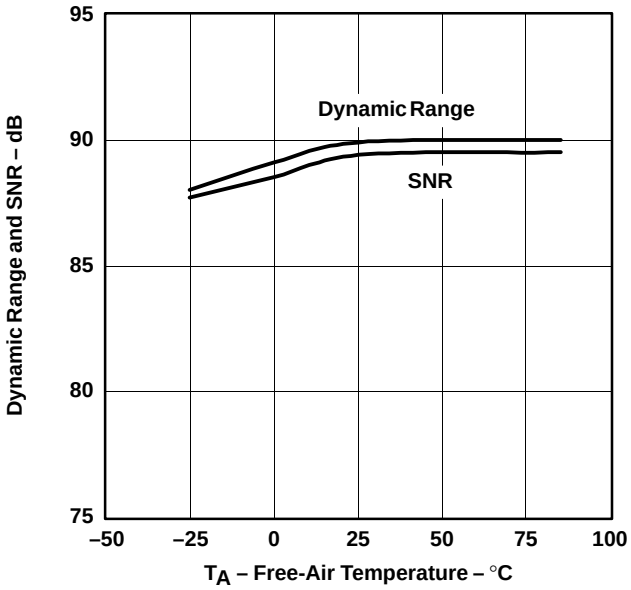


Figure 2

TOTAL HARMONIC DISTORTION + NOISE at –0.5 dB vs SUPPLY VOLTAGE

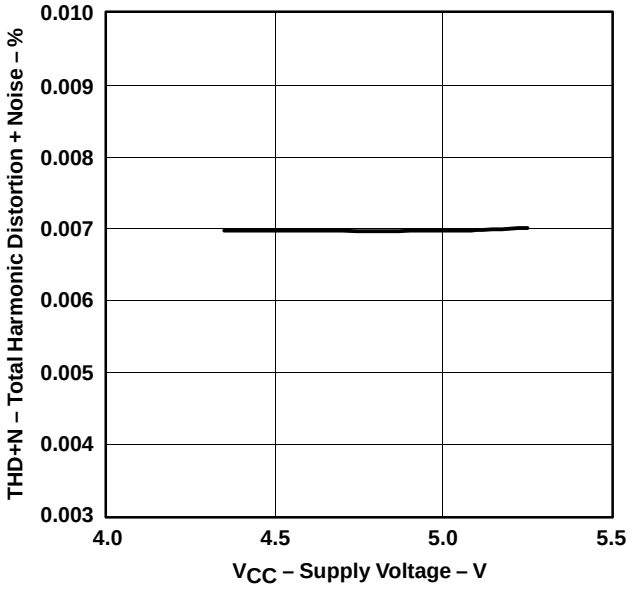


Figure 3

DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE

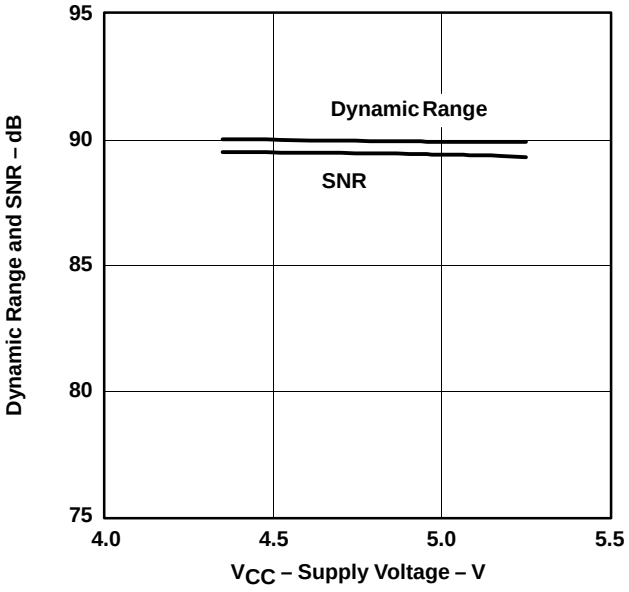


Figure 4

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted, if using the REG 103xA-A.

ADC (CONTINUED)

TOTAL HARMONIC DISTORTION + NOISE at –0.5 dB vs SAMPLING FREQUENCY

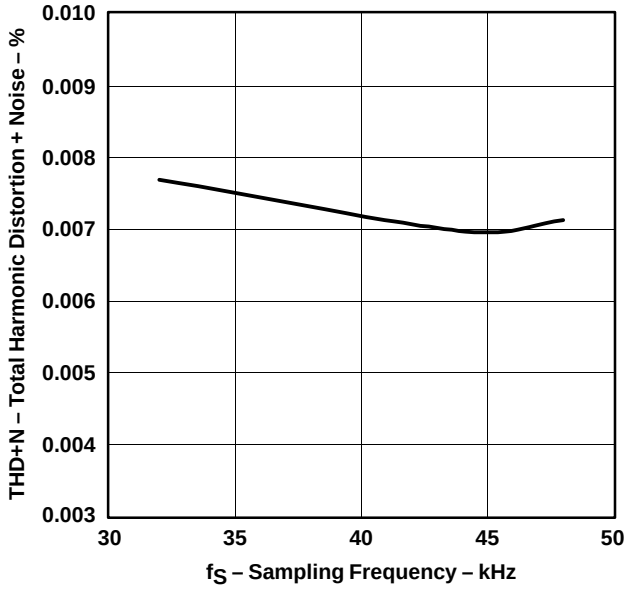


Figure 5

DYNAMIC RANGE and SNR vs SAMPLING FREQUENCY

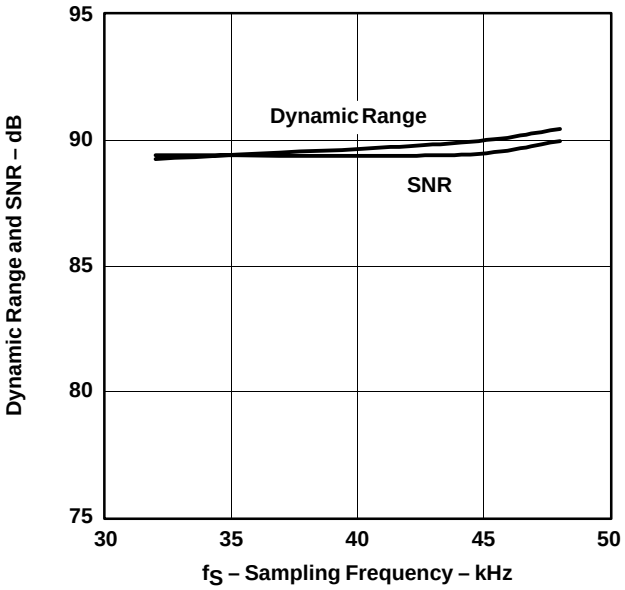


Figure 6

DAC

TOTAL HARMONIC DISTORTION + NOISE at 0 dB vs FREE-AIR TEMPERATURE

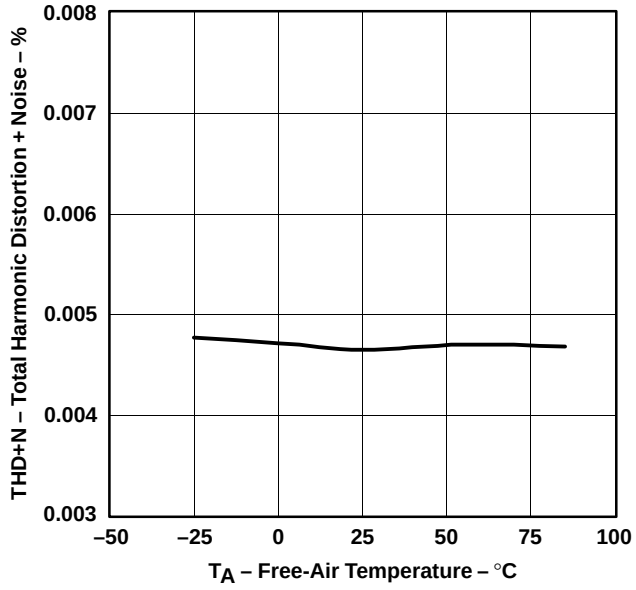


Figure 7

DYNAMIC RANGE and SNR vs FREE-AIR TEMPERATURE

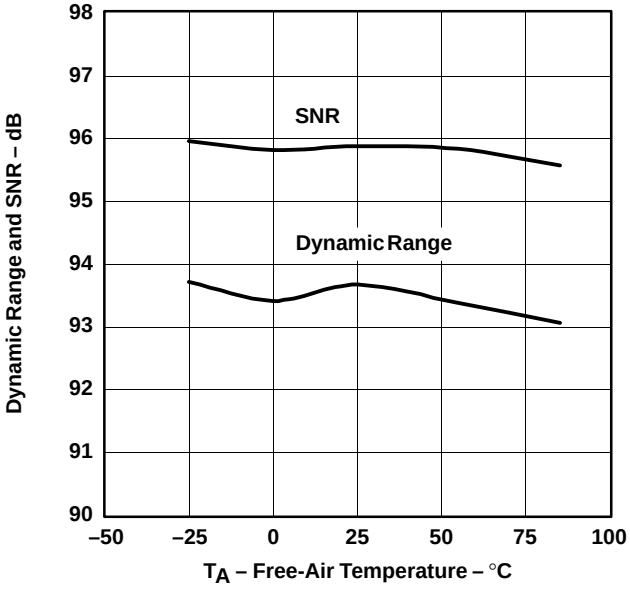


Figure 8

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted, if using the REG 103xA-A.

DAC (CONTINUED)

TOTAL HARMONIC DISTORTION + NOISE at 0 dB vs SUPPLY VOLTAGE

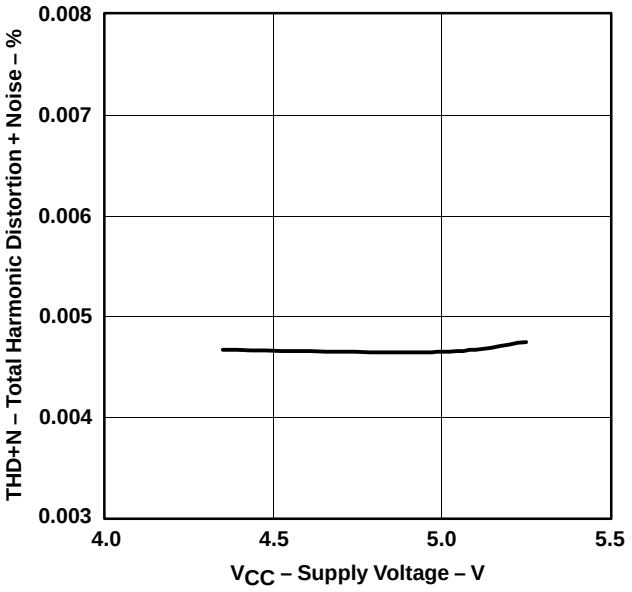


Figure 9

DYNAMIC RANGE and SNR vs SUPPLY VOLTAGE

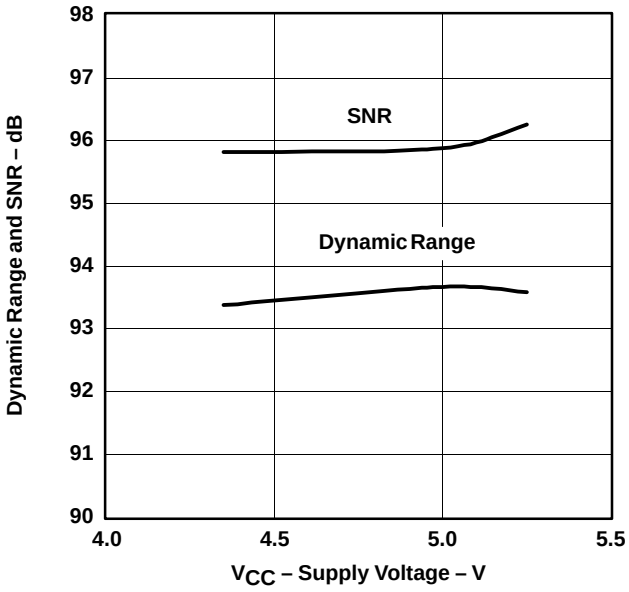


Figure 10

TOTAL HARMONIC DISTORTION + NOISE at 0 dB vs SAMPLING FREQUENCY

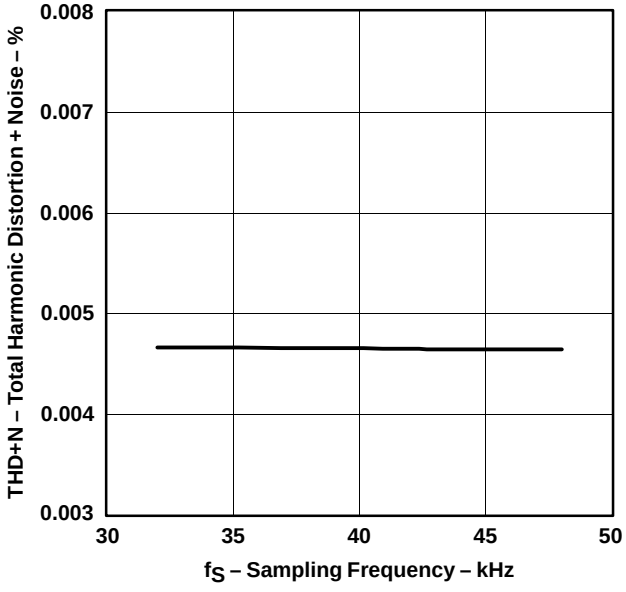


Figure 11

DYNAMIC RANGE and SNR vs SAMPLING FREQUENCY

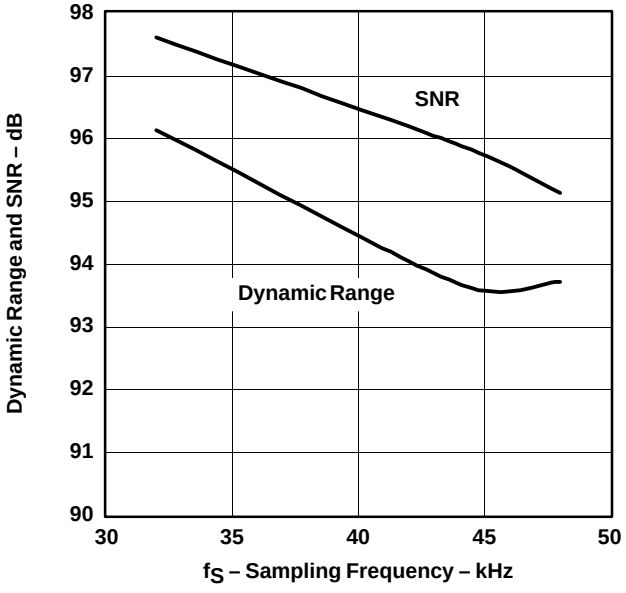


Figure 12

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted, if using the REG 103xA-A.

SUPPLY CURRENT

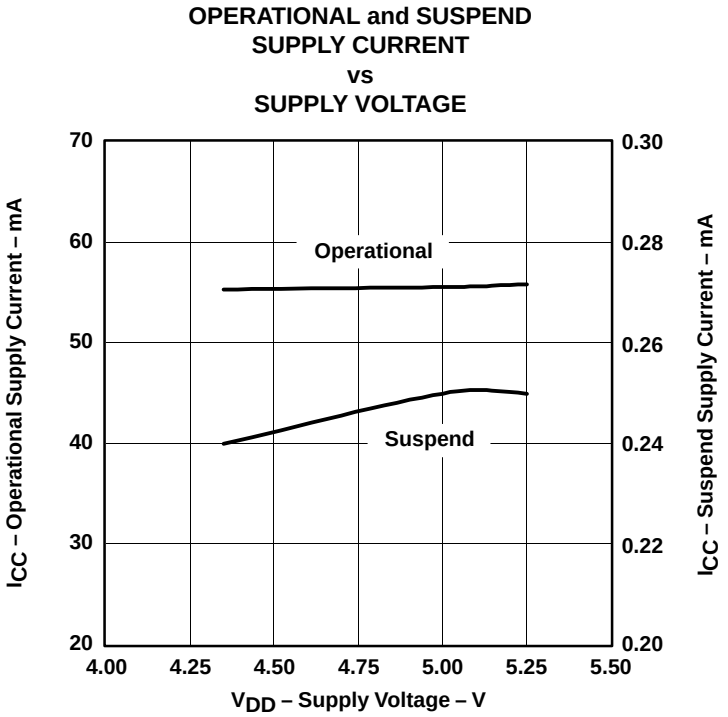


Figure 13

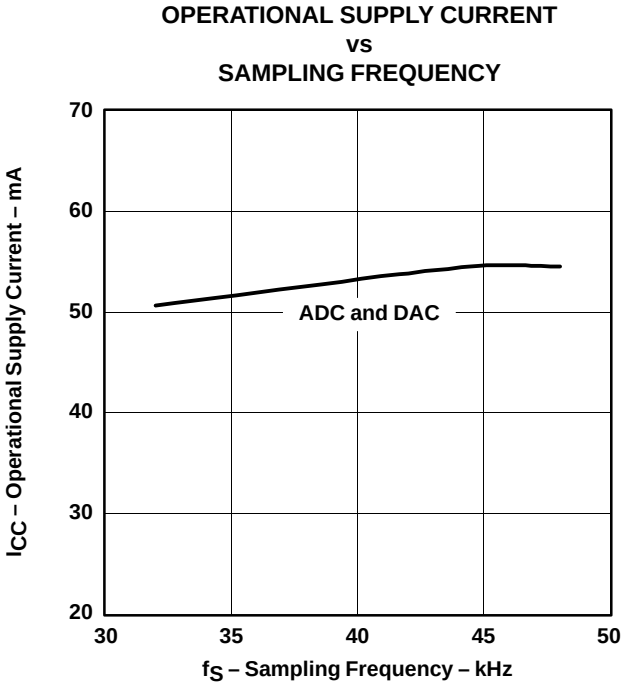


Figure 14

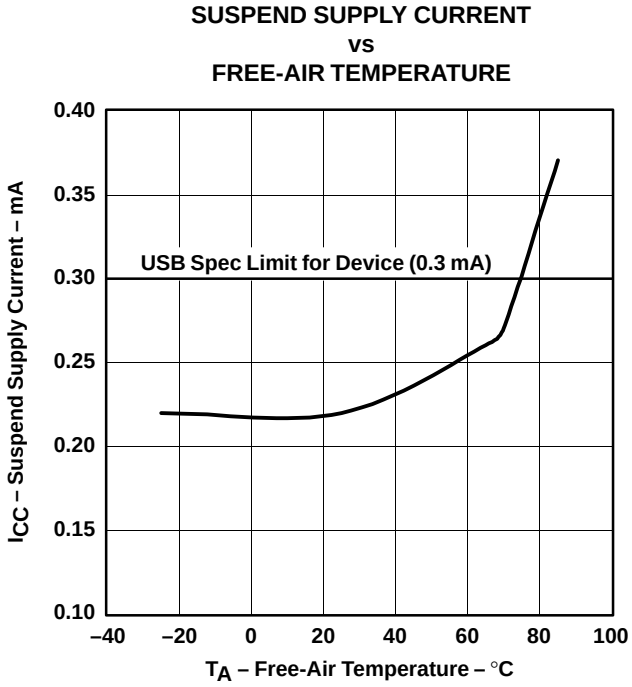


Figure 15

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted, if using the REG 103xA-A.

ADC DIGITAL DECIMATION FILTER FREQUENCY RESPONSE

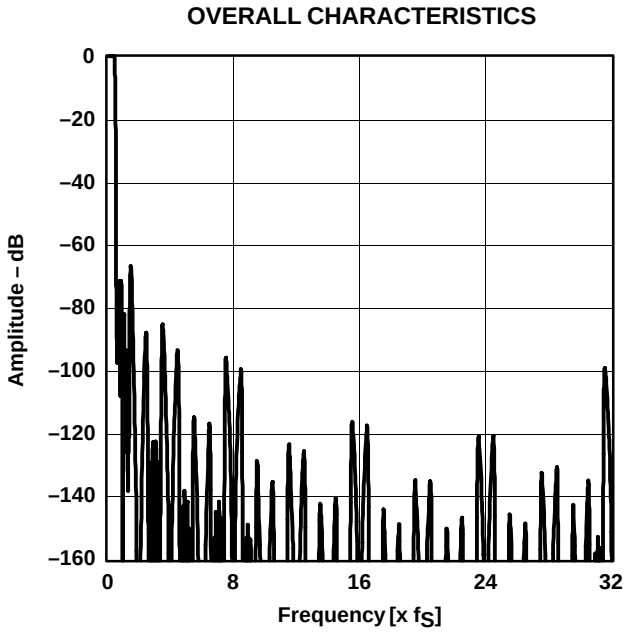


Figure 16

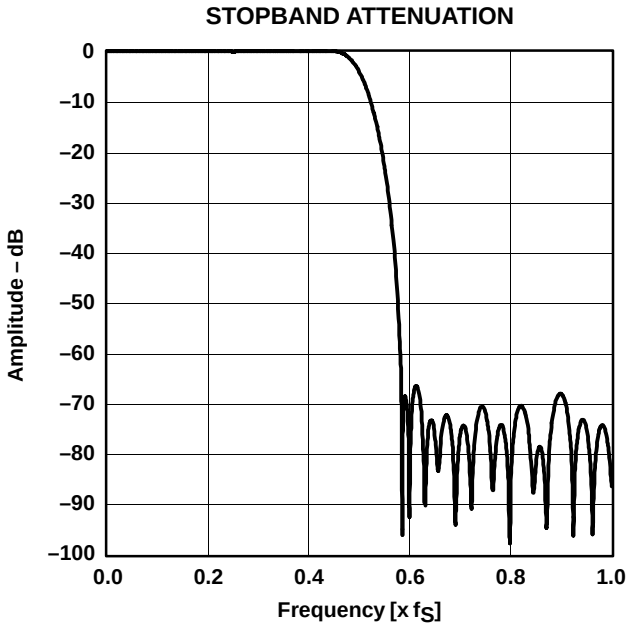


Figure 17

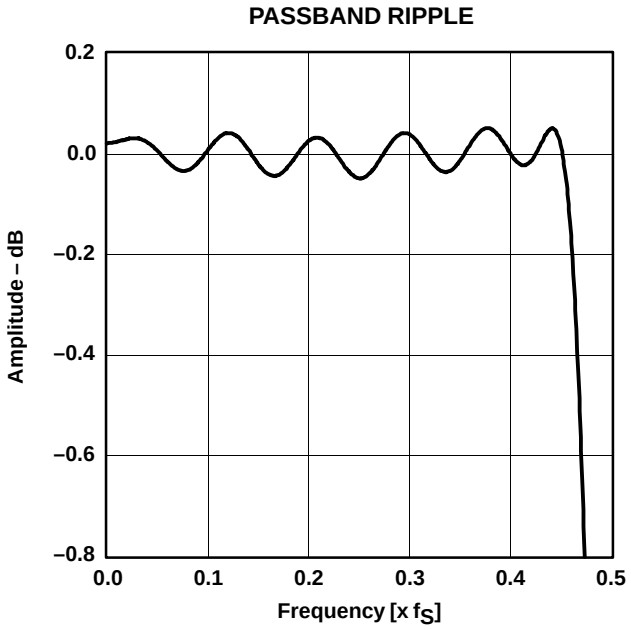


Figure 18

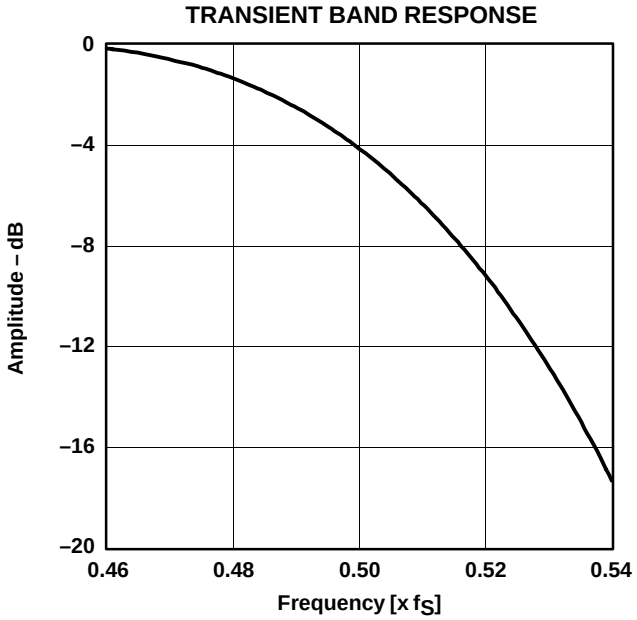


Figure 19

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted, if using the REG 103xA-A.

ADC DIGITAL HIGH PASS FILTER FREQUENCY RESPONSE

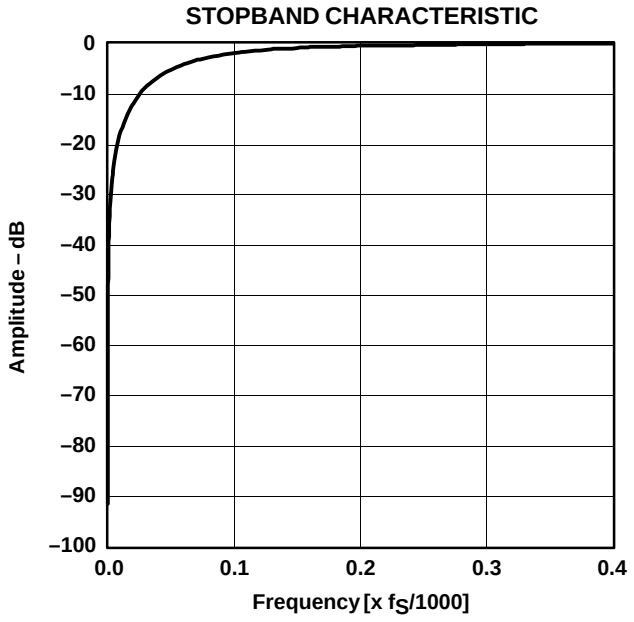


Figure 20

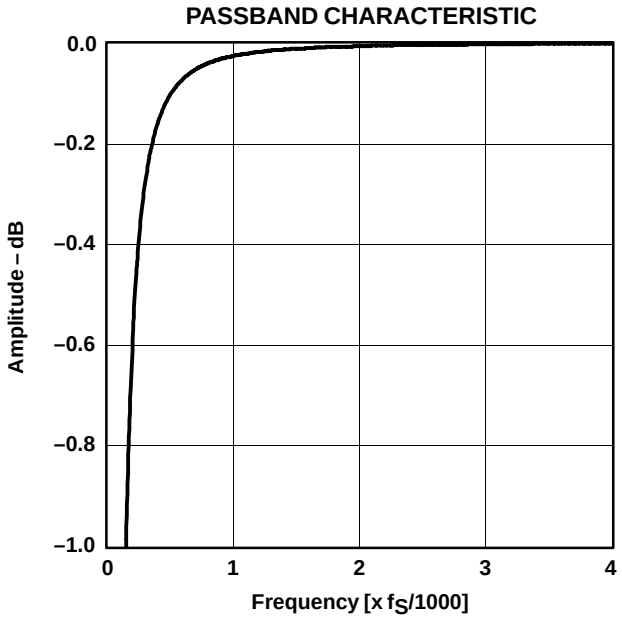


Figure 21

ADC ANALOG ANTIALIASING FILTER FREQUENCY RESPONSE

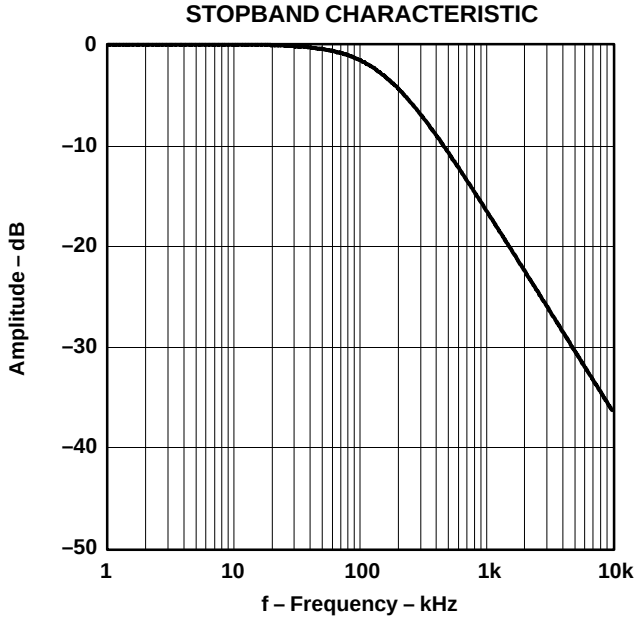


Figure 22

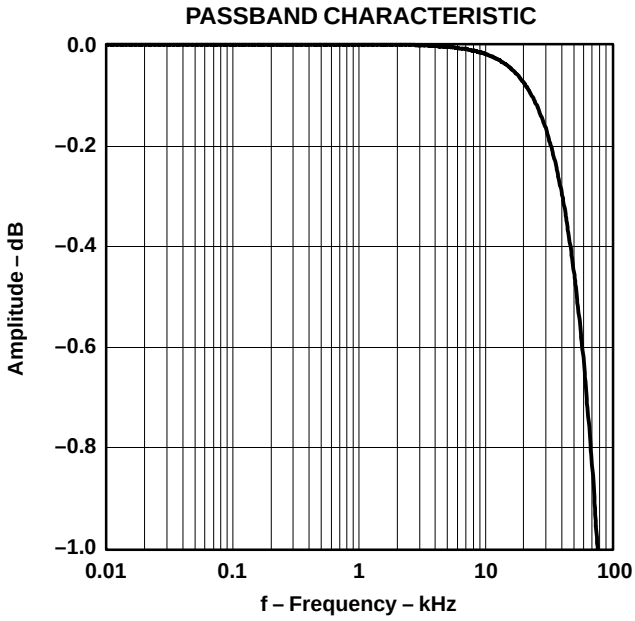


Figure 23

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted, if using the REG 103xA-A.

ADC DIGITAL INTERPOLATION FILTER FREQUENCY RESPONSE

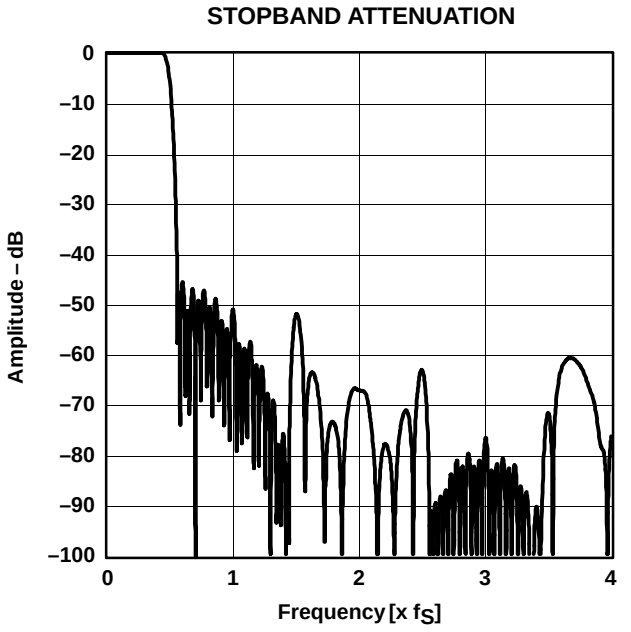


Figure 24

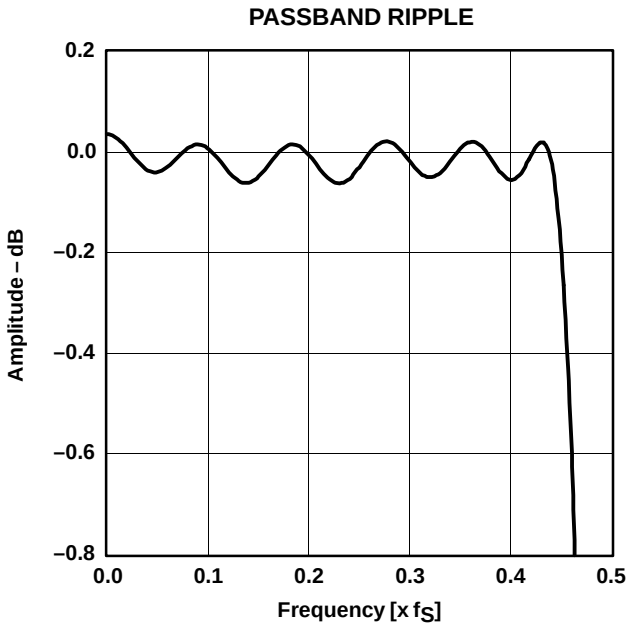


Figure 25

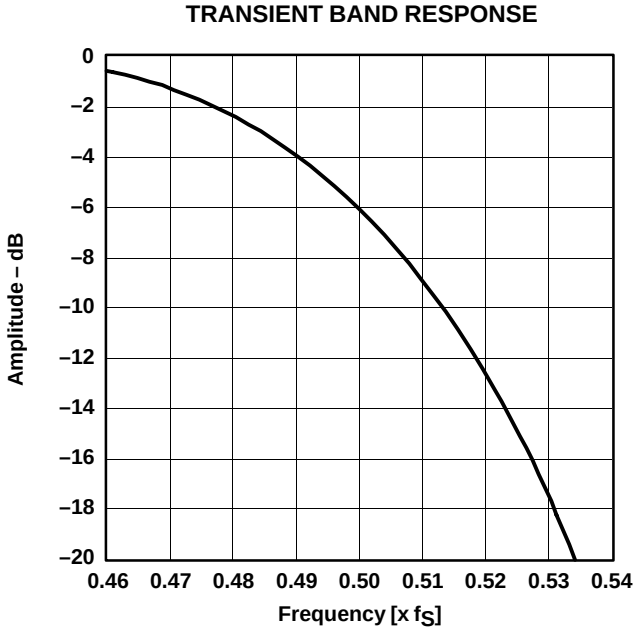


Figure 26

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted, if using the REG 103xA-A.

DAC ANALOG FIR FILTER FREQUENCY RESPONSE

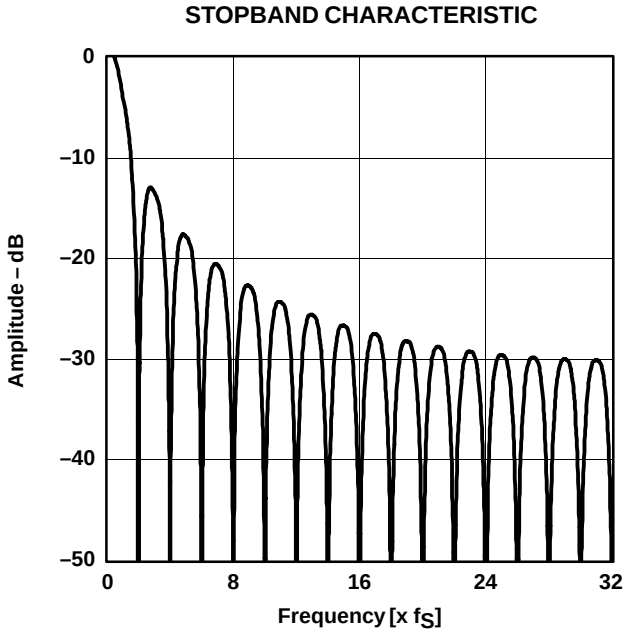


Figure 27

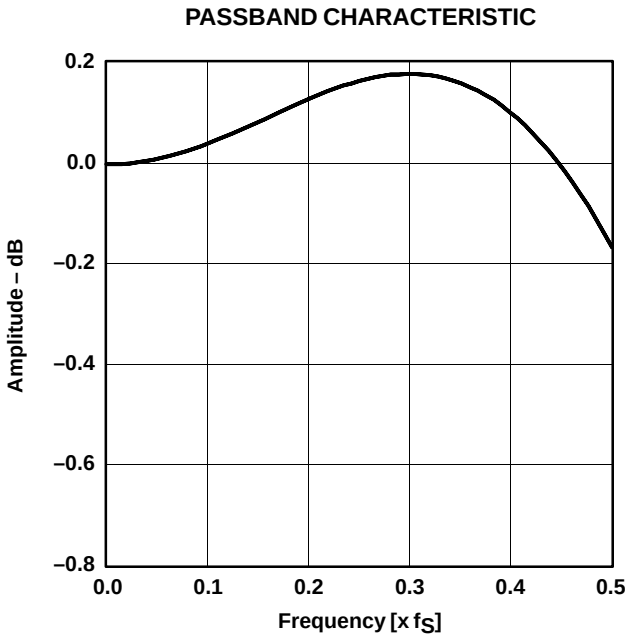


Figure 28

DAC ANALOG LOW PASS FILTER FREQUENCY RESPONSE

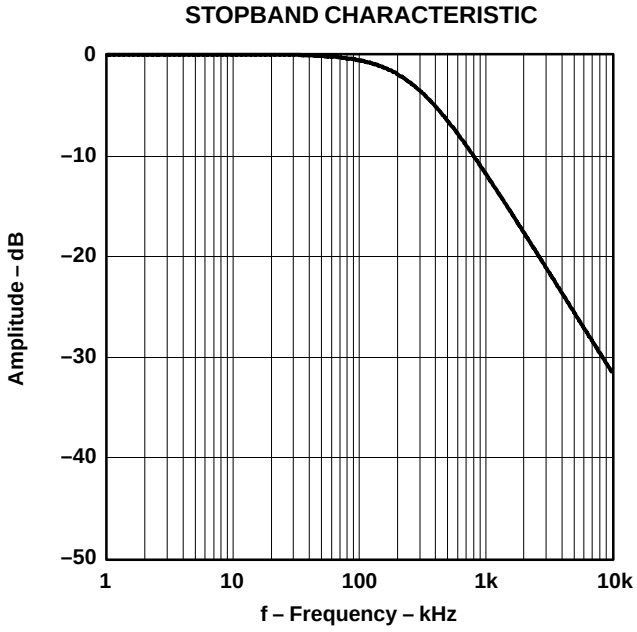


Figure 29

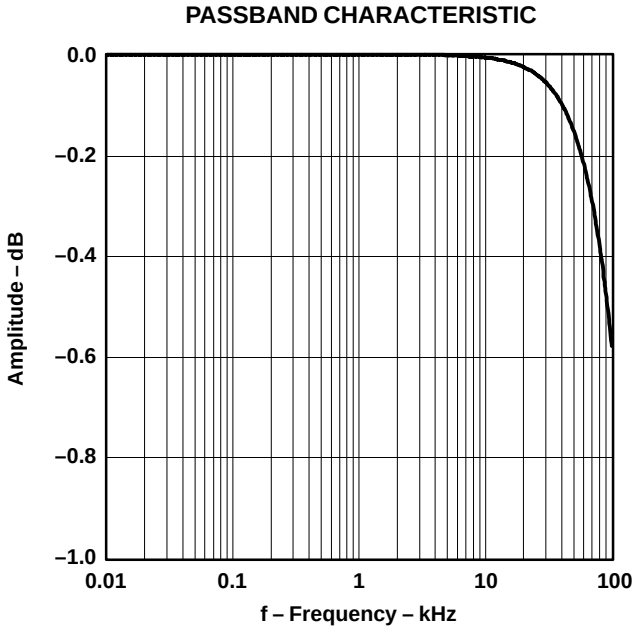


Figure 30

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{in} = 1 kHz, 16-bit data, unless otherwise noted, if using the REG 103xA-A.

USB INTERFACE

Control data and audio data are transferred to the PCM2900/2902 via D+ (pin 1) and D– (pin 2). All data to/from the PCM2900/2902 is performed in full speed. The device descriptor can be modified upon request, contact a Texas Instruments representative for details (see Table 1).

Table 1. Device Descriptor

USB revision	1.1 compliant
Device class	0x00 (device defined interface level)
Device sub class	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for endpoint 0	8 byte
Vendor ID	0x08BB (default value, can be modified)
Product ID	0x2900 / 0x2902 (default value, can be modified)
Device release number	1.0 (0x0100)
Number of configurations	1
Vendor strings	Burr-Brown from TI (default value, can be modified)
Product strings	USB audio codec (default value, can be modified)
Serial number	Not supported

The configuration descriptor can be modified upon request, contact your representative for details (see Table 2).

Table 2. Configuration Descriptor

Interface	Four interfaces
Power attribute	0x80 (Bus powered,no remote wakeup)
Max power	0x32 (100 mA. Default value, can be modified)

The string descriptor can be modified upon request, contact a Texas Instruments representative for details (see Table 3).

Table 3. String Descriptor

#0	0x0409
#1	Burr-Brown from TI (default value, can be modified)
#2	USB audio codec (default value, can be modified)

DEVICE CONFIGURATION

Figure 31 illustrates the USB audio function topology. The PCM2900/2902 has four interfaces. Each interface is constructed by alternative settings.

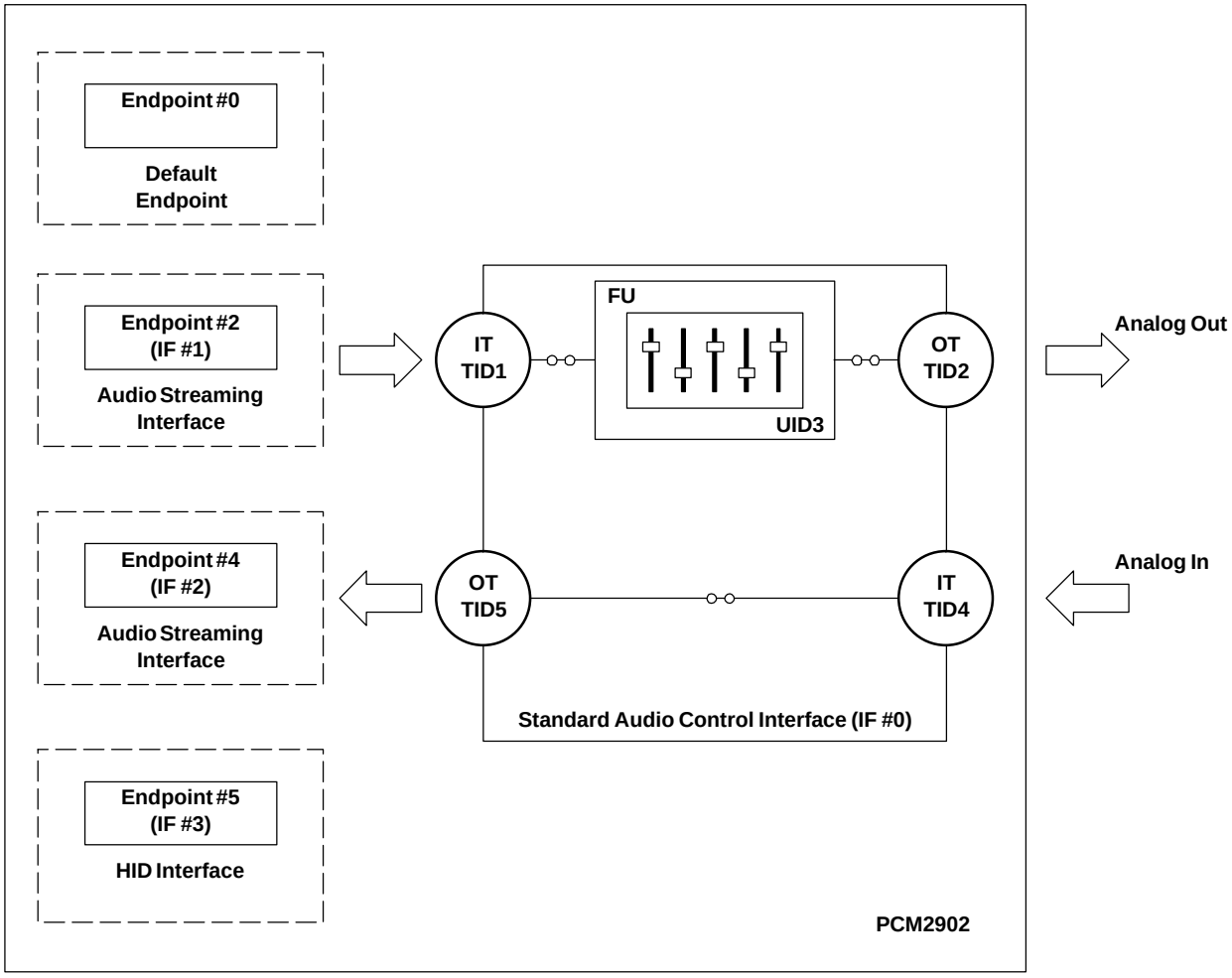


Figure 31. USB Audio Function Topology

Interface #0

Interface #0 is for the control interface. Alternative setting #0 is the only possible setting for interface #0. Alternative setting #0 describes the standard audio control interface. A terminal constructs the audio control interface. The PCM2900/2902 has five terminals as follows:

- Input terminal (IT #1) for isochronous-out stream
- Output terminal (OT #2) for audio analog output
- Feature unit (FU #3) for DAC digital attenuator
- Input terminal (IT #4) for audio analog input
- Output terminal (OT #5) for isochronous-in stream

Input terminal #1 is defined as USB stream (terminal type 0x0101). Input terminal #1 can accept 2-channel audio streams constructed by left and right channels. Output terminal #2 is defined as a speaker (terminal type 0x0301). Input terminal #4 is defined as microphon (terminal type 0x0201). Output terminal #5 is defined as a USB stream (terminal type 0x0101). Output terminal #5 can generate 2-channel audio streams constructed by left and right channels. Feature unit #3 supports the following sound control features.

- Volume control
- Mute control

The built-in digital volume controller can be manipulated by an audio class specific request from 0 dB to –64 dB in 1-dB steps. Changes are made by incrementing or decrementing by one step (1 dB) for every $1/f_S$ time interval until the volume level has reached the requested value. Each channel can be set for different values. The master

volume control is not supported. A request to the master volume is stalled and ignored. The built-in digital mute controller can be manipulated by audio class specific request. A master mute control request is acceptable. A request to an individual channel is stalled and ignored.

Interface #1

Interface #1 is for audio streaming data out interface. Interface #1 has the following seven alternative settings. Alternative setting #0 is the zero bandwidth setting. All other alternative settings are operational settings.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero Bandwidth				
01	16 bit	Stereo	2s complement (PCM)	Adaptive	32, 44.1, 48
02	16 bit	Mono	2s complement (PCM)	Adaptive	32, 44.1, 48
03	8 bit	Stereo	2s complement (PCM)	Adaptive	32, 44.1, 48
04	8 bit	Mono	2s complement (PCM)	Adaptive	32, 44.1, 48
05	8 bit	Stereo	Offset binary (PCM8)	Adaptive	32, 44.1, 48
06	8 bit	Mono	Offset binary (PCM8)	Adaptive	32, 44.1, 48

Interface #2

Interface #2 is for the audio streaming data in the interface. Interface #2 has the following 15 alternative settings. Alternative setting #0 is the zero bandwidth setting. All other alternative settings are operational settings.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero Bandwidth				
01	16 bit	Stereo	2s complement (PCM)	Asynchronous	48
02	16 bit	Mono	2s complement (PCM)	Asynchronous	48
03	16 bit	Stereo	2s complement (PCM)	Asynchronous	44.1
04	16 bit	Mono	2s complement (PCM)	Asynchronous	44.1
05	16 bit	Stereo	2s complement (PCM)	Asynchronous	32
06	16 bit	Mono	2s complement (PCM)	Asynchronous	32
07	16 bit	Stereo	2s complement (PCM)	Asynchronous	22.05
08	16 bit	Mono	2s complement (PCM)	Asynchronous	22.05
09	16 bit	Stereo	2s complement (PCM)	Asynchronous	16
0A	16 bit	Mono	2s complement (PCM)	Asynchronous	16
0B	8 bit	Stereo	2s complement (PCM)	Asynchronous	16
0C	8 bit	Mono	2s complement (PCM)	Asynchronous	16
0D	8 bit	Stereo	2s complement (PCM)	Asynchronous	8
0E	8 bit	Mono	2s complement (PCM)	Asynchronous	8

Interface #3

Interface #3 is for interrupt data in interface. Alternative setting #0 is the only possible setting for interface #3. Interface #3 constructs the HID consumer control device. Interface #3 reports the following three key statuses.

- Mute (0xE209)
- Volume up (0xE909)
- Volume down (0xEA09)

Endpoints

The PCM2900/2902 has the following four endpoints.

- Control endpoint (EP #0)
- Isochronous-out audio data stream endpoint (EP #2)
- Isochronous-in audio data stream endpoint (EP #4)
- HID endpoint (EP #5)

The control endpoint is a default endpoint. The control endpoint is used to control all functions of the PCM2900/2902 by the standard USB request and USB audio class specific request from the host. The isochronous-out audio data stream endpoint is an audio sink endpoint, which receives the PCM audio data. The isochronous-out audio data stream endpoint accepts the adaptive transfer mode. The isochronous-in audio data stream endpoint is an audio source endpoint, which transmits the PCM audio data. The isochronous-in audio data stream endpoint uses asynchronous transfer mode. The HID endpoint is an interrupt-in endpoint. HID endpoint reports HID0, HID1, and HID2 pin status in every 32 ms.

The human interface device (HID) pins are defined as consumer control devices. The HID function is designed as an independent endpoint from both isochronous-in and -out endpoints. This means that the result of affection for the HID operation is depending on the host software. Typically, the HID function is affected for the primary audio-out device.

Clock and Reset

The PCM2900/2902 requires a 12-MHz (±500 ppm) clock for the USB and audio function, which can be generated by a built in crystal oscillator with a 12-MHz crystal resonator. The 12-MHz crystal resonator must be connected to XTI (pin 21) and XTO (pin 20) with one high (1 MΩ) resistor and two small capacitors, which capacitance's depends on the load capacitance of the crystal resonator. The external clock can be supplied from XTI (pin 21), If the external clock is supplied, XTO (pin 20) must be left open. Because of no clock-disabling signal, it is not recommended to use the external clock supply. $\overline{\text{SSPND}}$ (pin 28) is unable to use clock disabling.

The PCM2900/2902 has an internal power-on reset circuit, which works automatically when V_{BUS} (pin 3) exceeds 2.5 V typical (2.7 V–2.2 V) and about 700 μs is required until internal reset release.

Digital Audio Interface (PCM2902)

The PCM2902 employs both S/PDIF input and output. Isochronous–out data from the host is encoded to the S/PDIF output and the DAC analog output. Input data is selected as either S/PDIF or ADC analog input. When device detect S/PDIF input and successfully locked received data, the isochronous–out transfer data source is automatically selected from S/PDIF itself, otherwise the data source is selected to ADC analog input.

Supported Input Data (PCM2902)

The following data formats are accepted by the S/PDIF input and output. All other data formats are unable to use S/PDIF.

- 48-kHz 16-bit stereo
- 44.1-kHz 16-bit stereo
- 32-kHz 16-bit stereo

Mismatch between input data format and host command may cause unexpected results except in the following conditions.

- Record monaural format from stereo data input at the same data rate
- Record 8-bit format from 16-bit data input at the same data rate

A combination between the above conditions is also accepted.

For the playback, all possible data rate source is converted to 16-bit stereo format at the same source data rate.

Copyright Management (PCM2902)

Isochronous-in data is affected by the serial copy management system (SCMS). Where receiving digital audio data that is indicated as original data in the control bit, input digital audio data transfers to the host. If the data is indicated as first generation or higher, transferred data is selected to analog input.

Digital audio data output is always encoded as original with SCMS control.

The implementation of this feature is an option for the customer. Note that it is the user's responsibility whether they implement this feature in their product or not.

INTERFACE SEQUENCE

Power On, Attach, and Play Back Sequence

The PCM2900/2902 is ready for setup when the reset sequence has finished and the USB bus is attached. After connection has been established by setup, the PCM2900/2902 is ready to accept USB audio data. While waiting, the audio data (idle state) and analog output are set to bipolar zero (BPZ).

When receiving the audio data, the PCM2900/2902 stores the first audio packet, which contained 1-ms audio data, into the internal storage buffer. The PCM2900/2902 starts playing the audio data when detecting the following start of frame (SOF) packet.

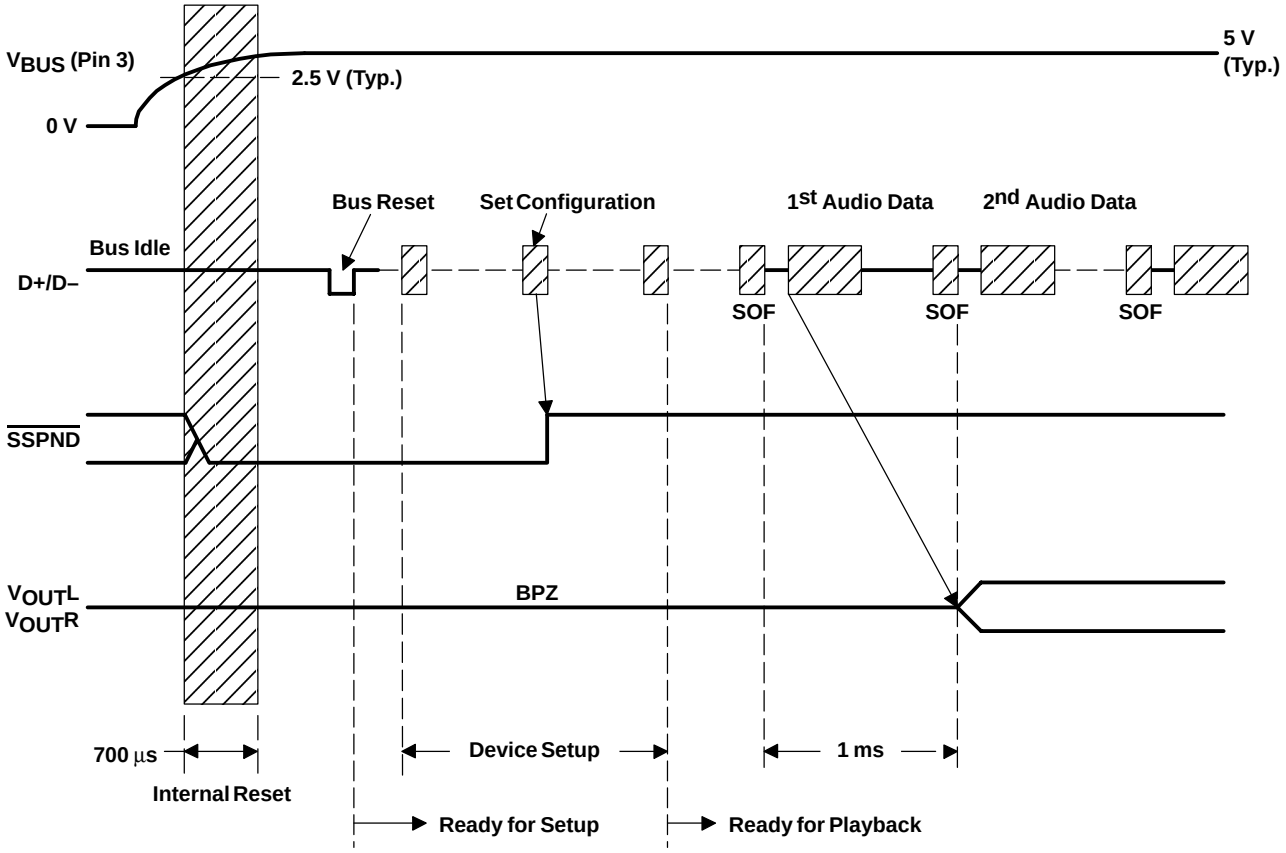


Figure 32. Initial Sequence

Play, Stop, and Detach Sequence

When the host finishes or aborts the play back, the PCM2900/2902 stops playing after the last audio data has played.

Record Sequence

The PCM2900/2902 starts the audio capture into the internal memory after receiving the SET_INTERFACE command.

Suspend and Resume Sequence

The PCM2900/2902 enters the suspend state after it sees a constant idle state on the USB bus, approximately 5 ms. While the PCM2900/2902 enters the suspend state, $\overline{\text{SSPND}}$ flag (pin 28) is asserted. The PCM2900/2902 wakes up immediately when detecting the non-idle state on the USB bus.

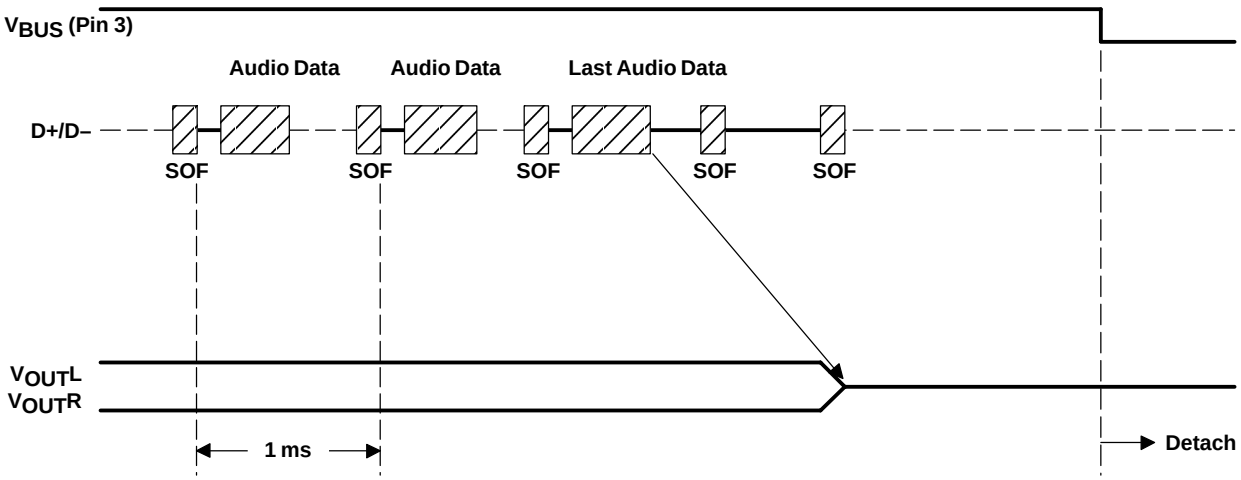


Figure 33. Play, Stop, and Detach

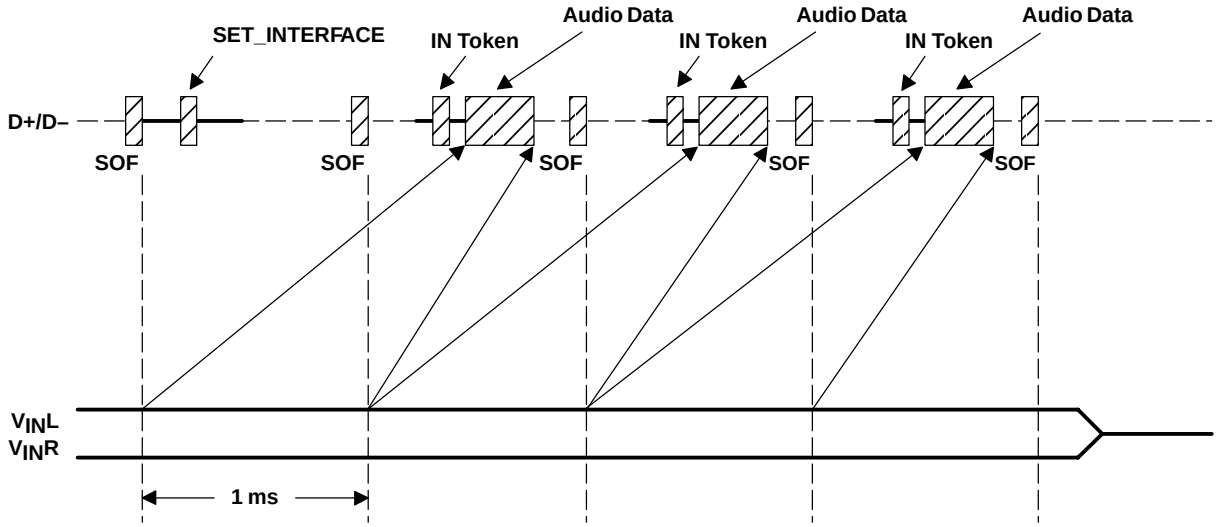


Figure 34. Record Sequence

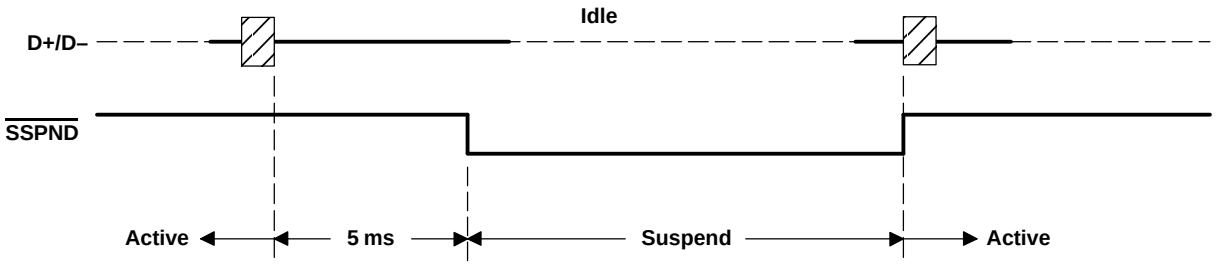
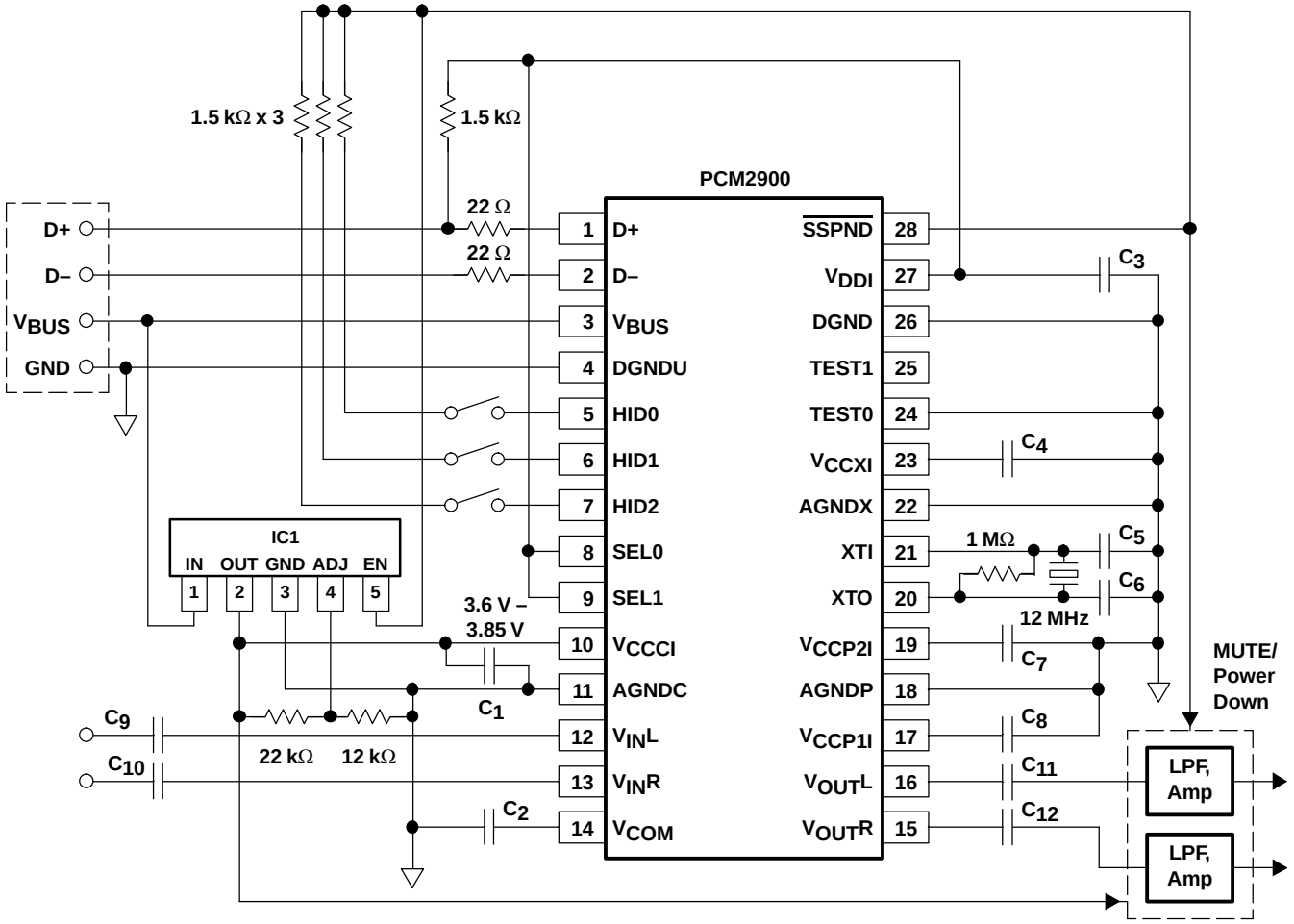


Figure 35. Suspend and Resume

PCM2900 TYPICAL CIRCUIT CONNECTION 1

Figure 36 illustrates a typical circuit connection for a high performance application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.



NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design
IC1: REG103xA–A (TI) or equivalent. Analog performance may vary depending on IC1.

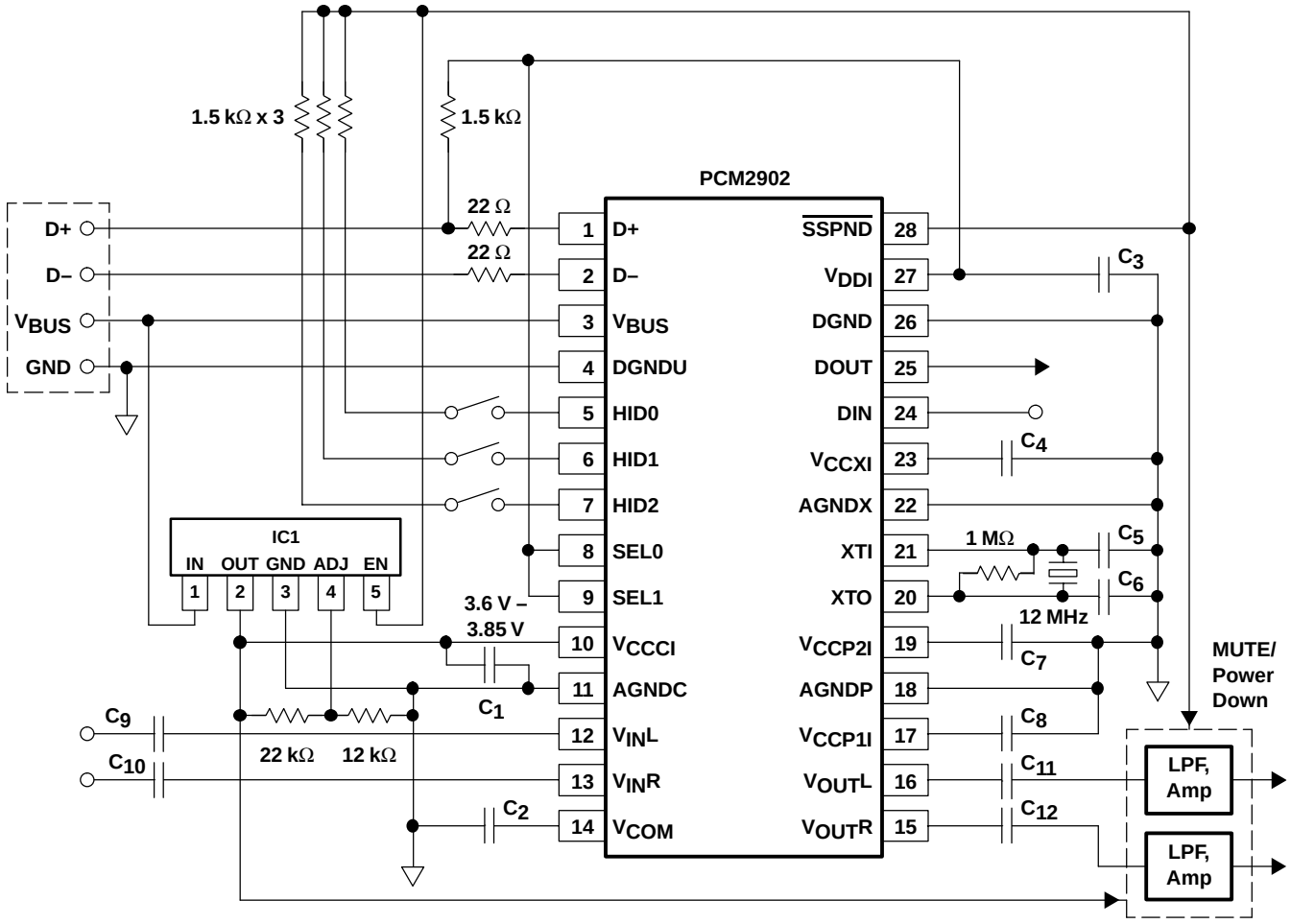
Figure 36. Bus-Powered Configuration for High-Performance Application

NOTE:

The circuit illustrated above is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.

PCM2902 TYPICAL CIRCUIT CONNECTION 1

Figure 37 illustrates a typical circuit connection for a high performance application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.



NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF)
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design
IC1: REG103xA–A (TI) or equivalent. Analog performance may vary depending on IC1.

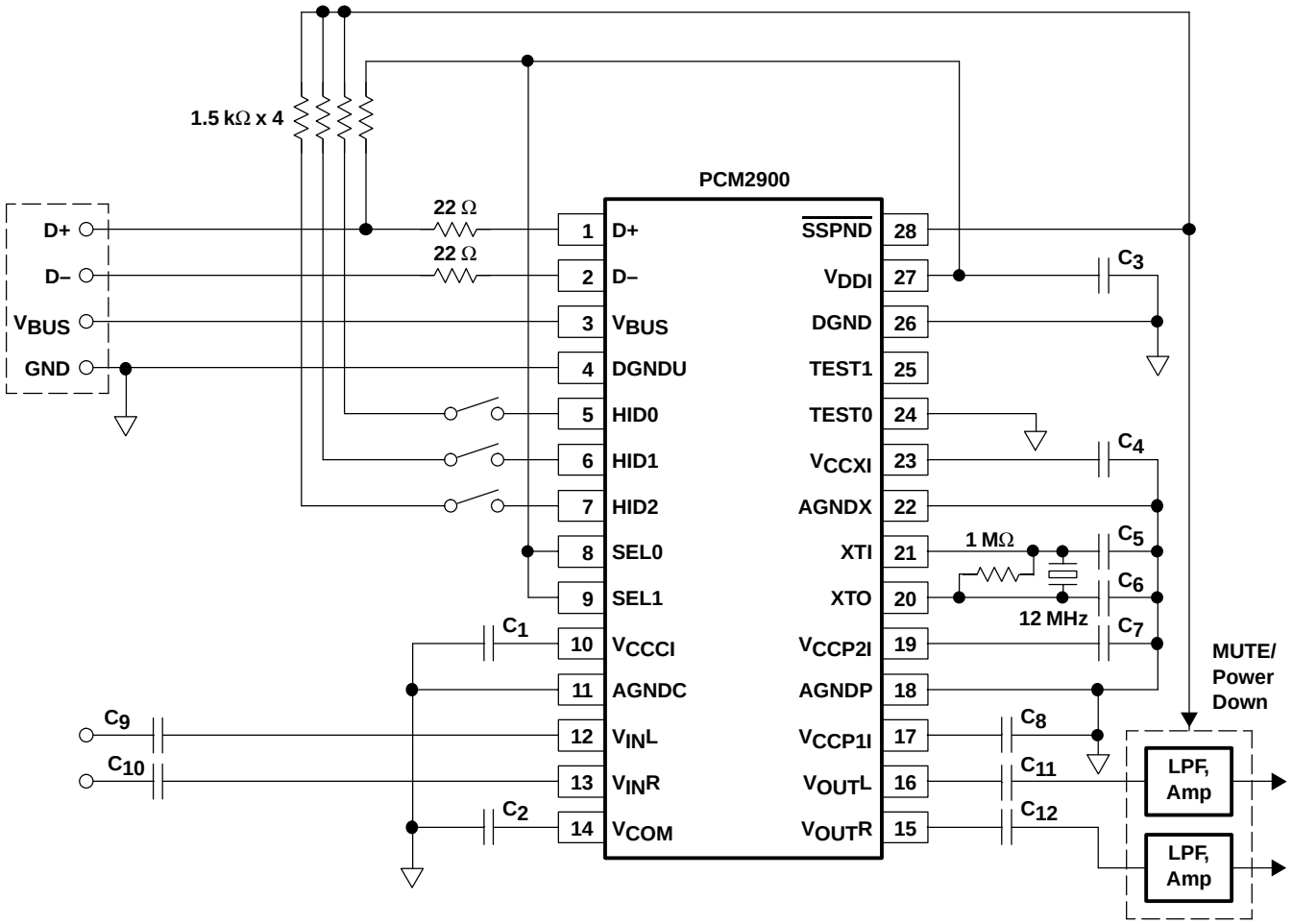
Figure 37. Bus-Powered Configuration for High-Performance Application

NOTE:

The circuit illustrated above is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.

PCM2900 TYPICAL CIRCUIT CONNECTION 2

Figure 38 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.



NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8: 1 µF
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design
In this case analog perfomance of the A/D converter may degrade.

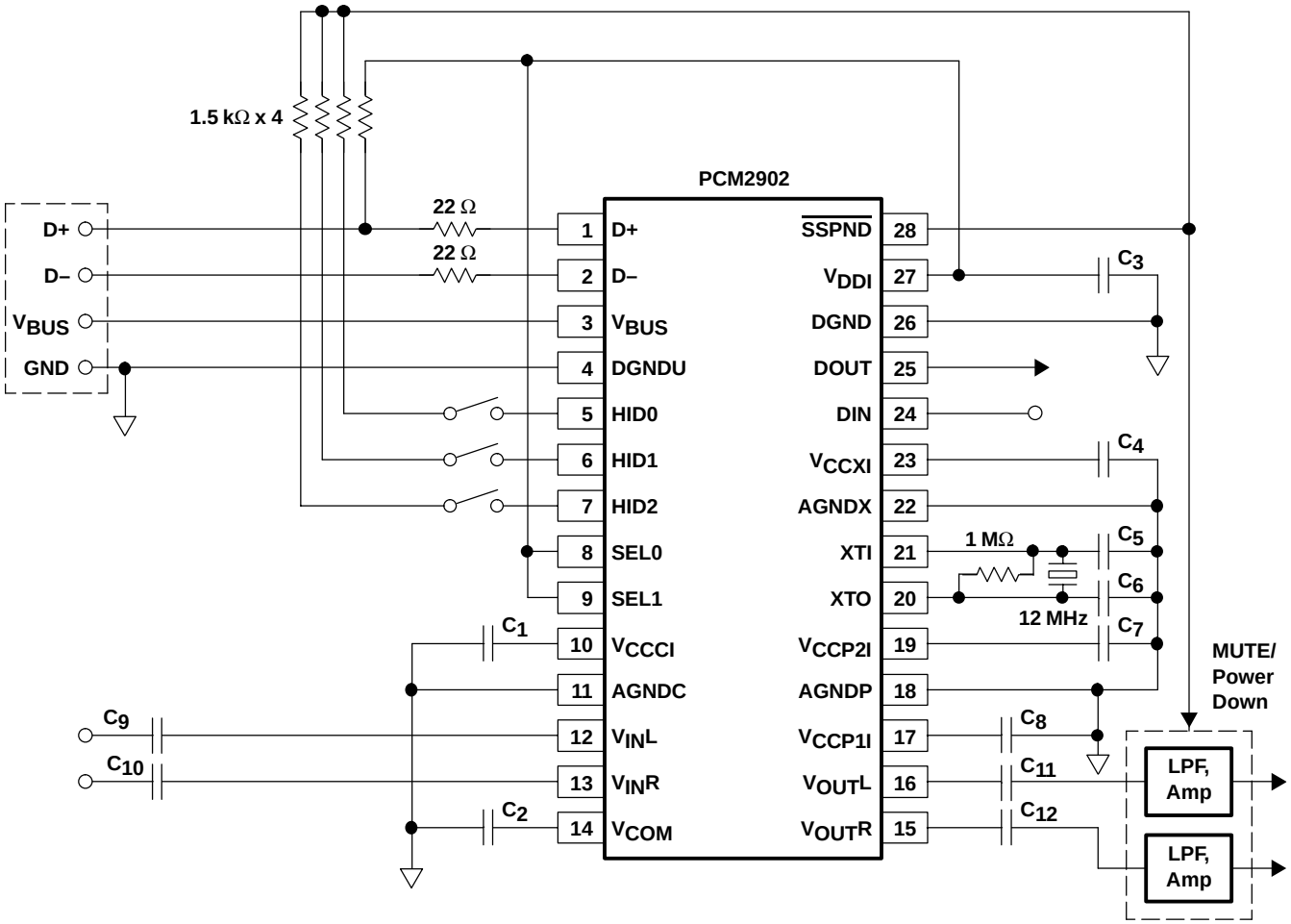
Figure 38. Bus-Powered Configuration

NOTE:

The circuit illustrated above is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.

PCM2902 TYPICAL CIRCUIT CONNECTION 2

Figure 39 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.



NOTE: C_1, C_2: 10 µF
C_3, C_4, C_7, C_8: 1 µF
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design
In this case analog perfomance of the A/D converter may degrade.

Figure 39. Bus-Powered Configuration

NOTE:

The circuit illustrated above is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.

APPLICATION INFORMATION

OPERATING ENVIRONMENT

To get the appropriate operation, one of the following operating systems must be working on the host PC that has the USB port assured by the manufacturer. If the condition is fulfilled, the operation of the PCM2900/2902 does not depend upon the operating speed of the CPU.

Texas Instruments has confirmed following operating environments.

- OS: Microsoft™ Windows™ 98/98SE/Me Japanese/English Edition
  - Microsoft™ Windows™ 2000 Professional Japanese/English Edition
  - Microsoft™ Windows™ XP Home/Professional Japanese/English Edition (For Windows™ XP, use the latest version of the USB audio driver that is available on Windows update site)
  - Apple Computer™ Mac OS 9.1 or later Japanese/English Edition
  - Apple Computer™ Mac OS X 10.0 or later English Edition
  - Apple Computer™ Mac OS X 10.1 or later Japanese Edition (For Mac OS X 10.0 Japanese Edition, plug and play does not work for USB audio device appropriately)
- PC: Following PC-AT compatible computers for above OS (OS requirement must meet)
  - Motherboard using Intel™ 440BX or ZX chip set (using USB controller in the chip set)
  - Motherboard using Intel™ i810 chip set (using USB controller in the chip set)
  - Motherboard using Intel™ i815 chip set (using USB controller in the chip set)
  - Motherboard using Intel™ i820 chip set (using USB controller in the chip set)
  - Motherboard using Intel™ i845 chip set (using USB controller in the chip set)
  - Motherboard using Intel™ i850 chip set (using USB controller in the chip set)
  - Motherboard using Apollo KT133 chip set (using USB controller in the chip set)
  - Motherboard using Apollo Pro plus chip set (using USB controller in the chip set)
  - Motherboard using MVP4 or MVP3 chip set (using USB controller in the chip set)
  - Motherboard using Aladdin V chip set (using USB controller in the chip set)
  - Motherboard using SiS530 or SiS559 chip set (using USB controller in the chip set)
  - Motherboard using SiS735 chip set (using USB controller in the chip set)

NOTE:

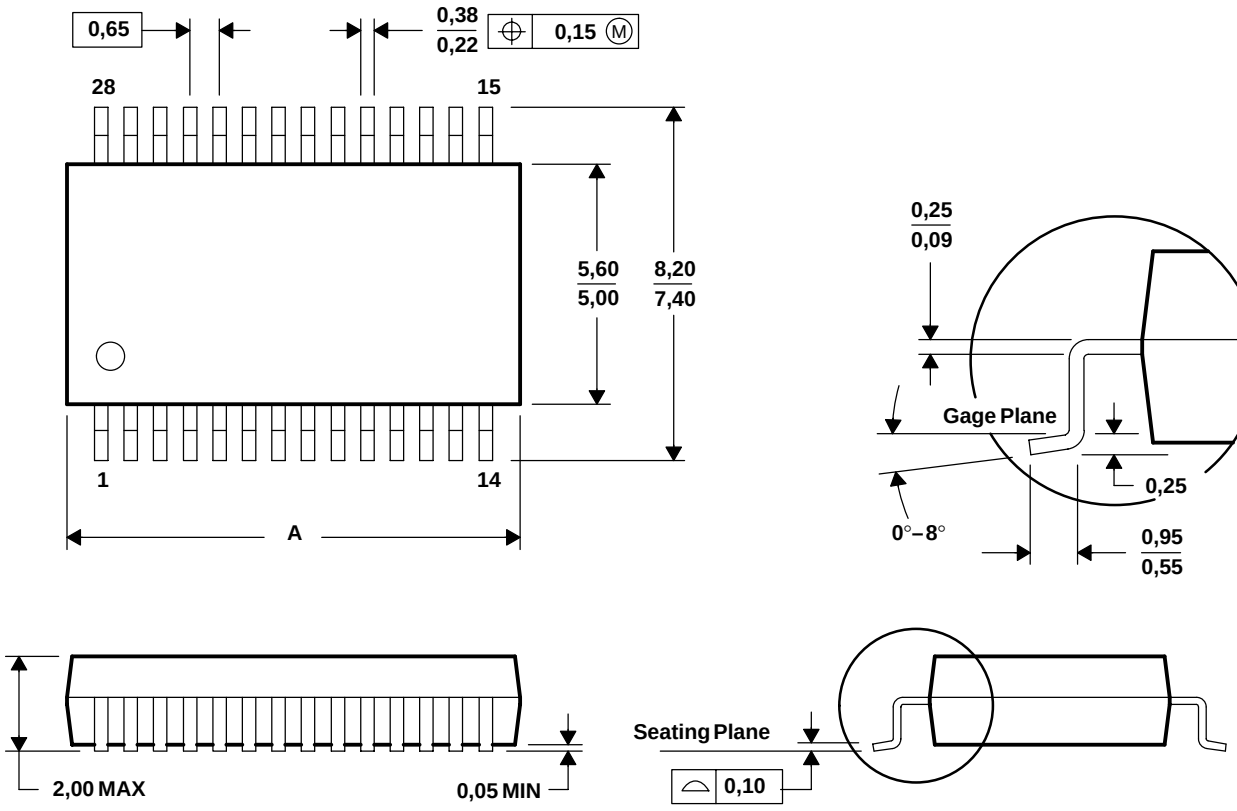
This does not mean that the operation of the PCM2900/2902 is not assured for the OS and PC except for the ones listed. The OSs and PCs for which the operation of the PCM2900/2902 was confirmed are written above.

PCM2900/2902 has been acknowledged in the USB compliance test. However, the acknowledgement is just for the PCM2900/2902 from Texas Instruments. Be careful that the acknowledgement is not for the customer's USB system using the PCM2900/2902.

MECHANICAL DATA

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065/E 12/01

NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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