HIGH-SPEED RAIL-TO-RAIL OUTPUT VIDEO AMPLIFIERS

FEATURES

- **High Speed**
  - **100 MHz Bandwidth (−3 dB, G= 2)**
  - **900 V/μs Slew Rate**
- **Excellent Video Performance**
  - **25 MHz Bandwidth (0.1 dB, G = 2)**
  - **0.007% Differential Gain**
  - **0.007° Differential Phase**
- **Rail-to-Rail Output Swing**
  - **V_O = −4.5 / 4.5 (R_L = 150 Ω)**
- **High Output Drive, I_O = 100 mA (typ)**
- **Ultralow Distortion**
  - **HD2 = −78 dBc (f = 5 MHz, R_L = 150Ω)**
  - **HD3 = −85 dBc (f = 5 MHz, R_L = 150Ω)**
- **Wide Range of Power Supplies**
  - **V_S = 3 V to 15 V**

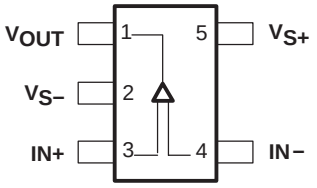
APPLICATIONS

- **Video Line Driver**
- **Imaging**
- **DVD / CD ROM**
- **Active Filtering**
- **General Purpose Signal Chain Conditioning**

DESCRIPTION

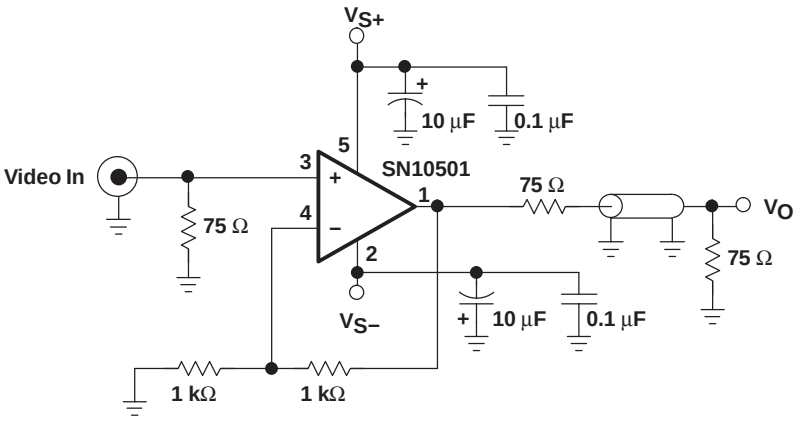
The SN10501 family is a set of rail-to-rail output single, dual, and triple low-voltage, high-output swing, low-distortion high-speed amplifiers ideal for driving data converters, video switching, or low distortion applications. This family of voltage feedback amplifiers can operate from a single 15-V power supply down to a single 3-V power supply while consuming only 14 mA of quiescent current per channel. In addition, the family offers excellent ac performance with 100-MHz bandwidth, 900-V/μs slew rate and harmonic distortion (THD) at –78 dBc at 5 MHz.

SN10501
DBV PACKAGE
(TOP VIEW)

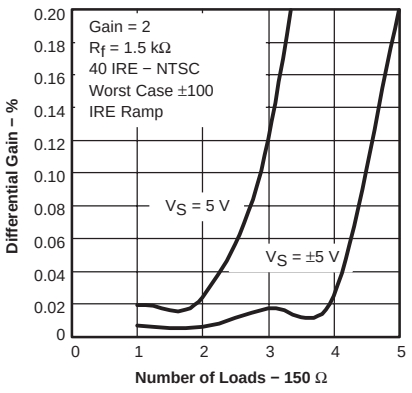


DEVICE	DESCRIPTION
SN10501	Single
SN10502	Dual
SN10503	Triple

VIDEO DRIVE CIRCUIT



DIFFERENTIAL GAIN
vs
NUMBER OF LOADS



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Supply voltage, V_S	16.5 V
Input voltage, V_I	$\pm V_S$
Output current, I_O (2)	150 mA
Differential input voltage, V_{ID}	4 V
Continuous power dissipation	See Dissipation Rating Table
Maximum junction temperature, T_J	150°C
Operating free-air temperature range, T_A	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The SN1050x may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ_{JC} (°C/W)	Θ_{JA} (°C/W)	POWER RATING	
			$T_A \le$ 25°C	$T_A =$ 85°C
DBV (5)	55	324.1	385 mW	201 mW
D (8)	38.3	176	710 mW	370 mW
D (14)	26.9	122.6	1.02 W	530 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, (V_{S+} and V_{S-})	Dual supply	±1.35	±7.5	V
	Single supply	2.7	15	
Input common-mode voltage range		V_{S-} + 1.1	V_{S+} − 1.1	V

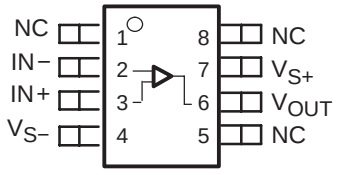
PACKAGE/ORDERING INFORMATION

TEMPERATURE	PACKAGED DEVICES			PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
	SINGLE ORDERABLE	DUAL ORDERABLE	TRIPLE ORDERABLE		
−40°C to 85°C	SN10501D	SN10502D	SN10503D	SOIC	Rails, 75
	SN10501DR	SN10502DR	SN10503DR	SOIC	Tape and Reel, 2500
	SN10501DBVR	−−−	−−−	SOT23−5	Tape and Reel, 3000
	SN10501DBVT	−−−	−−−	SOT23−5	Tape and Reel, 250

PIN ASSIGNMENTS

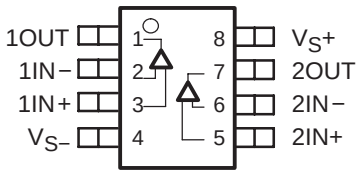
PACKAGE DEVICES

SN10501
D PACKAGE
(TOP VIEW)

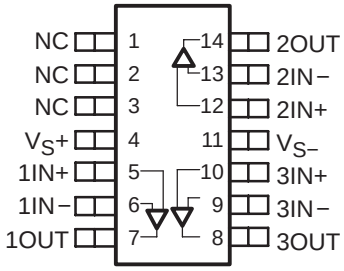


NC − No internal connection

SN10502
D PACKAGE
(TOP VIEW)



SN10503
D PACKAGE
(TOP VIEW)



NC − No internal connection

ELECTRICAL CHARACTERISTICS

V_S = ±5 V, R_L = 150 Ω, and G = 2 unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	−40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small signal bandwidth	G = 1, V_O = 100 mV_{PP}	170				MHz	Typ
	G = 2, V_O = 100 mV_{PP}, R_f = 1 kΩ	100				MHz	Typ
	G = 10, V_O = 100 mV_{PP}, R_f = 1 kΩ	12				MHz	Typ
0.1 dB flat bandwidth	G = 2, V_O = 100 mV_{PP}, R_f = 1 kΩ	25				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz, R_f = 1 kΩ	120				MHz	Typ
Full-power bandwidth(1)	G = 2, V_O = ±2.5 Vpp	57				MHz	Typ
Slew rate	G = 2, V_O = ±2.5 Vpp	900				V/µs	Min
Settling time to 0.1%	G = −2, V_O = ±2 Vpp	25				ns	Typ
Settling time to 0.01%	G = −2, V_O = ±2 Vpp	52				ns	Typ
Harmonic distortion	G = 2, V_O = 2 V_{PP}, f = 5 MHz						
Second harmonic distortion	R_L = 150 Ω	−78				dBc	Typ
Third harmonic distortion	R_L = 150 Ω	−85				dBc	Typ
Differential gain (NTSC, PAL)	G = 2, R = 150 Ω	0.007				%	Typ
Differential phase (NTSC, PAL)	G = 2, R = 150 Ω	0.007				°	Typ
Input voltage noise	f = 1 MHz	13				nV/√Hz	Typ
Input current noise	f = 1 MHz	0.8				pA/√Hz	Typ
Crosstalk (dual and triple only)	f = 5 MHz Ch-to-Ch	−90				dB	Typ

(1) Full-power bandwidth = SR / 2πVpp

DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = ±2 V	100	80	75	75	dB	Min
Input offset voltage	V_{CM} = 0 V	12	25	30	30	mV	Max
Input bias current	V_{CM} = 0 V	0.9	3	5	5	µA	Max
Input offset current	V_{CM} = 0 V	100	500	700	700	nA	Max
INPUT CHARACTERISTICS							
Common-mode input range		−4 / 4	−3.9 / 3.9			V	Min
Common-mode rejection ratio	V_{CM} = ±2 V	94	70	65	65	dB	Min
Input resistance		33				MΩ	Typ
Input capacitance	Common-mode / differential	1 / 0.5				pF	Max
OUTPUT CHARACTERISTICS							
Output voltage swing	R_L = 150 Ω	−4.5 / 4.5				V	Typ
	R_L = 499 Ω	−4.7 / 4.7	−4.5 / 4.5	−4.4 / 4.4	−4.4 / 4.4	V	Min
Output current (sourcing)	R_L = 10 Ω	100	92	88	88	mA	Min
Output current (sinking)	R_L = 10 Ω	−100	−92	−88	−88	mA	Min
Output impedance	f = 1 MHz	0.02				Ω	Typ
POWER SUPPLY							
Specified operating voltage		±5	±7.5	±7.5	±7.5	V	Max
Maximum quiescent current	Per channel	14	18	20	22	mA	Max
Power supply rejection (±PSRR)		75	62	60	60	dB	Min

ELECTRICAL CHARACTERISTICS

V_S = 5 V, R_L = 150 Ω, and G = 2 unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	−40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE							
Small signal bandwidth	G = 1, V_O = 100 mV_{PP}	170				MHz	Typ
	G = 2, V_O = 100 mV_{PP}, R_f = 1.5 kΩ	100				MHz	Typ
	G = 10, V_O = 100 mV_{PP}, R_f = 1.5 kΩ	12				MHz	Typ
0.1 dB flat bandwidth	G = 2, V_O = 100 mV_{PP}, R_f = 1.5 kΩ	10				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz, R_f = 1.5 kΩ	120				MHz	Typ
Full-power bandwidth(1)	G = 2, V_O = 4 V step	60				MHz	Typ
Slew rate	G = 2, V_O = 4 V step	750				V/µs	Min
Settling time to 0.1%	G = −2, V_O = 2 V step	27				ns	Typ
Settling time to 0.01%	G = −2, V_O = 2 Vpp	48				ns	Typ
Harmonic distortion	G = 2, V_O = 2 V_{PP}, f = 5 MHz						
Second harmonic distortion	R_L = 150 Ω	−82				dBc	Typ
Third harmonic distortion	R_L = 150 Ω	−88				dBc	Typ
Differential gain (NTSC, PAL)	G = 2, R = 150 Ω	0.014				%	Typ
Differential phase (NTSC, PAL)	G = 2, R = 150 Ω	0.011				°	Typ
Input voltage noise	f = 1 MHz	13				nV/√Hz	Typ
Input current noise	f = 1 MHz	0.8				pA/√Hz	Typ
Crosstalk (dual and triple only)	f = 5 MHz Ch-to-Ch	−90				dB	Typ

(1) Full-power bandwidth = SR / 2πVpp

DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = 1.5 V to 3.5 V	100	80	75	75	dB	Min
Input offset voltage	V_{CM} = 2.5 V	12	25	30	30	mV	Max
Input bias current	V_{CM} = 2.5 V	0.9	3	5	5	µA	Max
Input offset current	V_{CM} = 2.5 V	100	500	700	700	nA	Max
INPUT CHARACTERISTICS							
Common-mode input range		1 / 4	1.1 / 3.9			V	Min
Common-mode rejection ratio	V_{CM} = 1.5 V to 3.5 V	96	70	65	65	dB	Min
Input resistance		33				MΩ	Typ
Input capacitance	Common-mode / differential	1 / 0.5				pF	Max
OUTPUT CHARACTERISTICS							
Output voltage swing	R_L = 150 Ω	0.5 / 4.5				V	Typ
	R_L = 499 Ω	0.2 / 4.8	0.3 / 4.7	0.4 / 4.6	0.4 / 4.6	V	Min
Output current (sourcing)	R_L = 10 Ω	95	85	80	80	mA	Min
Output current (sinking)	R_L = 10 Ω	−95	−85	−80	−80	mA	Min
Output impedance	f = 1 MHz	0.02				Ω	Typ
POWER SUPPLY							
Specified operating voltage		5	15	15	15	V	Max
Maximum quiescent current	Per channel	12	15	17	19	mA	Max
Power supply rejection (±PSRR)		70	62	60	60	dB	Min

TYPICAL CHARACTERISTICS

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Large signal frequency response	3
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Harmonic distortion vs Frequency	6, 7
Voltage and current noise vs Frequency	8
Differential gain vs Number of loads	9, 11
Differential phase vs Number of loads	10, 12
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Rejection ratio vs Frequency	16
Rejection ratio vs Case temperature	17
Common-mode rejection ratio vs Input common-mode range	18, 19
Crosstalk vs Frequency	20
Input bias and offset current vs Case temperature	21, 22

SMALL SIGNAL FREQUENCY RESPONSE

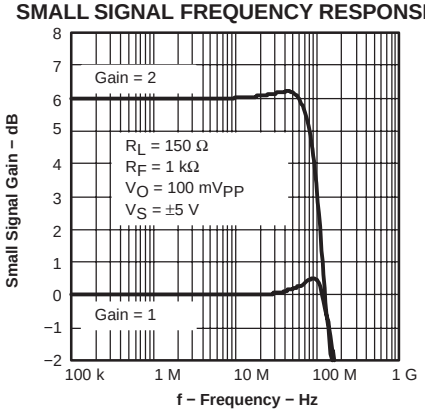


Figure 1

SMALL SIGNAL FREQUENCY RESPONSE

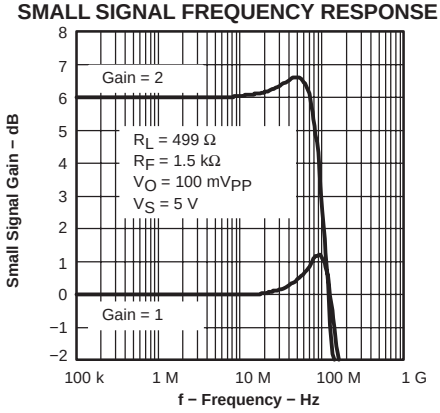


Figure 2

LARGE SIGNAL FREQUENCY RESPONSE

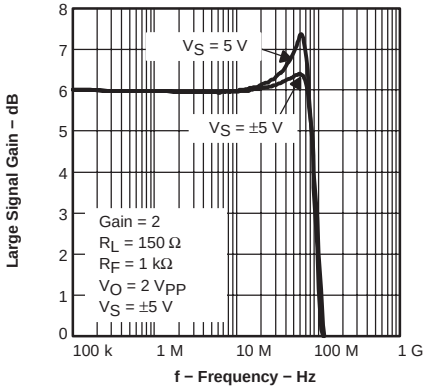


Figure 3

SLEW RATE vs OUTPUT VOLTAGE STEP

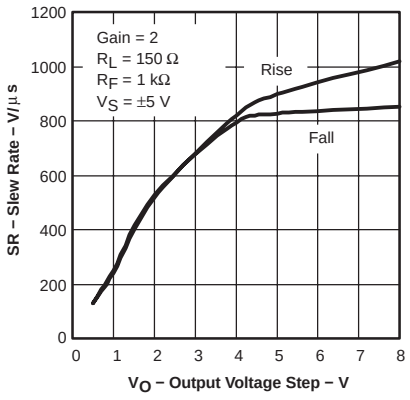


Figure 4

SLEW RATE vs OUTPUT VOLTAGE STEP

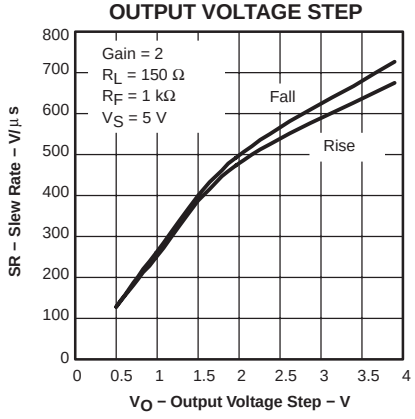


Figure 5

HARMONIC DISTORTION vs FREQUENCY

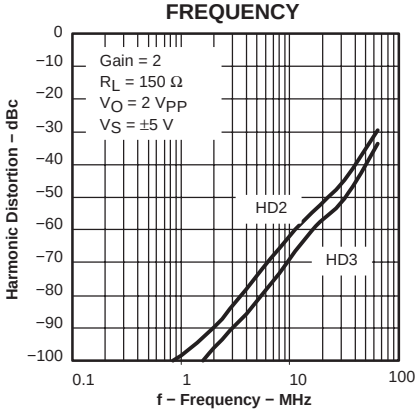


Figure 6

HARMONIC DISTORTION vs FREQUENCY

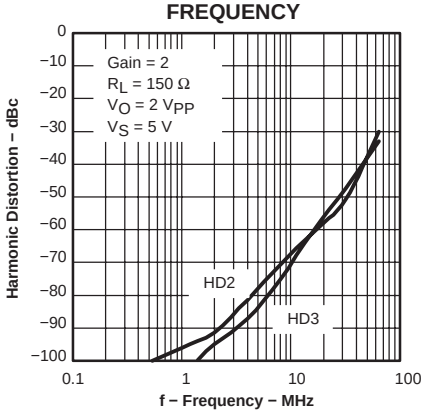


Figure 7

VOLTAGE AND CURRENT NOISE vs FREQUENCY

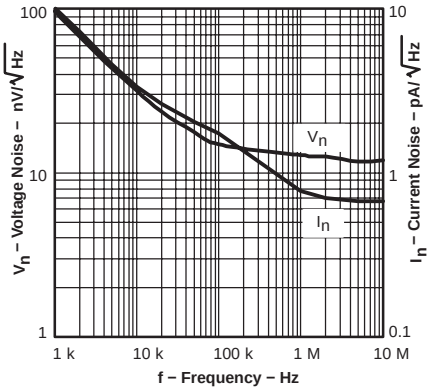


Figure 8

DIFFERENTIAL GAIN vs NUMBER OF LOADS

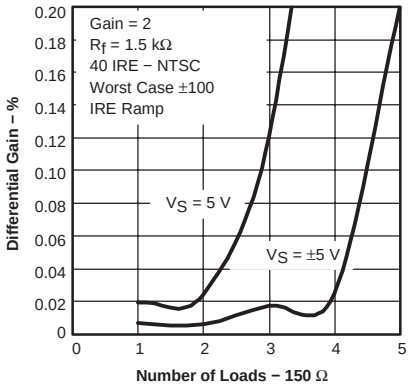


Figure 9

DIFFERENTIAL PHASE vs NUMBER OF LOADS

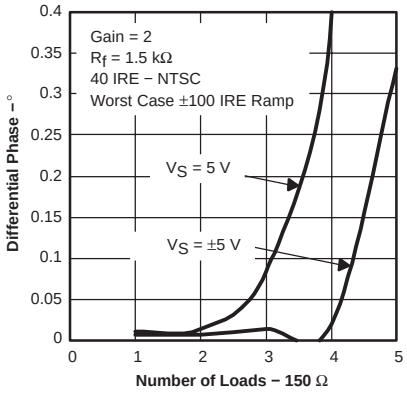


Figure 10

DIFFERENTIAL GAIN vs NUMBER OF LOADS

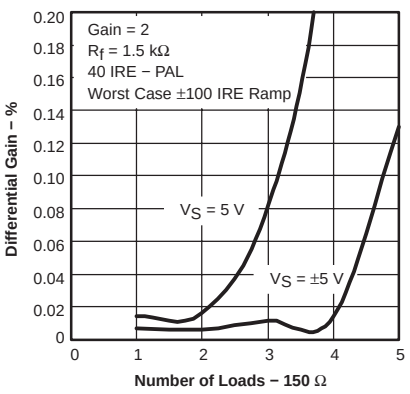


Figure 11

DIFFERENTIAL PHASE vs NUMBER OF LOADS

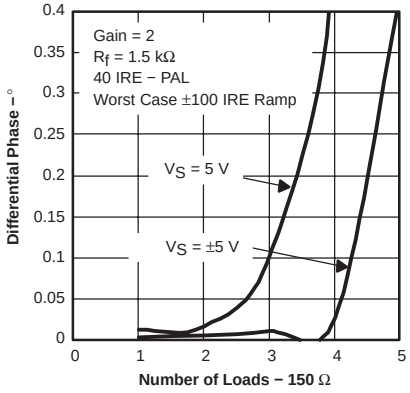


Figure 12

QUIESCENT CURRENT vs SUPPLY VOLTAGE

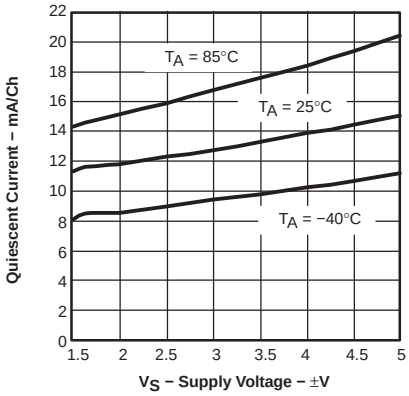


Figure 13

OUTPUT VOLTAGE vs LOAD RESISTANCE

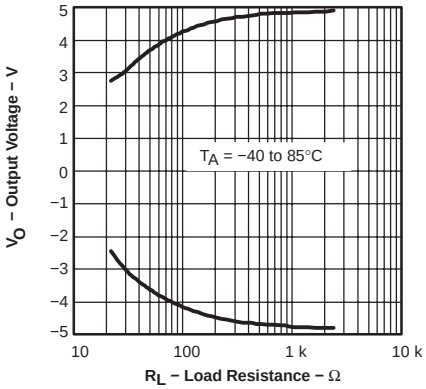


Figure 14

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

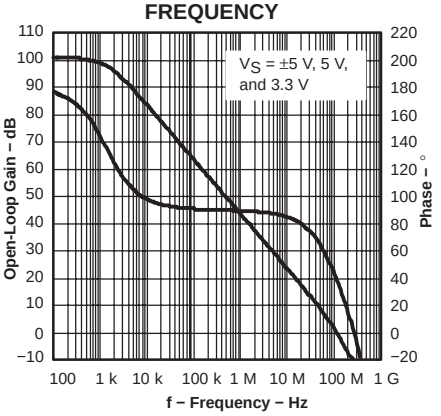


Figure 15

REJECTION RATIO vs FREQUENCY

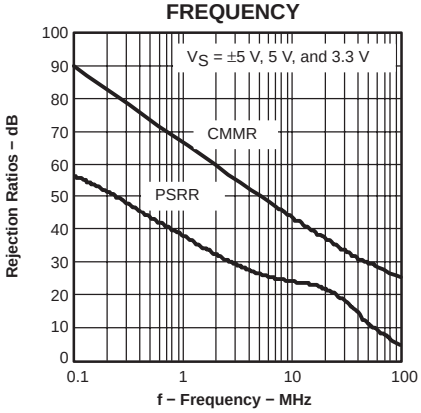


Figure 16

REJECTION RATIO vs CASE TEMPERATURE

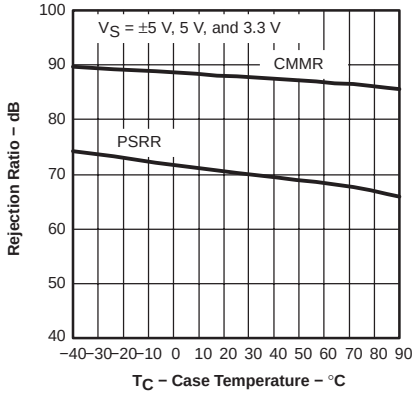


Figure 17

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

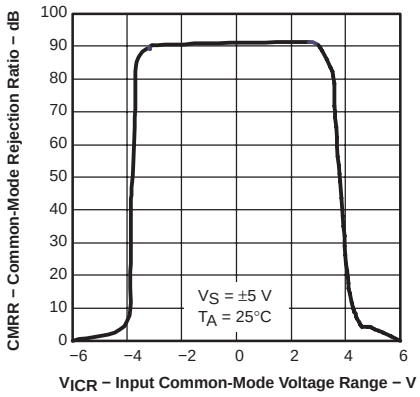


Figure 18

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

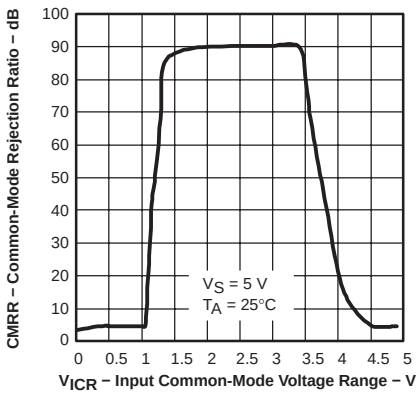


Figure 19

CROSSTALK vs FREQUENCY

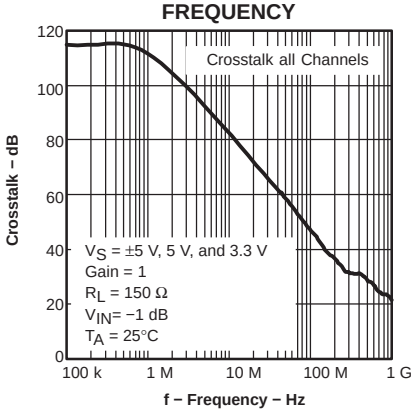


Figure 20

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

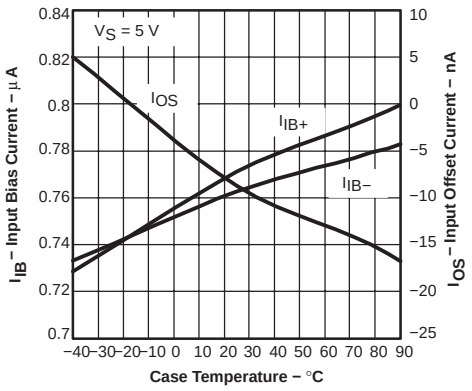


Figure 21

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

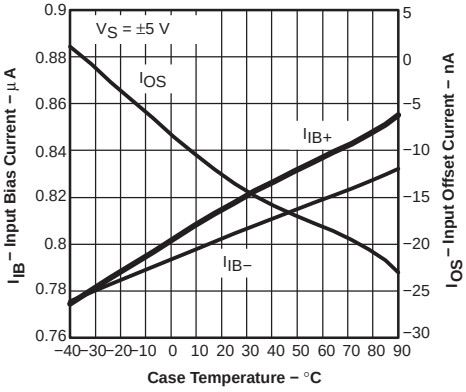


Figure 22

APPLICATION INFORMATION

HIGH-SPEED OPERATIONAL AMPLIFIERS

The SN10501 operational amplifiers are a family of single, dual, and triple rail-to-rail output voltage feedback amplifiers. The SN10501 family combines both a high slew rate and a rail-to-rail output stage.

Applications Section Contents

- Wideband, Noninverting Operation
- Wideband, Inverting Gain Operation
- Video Drive Circuits
- Single Supply Operation
- Power Supply Decoupling Techniques and Recommendations
- Active Filtering With the SN10501
- Driving Capacitive Loads
- Board Layout
- Thermal Analysis
- Additional Reference Material
- Mechanical Package Drawings

WIDEBAND, NONINVERTING OPERATION

The SN10501 is a family of unity gain stable rail-to-rail output voltage feedback operational amplifiers designed to operate from a single 3-V to 15-V power supply.

Figure 23 is the noninverting gain configuration of 2 V/V used to demonstrate the typical performance curves.

Voltage feedback amplifiers, unlike current feedback designs, can use a wide range of resistors values to set their gain with minimal impact on their stability and frequency response. Larger-valued resistors decrease the loading effect of the feedback network on the output of the amplifier, but this enhancement comes at the expense of additional noise and potentially lower bandwidth. Feedback resistor values between 1 kΩ and 2 kΩ are recommended for most situations.

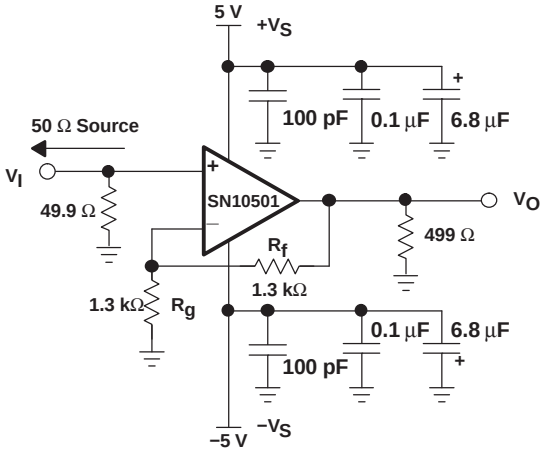


Figure 23. Wideband, Noninverting Gain Configuration

WIDEBAND, INVERTING OPERATION

Since the SN10501 family are general-purpose, wideband voltage-feedback amplifiers, several familiar operational amplifier applications circuits are available to the designer. Figure 24 shows a typical inverting configuration where the input and output impedances and noise gain from Figure 23 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. The inverting configuration shows improved slew rates and distortion due to the pseudo-static voltage maintained on the inverting input.

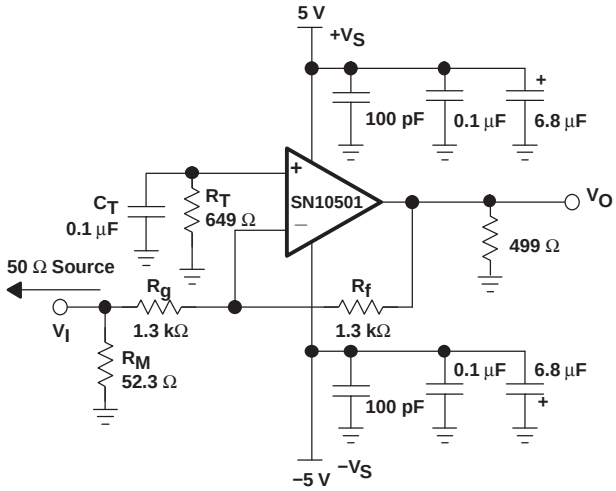


Figure 24. Wideband, Inverting Gain Configuration

In the inverting configuration, some key design considerations must be noted. One is that the gain resistor (R_g) becomes part of the signal channel input impedance. If the input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace, or other transmission line conductors), R_g may be set equal to the required termination value and R_f adjusted to give the desired gain. However, care must be taken when dealing with low inverting gains, as the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_g to 49.9 Ω for input matching eliminates the need for R_M but requires a 100-Ω feedback resistor. This has an advantage of the noise gain becoming equal to 2 for a 50-Ω source impedance—the same as the noninverting circuit in Figure 23. However, the amplifier output now sees the 100-Ω feedback resistor in parallel with the external load. To eliminate this excessive loading, it is preferable to increase both R_g and R_f, values, as shown in Figure 24, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_g and R_M.

The last major consideration to discuss in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input. If the resistance is set equal to the total dc resistance looking out of the inverting terminal, the output dc error, due to the input bias currents, is reduced to (input offset current) multiplied by R_f in Figure 24, the dc source impedance looking out of the inverting terminal is 1.3 kΩ || (1.3 kΩ + 25.6 Ω) = 649 Ω. To reduce the additional high-frequency noise introduced by the resistor at the noninverting input, and power-supply feedback, R_T is bypassed with a capacitor to ground.

VIDEO DRIVE CIRCUITS

Most video distribution systems are designed with 75-Ω series resistors to drive a matched 75-Ω cable. In order to deliver a net gain of 1 to the 75-Ω matched load, the amplifier is typically set up for a voltage gain of +2, compensating for the 6-dB attenuation of the voltage divider formed by the series and shunt 75-Ω resistors at either end of the cable. The circuit shown in Figure 25 applies to this requirement. Both the gain flatness and the differential gain / phase performance of the SN10501 provides exceptional results in video distribution applications.

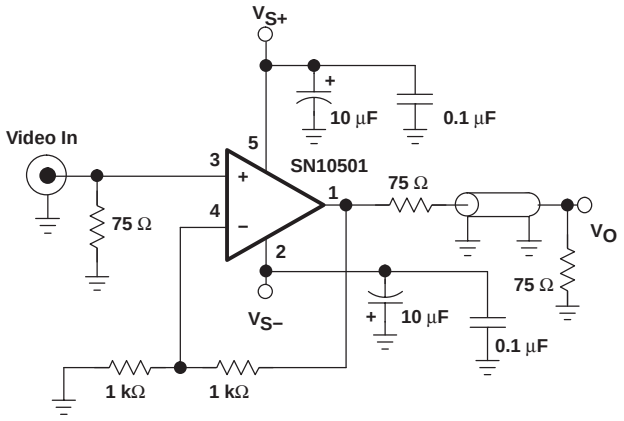


Figure 25. Cable Drive Application

Differential gain and phase measure the change in overall small-signal gain and phase for the color subcarrier frequency (3.58 MHz in NTSC systems) vs changes in the large-signal output level (which represents luminance information in a composite video signal). The SN10501, with the typical 150-Ω load of a single matched video cable, shows less than 0.007% / 0.007° differential gain/phase errors over the standard luminance range for a positive video (negative sync) signal. Similar performance is observed for negative video signals. In practice, similar performance is achieved even with three video loads as shown in Figure 26 due to the linear high-frequency output impedance of the SN10501.

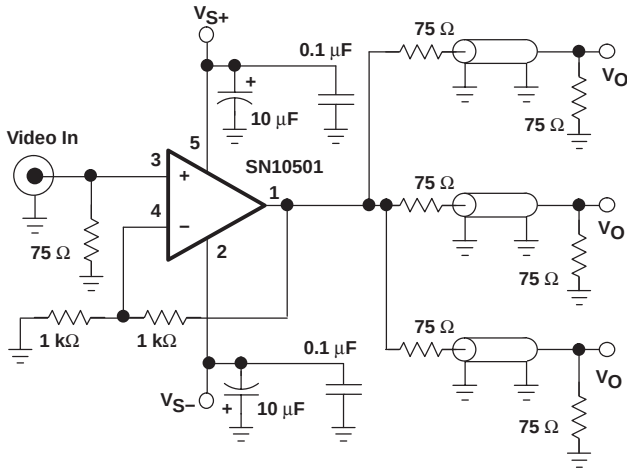


Figure 26. Video Distribution

The above circuit is suitable for driving video cables, provided that the length does not exceed a few feet. If longer cables are driven, the gain of the SN10501 can be increased to accommodate cable drops.

SINGLE SUPPLY OPERATION

The SN10501 family is designed to operate from a single 3-V to 15-V power supply. When operating from a single power supply, care must be taken to ensure the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing. The circuits shown in Figure 27 demonstrate methods to configure an amplifier in a manner conducive for single supply operation.

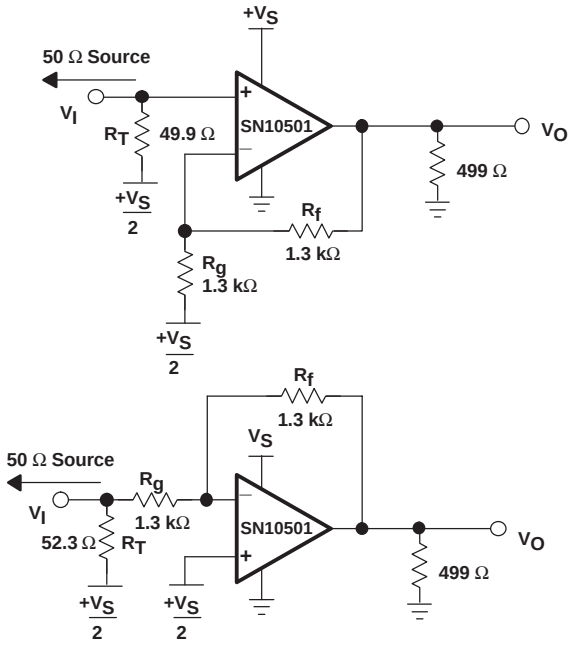


Figure 27. DC-Coupled Single Supply Operation

Power Supply Decoupling Techniques and Recommendations

Power supply decoupling is a critical aspect of any high-performance amplifier design process. Careful decoupling provides higher quality ac performance (most notably improved distortion performance). The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power supply inputs as possible, with the goal of minimizing the inductance of the path from ground to the power supply.

2. Placement priority should put the smallest valued capacitors closest to the device.

3. Use of solid power and ground planes is recommended to reduce the inductance along power supply return current paths, with the exception of the areas underneath the input and output pins.

4. Recommended values for power supply decoupling include a bulk decoupling capacitor (6.8 to 22 μF), a mid-range decoupling capacitor (0.1 μF) and a high frequency decoupling capacitor (1000 pF) for each supply. A 100 pF capacitor can be used across the supplies as well for extremely high frequency return currents, but often is not required.

APPLICATION CIRCUITS

Active Filtering With the SN10501

High-frequency active filtering with the SN10501 is achievable due to the amplifier's high slew rate, wide bandwidth, and voltage feedback architecture. Several options are available for high-pass, low-pass, bandpass, and bandstop filters of varying orders. A simple two-pole low pass filter is presented here as an example, with two poles at 25 MHz.

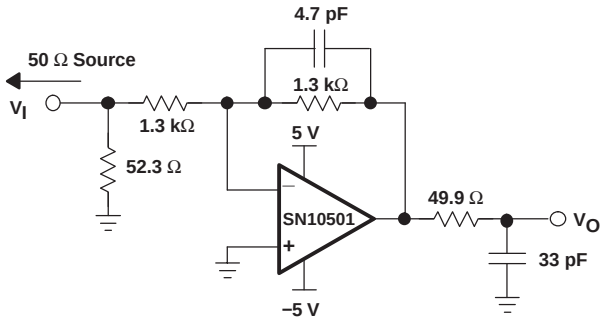


Figure 28. A Two-Pole Active Filter With Two Poles Between 90 MHz and 100 MHz

Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter, including additional external capacitance, which may be recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the SN10501 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. When the primary considerations are frequency response flatness, pulse response fidelity, or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

BOARD LAYOUT

Achieving optimum performance with a high frequency amplifier like the SN10501 requires careful attention to board layout parasitics and external component types.

Recommendations that will optimize performance include:

1. **Minimize parasitic capacitance to any ac ground for all of the signal I/O pins.** Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
2. **Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1-μF decoupling capacitors.** At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (2.2-μF to 6.8-μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserves the high frequency performance of the SN10501.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wire wound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero below 400 MHz that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations. It has been suggested that a good starting point for design is to set the R_f to 1.3 kΩ for low-gain, noninverting applications. Doing this automatically keeps the resistor noise terms low, and minimizes the effect of their parasitic capacitance.
4. **Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs Capacitive Load. Low parasitic capacitive loads (<4 pF) may not need an $R_{(ISO)}$, since the SN10501 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an $R_{(ISO)}$ are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the SN10501 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of $R_{(ISO)}$ vs Capacitive Load. This setting does not preserve signal integrity or a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

5. **Socketing a high speed part like the SN10501 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the SN10501 onto the board.

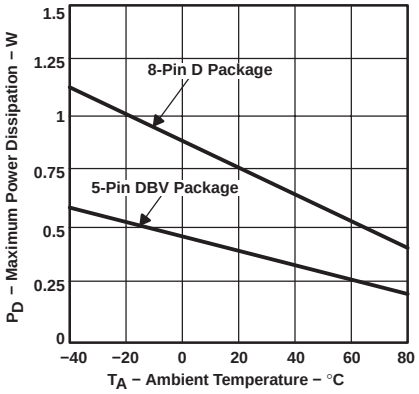
THERMAL ANALYSIS

The SN10501 family of devices does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150° C is exceeded.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:
P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).



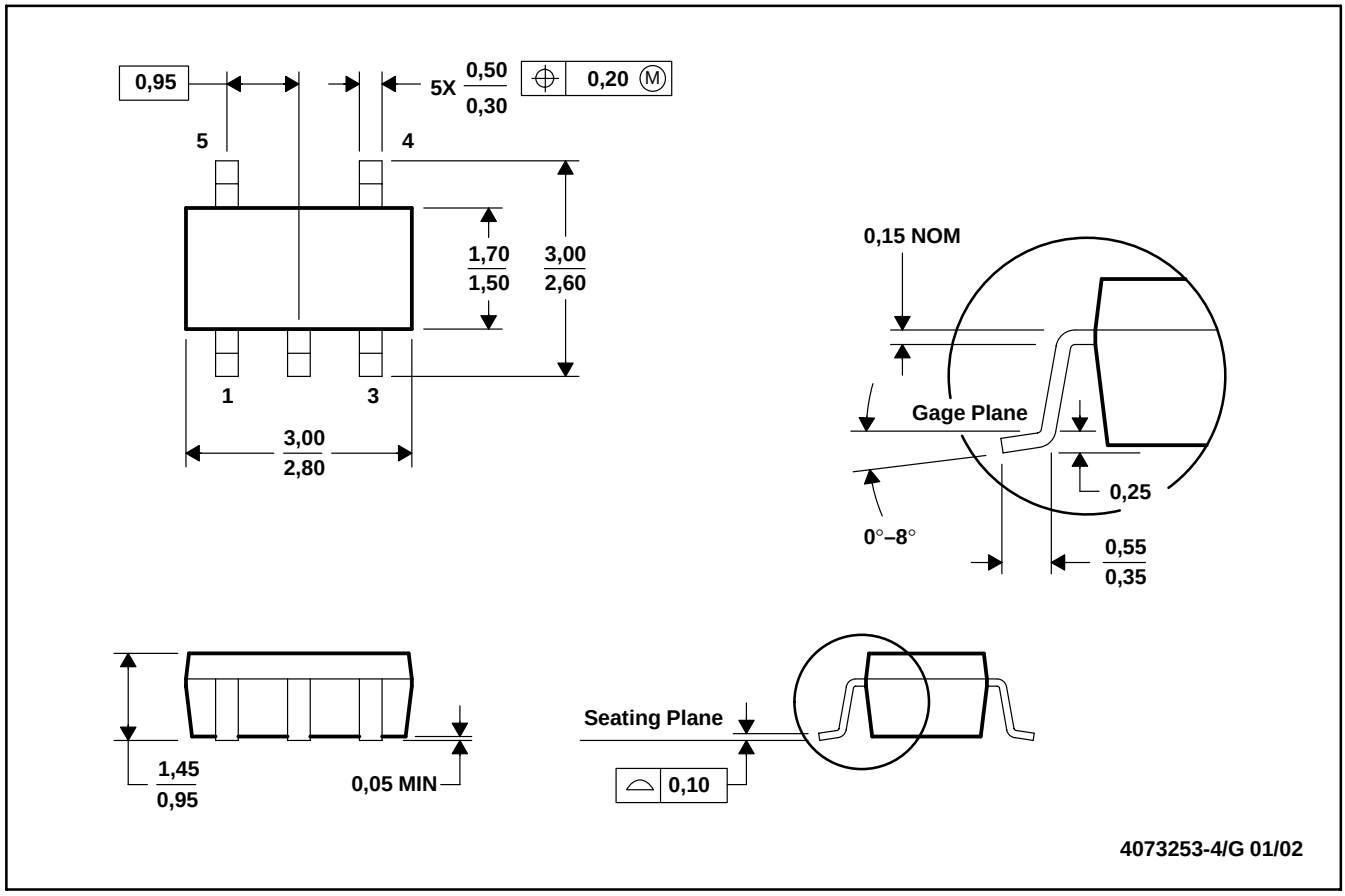
θ_{JA} = 170°C/W for 8-Pin SOIC (D)
θ_{JA} = 324.1°C/W for 5-Pin SOT−23 (DBV)
T_J = 150°C, No Airflow

Figure 29. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

MPDS018E – FEBRUARY 1996 – REVISED FEBRUARY 2002

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



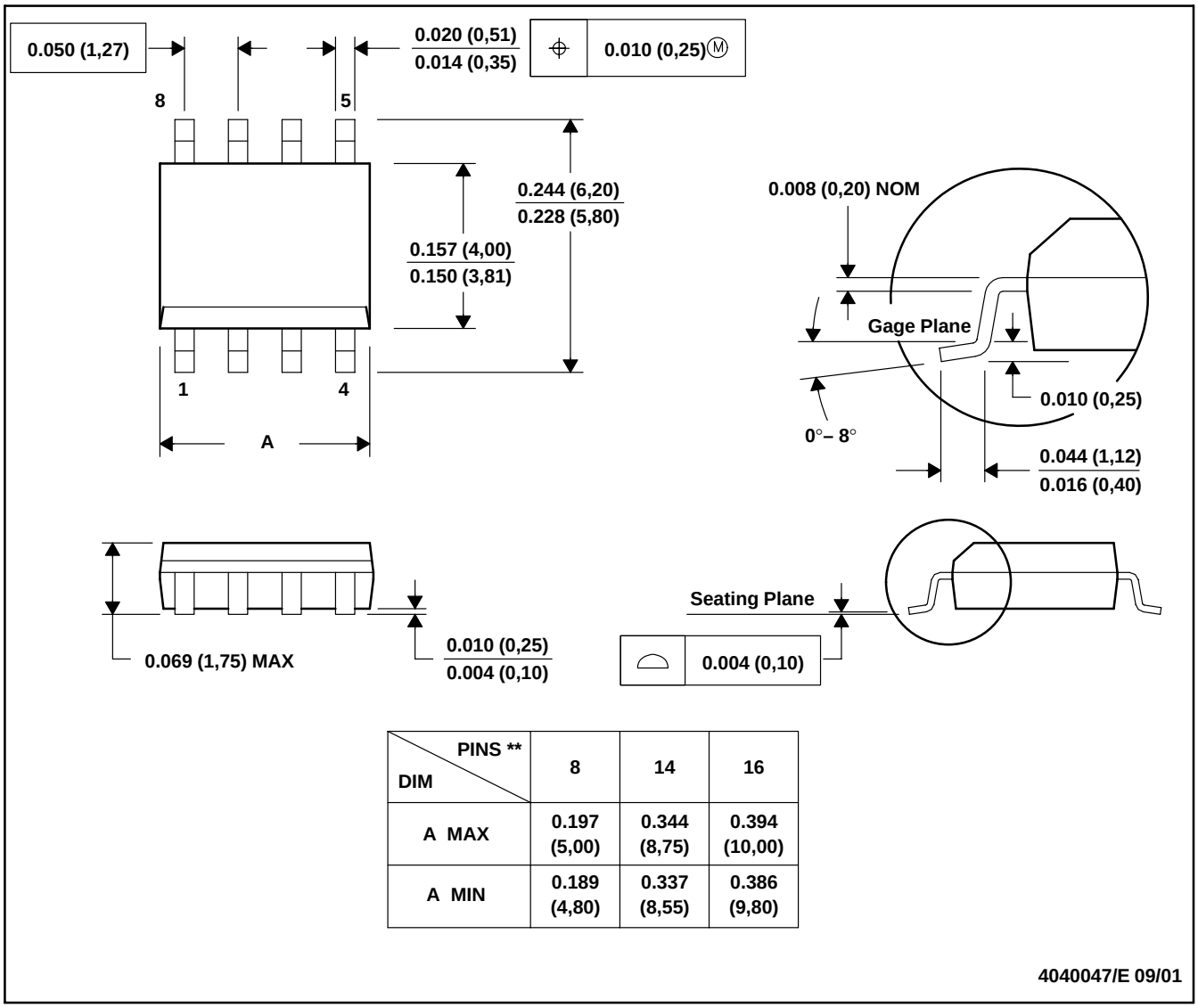
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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