OPA657

SBOS197 – DECEMBER 2001

1.6GHz, Low-Noise, FET-Input OPERATIONAL AMPLIFIER

FEATURES

- HIGH GAIN BANDWIDTH PRODUCT: 1.6GHz
- HIGH BANDWIDTH 275MHz (G = +10)
- LOW INPUT OFFSET VOLTAGE: ±0.25mV
- LOW INPUT BIAS CURRENT: 2pA
- LOW INPUT VOLTAGE NOISE: 4.8nV/$\sqrt{Hz}$
- HIGH OUTPUT CURRENT: 70mA
- FAST OVERDRIVE RECOVERY

APPLICATIONS

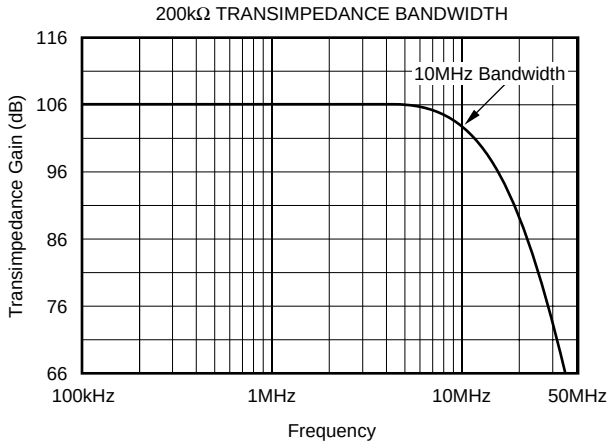
- WIDEBAND PHOTODIODE AMPLIFIER
- WAFER SCANNING EQUIPMENT
- ADC INPUT AMPLIFIER
- TEST AND MEASUREMENT FRONT END
- HIGH GAIN PRECISION AMPLIFIER

DESCRIPTION

The OPA657 combines a high gain bandwidth, low distor-tion, voltage-feedback op amp with a low voltage noise JFET-input stage to offer a very high dynamic range amplifier for high precision ADC (Analog-to-Digital Converter) driving or wideband transimpedance applications. Photodiode applications will see improved noise and bandwidth using this decompensated, high gain bandwidth amplifier.

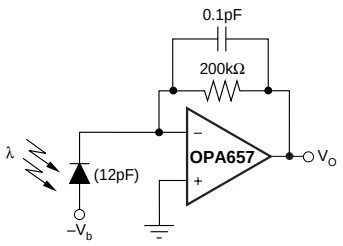
Very low level signals can be significantly amplified in a single OPA657 gain stage with exceptional bandwidth and accuracy. Having a high 1.6GHz gain bandwidth product will give > 10MHz signal bandwidths up to gains of 160V/V (44dB). The very low input bias current and capacitance will support this performance even for relatively high source impedances.

Broadband photodetector applications will benefit from the low voltage noise JFET inputs for the OPA657. The JFET input contributes virtually no current noise while for broadband applications, a low voltage noise is also required. The low 4.8nV/ $\sqrt{Hz}$ input voltage noise will provide exceptional input sensitivity for higher bandwidth applications. The example shown below will give a total equivalent input noise current of 1.8pA/ $\sqrt{Hz}$ over a 10MHz bandwidth.



RELATED OPERATIONAL AMPLIFIER PRODUCTS

DEVICE	V_S (V)	BW (MHz)	SLEW RATE (V/µS)	VOLTAGE NOISE (nV/$\sqrt{Hz}$)	AMPLIFIER DESCRIPTION
OPA355	+5	200	300	5.80	Unity-Gain Stable CMOS
OPA655	±5	400	290	6	Unity-Gain Stable FET-Input
OPA656	±5	500	170	7	Unity-Gain Stable FET-Input
OPA627	±15	16	55	4.5	Unity-Gain Stable FET-Input
THS4601	±15	180	100	5.4	Unity-Gain Stable FET-Input



Wideband Photodiode Transimpedance Amplifier

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[2]	TRANSPORT MEDIA, QUANTITY
OPA657U	SO-8 Surface Mount	D	–40°C to +85°C	OPA657U	OPA657U	Rails, 100
"	"	"	"	"	OPA657U/2K5	Tape and Reel, 2500
OPA657UB	SO-8 Surface Mount	D	–40°C to +85°C	OPA657UB	OPA657UB	Rails, 100
"	"	"	"	"	OPA657UB/2K5	Tape and Reel, 2500
OPA657N	SOT23-5	DBV	–40°C to +85°C	A57	OPA657N/250	Tape and Reel, 250
"	"	"	"	"	OPA657N/3K	Tape and Reel, 3000
OPA657NB	SOT23-5	DBV	–40°C to +85°C	A57	OPA657NB/250	Tape and Reel, 250
"	"	"	"	"	OPA657NB/3K	Tape and Reel, 3000

NOTES: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±6.5V
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	$\pm V_S$
Input Voltage Range	$\pm V_S$
Storage Temperature Range	–40°C to +125°C
Lead Temperature	+260°C
Junction Temperature (T_J)	+175°C
ESD Rating (Human Body Model)	2000V
(Machine Model)	200V

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

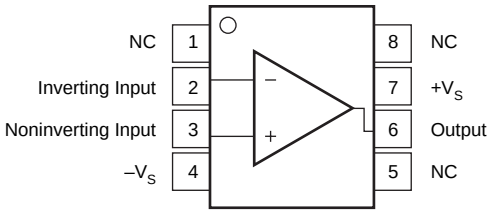
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

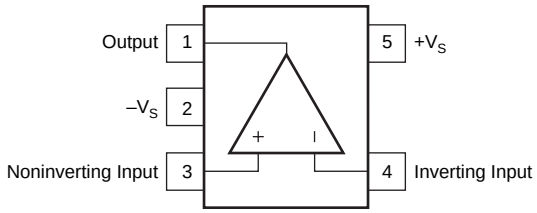
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

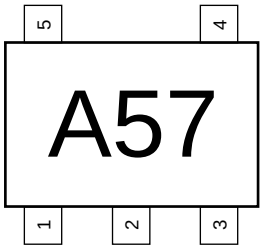
PIN CONFIGURATIONS

Top View **SO-8**



Top View **SOT23-5**





Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

$R_F = 453\Omega$, $R_L = 100\Omega$, and G = +10, unless otherwise noted. Figure 1 for AC performance.

PARAMETER	CONDITIONS	OPA657U, N (Standard-Grade)						TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	
AC PERFORMANCE (Figure 1)								
Small-Signal Bandwidth	G = +7, V_O = 200mVp-p	350				MHz	Typ	C
	G = +10, V_O = 200mVp-p	275				MHz	Typ	C
	G = +20, V_O = 200mVp-p	90				MHz	Typ	C
Gain-Bandwidth Product	G > +40	1600				MHz	Typ	C
Bandwidth for 0.1dB flatness	G = +10, 2Vp-p	30				MHz	Typ	C
Peaking at a Gain of +7		7				dB	Typ	C
Large-Signal Bandwidth	G = +10, 2Vp-p	180				MHz	Typ	C
Slew Rate	G = +10, 1V Step	700				V/µs	Typ	C
Rise-and-Fall Time	0.2V Step	1				ns	Typ	C
Settling Time to 0.02%	G = +10, V_O = 2V Step	20				ns	Typ	C
Harmonic Distortion	G = +10, f = 5MHz, V_O = 2Vp-p							C
2nd-Harmonic	$R_L = 200\Omega$	–70				dBc	Typ	C
	$R_L > 500\Omega$	–74				dBc	Typ	C
3rd-Harmonic	$R_L = 200\Omega$	–99				dBc	Typ	C
	$R_L > 500\Omega$	–106				dBc	Typ	C
Input Voltage Noise	f > 100kHz	4.8				nV/√Hz	Typ	C
Input Current Noise	f > 100kHz	1.3				fA/√Hz	Typ	**C**
DC PERFORMANCE(4)								
Open-Loop Voltage Gain (A_{OL})	V_{CM} = 0V, $R_L = 100\Omega$	70	**65**	64	63	dB	Min	A
Input Offset Voltage	V_{CM} = 0V	±0.25	**±1.8**	±2.2	±2.6	mV	Max	A
Average Offset Voltage Drift	V_{CM} = 0V	±2	**±12**	±12	±12	µV/°C	Max	A
Input Bias Current	V_{CM} = 0V	±2	**±20**	±1800	±5000	pA	Max	A
Input Offset Current	V_{CM} = 0V	±1	**±10**	±900	±2500	pA	Max	A
INPUT								
Most Positive Input Voltage(5)		+2.5	**+2.0**	+1.9	+1.8	V	Min	A
Most Negative Input Voltage(5)		–4.0	**–3.5**	–3.4	–3.3	V	Min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±0.5V	89	**83**	81	79	dB	Min	A
Input Impedance								
Differential		10^{12} || 0.7				Ω || pF	Typ	C
Common-Mode		10^{12} || 4.5				Ω || pF	Typ	C
OUTPUT								
Voltage Output Swing	No Load	±3.9	±3.7			V	Typ	B
	$R_L = 100\Omega$	±3.5	**±3.3**	±3.2	±3.1	V	Min	A
Current Output, Sourcing		+70	**+56**	+54	+50	mA	Min	A
Current Output, Sinking		–70	**–56**	–54	–50	mA	Min	A
Closed-Loop Output Impedance	G = +10, f = 0.1MHz	0.02				Ω	Typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	Typ	A
Maximum Operating Voltage Range			**±6**	±6	±6	V	Max	A
Maximum Quiescent Current		14	**15.8**	16	16.1	mA	Max	A
Minimum Quiescent Current		14	**11.7**	11.4	11.1	mA	Min	A
Power-Supply Rejection Ratio (+PSRR)	$+V_S$ = 4.50V to 5.50V	80	**76**	74	72	dB	Min	A
(–PSRR)	$–V_S$ = 4.50V to –5.50V	80	**62**	60	58	dB	Min	A
TEMPERATURE RANGE								
Specified Operating Range: U,N Package		–40 to 85				°C	Typ	
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
U: SO-8		125				°C/W	Typ	
N: SOT23-5		150				°C/W	Typ	

NOTES: (1) Junction temperature = ambient for 25°C guaranteed specifications.(2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +20°C at high temperature limit for over temperature guaranteed specifications. (3) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = ±5V: High Grade DC Specifications[1]

R_F = 453Ω, R_L = 100Ω, and G = +10, unless otherwise noted.

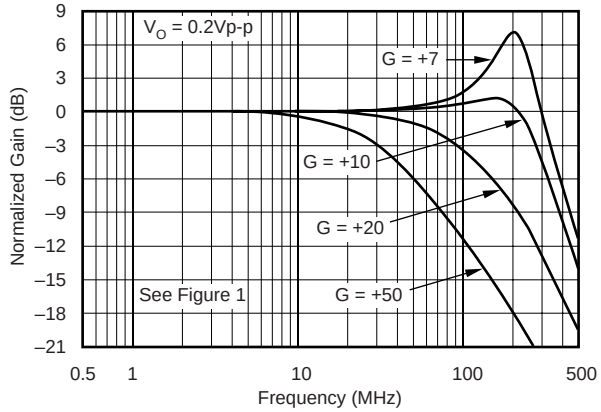
PARAMETER	CONDITIONS	OPA657UB, NB (High-Grade)						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[4]
Input Offset Voltage	V_{CM} = 0V	±0.1	**±0.6**	±0.85	±0.9	mV	Max	A
Input Offset Voltage Drift	V_{CM} = 0V	±2	**±6**	±6	±6	µV/°C	Max	A
Input Bias Current	V_{CM} = 0V	±1	**±5**	±450	±1250	pA	Max	A
Input Offset Current	V_{CM} = 0V	±0.5	**±5**	±450	±1250	pA	Max	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±0.5V	98	**91**	89	87	dB	Min	A
Power-Supply Rejection Ratio (+PSRR)	$+V_S$ = 4.5V to 5.5V	82	**78**	76	74	dB	Min	A
(–PSRR)	$–V_S$ = –4.5V to –5.5V	74	**68**	66	64	dB	Min	A

NOTES: (1) All other specifications are the same as the standard-grade. (2) Junction temperature = ambient for 25°C guaranteed specifications.(3) Junction temperature = ambient at low temperature limit: junction temperature = ambient +20°C at high temperature limit for over temperature guaranteed specifications. (4) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation.

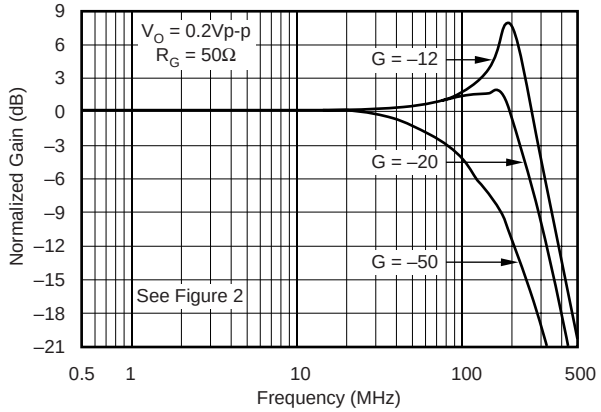
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

T_A = +25°C, G = +10, R_F = 453Ω, R_L = 100Ω, unless otherwise noted.

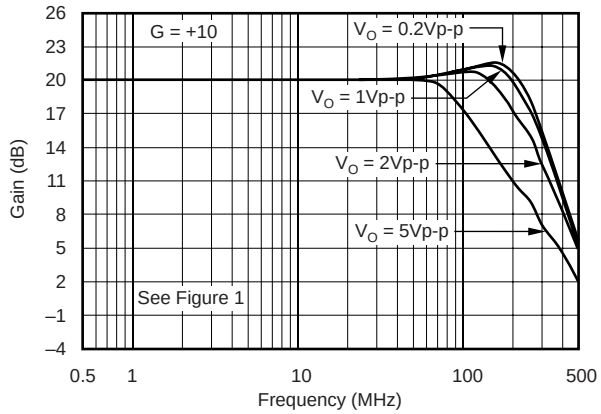
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



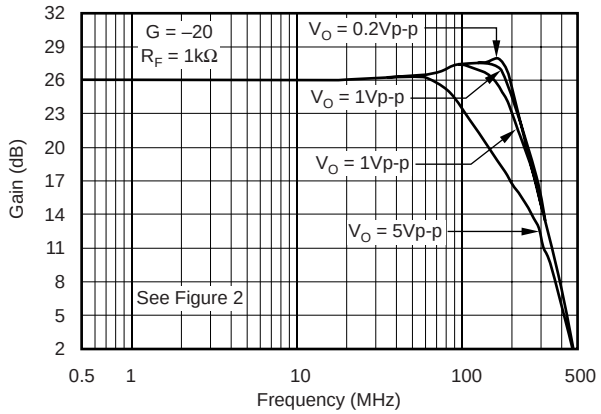
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



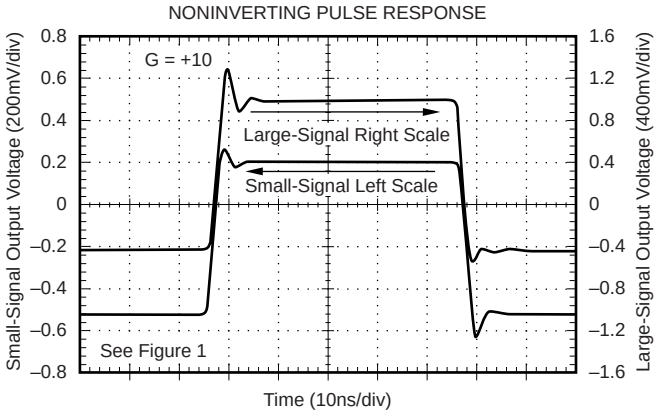
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



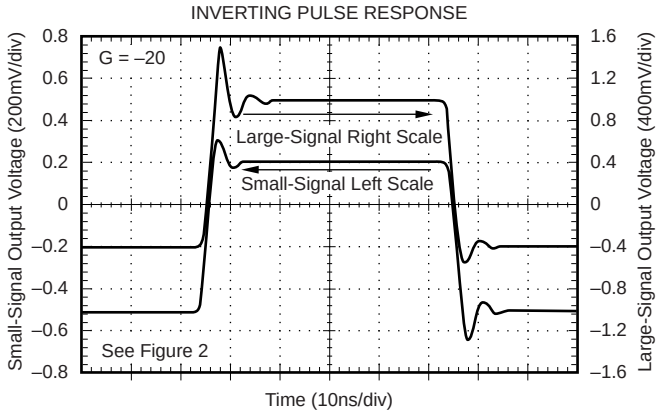
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



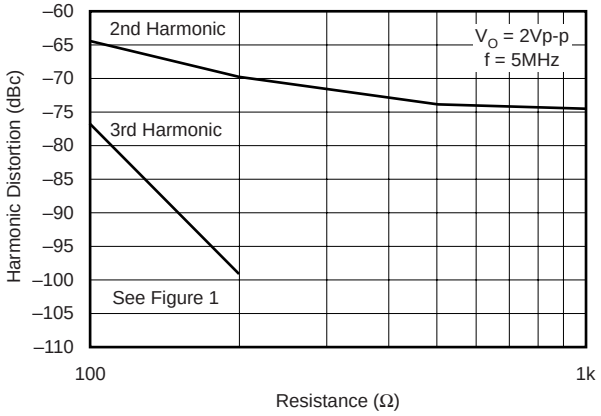
INVERTING PULSE RESPONSE



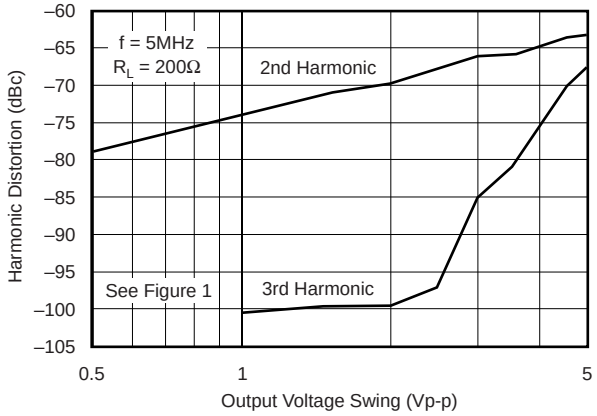
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +10, R_F = 453Ω, R_L = 100Ω, unless otherwise noted.

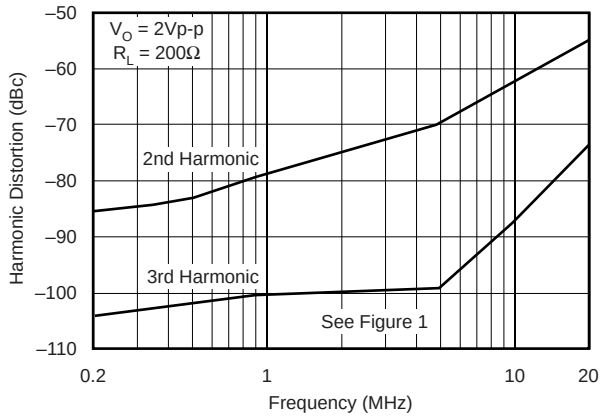
HARMONIC DISTORTION vs LOAD RESISTANCE



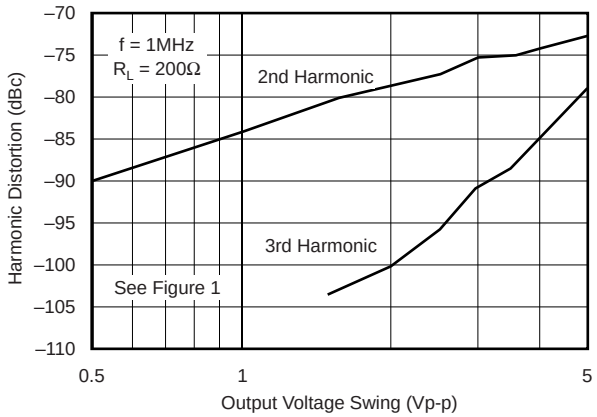
HARMONIC DISTORTION vs OUTPUT VOLTAGE (5MHz)



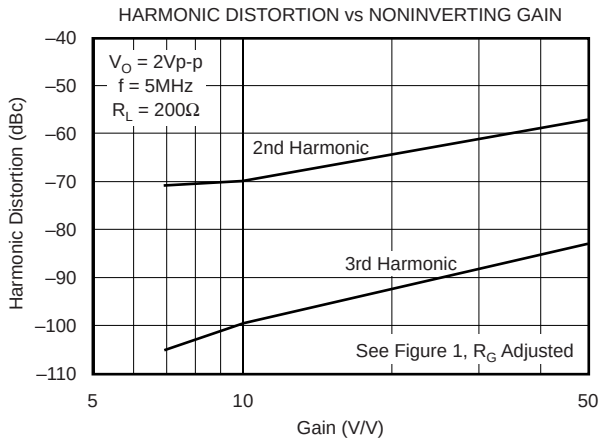
HARMONIC DISTORTION vs FREQUENCY



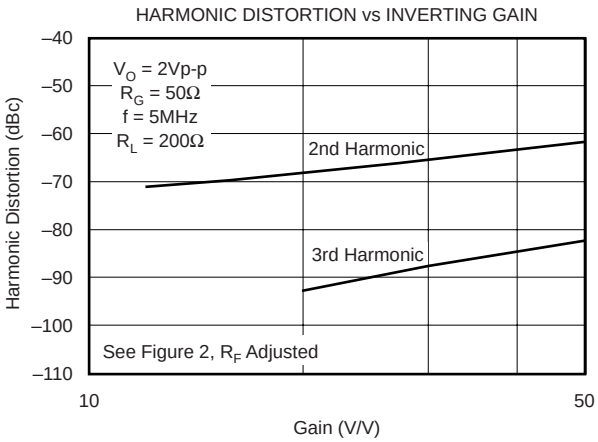
HARMONIC DISTORTION vs OUTPUT VOLTAGE (1MHz)



HARMONIC DISTORTION vs NONINVERTING GAIN



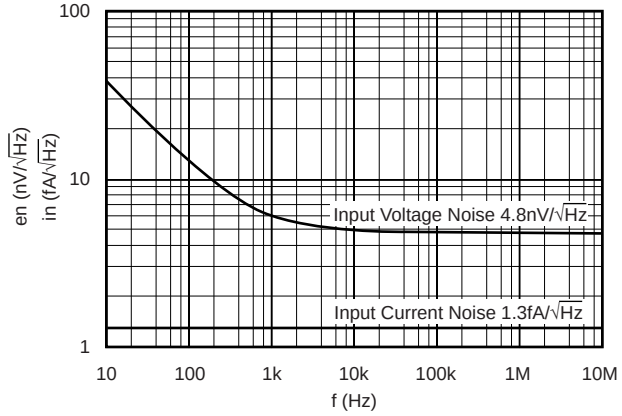
HARMONIC DISTORTION vs INVERTING GAIN



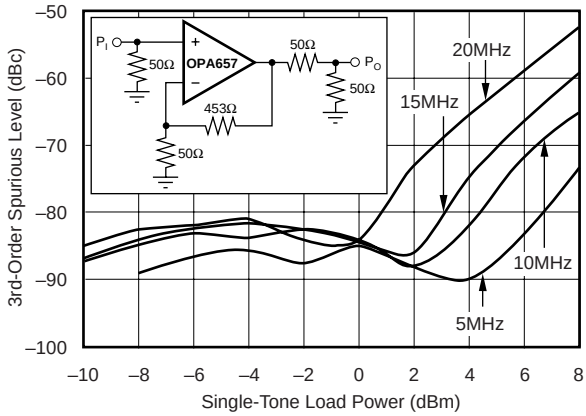
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +10, R_F = 453Ω, R_L = 100Ω, unless otherwise noted.

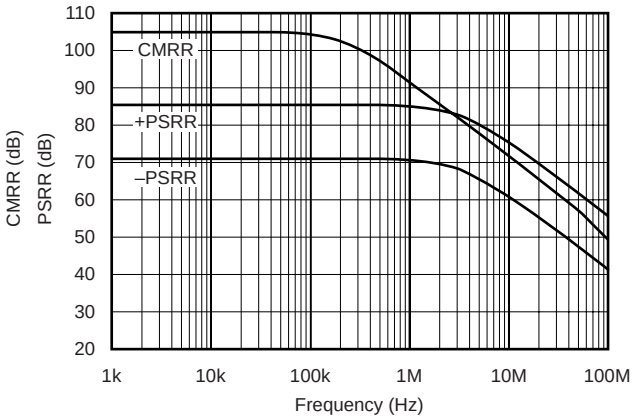
INPUT CURRENT AND VOLTAGE NOISE DENSITY



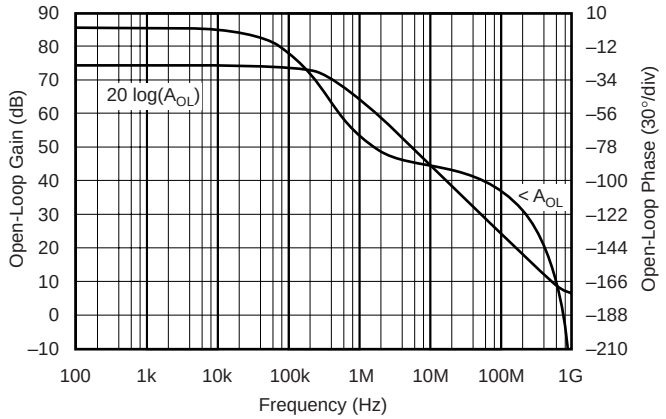
2-TONE, 3RD-ORDER
INTERMODULATION SPURIOUS



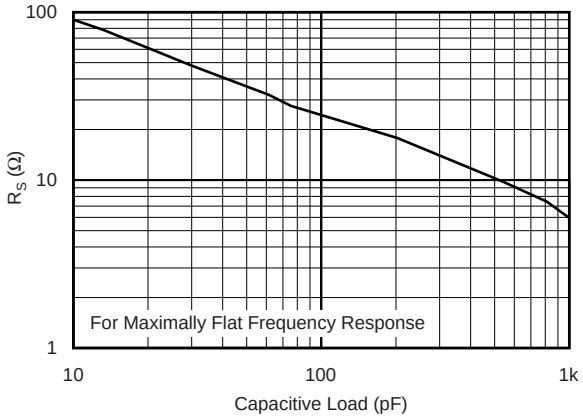
COMMON-MODE REJECTION RATIO AND
POWER-SUPPLY REJECTION RATIO vs FREQUENCY



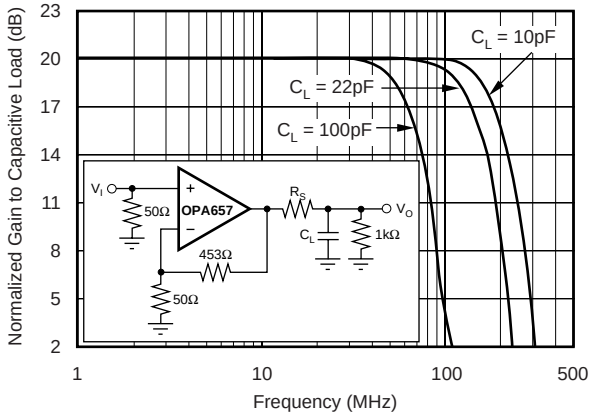
OPEN-LOOP GAIN AND PHASE



RECOMMENDED R_S vs CAPACITIVE LOAD



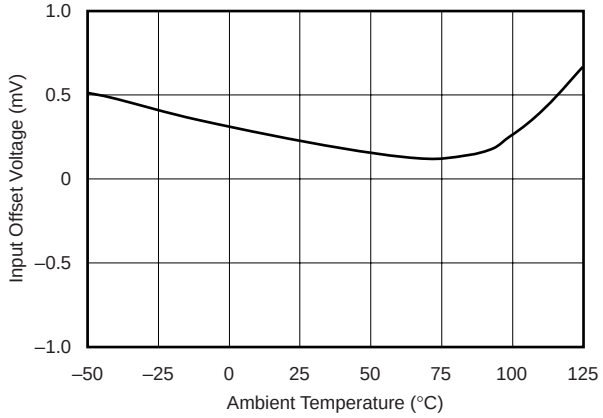
FREQUENCY RESPONSE vs CAPACITIVE LOAD



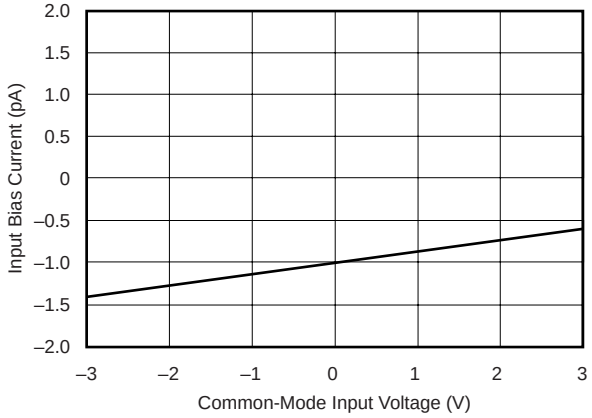
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +10, R_F = 453Ω, R_L = 100Ω, unless otherwise noted.

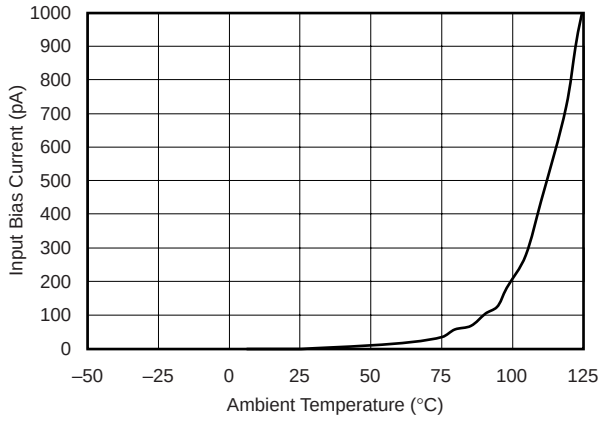
TYPICAL INPUT OFFSET VOLTAGE DRIFT OVER TEMPERATURE



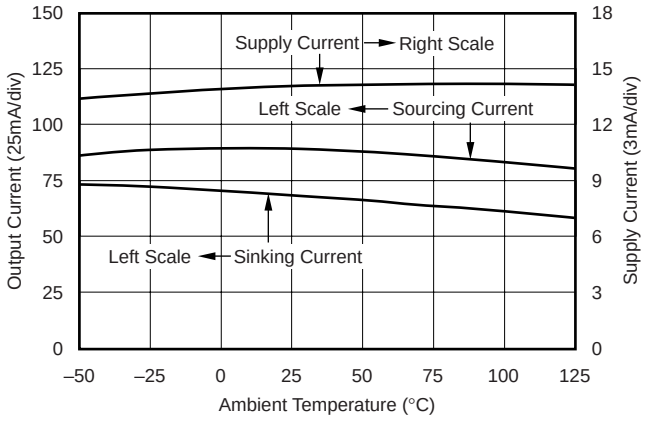
TYPICAL INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE



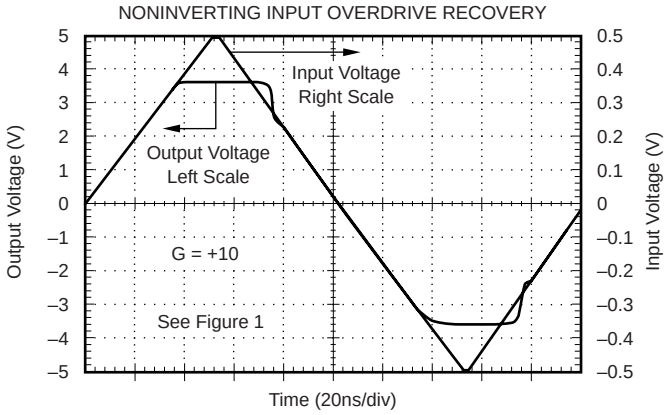
TYPICAL INPUT BIAS CURRENT DRIFT OVER TEMPERATURE



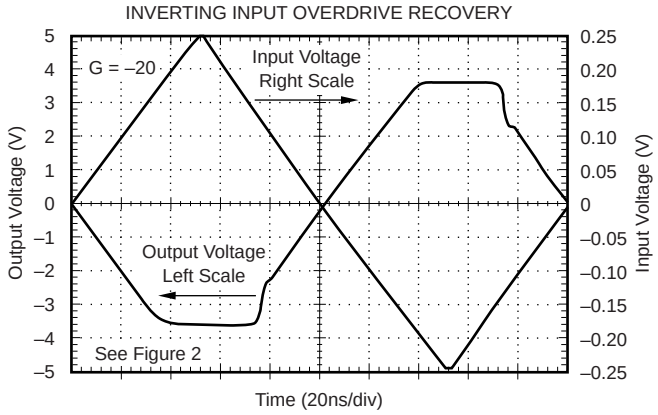
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



NONINVERTING INPUT OVERDRIVE RECOVERY



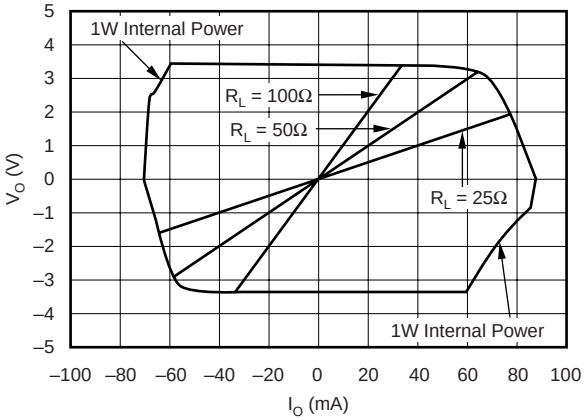
INVERTING INPUT OVERDRIVE RECOVERY



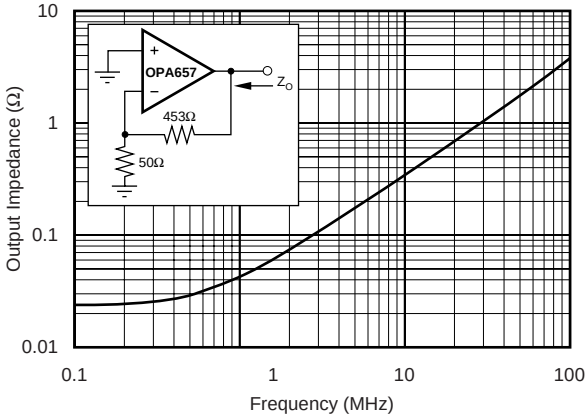
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

T_A = +25°C, G = +10, R_F = 453Ω, R_L = 100Ω, unless otherwise noted.

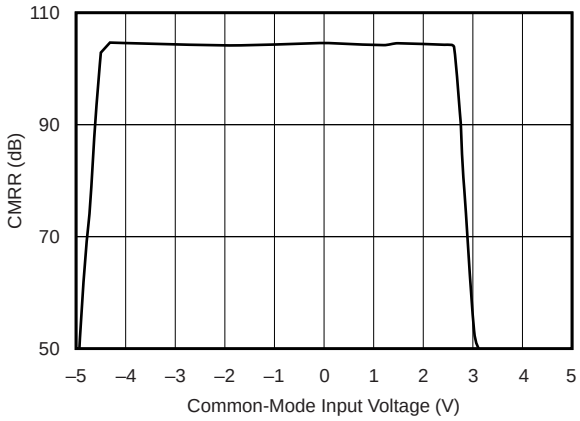
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND, NON-INVERTING OPERATION

The OPA657 provides a unique combination of low input voltage noise, very high gain bandwidth, and the DC precision of a trimmed JFET-input stage to give an exceptional high input impedance, high gain stage amplifier. Its very high Gain Bandwidth Product (GBP) can be used to either deliver high signal bandwidths at high gains, or to extend the achievable bandwidth or gain in photodiode-transimpedance applications. To achieve the full performance of the OPA657, careful attention to PC board layout and component selection is required as discussed in the following sections of this data sheet.

Figure 1 shows the noninverting gain of +10 circuit used as the basis for most of the Typical Characteristics. Most of the curves were characterized using signal sources with 50Ω driving impedance, and with measurement equipment presenting a 50Ω load impedance. In Figure 1, the 50Ω shunt resistor at the V_I terminal matches the source impedance of the test generator, while the 50Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet voltage swing specifications are at the output pin (V_O in Figure 1) while output power specifications are at the matched 50Ω load. The total 100Ω load at the output combined with the 500Ω total feedback network load, presents the OPA657 with an effective output load of 83Ω for the circuit of Figure 1.

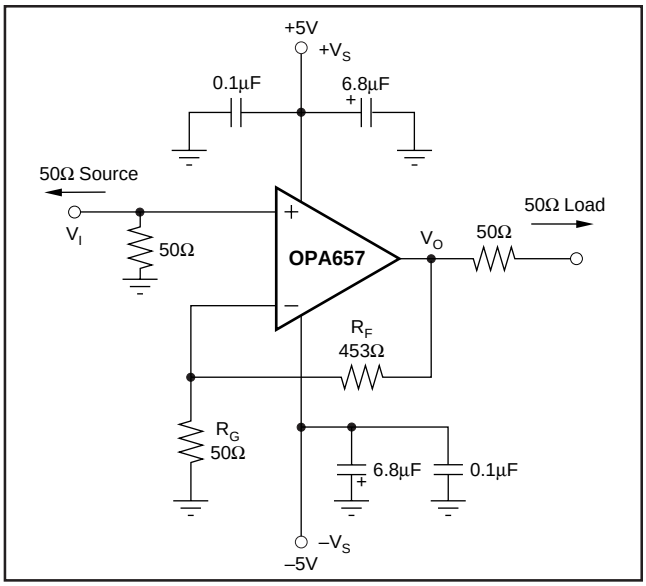


FIGURE 1. Noninverting G = +10 Specifications and Test Circuit.

Voltage-feedback op amps, unlike current-feedback amplifiers, can use a wide range of resistor values to set their gain. To retain a controlled frequency response for the noninverting voltage amplifier of Figure 1, the parallel combination of R_F || R_G should always < 150Ω. In the noninverting configuration, the parallel combination of R_F || R_G will form a pole with the parasitic input capacitance at the inverting node of the OPA657 (including layout parasitics). For best performance, this pole should be at a frequency greater than the closed-loop bandwidth for the OPA657. For lower non-inverting gains than the minimum recommended gain of +7 for the OPA657, consider the unity gain stable JFET input OPA656.

WIDEBAND, INVERTING GAIN OPERATION

There can be significant benefits to operating the OPA657 as an inverting amplifier. This is particularly true when a matched input impedance is required. Figure 2 shows the inverting gain circuit used as a starting point for the typical characteristics showing inverting-mode performance.

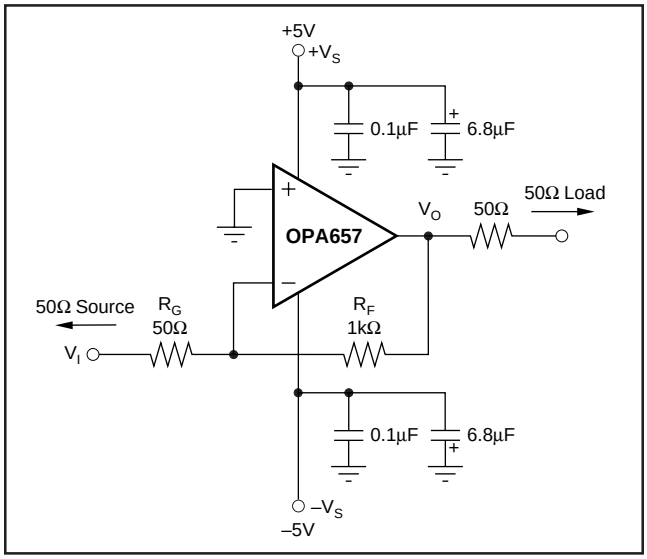


FIGURE 2. Inverting G = –20 Specifications and Test Circuit.

Driving this circuit from a 50Ω source, and constraining the gain resistor (R_G) to equal 50Ω will give both a signal bandwidth and noise advantage. R_G in this case is acting as both the input termination resistor and the gain setting resistor for the circuit. Although the signal gain for the circuit of Figure 2 is double that for Figure 1, their noise gains are equal when the 50Ω source resistor is included. This has the interesting effect of doubling the equivalent GBP for the amplifier. This can be seen in comparing the G = +10 and G = –20 small signal frequency response curves. Both show about 250MHz bandwidth, but the inverting configuration of Figure 2 is giving 6dB higher signal gain. If the signal source is actually the low impedance output of another amplifier, R_G should be increased to the minimum value allowed at the output of that amplifier and R_F adjusted to get the desired gain. It is critical for stable operation of the OPA657 that this driving amplifier show a very low output impedance through frequencies exceeding the expected closed-loop bandwidth for the OPA657.

Figure 2 also shows the noninverting input tied directly to ground. Often, a bias current canceling resistor to ground is included here to null out the DC errors caused by the input bias currents. This is only useful when the input bias currents are matched. For a JFET part like the OPA657, the input bias currents do not match but are so low to begin with (< 5pA) that DC errors due to input bias currents are negligible. Hence, no resistor is recommended at the noninverting input for the inverting signal gain condition.

WIDEBAND, HIGH SENSITIVITY, TRANSIMPEDANCE DESIGN

The high GBP and low input voltage and current noise for the OPA657 make it an ideal wideband-transimpedance amplifier for moderate to high transimpedance gains. Unity-gain stability in the op amp is not required for application as a transimpedance amplifier. One transimpedance design example is shown on the front page of the data sheet. Designs that require high bandwidth from a large area detector with relatively high transimpedance gain will benefit from the low input voltage noise for the OPA657. This input voltage noise is peaked up over frequency by the diode source capacitance, and can, in many cases, become the limiting factor to input sensitivity. The key elements to the design are the expected diode capacitance (C_D) with the reverse bias voltage ($-V_B$) applied, the desired transimpedance gain, R_F, and the GBP for the OPA657 (1600MHz). Figure 3 shows a design from a 50pF source capacitance diode through a 200kΩ transimpedance gain. With these 3 variables set (and including the parasitic input capacitance for the OPA657 added to C_D), the feedback capacitor value (C_F) may be set to control the frequency response.

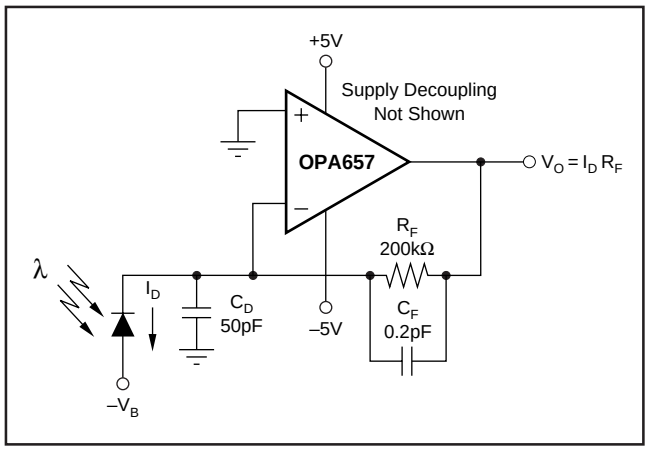


FIGURE 3. Wideband, Low Noise, Transimpedance Amplifier.

To achieve a maximally flat 2nd-order Butterworth frequency response, the feedback pole should be set to:

$$1/(2\pi R_F C_F) = \sqrt{(GPB/(4\pi R_F C_D))}$$

Adding the common-mode and differential mode input capacitance (0.7 + 4.5)pF to the 50pF diode source capacitance of Figure 3, and targeting a 200kΩ transimpedance gain using the 1600MHz GBP for the OPA657 will require a feedback pole set to 3.5MHz. This will require a total feedback capacitance of 0.2pF. Typical surface-mount resistors have a parasitic capacitance of 0.2pF, therefore, while Figure 3 shows a 0.2pF feedback-compensation capacitor, this will actually be the parasitic capacitance of the 200kΩ resistor.

This will give an approximate –3dB bandwidth set by:

$$f_{-3dB} = \sqrt{GPB/2\pi R_F C_D)}\ Hz$$

The example of Figure 3 will give approximately 5MHz flat bandwidth using the 0.2pF feedback compensation.

If the total output noise is bandlimited to a frequency less than the feedback pole frequency, a very simple expression for the equivalent input noise current can be derived as:

$$I_{EQ} = \sqrt{I_N^2 + \frac{4kT}{R_F} + \left(\frac{E_N}{R_F}\right)^2 + \frac{(E_N 2\pi C_D F)^2}{3}}$$

Where:

i_{EQ} = Equivalent input noise current if the output noise is bandlimited to $F < 1/(2\pi R_F C_F)$.

i_N = Input current noise for the op amp inverting input.

e_N = Input voltage noise for the op amp.

C_D = Diode capacitance.

F = Bandlimiting frequency in Hz (usually a postfilter prior to further signal processing).

4kT = 1.6E – 21J at T = 290°K

Evaluating this expression up to the feedback pole frequency at 3.9MHz for the circuit of Figure 3, gives an equivalent input noise current of 3.4pA/$\sqrt{Hz}$. This is much higher than the 1.2fA/$\sqrt{Hz}$ for just the op amp itself. This result is being dominated by the last term in the equivalent input noise expression. It is essential in this case to use a low voltage noise op amp like the OPA657. If lower transimpedance gain, wider bandwidth solutions are needed, consider the bipolar input OPA686 or OPA687. These parts offer comparable gain bandwidth products but much lower input noise voltage at the expense of higher input current noise.

LOW GAIN COMPENSATION

Where a low gain is desired, and inverting operation is acceptable, a new external compensation technique may be used to retain the full slew rate and noise benefits of the OPA657 while maintaining the increased loop gain and the associated improvement in distortion offered by the decompensated architecture. This technique shapes the loop gain for good stability while giving an easily controlled 2nd-order low-pass frequency response. Considering only the noise gain for the circuit of Figure 4, the low-frequency noise gain, (N_{G1}) will be set by the resistor ratios while the high frequency noise gain (N_{G2}) will be set by the capacitor ratios. The capacitor values set both the transition frequencies and the high-frequency noise gain. If this noise gain, determined by $N_{G2} = 1 + C_S/C_F$, is set to a value greater than the recommended minimum stable gain for the op amp and the noise gain pole, set by $1/R_F C_F$, is placed correctly, a very well controlled 2nd-order low-pass frequency response will result.

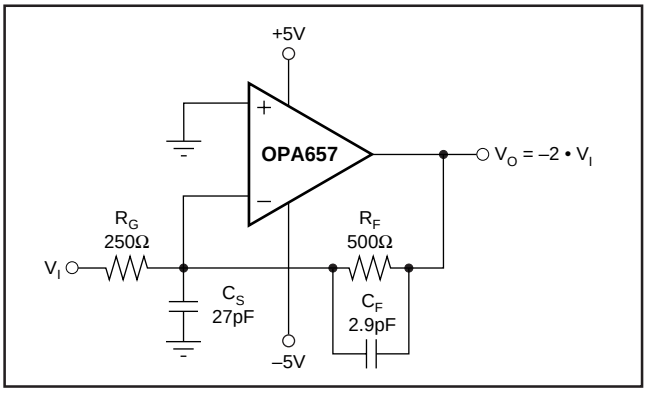


FIGURE 4. Broadband Low Gain Inverting External Compensation.

To choose the values for both C_S and C_F, two parameters and only three equations need to be solved. The first parameter is the target high-frequency noise gain NG_2, which should be greater than the minimum stable gain for the OPA657. Here, a target NG_2 of 10.5 will be used. The second parameter is the desired low-frequency signal gain, which also sets the low-frequency noise gain NG_1. To simplify this discussion, we will target a maximally flat 2nd-order low-pass Butterworth frequency response (Q = 0.707). The signal gain of –2 shown in Figure 4 will set the low frequency noise gain to $NG_1 = 1 + R_F/R_G$ (= 3 in this example). Then, using only these two gains and the GBP for the OPA657 (1600MHz), the key frequency in the compensation can be determined as:

$$Z_O = \frac{GBP}{NG_1^2}\left[\left(1-\frac{NG_1}{NG_2}\right)-\sqrt{1-2\frac{NG_1}{NG_2}}\right]$$

Physically, this Z_0 (10.6MHz for the values shown above) is set by $1/(2\pi \cdot R_F(C_F + C_S))$ and is the frequency at which the rising portion of the noise gain would intersect unity gain if projected back to 0dB gain. The actual zero in the noise gain occurs at $NG_1 \cdot Z_0$ and the pole in the noise gain occurs at $NG_2 \cdot Z_0$. Since GBP is expressed in Hz, multiply Z_0 by 2π and use this to get C_F by solving:

$$C_F = \frac{1}{2\pi \cdot R_F Z_O NG_2} \qquad (= 2.86pF)$$

Finally, since C_S and C_F set the high-frequency noise gain, determine C_S by [Using $NG_2 = 10.5$]:

$$C_S = (NG_2 - 1)C_F \qquad (= 27.2pF)$$

The resulting closed-loop bandwidth will be approximately equal to:

$$f_{-3dB} \cong \sqrt{Z_O\ GBP} \qquad (= 130MHz)$$

For the values shown in Figure 4, the f_{-3dB} will be approximately 130MHz. This is less than that predicted by simply dividing the GBP product by NG_1. The compensation network controls the bandwidth to a lower value while providing the full slew rate at the output and an exceptional distortion performance due to increased loop gain at frequencies below $NG_1 \cdot Z_0$. The capacitor values shown in Figure 4 are calculated for $NG_1 = 3$ and $NG_2 = 10.5$ with no adjustment for parasitics.

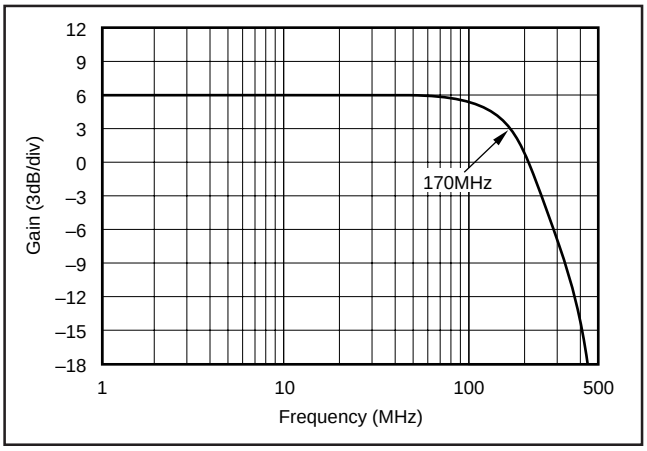


FIGURE 5. G = –2 Frequency Response with External Compensation.

Figure 5 shows the measured frequency response for the circuit of Figure 4. This is showing the expected gain of –2 with exceptional flatness through 70MHz and a –3dB bandwidth of 170MHz.

The real benefit to this compensation is to allow a high slew rate, exceptional DC precision op amp to provide a low overshoot, fast settling pulse response. For a 1V output step, the 700V/µs slew rate of the OPA657 will allow a rise time limited edge rate (2ns for a 170Mhz bandwidth). While unity-gain stable op amps may offer comparable bandwidths, their lower slew rates will extend the settling time for larger steps. For instance, the OPA656 can also provide a 150MHz gain of –2 bandwidth implying a 2.3ns transition time. However, the lower slew rate of this unity gain stable amplifier (290V/us) will limit a 1V step transition to 3.5ns and delay the settling time as the slewing transition is recovered. The combination of higher slew rate and exceptional DC precision for the OPA657 can yield one of the fastest, most precise, pulse amplifiers using the circuit of Figure 4.

An added benefit to the compensation of Figure 4 is to increase the loop gain above that achievable at comparable gains by internally compensated amplifiers. The circuit of Figure 4 will have lower harmonic distortion through 10Mhz than the OPA656 operated at a gain of –2.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO MINIMIZE NOISE

The OPA657 provides a very low input noise voltage while requiring a low 14mA of quiescent current. To take full advantage of this low input noise, a careful attention to the other possible noise contributors is required. Figure 6 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

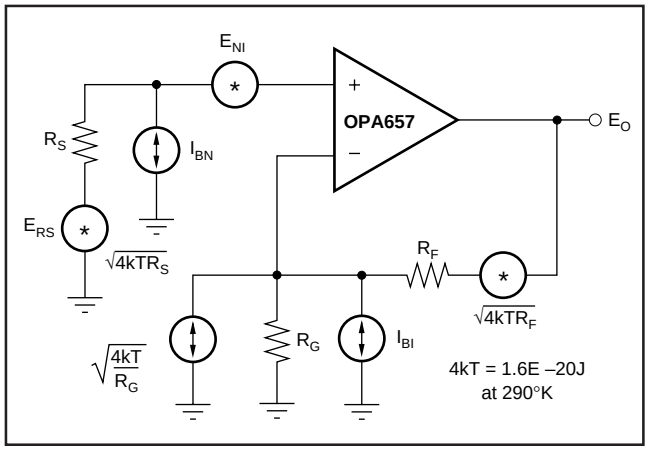


FIGURE 6. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 1 shows the general form for this output noise voltage using the terms shown in Figure 7:

(1)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Dividing this expression by the noise gain ($G_N = 1 + R_F/R_G$) will give the equivalent input referred spot noise voltage at the non-inverting input as shown in Equation 2:

(2)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Putting high resistor values into Equation 2 can quickly dominate the total equivalent input referred noise. A source impedance on the noninverting input of 1.6kΩ will add a Johnson voltage noise term equal to just that for the amplifier itself (5nV/$\sqrt{Hz}$). While the JFET input of the OPA657 is ideal for high source impedance applications, both the overall bandwidth and noise may be limited by these higher source impedances in the non-inverting configuration of Figure 1.

FREQUENCY RESPONSE CONTROL

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the specifications. Ideally, dividing GBP by the non-inverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low gains (increased feedback factors), most high-speed amplifiers will exhibit a more complex response with lower phase margin. The OPA657 is compensated to give a maximally flat 2nd-order Butterworth closed-loop response at a noninverting gain of +10 (Figure 1). This results in a typical gain of +10 bandwidth of 275MHz, far exceeding that predicted by dividing the 1600MHz GBP by 10. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +50 the OPA657 will show the 32MHz bandwidth predicted using the simple formula and the typical GBP of 1600MHz.

Inverting operation offers some interesting opportunities to increase the available gain-bandwidth product. When the source impedance is matched by the gain resistor (Figure 2), the signal gain is $-(R_F/R_G)$ while the noise gain for bandwidth purposes is $(1 + R_F/R_G)$. This cuts the noise gain in half, increasing the minimum stable gain for inverting operation under these condition to –12 and the equivalent gain bandwidth product to 3.2GHz.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter — including additional external capacitance which may be recommended to improve A/D linearity. A high speed, high open-loop gain amplifier like the OPA657 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics illustrate Recommended R_S vs Capacitive Load and the resulting frequency response at the load. In this case, a design target of a maximally flat frequency response was used. Lower values of R_S may be used if some peaking can be tolerated. Also, operating at higher gains (than the +10 used in the Typical Characteristics) will require lower values of R_S for a minimally peaked frequency response. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA657. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA657 output pin (see Board Layout section).

DISTORTION PERFORMANCE

The OPA657 is capable of delivering a low distortion signal at high frequencies over a wide range of gains. The distortion plots in the Typical Characteristics show the typical distortion under a wide variety of conditions.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic will dominate the distortion with negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the non-inverting configuration this is sum of $R_F + R_G$, while in the inverting configuration this is just R_F (Figure 1). Increasing output voltage swing increases harmonic distortion directly. A 6dB increase in output swing will generally increase the 2nd-harmonic 12dB and the 3rd-harmonic 18dB. Increasing the signal gain will also increase the 2nd-harmonic distortion. Again a 6dB increase in gain will increase the 2nd- and 3rd-harmonic by about 6dB even with a constant output power and frequency. And finally, the distortion increases as the fundamental frequency increases due to the rolloff in the loop gain with frequency. Conversely, the distortion will improve going to lower frequencies down to the dominant open loop pole at approximately 100kHz. Starting from the –70dBc 2nd-harmonic for a 5MHz, 2Vp-p fundamental into a 200Ω load at G = +10 (from the Typical Characteristics), the 2nd-harmonic distortion for frequencies lower than 100kHz will be approximately < –90dBc.

The OPA657 has an extremely low 3rd-order harmonic distortion. This also shows up in the 2-tone 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low (< –80dBc) at low output power levels. The output stage continues to hold them low even as the fundamental power reaches higher levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For 2 tones centered at 10MHz, with 4dBm/tone into a matched 50Ω load (i.e., 1Vp-p for each tone at the load, which requires 4Vp-p for the overall 2-tone envelope at the output pin), the Typical Characteristics show a 82dBc difference between the test tone and the 3rd-order intermodulation spurious levels. This exceptional performance improves further when operating at lower frequencies and/or higher load impedances.

D.C. ACCURACY AND OFFSET CONTROL

The OPA657 can provide excellent DC accuracy due to its high open-loop gain, high common-mode rejection, high power-supply rejection, and its trimmed input offset voltage (and drift) along with the negligible errors introduced by the low input bias current. For the best DC precision, a high-grade version (OPA657UB or OPA657NB) screens the key DC parameters to an even tighter limit. Both standard- and high-grade versions take advantage of a new final test technique to 100% test input offset voltage drift over temperature. This discussion will use the high-grade typical and min/max electrical characteristics for illustration, however, an identical analysis applies to the standard-grade version.

The total output DC offset voltage in any configuration and temperature will be the combination of a number of possible error terms. In a JFET part like the OPA657, the input bias current terms are typically quite low but are unmatched. Using bias current cancellation techniques, more typical in bipolar input amplifiers, does not improve output DC offset errors. Errors due to the input bias current will only become dominant at elevated temperatures. The OPA657 shows the typical 2X increase in every 10°C common to JFET-input stage amplifiers. Using the 5pA maximum tested value at 25°C, and a 20°C internal self heating (see thermal analysis), the maximum input bias current at 85°C ambient will be $5pA \bullet 2^{(105\ -\ 25)/10} = 1280pA$. For noninverting configurations, this term only begins to be a significant term versus the input offset voltage for source impedances > 750kΩ. This would also be the feedback resistor value for transimpedance applications (Figure 3) where the output DC error due to inverting input bias current is on the order of that contributed by the input offset voltage. In general, except for these extremely high-impedance values, the output DC errors due to the input bias current may be neglected.

After the input offset voltage itself, the most significant term contributing to output offset voltage is the PSRR for the negative supply. This term is modeled as an input offset voltage shift due to changes in the negative power supply voltage (and similarly for the +PSRR). The high-grade test limit for –PSRR is 68dB. This translates into $0.40mV/V$ input offset voltage shift $= 10^{(-68/20)}$. This low sensitivity to the negative supply voltage would require a 1.5V change in the negative supply to match the ±0.6mV input offset voltage error. The +PSRR is tested to a minimum value of 78dB. This translates into $10^{(-78/20)} = 0.125mV/V$ sensitivity for the input offset voltage to positive power-supply changes.

As an example, compute the worst-case output DC error for the transimpedance circuit of Figure 3 at 25°C and then the shift over the 0°C to 70°C range given the following assumptions.

Negative Power Supply

= –5V ±0.2V with a ±5mV/°C worst-case shift

Positive Power Supply

= +5V ±0.2V with a ±5mV/°C worst-case shift

Initial 25°C Output DC Error Band

= ±0.6mV (OPA657 high-grade input offset voltage limit)

±0.08mV (due to the –PSRR = 0.4mV/V • ±0.2V)

±0.04mV (due to the +PSRR = 0.2mV/V • ±0.2V)

Total = ±0.72mV

This would be the worst-case error band in volume production at 25°C acceptance testing given the conditions stated.

Over the temperature range (0°C to 70°C), we can expect the following worst-case shifting from initial value. A 20°C internal junction self-heating is assumed here.

±0.36mV (OPA656 high-grade input offset drift)

= ±6µV/°C • (70°C + 20°C – 25°C)

±0.11mV (–PSRR of 66dB with 5mV • (70°C – 25°C) supply shift)

±0.04mV (+PSRR of 76dB with 5mV • (70°C – 25°C) supply shift)

Total = ±0.51mV

This would be the worst-case shift from an initial offset over a 0°C to 70°C ambient for the conditions stated. Typical initial output DC error bands and shifts over temperature will be much lower than these worst-case estimates.

In the transimpedance configuration, the CMRR errors can be neglected since the input common-mode voltage is held at ground. For noninverting gain configurations (Figure 1), the CMRR term will need to be considered but will typically be far lower than the input offset voltage term. With a tested minimum of 91dB (28uV/V), the added apparent DC error will be no more than ±0.06mV for a ±2V input swing to the circuit of Figure 1.

POWER-SUPPLY CONSIDERATIONS

The OPA657 is intended for operation on ±5V supplies. Single-supply operation is allowed with minimal change from the stated specifications and performance from a single supply of +8V to +12V maximum. The limit to lower supply voltage operation is the useable input voltage range for the JFET-input stage. Operating from a single supply of +12V can have numerous advantages. With the negative supply at ground, the DC errors due to the –PSRR term can be minimized. Typically, AC performance improves slightly at +12V operation with minimal increase in supply current.

THERMAL ANALYSIS

The OPA657 will not require heatsinking or airflow in most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would—for a grounded resistive load—be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA657N (SOT23-5 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load.

$P_D = 10V \bullet 16.1mA + 5^2 /(4 \bullet (100\Omega \parallel 500\Omega)) = 236mW$

Maximum T_J = +85°C + (0.24W • 150°C/W) = 121°C.

All actual applications will be operating at lower internal power and junction temperature.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier like the OPA657 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability—on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) **Minimize the distance** (< 0.25”) from the power-supply pins to high-frequency 0.1uF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) **Careful selection and placement of external components will preserve the high frequency performance of the OPA657**. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound-type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic

capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. It has been suggested here that a good starting point for design would be to keep $R_F \parallel R_G < 150\Omega$ for voltage amplifier applications. Doing this will automatically keep the resistor noise terms low, and minimize the effect of their parasitic capacitance. Transimpedance applications (Figure 3) can use whatever feedback resistor is required by the application as long as the feedback-compensation capacitor is set considering all parasitic capacitance terms on the inverting node.

d) **Connections to other wideband devices** on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA657 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin) If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA657 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device—this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of R_S vs Capacitive Load. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) **Socketing a high-speed part like the OPA657 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA657 onto the board.

INPUT AND ESD PROTECTION

The OPA657 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 7.

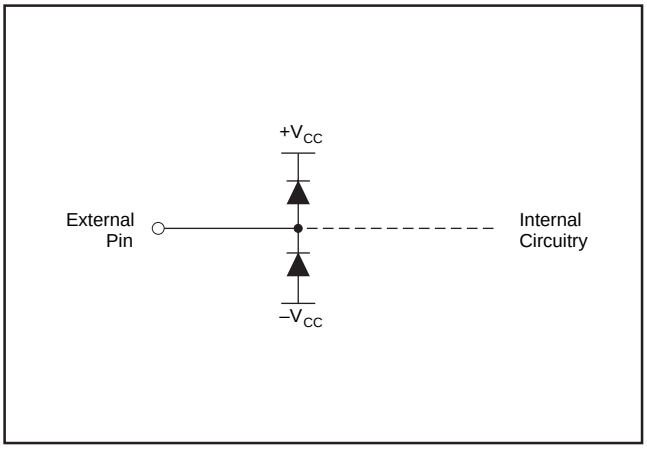


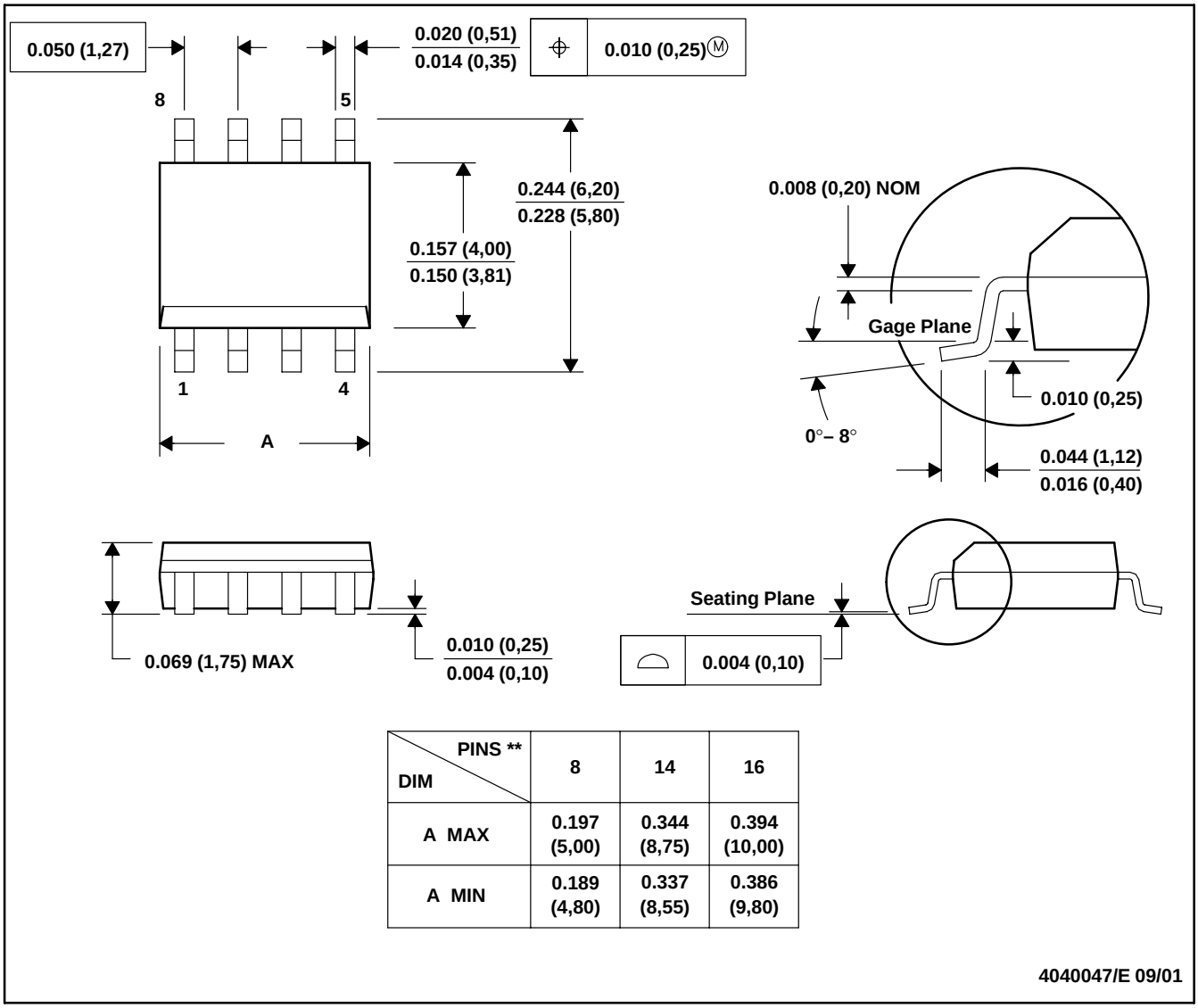
FIGURE 7. Internal ESD Protection.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±12V supply parts driving into the OPA657), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

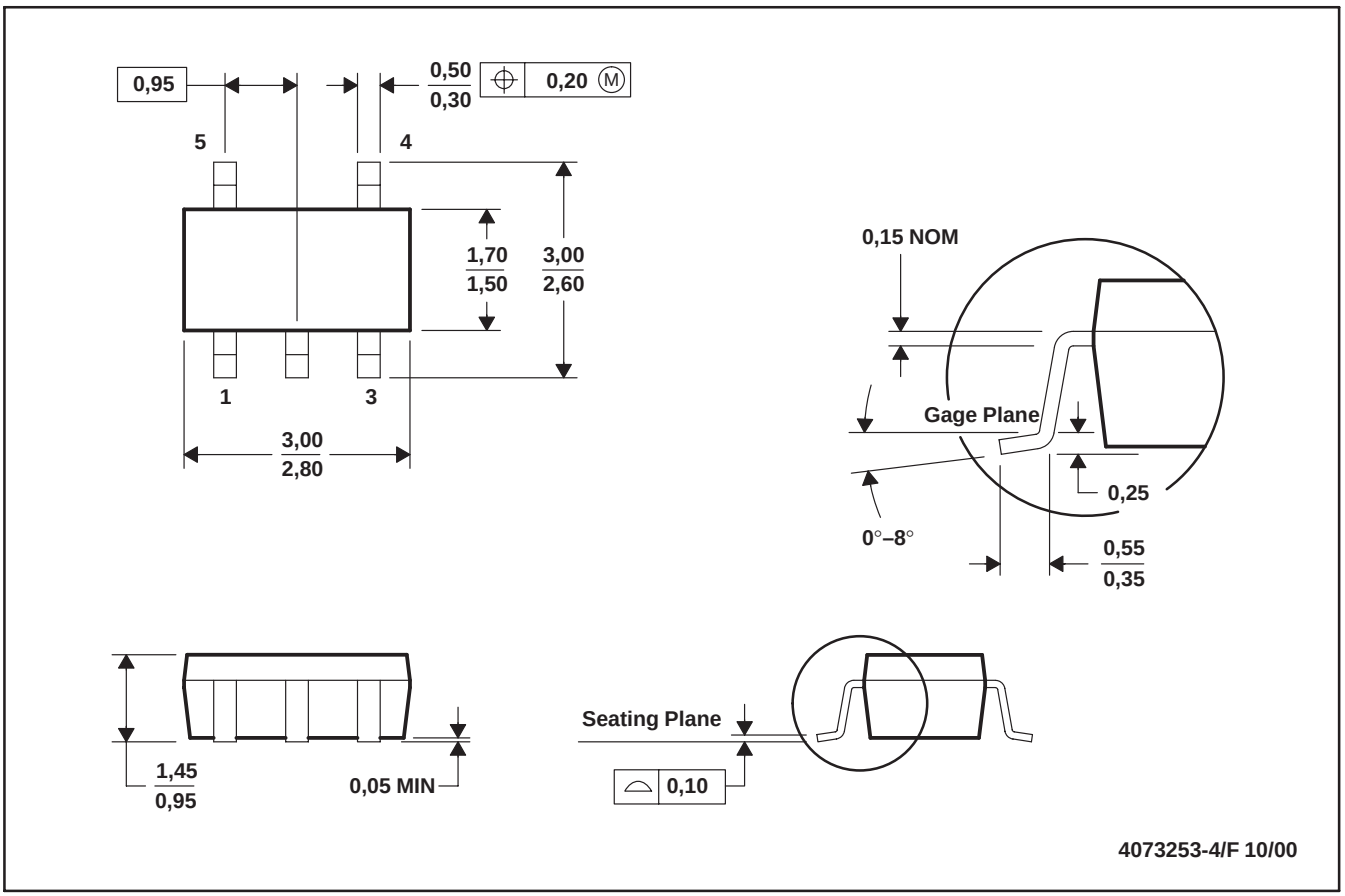


DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
OPA657N/250	ACTIVE	SOP	DBV	5	250
OPA657N/3K	ACTIVE	SOP	DBV	5	3000
OPA657NB/250	ACTIVE	SOP	DBV	5	250
OPA657NB/3K	ACTIVE	SOP	DBV	5	3000
OPA657U	ACTIVE	SOIC	D	8	100
OPA657U/2K5	ACTIVE	SOIC	D	8	2500
OPA657UB	ACTIVE	SOIC	D	8	100
OPA657UB/2K5	ACTIVE	SOIC	D	8	2500

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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