

## 1MHz, 45 $\mu$ A, CMOS, Rail-to-Rail OPERATIONAL AMPLIFIERS

### FEATURES

- **LOW  $I_Q$ : 45 $\mu$ A typical**
- **LOW COST**
- **RAIL-TO-RAIL INPUT AND OUTPUT**
- **SINGLE SUPPLY: +2.1V to +5.5V**
- **INPUT BIAS CURRENT: 0.5pA**
- **MicroSIZE PACKAGES: SC70-5, SOT23-8 and TSSOP-14**
- **HIGH SPEED:POWER WITH BANDWIDTH: 1MHz**

### APPLICATIONS

- **PORTABLE EQUIPMENT**
- **BATTERY-POWERED EQUIPMENT**
- **SMOKE ALARMS**
- **CO DETECTORS**
- **MEDICAL INSTRUMENTATION**

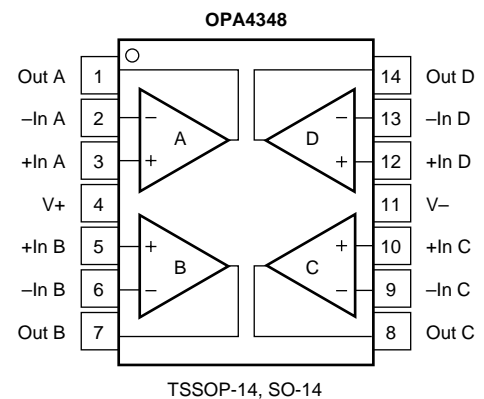
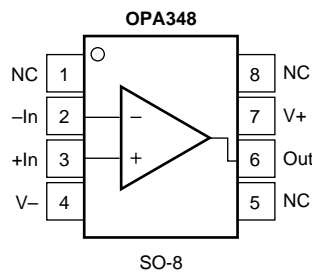
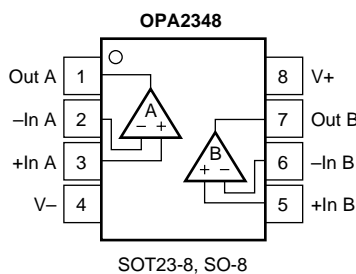
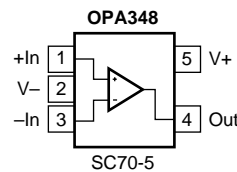
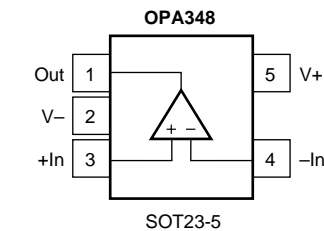
### DESCRIPTION

The OPA348 series amplifiers are single supply, low-power, CMOS op amps in micro packaging. Featuring an extended bandwidth of 1MHz, and a supply current of 45 $\mu$ A, the OPA348 series is useful for low-power applications on single supplies of 2.1V to 5.5V.

Low supply current of 45 $\mu$ A, and an input bias current of 0.5pA, make the OPA348 series an optimal candidate for low-power, high-impedance applications such as smoke detectors and other sensors.

The OPA348 is available in the miniature SC70-5, SOT23-5 and SO-8 packages. The OPA2348 is available in SOT23-8 and SO-8 packages, and the OPA4348 is offered in space-saving TSSOP-14 and SO-14 packages. The extended temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  over all supply voltages offers additional design flexibility.

PACKAGES	OPA348	OPA2348	OPA4348
SOT23-5	X		
SOT23-8		X	
SO-8	X	X	
TSSOP-14			X
SO-14			X
SC70-5	X		



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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage, V <sub>-</sub> to V <sub>+</sub> .....	7.5V
Signal Input Terminals, Voltage <sup>(2)</sup> .....	(V <sub>-</sub> ) - 0.5V to (V <sub>+</sub> ) + 0.5V
Current <sup>(2)</sup> .....	10mA
Output Short-Circuit <sup>(3)</sup> .....	Continuous
Operating Temperature .....	-65°C to +150°C
Storage Temperature .....	-65°C to +150°C
Junction Temperature .....	150°C
Lead Temperature (soldering, 10s) .....	300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only. Functional operation of the device at these conditions, or beyond the specified operating conditions, is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER <sup>(2)</sup>	TRANSPORT MEDIA, QUANTITY
<b>Single</b>						
OPA348AI	SOT23-5	DBV	-40°C to +125°C	A48	OPA348AIDBVT	Tape and Reel, 250
"	"	"	"	"	OPA348AIDBVR	Tape and Reel, 3000
OPA348AI	SO-8	D	-40°C to +125°C	348A	OPA348AID	Tubes, 100
"	"	"	"	"	OPA348AIDR	Tape and Reel, 2500
OPA348AI	SC70-5	DCK	-40°C to 125°C	S48	OPA348AIDCKT	Tape and Reel, 250
"	"	"	"	"	OPA348AIDCKR	Tape and Reel, 3000
<b>Dual</b>						
OPA2348AI	SOT23-8	DCN	-40°C to +125°C	B48	OPA2348AIDCNT	Tape and Reel, 250
"	"	"	"	"	OPA2348AIDCNR	Tape and Reel, 3000
OPA2348AI	SO-8	D	-40°C to +125°C	2348A	OPA2348AID	Tubes, 100
"	"	"	"	"	OPA2348AIDR	Tape and Reel, 2500
<b>Quad</b>						
OPA4348AI	SO-14	D	-40°C to +125°C	OPA4348	OPA4348AID	Tubes, 58
"	"	"	"	"	OPA4348AIDR	Tape and Reel, 2500
OPA4348AI	TSSOP-14	PW	-40°C to +125°C	4348A	OPA4348AIPWT	Tubes, 250
"	"	"	"	"	OPA4348AIPWR	Tape and Reel, 2500

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Models labeled with "T" indicate smaller quantity tape and reel, "R" indicates large quantity tape and reel, and "D" indicates tubes of specified quantity.

# ELECTRICAL CHARACTERISTICS: $V_S = 2.5V$ to $5.5V$

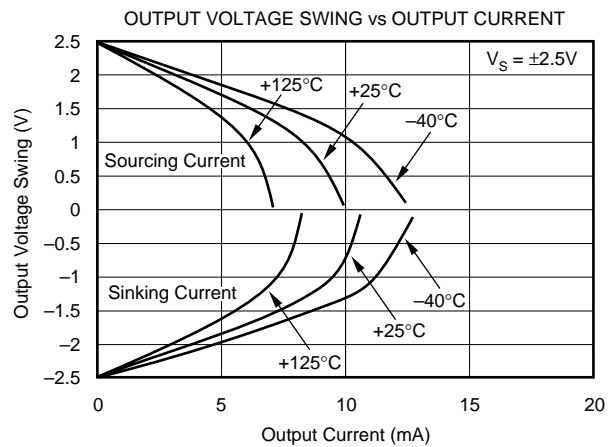
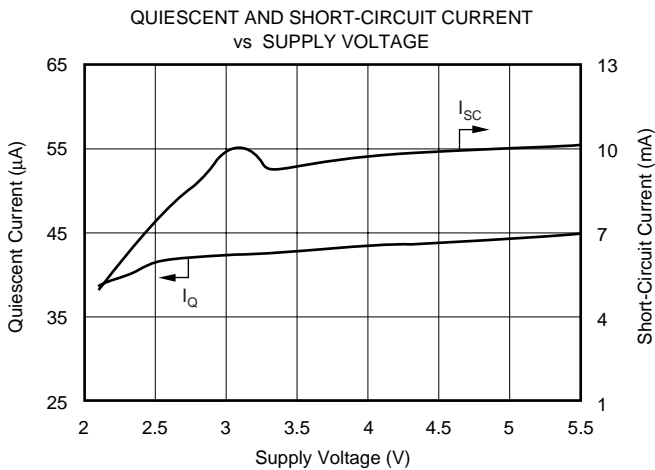
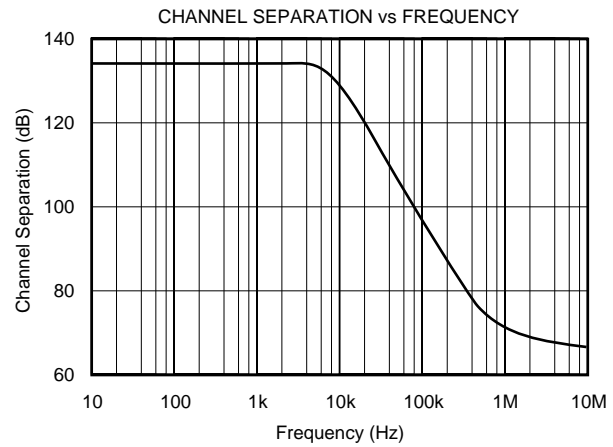
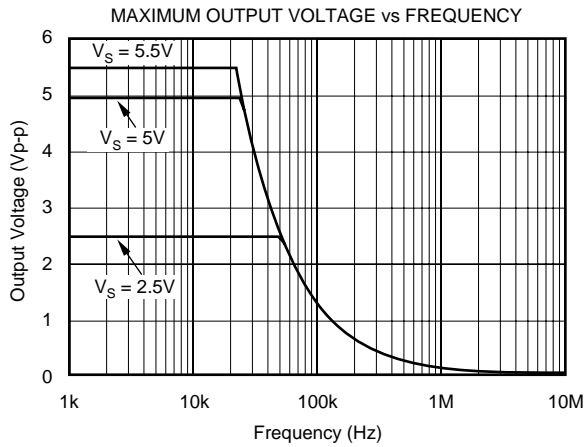
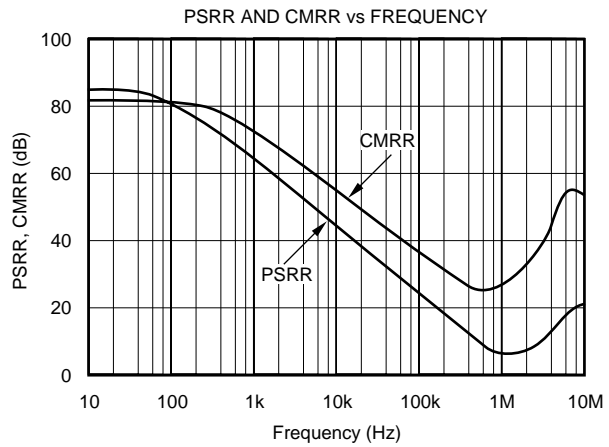
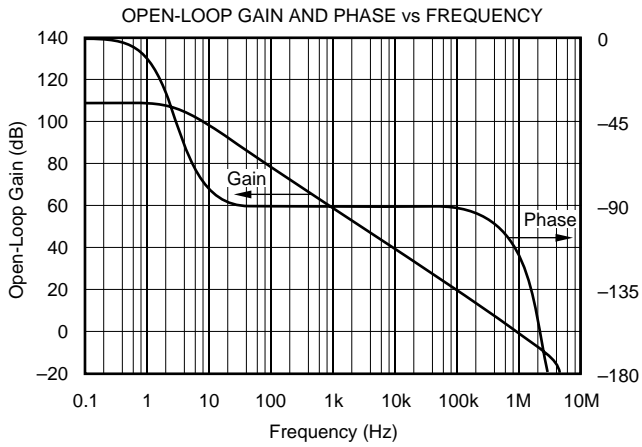
**Boldface** limits apply over the specified temperature range,  $T_A = -40^\circ C$  to  $+125^\circ C$

At  $T_A = +25^\circ C$ ,  $R_L = 100k\Omega$  connected to  $V_S/2$  and  $V_{OUT} = V_S/2$ , unless otherwise noted.

PARAMETER	CONDITION	OPA348 OPA2348 OPA4348			UNITS
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> Input Offset Voltage $V_{OS}$ <b>Over Temperature</b> <b>Drift</b> $dV_{OS}/dT$ vs Power Supply PSRR <b>Over Temperature</b> Channel Separation, dc $f = 1kHz$	$V_S = 5V, V_{CM} = (V-) + 0.8V$		1	5	mV
	$V_S = 2.5V$ to $5.5V, V_{CM} < (V+) - 1.7V$		<b>4</b>	<b>6</b>	<b>mV</b>
	$V_S = 2.5V$ to $5.5V, V_{CM} < (V+) - 1.7V$		60	175	$\mu V/V$
			0.2	<b>300</b>	$\mu V/V$
			134		dB
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range $V_{CM}$ Common-Mode Rejection Ratio <b>over Temperature</b> <b>over Temperature</b>	$(V-) - 0.2V < V_{CM} < (V+) - 1.7V$	$(V-) - 0.2$	70	$(V+) + 0.2$	V
	$(V-) < V_{CM} < (V+) - 1.7V$	<b>66</b>	82		dB
	$V_S = 5.5V, (V-) - 0.2V < V_{CM} < (V+) + 0.2V$	60	71		dB
	$V_S = 5.5V, (V-) < V_{CM} < (V+)$	<b>56</b>			<b>dB</b>
<b>INPUT BIAS CURRENT</b> Input Bias Current $I_B$ Input Offset Current $I_{OS}$			$\pm 0.5$	$\pm 10$	pA
			$\pm 0.5$	$\pm 10$	pA
<b>INPUT IMPEDANCE</b> Differential Common-Mode			$10^{13} \parallel 3$		$\Omega \parallel pF$
			$10^{13} \parallel 6$		$\Omega \parallel pF$
<b>NOISE</b> Input Voltage Noise, $f = 0.1Hz$ to $10Hz$ Input Voltage Noise Density, $f = 1kHz$ $e_n$ Input Current Noise Density, $f = 1kHz$ $i_n$	$V_{CM} < (V+) - 1.7V$		10		$\mu Vp-p$
			35		$nV/\sqrt{Hz}$
			4		$fA/\sqrt{Hz}$
<b>OPEN-LOOP GAIN</b> Open-Loop Voltage Gain $A_{OL}$ <b>over Temperature</b> <b>over Temperature</b>	$V_S = 5V, R_L = 100k\Omega, 0.025V < V_O < 4.975V$	94	108		dB
	$V_S = 5V, R_L = 100k\Omega, 0.025V < V_O < 4.975V$	<b>90</b>			<b>dB</b>
	$V_S = 5V, R_L = 5k\Omega, 0.125V < V_O < 4.875V$	90	98		dB
	$V_S = 5V, R_L = 5k\Omega, 0.125V < V_O < 4.875V$	<b>88</b>			<b>dB</b>
<b>OUTPUT</b> Voltage Output Swing from Rail <b>over Temperature</b> <b>over Temperature</b> Short-Circuit Current $I_{SC}$ Capacitive Load Drive $C_{LOAD}$	$R_L = 100k\Omega, A_{OL} > 94dB$		18	25	mV
	$R_L = 100k\Omega, A_{OL} > 90dB$			<b>25</b>	<b>mV</b>
	$R_L = 5k\Omega, A_{OL} > 90dB$		100	125	mV
	$R_L = 5k\Omega, A_{OL} > 88dB$			<b>125</b>	<b>mV</b>
			$\pm 10$		mA
			See Typical Characteristics		
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product GBW Slew Rate SR Settling Time, 0.1% $t_s$ 0.01% Overload Recovery Time Total Harmonic Distortion + Noise THD+N	$C_L = 100pF$				MHz
	$G = +1$		1		
	$V_S = 5.5V, 2V$ Step, $G = +1$		0.5		V/ $\mu s$
	$V_S = 5.5V, 2V$ Step, $G = +1$		5		$\mu s$
	$V_{IN} \cdot \text{Gain} > V_S$		7		$\mu s$
	$V_S = 5.5V, V_O = 3Vp-p, G = +1, f = 1kHz$		1.6		$\mu s$
			0.0023		%
<b>POWER SUPPLY</b> Specified Voltage Range $V_S$ Minimum Operating Voltage Quiescent Current (per amplifier) $I_Q$ <b>over Temperature</b>		2.5		5.5	V
			2.1 to 5.5		V
			45	65	$\mu A$
	$I_O = 0$			<b>75</b>	$\mu A$
<b>TEMPERATURE RANGE</b> Specified Range Operating Range Storage Range Thermal Resistance $\theta_{JA}$ SOT23-5 Surface-Mount SOT23-8 Surface-Mount MSOP-8 Surface-Mount SO-8 Surface-Mount SO-14 Surface-Mount TSSOP-14 Surface-Mount SC70-5 Surface-Mount		-40		125	$^\circ C$
		-65		150	$^\circ C$
		-65		150	$^\circ C$
			200		$^\circ C/W$
			150		$^\circ C/W$
			150		$^\circ C/W$
			150		$^\circ C/W$
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			100		$^\circ C/W$
			250		$^\circ C/W$

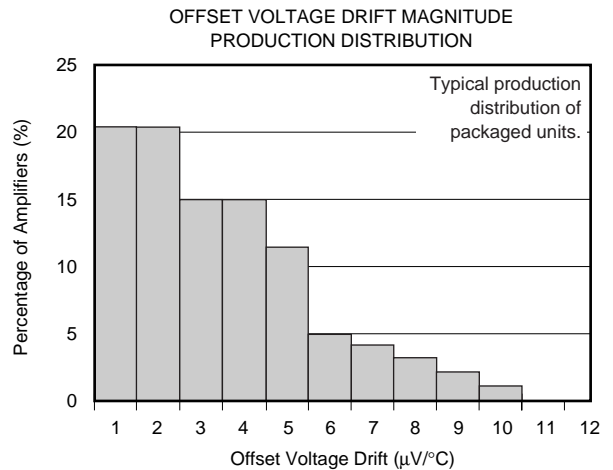
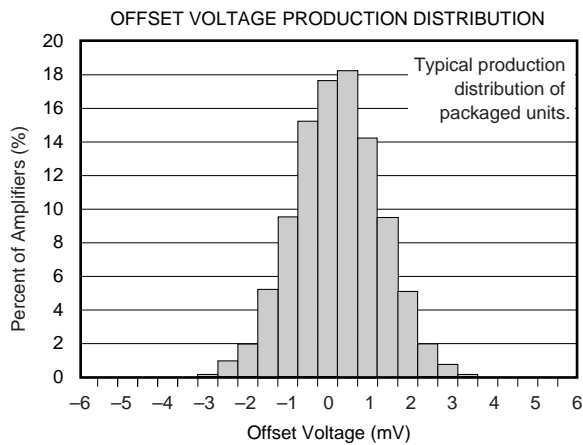
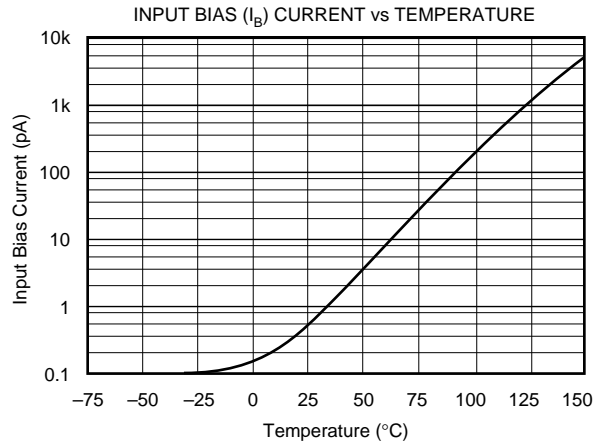
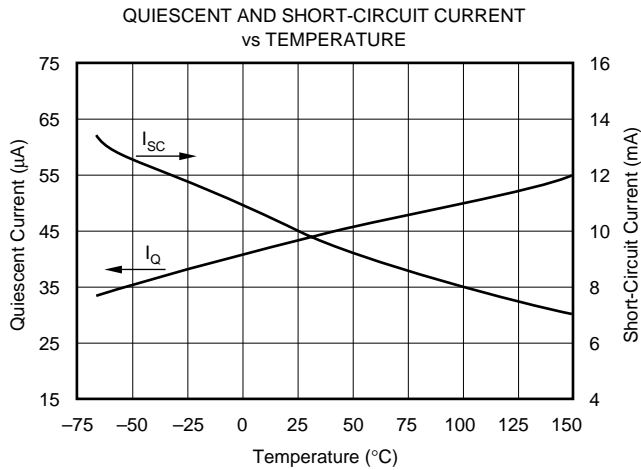
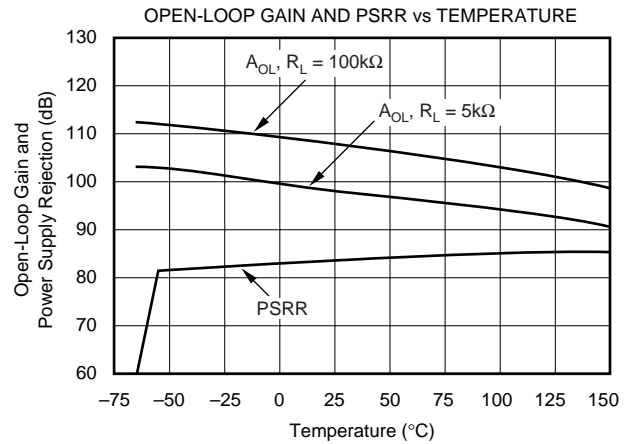
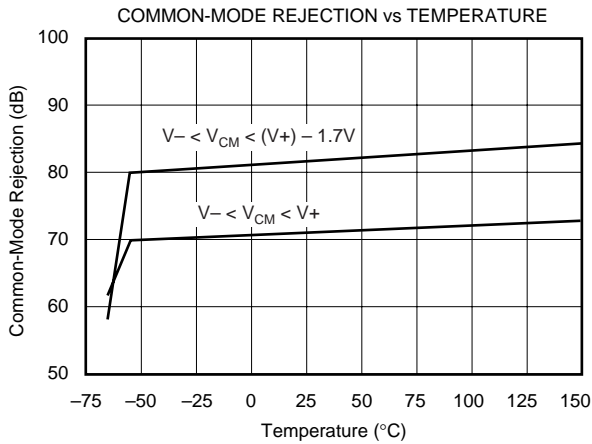
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 100\text{k}\Omega$  connected to  $V_S/2$  and  $V_{OUT} = V_S/2$ , unless otherwise noted.



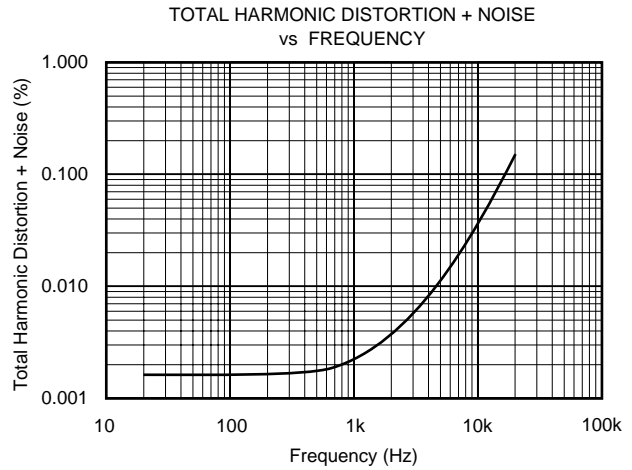
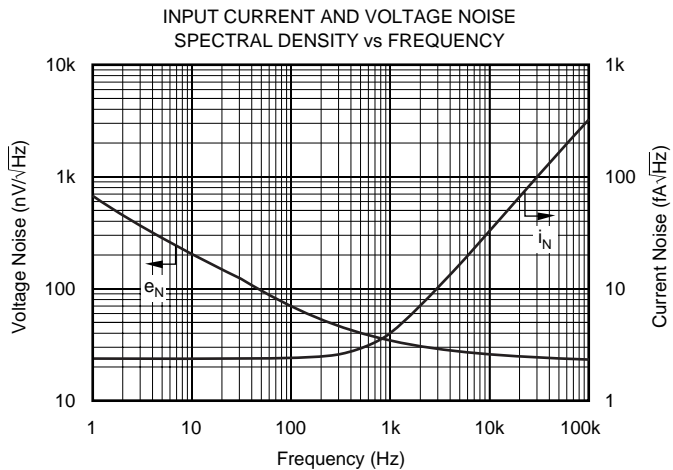
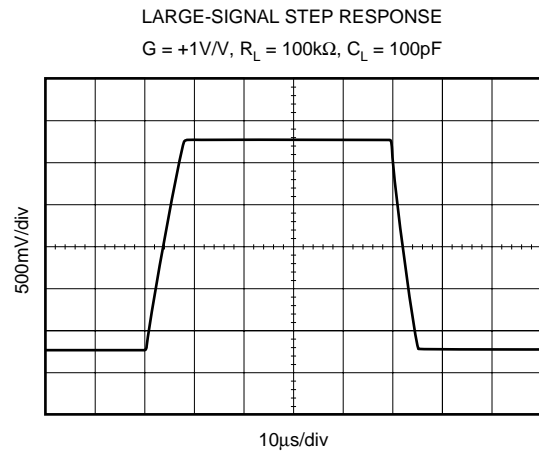
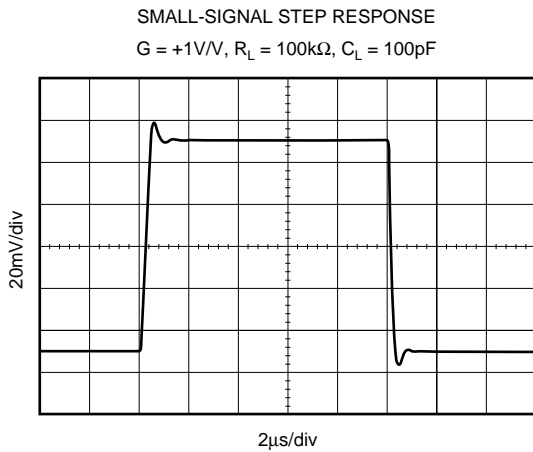
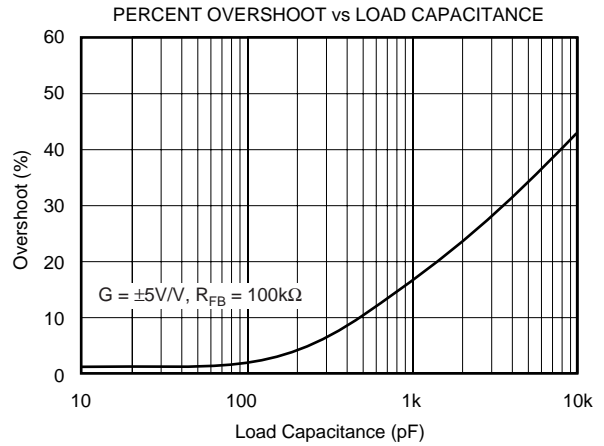
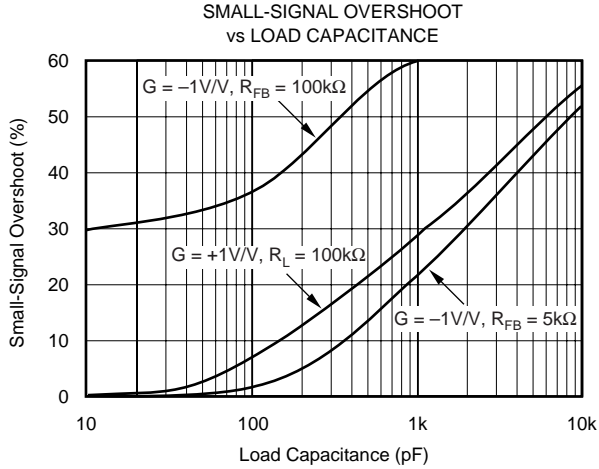
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# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 100\text{k}\Omega$  connected to  $V_S/2$  and  $V_{OUT} = V_S/2$ , unless otherwise noted.



# APPLICATIONS INFORMATION

OPA348 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications.

The OPA348 series features wide bandwidth and unity-gain stability with rail-to-rail input and output for increased dynamic range. Figure 1 shows the input and output waveforms for the OPA348 in unity-gain configuration. Operation is from a single +5V supply with a 100kΩ load connected to  $V_S/2$ . The input is a 5Vp-p sinusoid. Output voltage is approximately 4.98Vp-p.

Power-supply pins should be bypassed with 0.01μF ceramic capacitors.

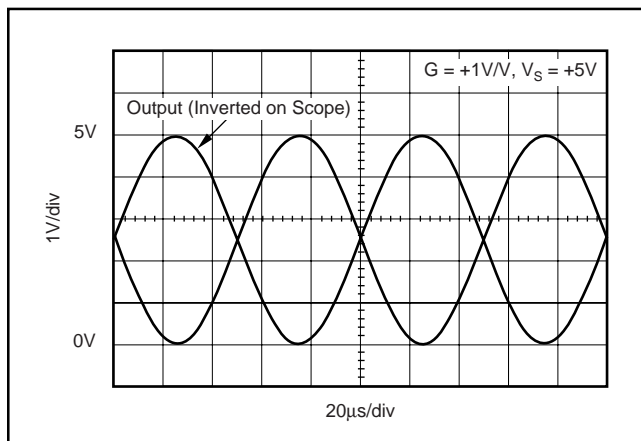


FIGURE 1. The OPA348 Features Rail-to-Rail Input/Output.

## OPERATING VOLTAGE

OPA348 series op amps are fully specified and tested from +2.5V to +5.5V. However, supply voltage may range from +2.1V to +5.5V. Parameters are tested over the specified supply range—a unique feature of the OPA348 series. In addition, all temperature specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Most behavior remains virtually unchanged throughout the full operating voltage range. Parameters that vary significantly with operating voltages or temperature are shown in the Typical Characteristics.

## COMMON-MODE VOLTAGE RANGE

The input common-mode voltage range of the OPA348 series extends 200mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.2\text{V}$  to 300mV above the positive supply, while the P-channel pair is on for inputs from 300mV below the negative supply to approximately  $(V+) - 1.4\text{V}$ . There is a small transition region, typically  $(V+) - 1.4\text{V}$  to  $(V+) - 1.2\text{V}$ , in which both pairs are on. This 200mV transition region, shown in Figure 2, can vary  $\pm 300\text{mV}$  with process variation. Thus, the transition region (both stages on) can range from  $(V+) - 1.7\text{V}$  to  $(V+) - 1.5\text{V}$  on the low end, up to  $(V+) - 1.1\text{V}$  to  $(V+) - 0.9\text{V}$

on the high end. Within the 200mV transition region PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to operation outside this region.

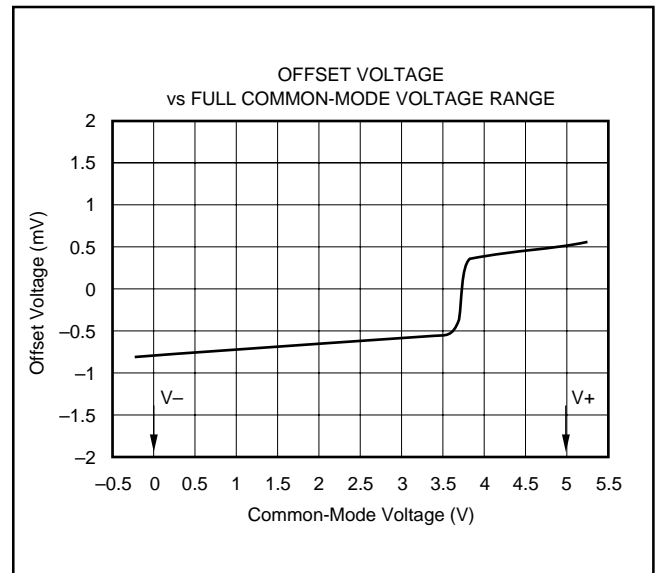


FIGURE 2. Behavior of Typical Transition Region at Room Temperature.

## RAIL-TO-RAIL INPUT

The input common-mode range extends from  $(V-) - 0.2\text{V}$  to  $(V+) + 0.2\text{V}$ . For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 500mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, will not cause any damage to the op amp. Unlike some other op amps, if input current is limited the inputs may go beyond the power supplies without phase inversion, as shown in Figure 3.

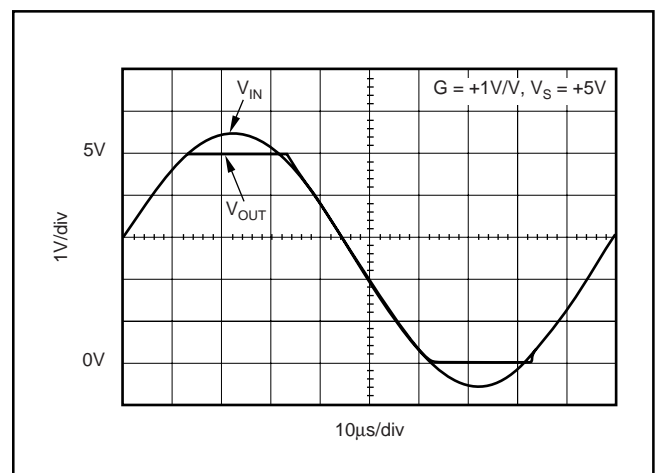


FIGURE 3. OPA348—No Phase Inversion with Inputs Greater than the Power-Supply Voltage.

Normally, input currents are 0.5pA. However, large inputs (greater than 500mV beyond the supply rails) can cause excessive current to flow in or out of the input pins. Therefore, as well as keeping the input voltage below the maximum rating, it is also important to limit the input current to less than 10mA. This is easily accomplished with an input voltage resistor, as shown in Figure 4.

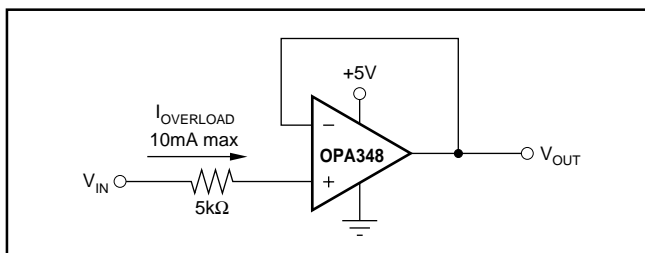


FIGURE 4. Input Current Protection for Voltages Exceeding the Supply Voltage.

### RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. This output stage is capable of driving 5kΩ loads connected to any potential between V+ and ground. For light resistive loads (> 100kΩ), the output voltage can typically swing to within 18mV from supply rail. With moderate resistive loads (10kΩ to 50kΩ), the output voltage can typically swing to within 100mV of the supply rails while maintaining high open-loop gain (see the typical characteristic “Output Voltage Swing vs Output Current”).

### CAPACITIVE LOAD AND STABILITY

The OPA348 in a unity-gain configuration can directly drive up to 250pF pure capacitive load. Increasing the gain enhances the amplifier’s ability to drive greater capacitive loads (see the typical characteristic “Small-Signal Overshoot vs Capacitive Load”). In unity-gain configurations, capacitive load drive can be improved by inserting a small (10Ω to 20Ω) resistor,  $R_S$ , in series with the output, as shown in Figure 5. This significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if there is a resistive load in parallel with the capacitive load, a voltage divider is created, introducing a Direct Current (DC) error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio  $R_S/R_L$ , and is generally negligible.

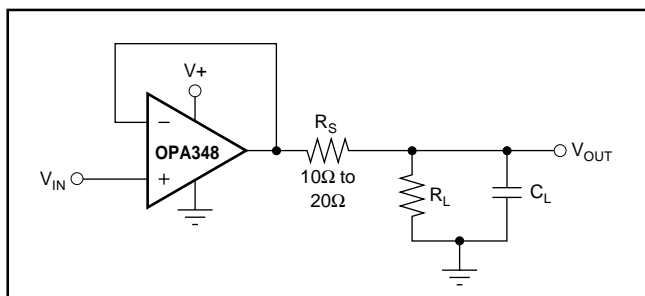


FIGURE 5. Series Resistor in Unity-Gain Buffer Configuration Improves Capacitive Load Drive.

In unity-gain inverter configuration, phase margin can be reduced by the reaction between the capacitance at the op amp input, and the gain setting resistors, thus degrading capacitive load drive. Best performance is achieved by using small valued resistors. For example, when driving a 500pF load, reducing the resistor values from 100kΩ to 5kΩ decreases overshoot from 55% to 13% (see the typical characteristic “Small-Signal Overshoot vs. Load Capacitance”). However, when large valued resistors cannot be avoided, a small (4pF to 6pF) capacitor,  $C_{FB}$ , can be inserted in the feedback, as shown in Figure 6. This significantly reduces overshoot by compensating the effect of capacitance,  $C_{IN}$ , which includes the amplifier’s input capacitance and PC board parasitic capacitance.

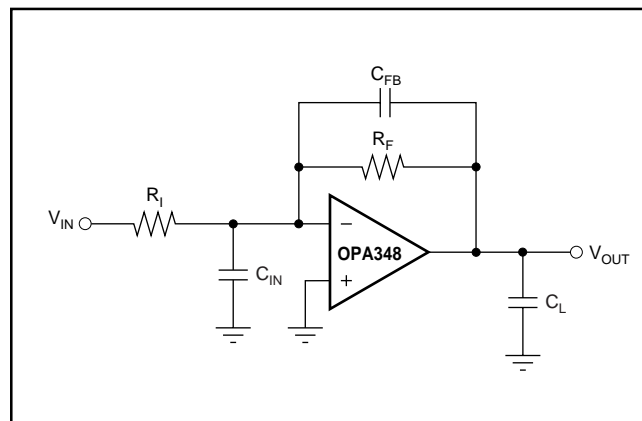


FIGURE 6. Improving Capacitive Load Drive.

### DRIVING A/D CONVERTERS

The OPA348 series op amps are optimized for driving medium-speed sampling Analog-to-Digital Converters (ADCs). The OPA348 op amps buffer the ADCs input capacitance and resulting charge injection while providing signal gain.

The OPA348 in a basic noninverting configuration driving the ADS7822, see Figure 7. The ADS7822 is a 12-bit, *microPOWER* sampling converter in the MSOP-8 package. When used with the low-power, miniature packages of the OPA348, the combination is ideal for space-limited, low-power applications. In this configuration, an RC network at the ADC’s input can be used to provide for anti-aliasing filter and charge injection current.

The OPA348 in noninverting configuration driving ADS7822 limited, low-power applications. In this configuration, an RC network at the ADC’s input can be used to provide for anti-aliasing filter and charge injection current. See Figure 8 for the OPA2348 driving an ADS7822 in a speech bandpass filtered data acquisition system. This small, low-cost solution provides the necessary amplification and signal conditioning to interface directly with an electret microphone. This circuit will operate with  $V_S = 2.7V$  to 5V with less than 250μA typical quiescent current.



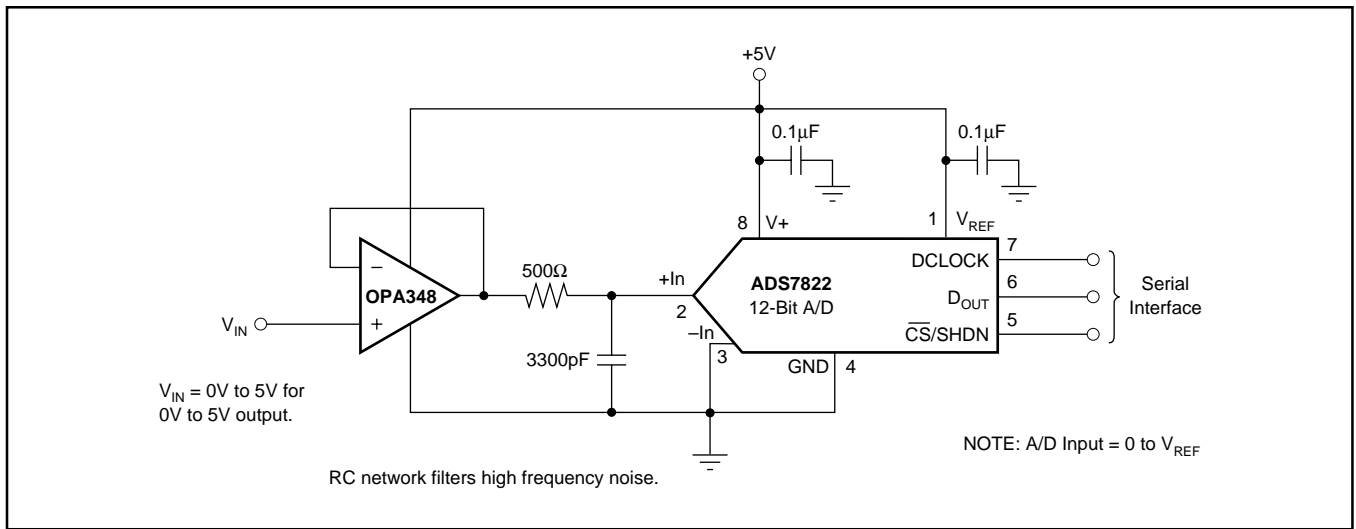


FIGURE 7. OPA348 in Noninverting Configuration Driving ADS7822.

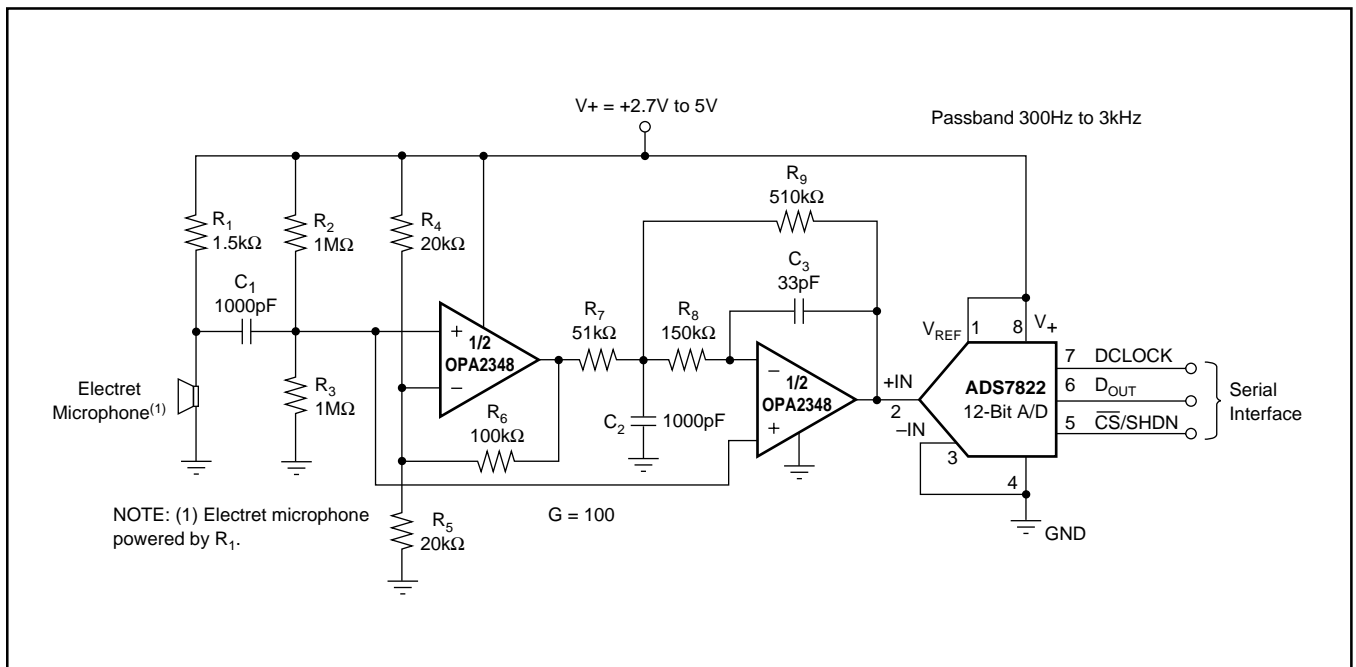


FIGURE 8. OPA2348 as a Speech Bandpass Filtered Data Acquisition System.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
OPA2348AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2348AIDCNR	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA2348AIDCNRG4	ACTIVE	SOT-23	DCN	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA2348AIDCNT	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA2348AIDCNTG4	ACTIVE	SOT-23	DCN	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA2348AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2348AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA2348AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA348AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA348AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA348AIDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA348AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA348AIDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA348AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA348AIDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA348AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
OPA348AIDCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
OPA348AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA348AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA348AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4348AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4348AIDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4348AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4348AIDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4348AIPWR	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4348AIPWRG4	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4348AIPWT	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
OPA4348AIPWTG4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF OPA2348, OPA4348 :**

- Automotive: [OPA2348-Q1](#), [OPA4348-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2348AIDCNR	SOT-23	DCN	8	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2348AIDCNT	SOT-23	DCN	8	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
OPA2348AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA348AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA348AIDCKR	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA348AIDCKT	SC70	DCK	5	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
OPA348AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4348AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4348AIPWR	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4348AIPWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2348AIDCNR	SOT-23	DCN	8	3000	203.0	203.0	35.0
OPA2348AIDCNT	SOT-23	DCN	8	250	203.0	203.0	35.0
OPA2348AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA348AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA348AIDCKR	SC70	DCK	5	3000	203.0	203.0	35.0
OPA348AIDCKT	SC70	DCK	5	250	203.0	203.0	35.0
OPA348AIDR	SOIC	D	8	2500	346.0	346.0	29.0
OPA4348AIDR	SOIC	D	14	2500	346.0	346.0	33.0
OPA4348AIPWR	TSSOP	PW	14	2500	346.0	346.0	29.0
OPA4348AIPWT	TSSOP	PW	14	250	210.0	185.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE

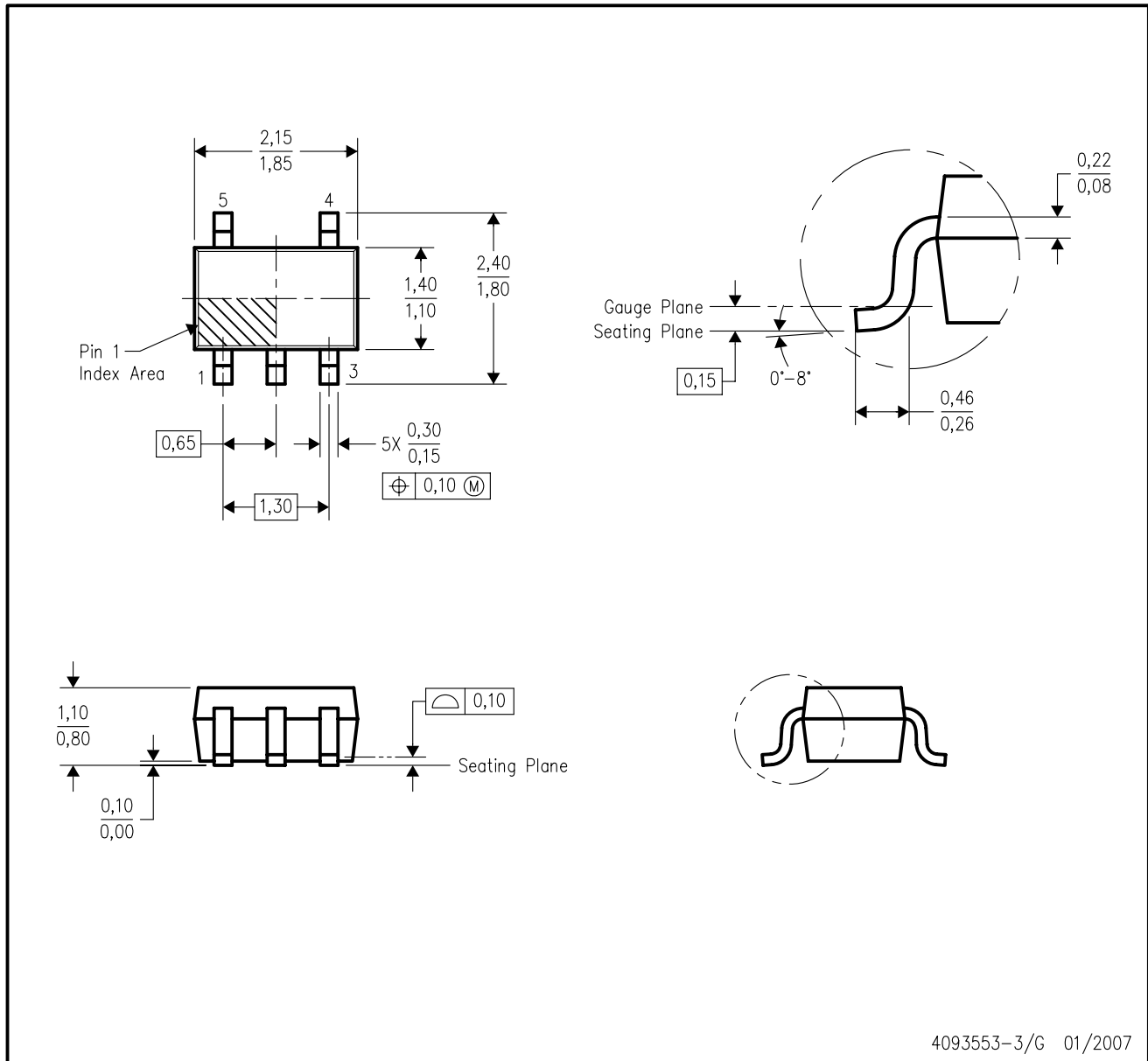


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

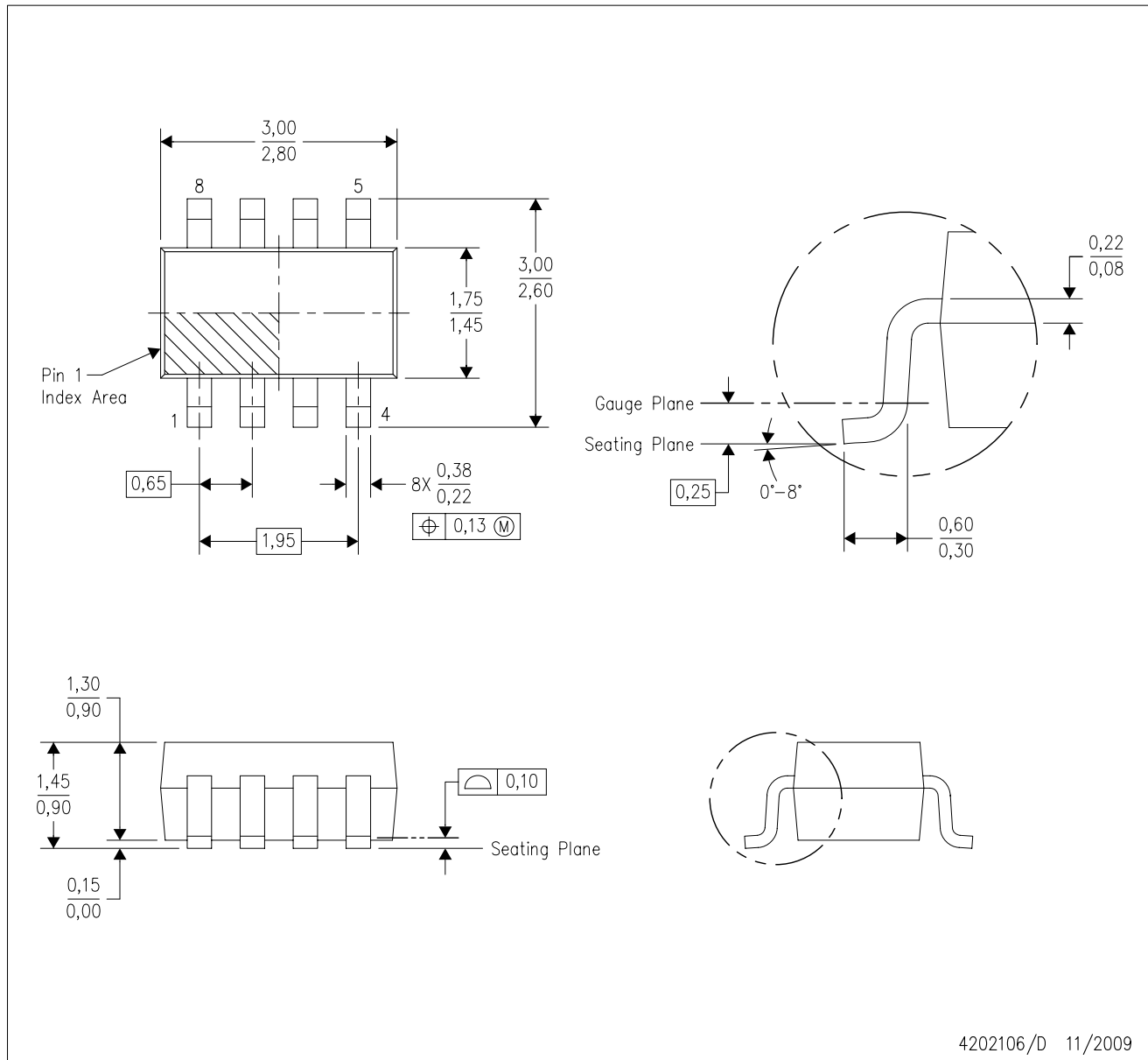
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCN (R-PDSO-G8)

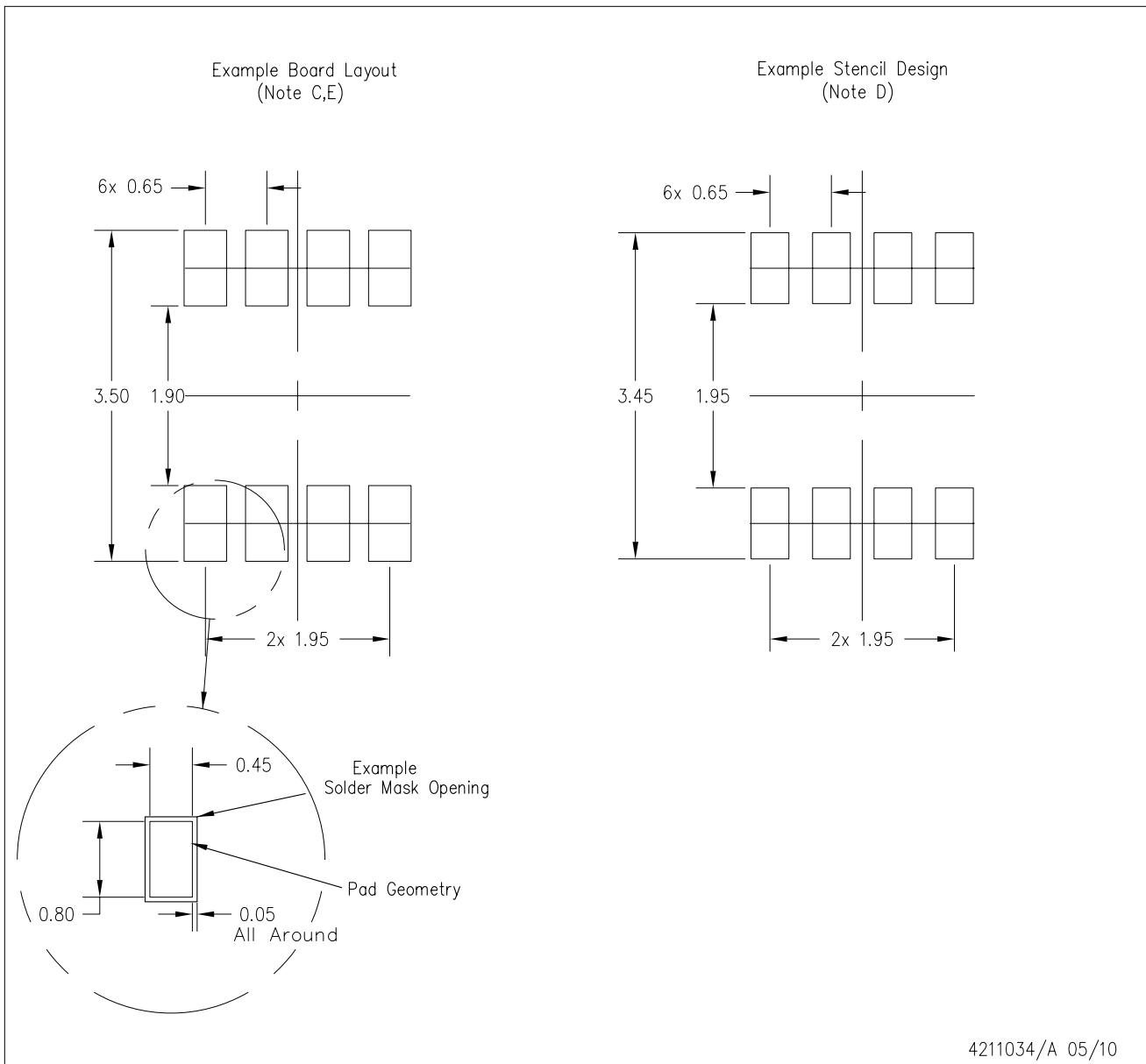
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Package outline exclusive of metal burr & dambar protrusion/intrusion.
  - D. Package outline inclusive of solder plating.
  - E. A visual index feature must be located within the Pin 1 index area.
  - F. Falls within JEDEC MO-178 Variation BA.
  - G. Body dimensions do not include flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.

DCN (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



4211034/A 05/10

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

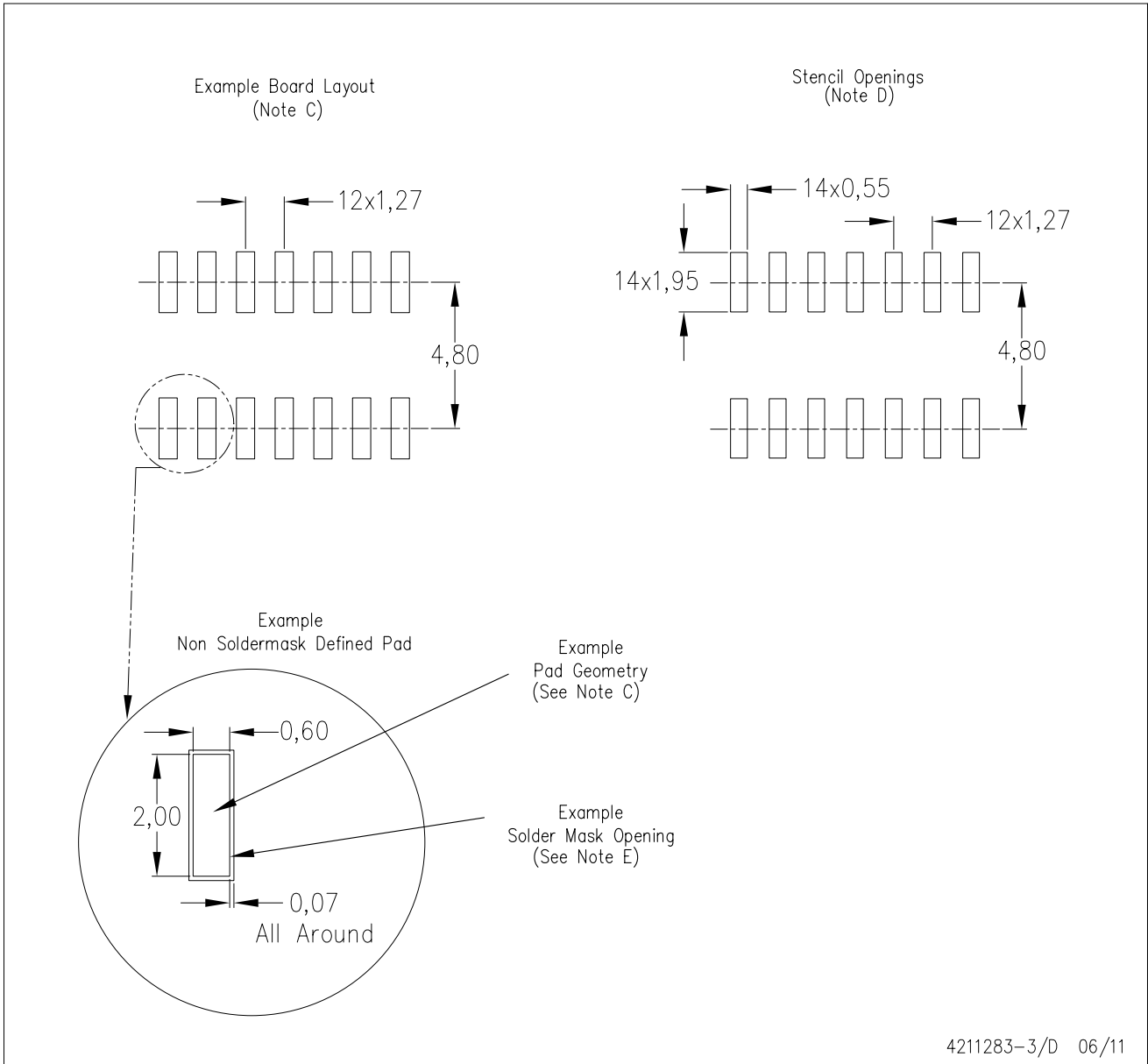


4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

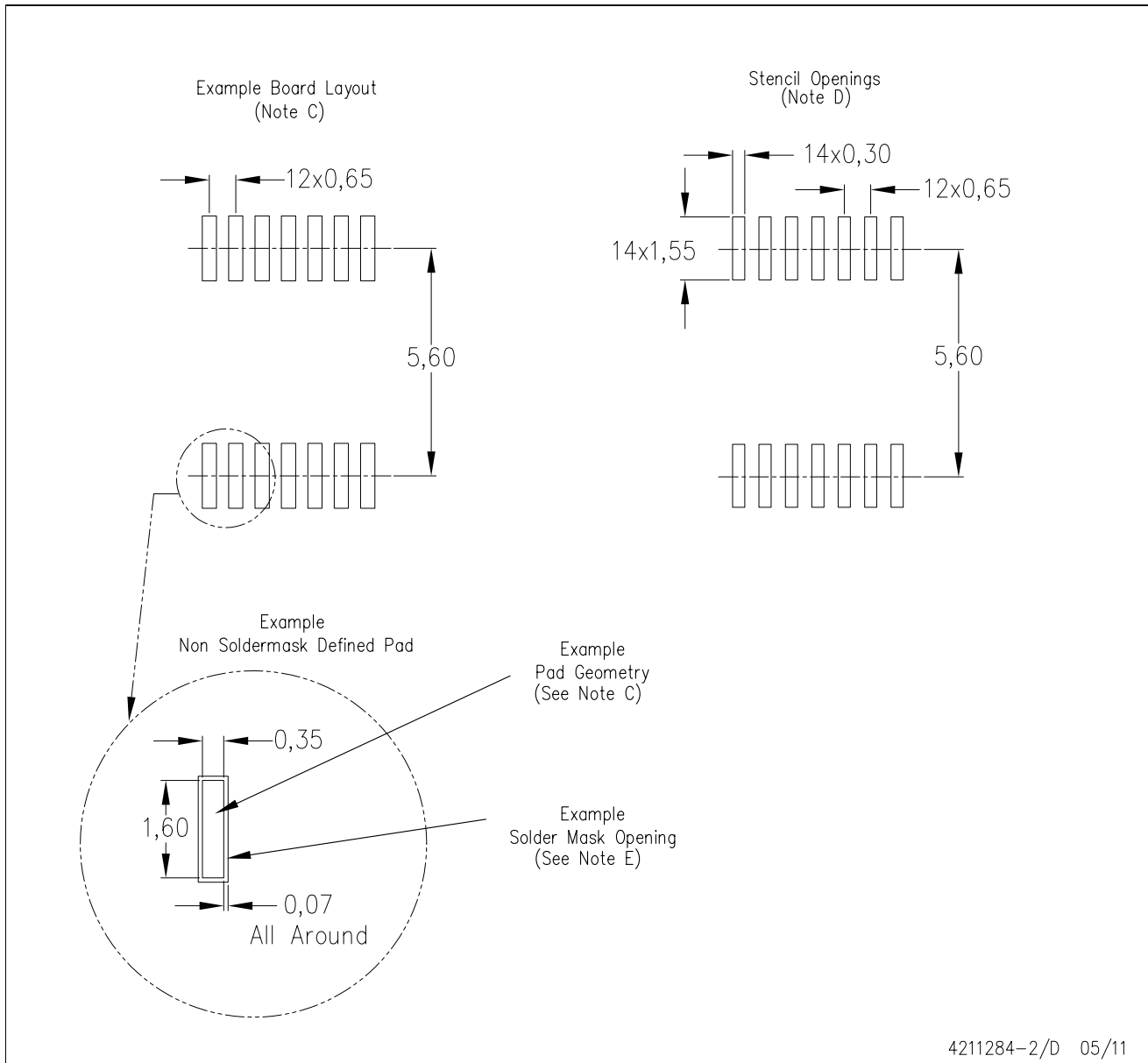
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDSO-G8)

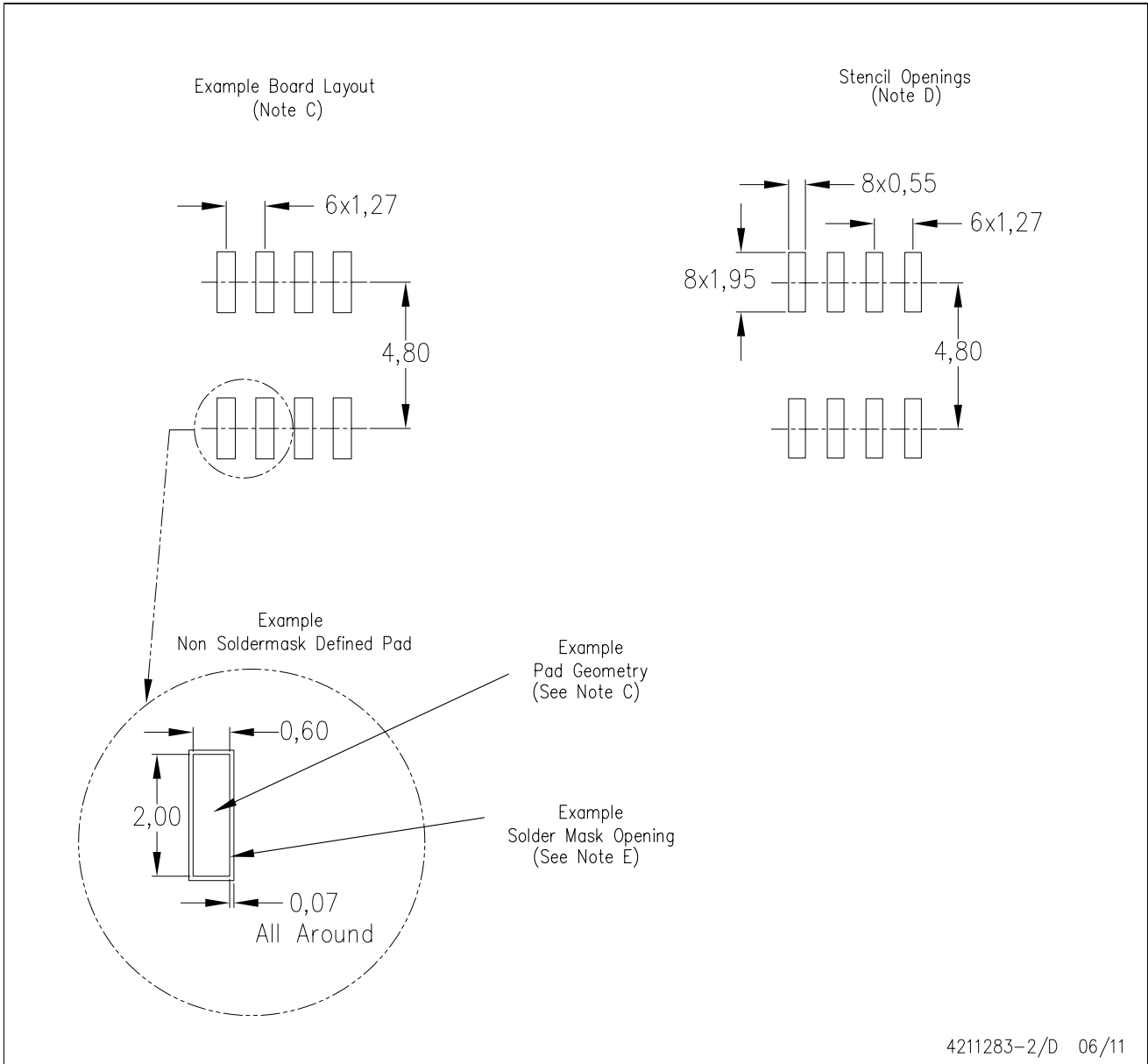
PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.  
 D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.  
 E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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