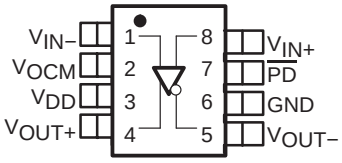
features

- **High Performance**
  - **100 MHz −3 dB Bandwidth**
  - **50 V/μs Slew Rate**
  - **−75 dB Total Harmonic Distortion at 1 MHz (V_O = 2 V_{PP})**
  - **5.4 nV/√Hz Input-Referred Noise (10 kHz)**
- **Differential Input/Differential Output**
  - **Balanced Outputs Reject Common-Mode Noise**
  - **Differential Reduced Second Harmonic Distortion**
- **Power Supply Range**
  - **V_{DD} = 3.3 V**

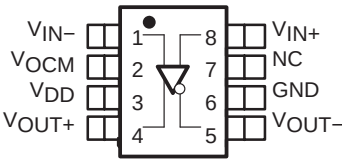
key applications

- **Simple Single-Ended To Differential Conversion**
- **Differential ADC Driver/Differential Antialiasing**
- **Differential Transmitter And Receiver**
- **Output Level Shifter**

THS4120
D, DGN, OR DGK PACKAGE
(TOP VIEW)



THS4121
D, DGN, OR DGK PACKAGE
(TOP VIEW)



description

The THS412x is one in a family of fully differential input/differential output devices fabricated using Texas Instruments' state-of-the-art submicron CMOS process.

The THS412x consists of a true fully differential signal path from input to output. This results in excellent common-mode noise rejection and improved total harmonic distortion.

HIGH-SPEED DIFFERENTIAL I/O FAMILY

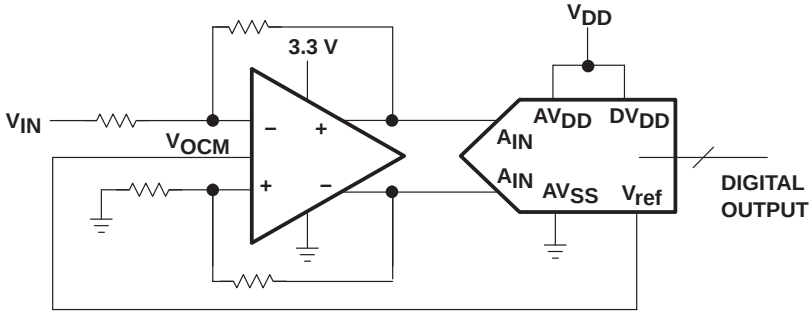
DEVICE	NUMBER OF CHANNELS	SHUTDOWN
THS4120	1	X
THS4121	1	–

RELATED DEVICES

DEVICE†	DESCRIPTION	SINGLE SUPPLY VOLTAGE RANGE	SPLIT SUPPLY VOLTAGE RANGE
THS413x	150 MHz, 51 V/μs, 1.3 nV/√Hz	5 V to 30 V	±2.5 to ±15
THS414x	160 MHz, 450 V/μs, 6.5 nV/√Hz	5 V to 30 V	±2.5 to ±15
THS415x	150 MHz, 650 V/μs, 7.6 nV/√Hz	5 V to 30 V	±2.5 to ±15

† See the TI web site for additional high speed amplifier devices.

typical A/D application circuit



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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AVAILABLE OPTIONS

T_A	PACKAGED DEVICES					EVALUATION MODULES
	SMALL OUTLINE (D)	MSOP PowerPAD™ (DGN)	SYMBOL	MSO (DGK)	SYMBOL	
0°C to 70°C	THS4120CD	THS4120CDGN	ARL	THS4120CDGK	ATZ	THS4120EVM
	THS4121CD	THS4121CDGN	ASB	THS4121CDGK	ATO	THS4121EVM
−40°C to 85°C	THS4120ID	THS4120IDGN	ARM	THS4120IDGK	ARN	−
	THS4121ID	THS4121IDGN	ASC	THS4121IDGK	ASN	−

absolute maximum ratings over operating free−air temperature range (unless otherwise noted)†

Supply voltage, GND to V_{DD} . . . . . 3.6 V
Input voltage, V_I . . . . . $\pm V_{DD}$
Output current (sink), I_O (see Note 1) . . . . . 110 mA
Differential input voltage, V_{ID} . . . . . $\pm V_{DD}$
Continuous total power dissipation . . . . . See Dissipation Rating Table
Maximum junction temperature, T_J (see Note 2) . . . . . 150°C
Maximum junction temperature, continuous operation, long term reliability, T_J (see Note 3) . . . . . 125°C
Operating free-air temperature, T_A: C suffix . . . . . 0°C to 70°C
I suffix . . . . . −40°C to 85°C
Storage temperature, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds . . . . . 300°C
ESD ratings: HBM . . . . . 4000 V
CDM . . . . . 1500 V
MM . . . . . 200 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS412x may incorporate a PowerPad™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 and SLMA004 for more information about utilizing the PowerPad™ thermally enhanced package.

NOTE 2: The absolute maximum temperature under any condition is limited by the constraints of the silicon process.

NOTE 3: The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} ‡ (°C/W)	θ_{JC} (°C/W)	POWER RATING§ T_A = 25°C	POWER RATING§ T_A = 85°C
D	97.5	38.3	1.02 W	410 mW
DGN	58.4	4.7	1.71 W	685 mW
DGK	260	54.2	385 mW	154 mW

‡ This data was taken using the JEDEC standard High−K test PCB.

§ Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	Split supply	±1.5	±1.65	±1.75	V
	Single supply	3	3.3	3.5	
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	−40		85	

PowerPAD is a trademark of Texas Instruments.

electrical characteristics, V_{DD} = 3.3 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)†

dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Small signal bandwidth (−3 dB)	V_{DD} = 3.3 V	Gain = 1, R_f = 200 Ω		100		MHz
SR	Slew rate (see Note 1)	V_{DD} = 3.3 V,	Gain = 1		55		V/μs
t_S	Settling time to 0.1%	Differential step voltage = 2 V_{PP},	Gain = 1		60		ns
	Settling time to 0.01%				292		

† The full range temperature is 0°C to 70°C for the C suffix, and −40°C to 85°C for the I suffix.
NOTE 4: Slew rate is measured differentially from an output level range of 25% to 75%.

distortion performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion Differential input, differential output Gain = 1, R_f = 200 Ω, R_L = 800 Ω, V_O = 2 V_{PP}	V_{DD} = 3.3 V	f = 1 MHz		−75		dB
THD	Total harmonic distortion Differential input, differential output Gain = 1, R_f = 200 Ω, R_L = 800 Ω, V_O = 4 V_{PP}	V_{DD} = 3.3 V	f = 1 MHz		−66		dB
Spurious free dynamic range (SFDR) Differential input, differential output, V_O = 4 V_{PP}		R_f = 200 Ω	f = 1 MHz		−69		dB
Third intermodulation distortion		V_I = 0.071 V_{RMS}	Gain = 1, f = 10 MHz		−75		dBc

† The full range temperature is 0°C to 70°C for the C suffix, and −40°C to 85°C for the I suffix.

noise performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_n	Input voltage noise	f = 10 kHz		5.4		nV/√Hz
I_n	Input current noise	f = 10 kHz		1		fA/√Hz

† The full range temperature is 0°C to 70°C for the C suffix, and −40°C to 85°C for the I suffix.

dc performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Open loop gain		T_A = 25°C	60	66		dB
		T_A = full range		66		
V_S	Input offset voltage	T_A = 25°C		3	8	mV
		T_A = full range		4	9	
	Input offset voltage, referred to V_{OCM}	T_A = 25°C		5	13	
		T_A = full range			14	
	Offset voltage drift	T_A = full range		25		μV/°C
I_{IB}	Input bias current	T_A = full range		1.2		pA
I_{OS}	Input offset current			100		fA
Current offset drift		T_A = full range		5		fA/°C

† The full range temperature is 0°C to 70°C for the C suffix, and −40°C to 85°C for the I suffix.

electrical characteristics, V_{DD} = 3.3 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted) (continued)†

input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	T_A = full range	64	96		dB
V_{ICR}	Common-mode input voltage range	T_A = full range	0.65 to V_{DD} − 0.1	0.35 to V_{DD}		V
r_i	Input resistance (dc level)	Measured into each input terminal		820		MΩ
C_i	Input capacitance, closed loop			3		pF
r_o	Output resistance	See figure 16		1		Ω

† The full range temperature is 0°C to 70°C for the C suffix, and −40°C to 85°C for the I suffix.

output characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output Voltage	V_{IC} = V_{DD}/2, V_{DD} = 3.3 V	T_A = 25°C	3.05	3.15		V
V_{OL}	Low-level output Voltage	V_{IC} = V_{DD}/2, V_{DD} = 3.3 V	T_A = 25°C	0.25	0.15		V
I_O	Output current (sink), R_L = 7 Ω	V_{DD} = 3.3 V	T_A = 25°C	80	100		mA
I_O	Output current (source), R_L = 7 Ω	V_{DD} = 3.3 V	T_A = 25°C	20	25		mA

† The full range temperature is 0°C to 70°C for the C suffix, and −40°C to 85°C for the I suffix.

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range	Single supply			3.3		V
I_{DD}	Quiescent current (per amplifier)	V_{DD} = 3.3 V	T_A = 25°C		11	13.5	mA
			T_A = full range			16	
$I_{DD(SD)}$	Quiescent current (shutdown) (THS4120)	T_A = 25°C			120		μA
		T_A = full range			130		
PSRR	Power supply rejection ratio	T_A = 25°C		68	85		dB

† The full range temperature is 0°C to 70°C for the C suffix, and −40°C to 85°C for the I suffix.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Small signal frequency response		1
SR	Slew rate		2
THD	Total harmonic distortion	vs Frequency	3
		vs Output voltage	4
	Harmonic distortion	vs Frequency	5, 6, 7
		vs Output voltage	8, 9
	Third intermodulation distortion	vs Output voltage	10
V_O	Output voltage	vs Load resistance	11
	Settling time		12
V_n	Voltage noise	vs Frequency	13
V_{OO}	Output offset voltage	vs Common-mode input voltage	14
CMMR	Common-mode rejection ratio	vs Frequency	15
z_{os}	Single-ended output impedance (closed loop)	vs Frequency	16
z_o	Single-ended (V_{OCM}) input impedance	vs Frequency	17

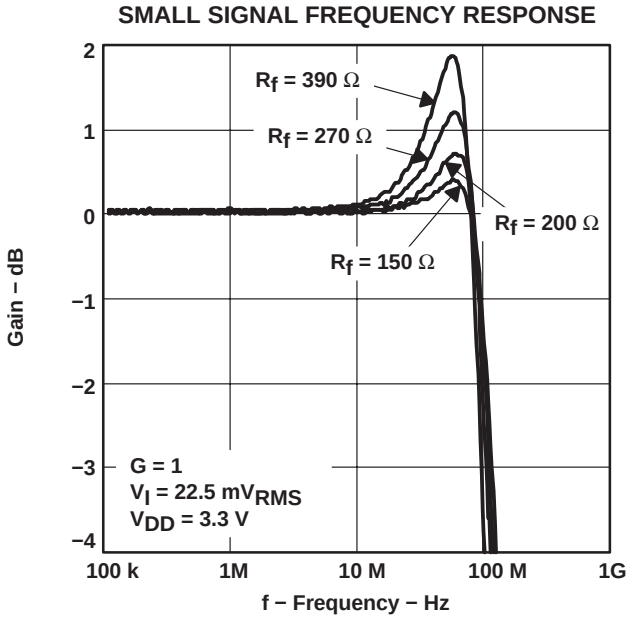


Figure 1

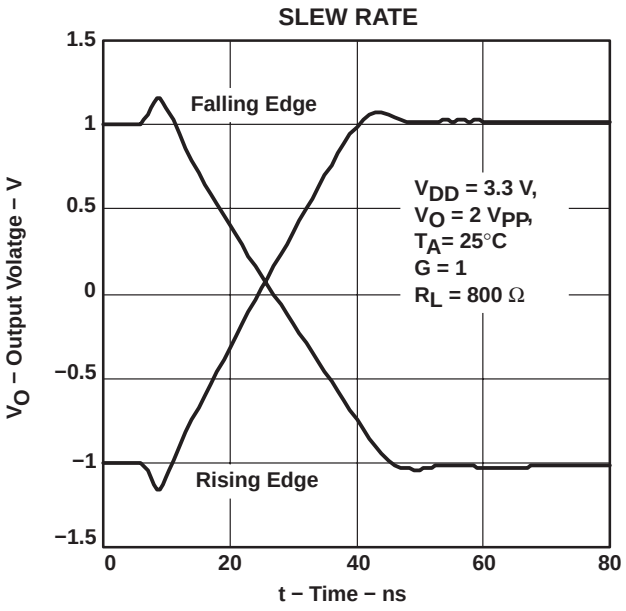


Figure 2

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

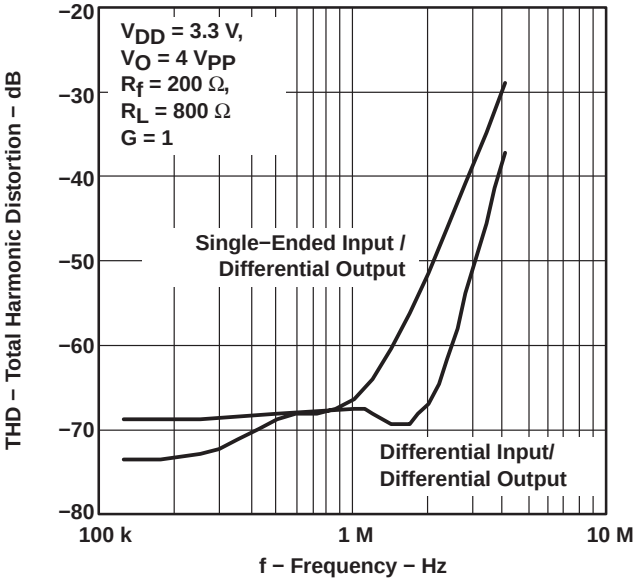


Figure 3

TOTAL HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

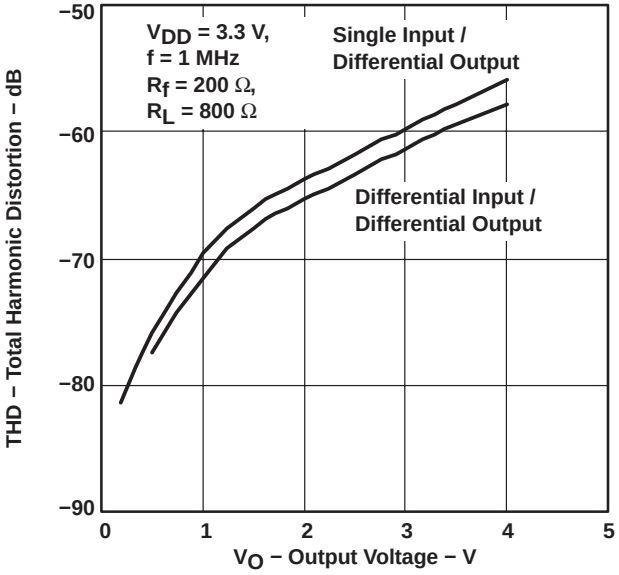


Figure 4

THS4121
HARMONIC DISTORTION
vs
FREQUENCY

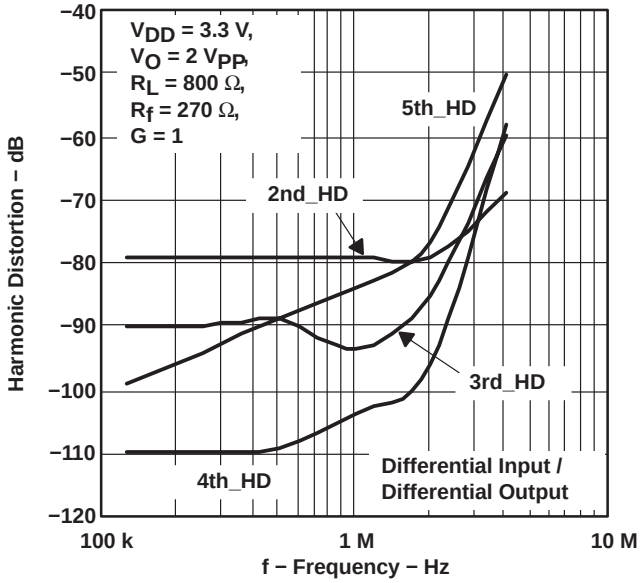


Figure 5

THS4121
HARMONIC DISTORTION
vs
FREQUENCY

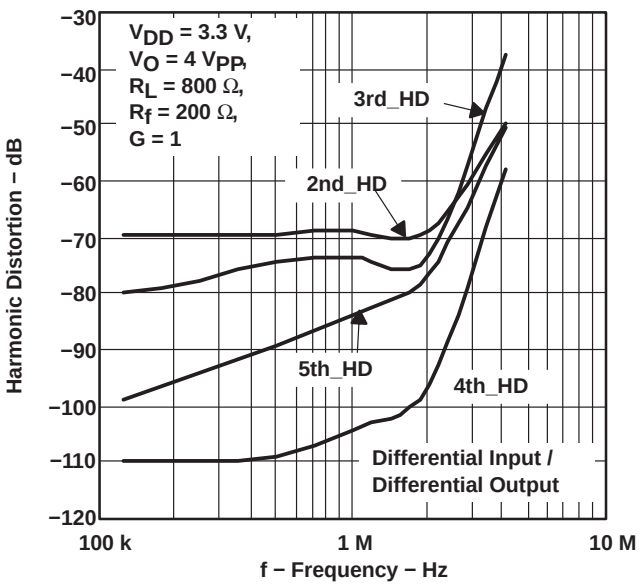


Figure 6

TYPICAL CHARACTERISTICS

THS4121
HARMONIC DISTORTION
vs
FREQUENCY

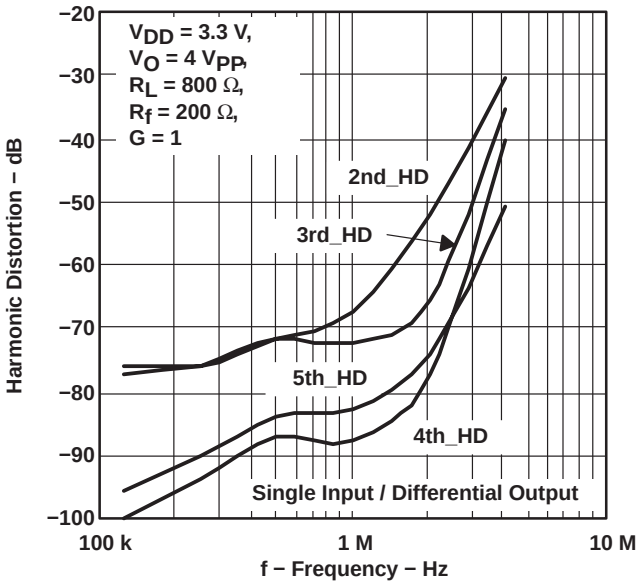


Figure 7

THS4121
HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

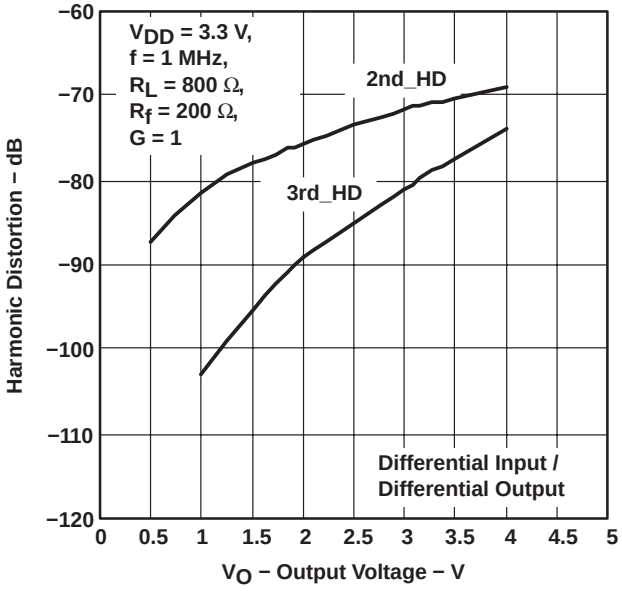


Figure 8

THS4121
HARMONIC DISTORTION
vs
OUTPUT VOLTAGE

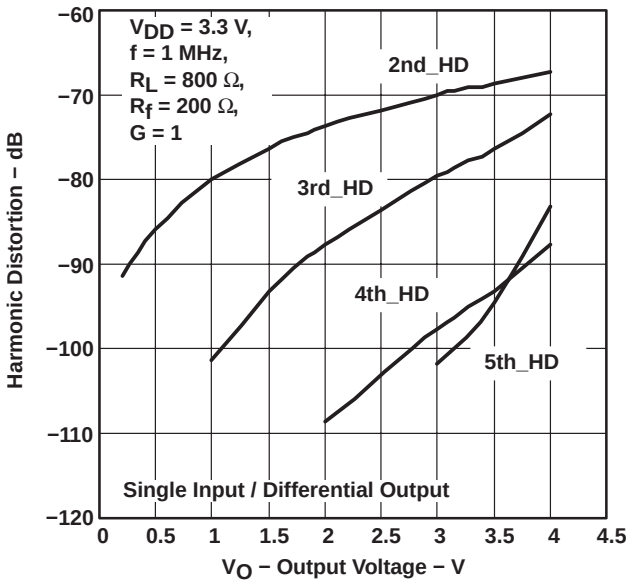


Figure 9

THIRD INTERMODULATION DISTORTION
vs
OUTPUT VOLTAGE

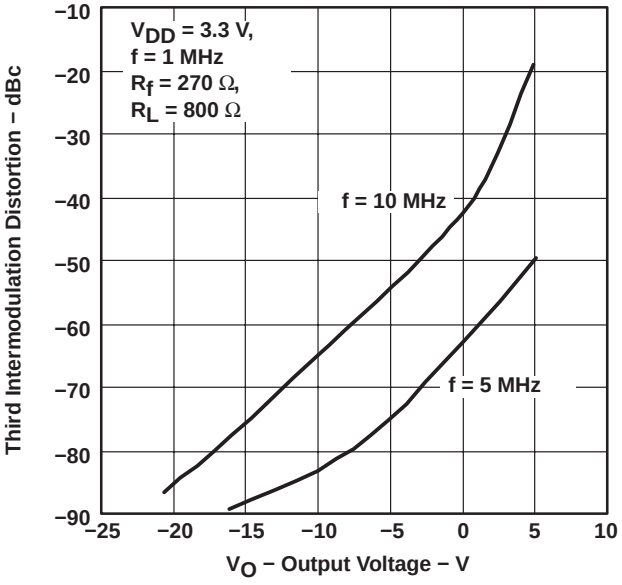


Figure 10

TYPICAL CHARACTERISTICS

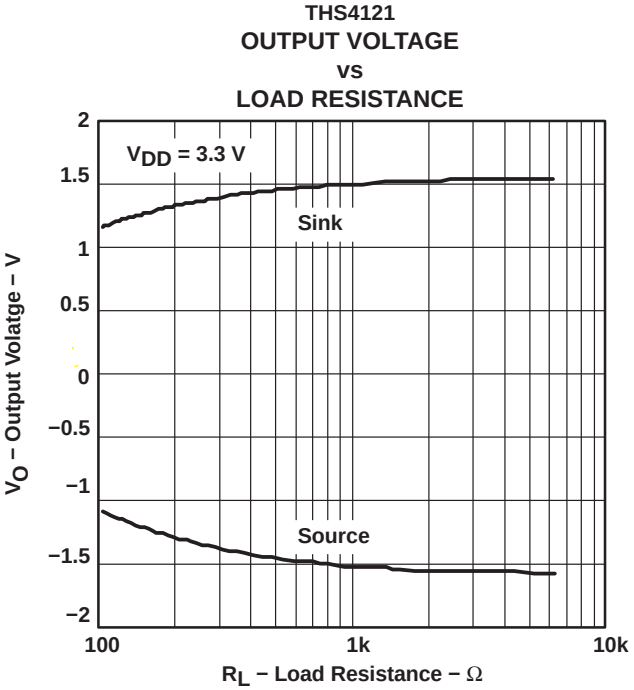


Figure 11

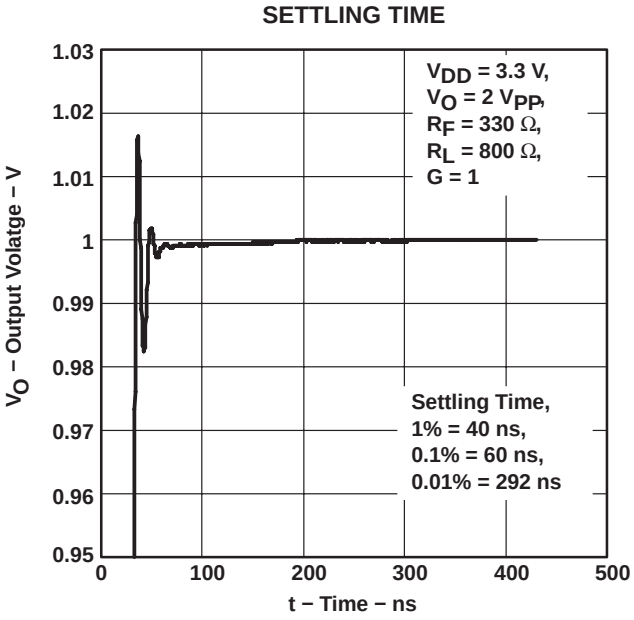


Figure 12

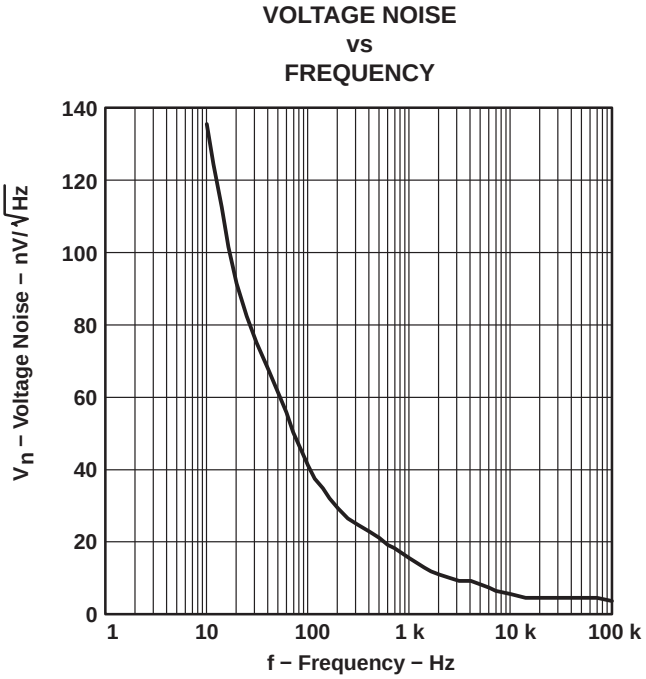


Figure 13

TYPICAL CHARACTERISTICS

OUTPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

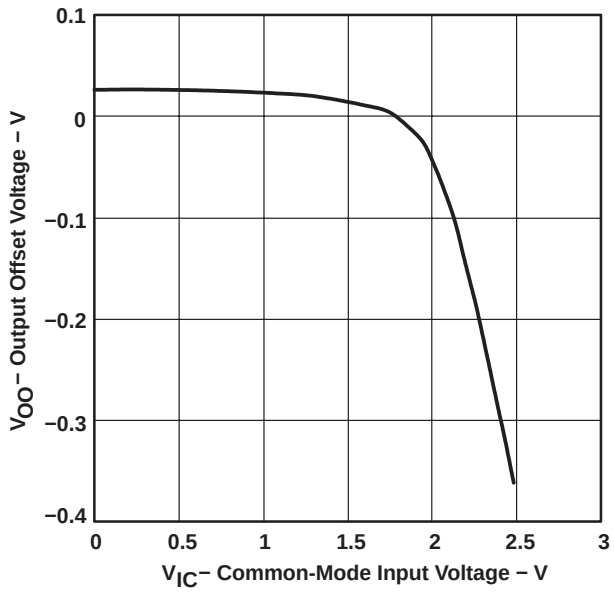


Figure 14

THS4121
COMMON-MODE REJECTION RATIO vs FREQUENCY

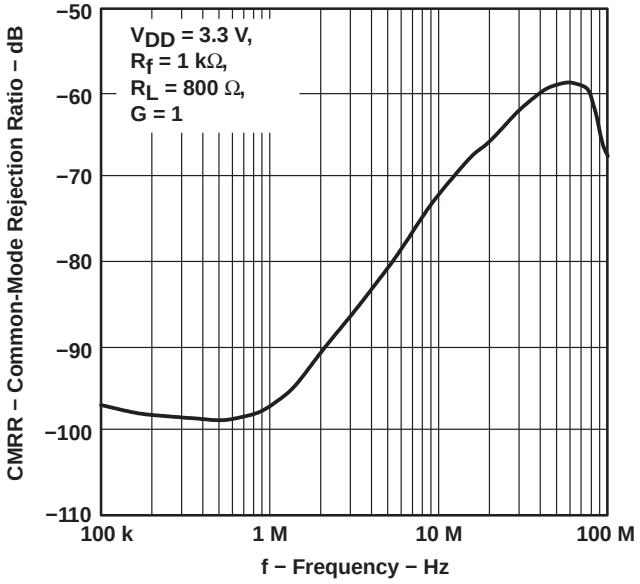


Figure 15

THS4121
SINGLE-ENDED OUTPUT IMPEDANCE vs FREQUENCY

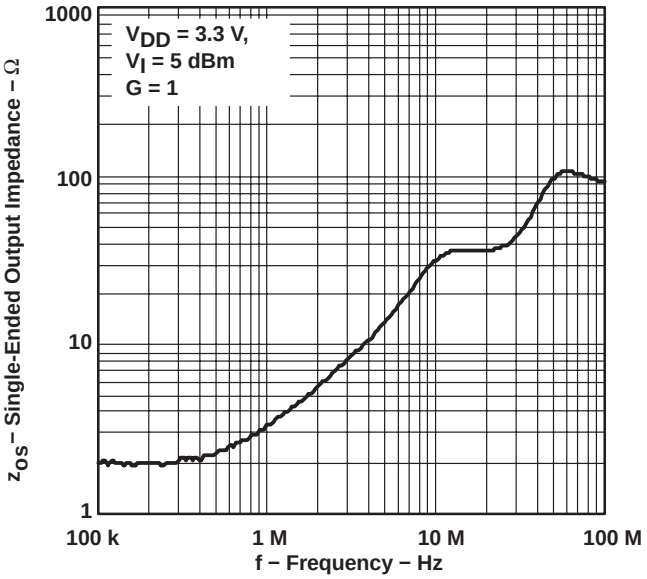


Figure 16

THS4121
SINGLE-ENDED (V_{OCM}) INPUT IMPEDANCE vs FREQUENCY

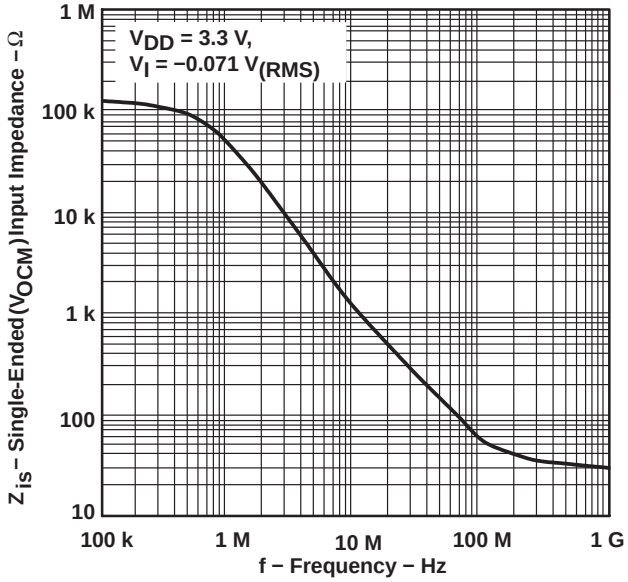


Figure 17

APPLICATION INFORMATION

resistor matching

Resistor matching is important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion will diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM} pin, it will be set to the midrail voltage internally defined as:

$$\frac{\left(V_{DD}\right) + \left(V_{SS}\right)}{2}$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input with the gain of 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a 0.1 µF capacitor on the V_{OCM} pin as a bypass capacitor. The following graph shows the simplified diagram of the THS412x.

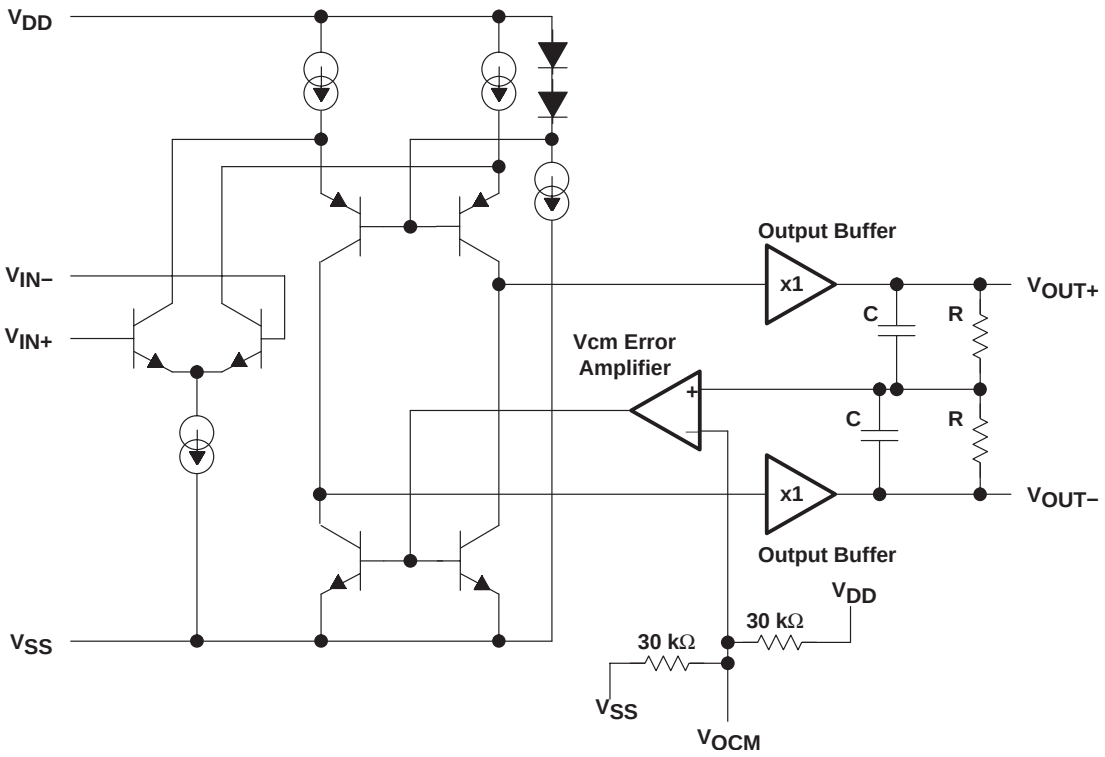


Figure 18. THS412x Simplified Diagram

APPLICATION INFORMATION

data converters

Data converters are one of the most popular applications for the fully differential amplifiers.

Fully differential amplifiers can operate with a single supply. V_{OCM} defaults to the midrail voltage, $V_{DD}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor for stability. For proper operation, the input common-mode voltage to the input terminal of the amplifier should not exceed the common-mode input voltage range.

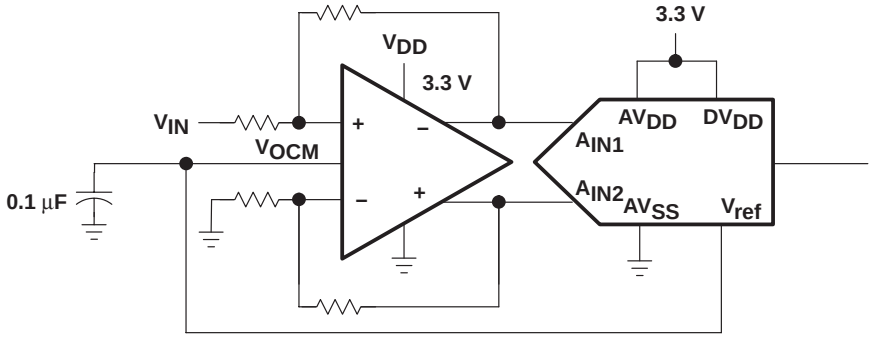


Figure 19. Differential Amplifier Using a Single Supply

Some single supply applications may require the input voltage to exceed the common-mode input voltage range. In such cases, the following circuit configuration is suggested to bring the common-mode input voltage within the specifications of the amplifier.

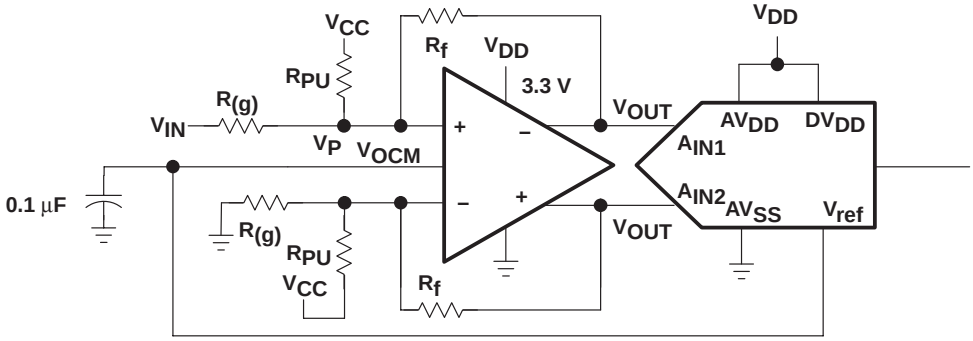


Figure 20. Circuit With Improved Common-Mode Input Voltage

The following equation is used to calculate R_{PU}:

$$R_{PU} = \frac{V_P - V_{DD}}{\left(V_{IN} - V_P\right)\frac{1}{R_{(g)}} + \left(V_{OUT} - V_P\right)\frac{1}{R_f}}$$

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS412x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 21. A minimum value of 20 Ω should work well for most applications. For example, in 50-Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

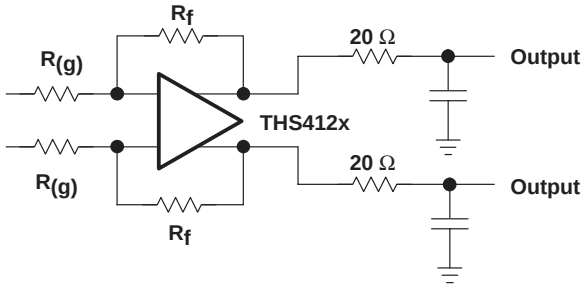


Figure 21. Driving a Capacitive Load

Active antialias filtering

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high frequency noise with the frequency of operation. The following figure presents a method by which the noise may be filtered in the THS412x. Proper ground referencing should be considered.

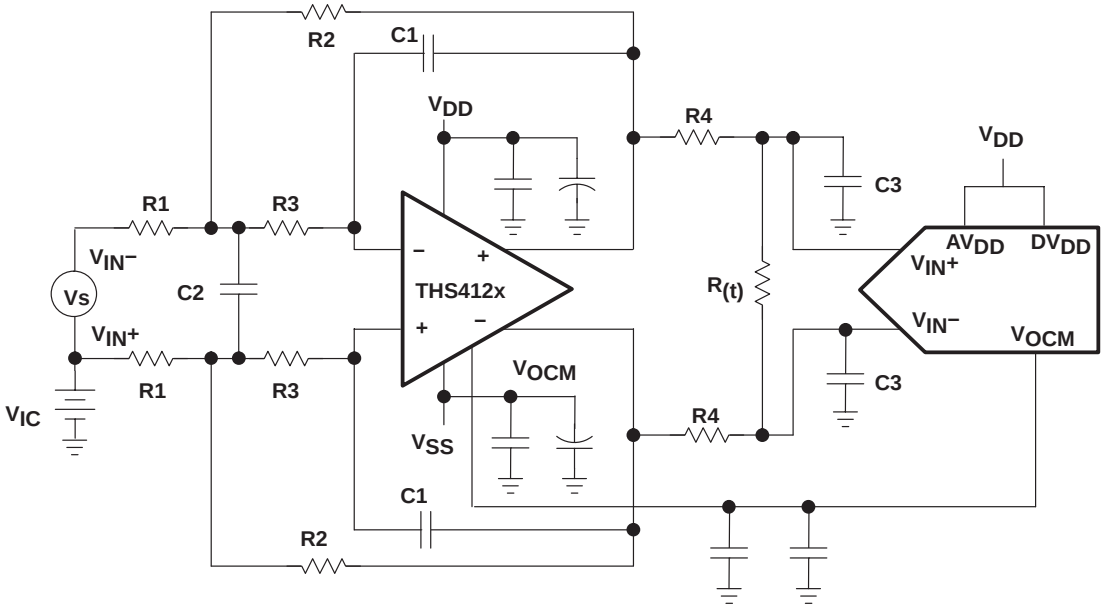


Figure 22. Antialias Filtering

APPLICATION INFORMATION

Active antialias filtering (continued)

The transfer function for this filter circuit is:

$$H_d(f) = \left(\frac{K}{-\left(\frac{f}{FSF \times fc}\right)^2 + \frac{1}{Q}\frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi fR4RtC3}{2R4 + Rt}} \right) \quad \text{Where } K = \frac{R2}{R1}$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2R3C1C2}} \text{ and } Q = \frac{\sqrt{2 \times R2R3C1C2}}{R3C1 + R2C1 + KR3C1}$$

K sets the pass band gain, fc is the cutoff frequency for the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \text{ and } Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re}$$

Where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi RC\sqrt{2 \times mn}} \text{ and } Q = \frac{\sqrt{2 \times mn}}{1 + m(1 + K)}$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

PRINCIPLES OF OPERATION

theory of operation

The THS412x is a fully differential amplifier. Differential amplifiers are typically *differential in/single out*, whereas fully differential amplifiers are *differential in/differential out*.

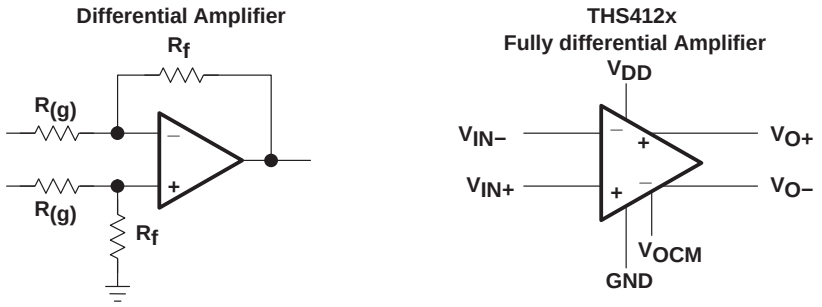


Figure 23. Differential Amplifier Versus a Fully Differential Amplifier

To understand the THS412x fully differential amplifiers, the definition for the pinouts of the amplifier are provided.

Input voltage definition $V_{ID} = (V_{I+}) - (V_{I-})$ $V_{IC} = \frac{(V_{I+}) + (V_{I-})}{2}$

Output voltage definition $V_{OD} = (V_{O+}) - (V_{O-})$ $V_{OC} = \frac{(V_{O+}) + (V_{O-})}{2}$

Transfer function $V_{OD} = V_{ID} \times A_{(f)}$

Output common mode voltage $V_{OC} = V_{OCM}$

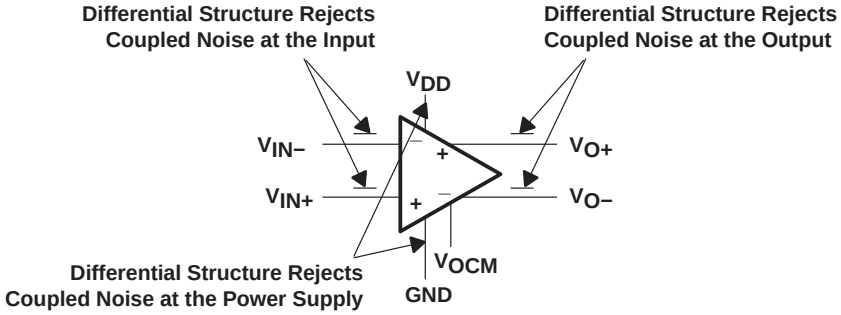


Figure 24. Definition of the Fully Differential Amplifier

PRINCIPLES OF OPERATION

theory of operation (continued)

The following schematics depict the differences between the operation of the THS412x, fully differential amplifier, in two different modes. Fully differential amplifiers can work with differential input or can be implemented as single in/differential out.

Note: For proper operation, maintain symmetry by setting
$R_f1 = R_f2 = R_f$ and $R_{(g)}1 = R_{(g)}2 = R_{(g)}$
$\Rightarrow A = R_f/R_{(g)}$

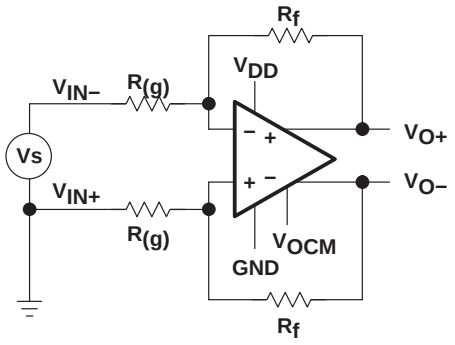
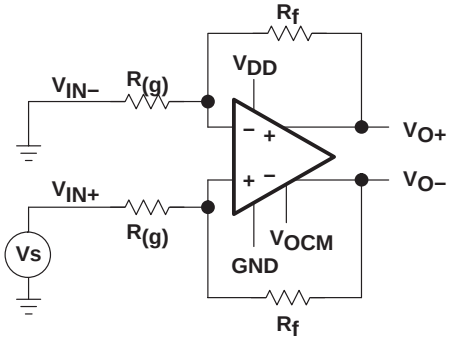


Figure 25. Amplifying Differential Signals



RECOMMENDED RESISTOR VALUES

GAIN	$R_{(g)}$ Ω	R_f Ω
1	150	150

Figure 26. Single In With Differential Out

If each output is measured independently, each output is one-half of the input signal when gain is 1. The following equations express the transfer function for each output:

$$V_O = \frac{1}{2} V_I$$

The second output is equal and opposite in sign:

$$V_O = -\frac{1}{2} V_I$$

Fully differential amplifiers may be viewed as two inverting amplifiers. In this case, the equation of an inverting amplifier holds true for gain calculations. One advantage of fully differential amplifiers is that they offer twice as much dynamic range compared to single-ended amplifiers. For example, a 1-V_{PP} ADC can only support an input signal of 1 V_{PP}. If the output of the amplifier is 2 V_{PP}, then it will not be practical to feed a 2-V_{PP} signal into the targeted ADC. Using a fully differential amplifier enables the user to break down the output into two 1-V_{PP} signals with opposite signs and feed them into the differential input nodes of the ADC. In practice, the designer has been able to feed a 2-V peak-to-peak signal into a 1-V differential ADC with the help of a fully differential amplifier. The final result indicates twice as much dynamic range. Figure 27 illustrates the increase in dynamic range. The gain factor should be considered in this scenario. The THS412x fully differential amplifier offers an improved CMRR and PSRR due to its symmetrical input and output. Furthermore, second harmonic distortion is improved. Second harmonics tend to cancel because of the symmetrical output.

PRINCIPLES OF OPERATION

theory of operation (continued)

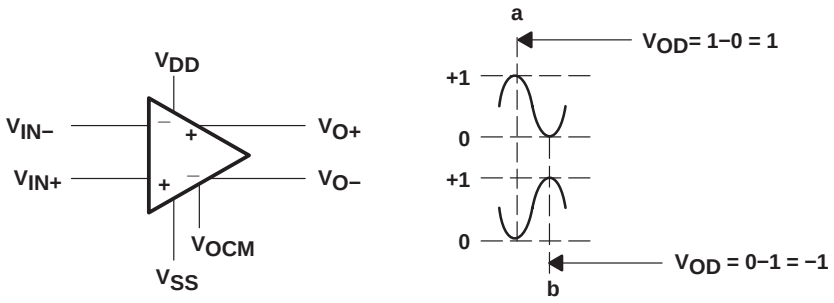


Figure 27. Fully Differential Amplifier With Two 1-V_{PP} Signals

circuit layout considerations

To achieve the levels of high frequency performance of the THS412x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS412x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes − It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling − Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets − Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements − Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components − Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

PRINCIPLES OF OPERATION

power-down mode

Due to the similarity of the standard inverting amplifier configuration, the output impedance appears to be very low while in the power-down state. This is because the feedback resistor (R_f) and the gain resistor ($R_{(g)}$) are still connected to the circuit. Therefore, a current path is allowed between the input of the amplifier and the output of the amplifier. An example of the closed loop output impedance is shown in Figure 28.

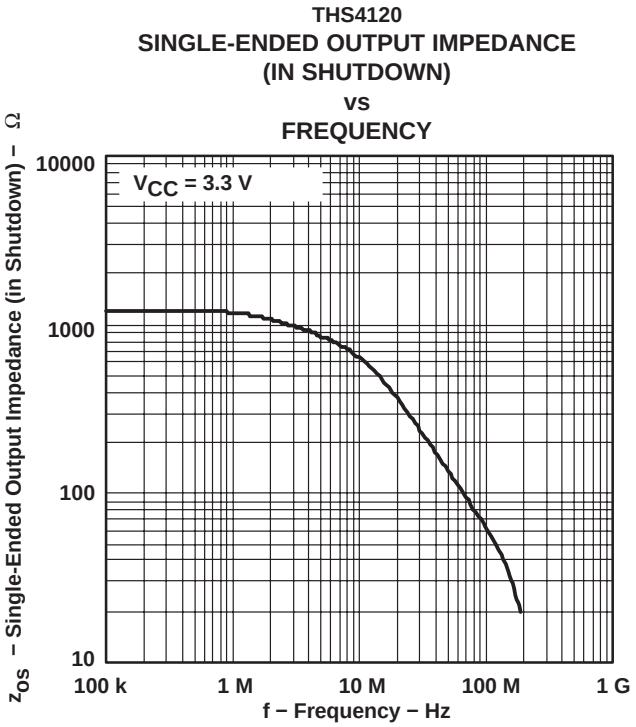


Figure 28

PRINCIPLES OF OPERATION

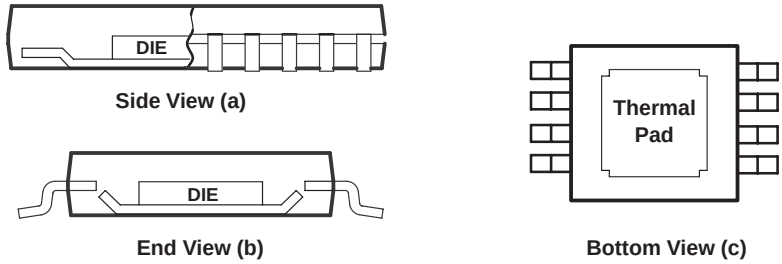
general PowerPAD design considerations (applicable to differential amplifier family)

The THS412x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 29(a) and Figure 29(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 29(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

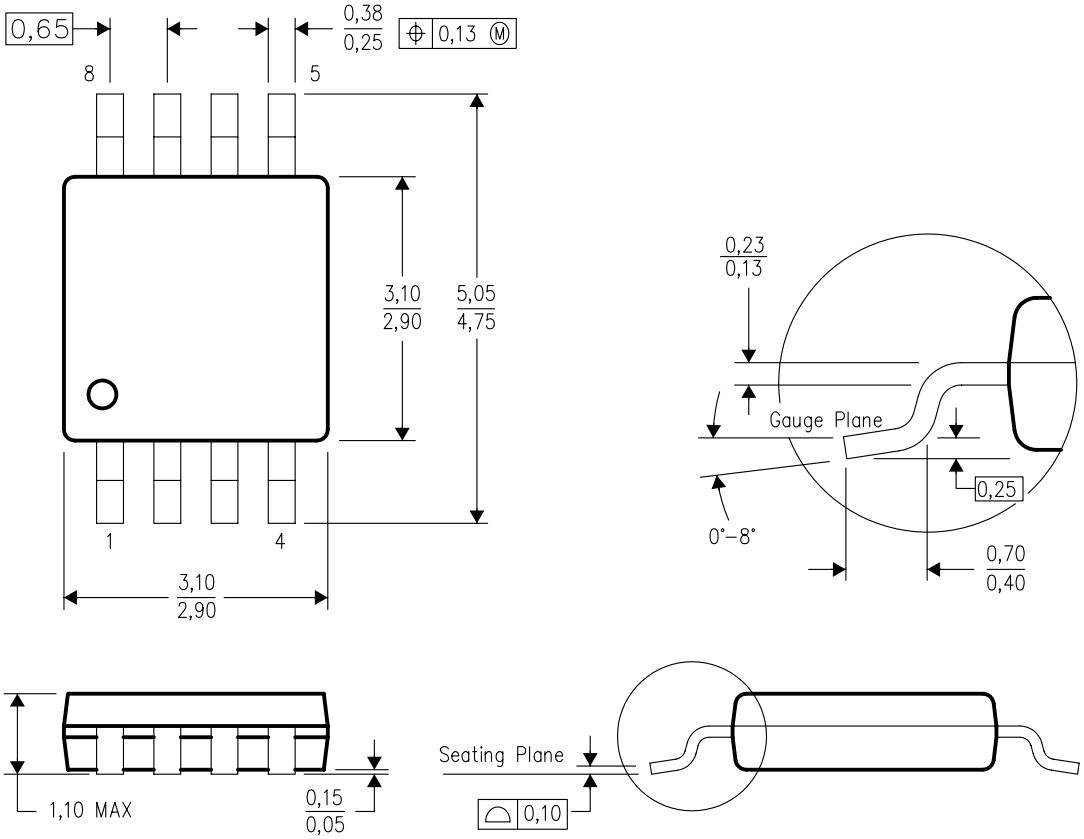
More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package (SLMA002).* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 29. Views of Thermally Enhanced DGN Package

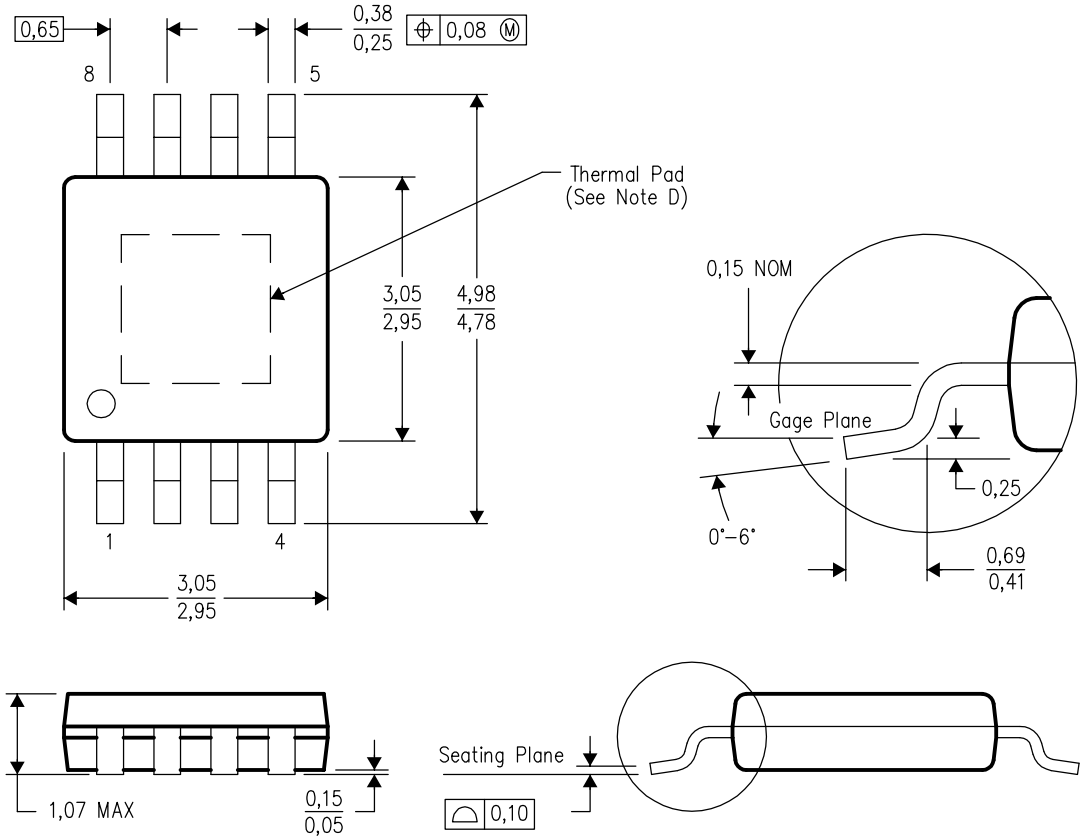
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/D 12/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation AA.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



4073271/C 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187

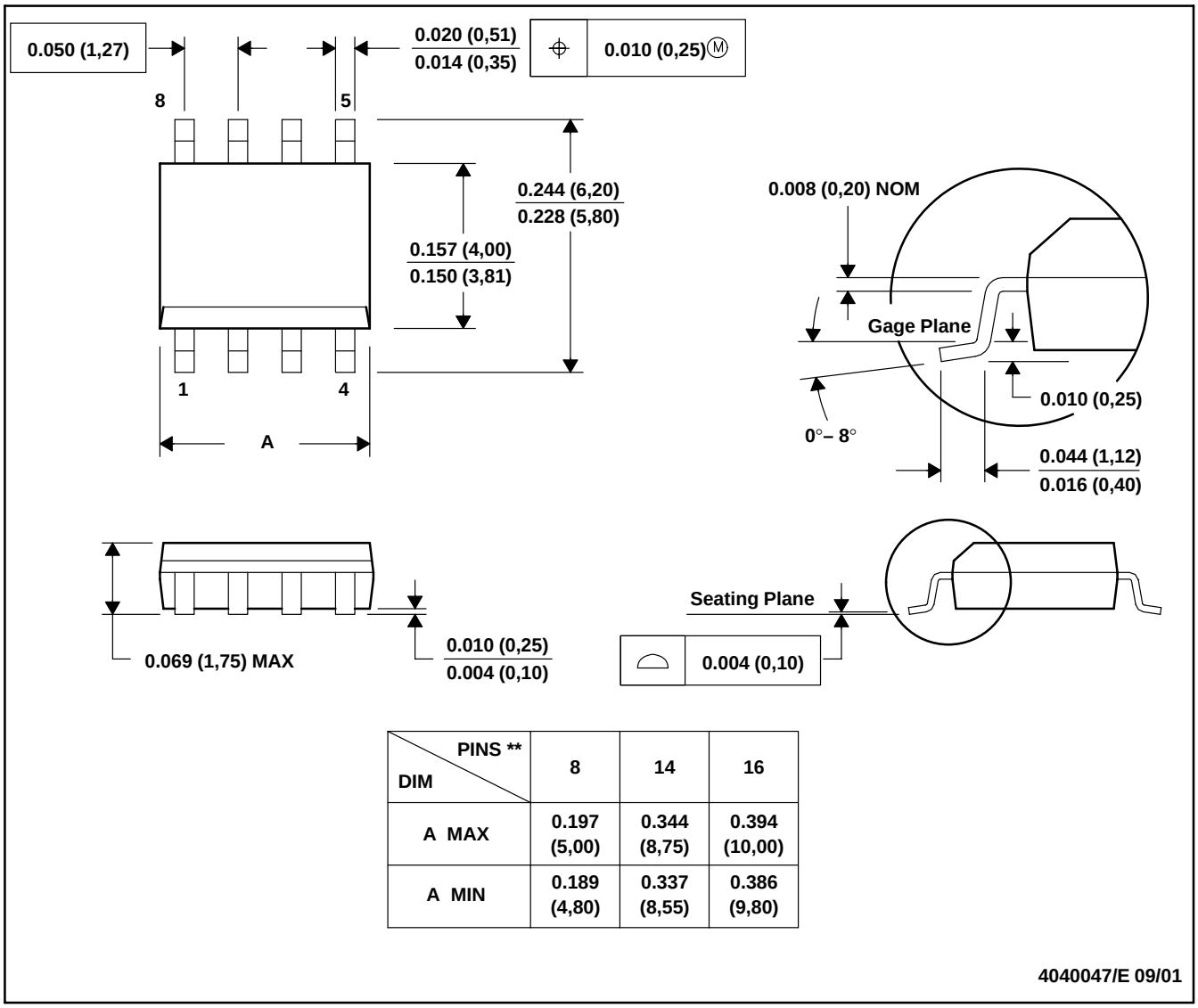
PowerPAD is a trademark of Texas Instruments.

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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