SLLS266E − FEBRUARY 1997 − REVISED NOVEMBER 2003

USB PORT TRANSIENT SUPPRESSORS

FEATURES

- **Design to Protect Submicron 3-V or 5-V Circuits from Noise Transients**
- **Port ESD Protection Capability Exceeds:**
  - **15-kV Human Body Model**
  - **2-kV Machine Model**
- **Available in a WCSP Chip-Scale Package**
- **Stand-Off Voltage . . . 6.0 V Min**
- **Low Current Leakage . . . 1 μA Max at 6 V**
- **Low Capacitance . . . 35 pF Typ**

DESCRIPTION

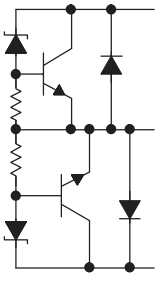
The SN65220 is a single transient voltage suppressor and the SN65240 and SN75240 are dual transient voltage suppressors designed to provide electrical noise transient protection to Universal Serial Bus (USB) 1.1 ports. Note that the input capacitance of the device makes it unsuitable for high-speed USB 2.0 applications.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the USB transceiver and/or the USB ASIC if they are of sufficient magnitude and duration.

USB ports are typically implemented in 3-V or 5-V digital CMOS with very limited ESD protection. The SN65220, SN65240, and SN75240 can significantly increase the port ESD protection level and reduce the risk of damage to the circuits of the USB port.

The IEC1000-4-2 ESD performance of the SN65220, SN65240, and SN75240 is measured at the system level. Therefore, system design impacts the results of these tests. A high compliance level may be attained with proper board design and layout.

EQUIVALENT SCHEMATIC DIAGRAM



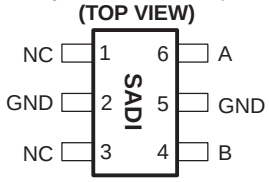
(One SN65240 or SN75240 Suppressor Shown)

NOTE: All four GND terminals should be connected to ground.

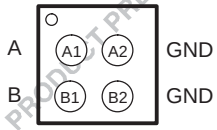
APPLICATIONS

- **USB 1.1 Host, Hub, or Peripheral Ports**

SN65220DBV
(Marked as **SADI**†**)**
(TOP VIEW)



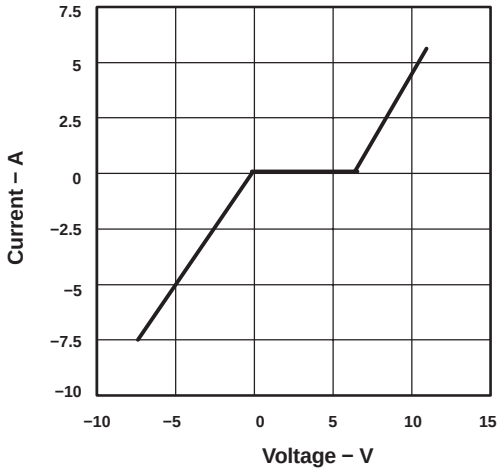
SN65220YZB
(Size: 925.38 μm x 925.38 μm ±6.34μm)
(TOP VIEW)



NC − No internal connection
†When read horizontally, Pin 1 is the bottom left pin.

SN65240P, SN65240PW
(Marked as **A65240P or A65240PW)**
SN75240P, SN75240PW
(Marked as **A75240P or A75240PW)**
(TOP VIEW)

CURRENT vs VOLTAGE



NOTE A: Typical current versus voltage curve was derived using the IEC 1.2/50-μs surge waveform.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

IEC1000-4-2 COMPLIANCE LEVEL

IEC1000-4-2 COMPLIANCE LEVEL	MAXIMUM TEST VOLTAGE	
	CONTACT DISCHARGE (kV)	AIR DISCHARGE (kV)
1	2	2
2	4	4
3	6	8
4	8	15

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	T_A	MARKED AS	SUPRESSORS	ORDER NUMBER
SN65220	WCSP−4	YZB	−40°C to 85°C	NWP	1	SN65220YZBR (Reel)
	SOT23−6	DBV		SADI	1	SN65220DBVR (Reel)
					1	SN65220DBVT (Mini Reel)
SN65240	DIP−8	P	−40°C to 85°C	A65240	2	SN65240P (Rail)
	TSSOP−8	PW			2	SN65240PW (Rail)
					2	SN65240PWR (Reel)
SN75240	DIP−8	P	0°C to 70°C	A75240	2	SN75240P (Rail)
	TSSOP−8	PW			2	SN75240PW (Rail)
					2	SN75240PWR (Reel)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Continuous power dissipation	See Dissipation Rating Table
Electrostatic discharg	15 kV(2), 2 kV(3)
Peak power dissipation, $P_{D(peak)}$	60 W
Peak forward surge current, I_{FSM}	3 A
Peak reverse surge current, I_{RSM}	−9 A
Storage temperature range, T_{stg}	−65°C to 150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Human Body Model − Tested in accordance with JEDEC Standard 22, Test Method A114−A.

(3) Charged Device Model − Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	385 mW	3.1 mW/°C	246 mW	200 mW
P	1150 mW	9.2 mW/°C	736 mW	598 mW
PW	520 mW	4.2 mW/°C	331 mW	268 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

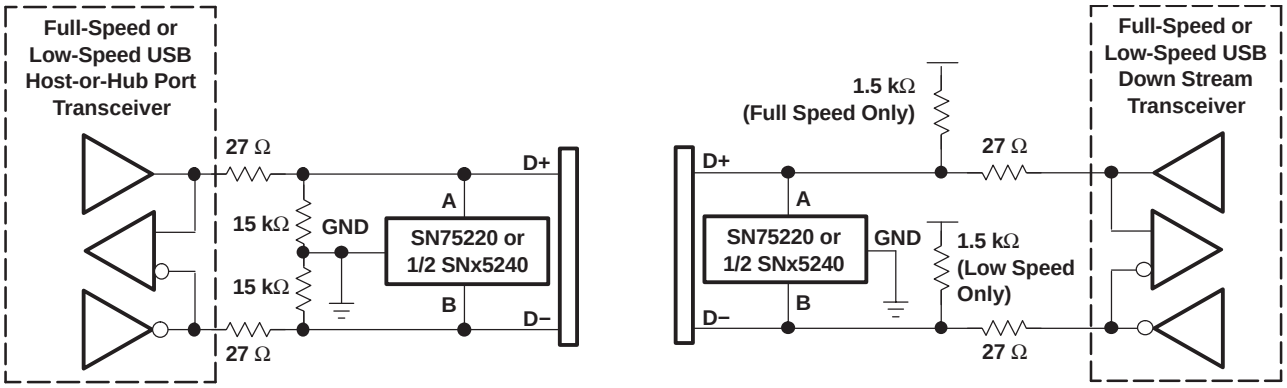
recommended operating conditions

		MIN	MAX	UNIT
Operating free-air temperature, T_A	SN75240	0	70	°C
	SN65220, SN65240	−40	85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

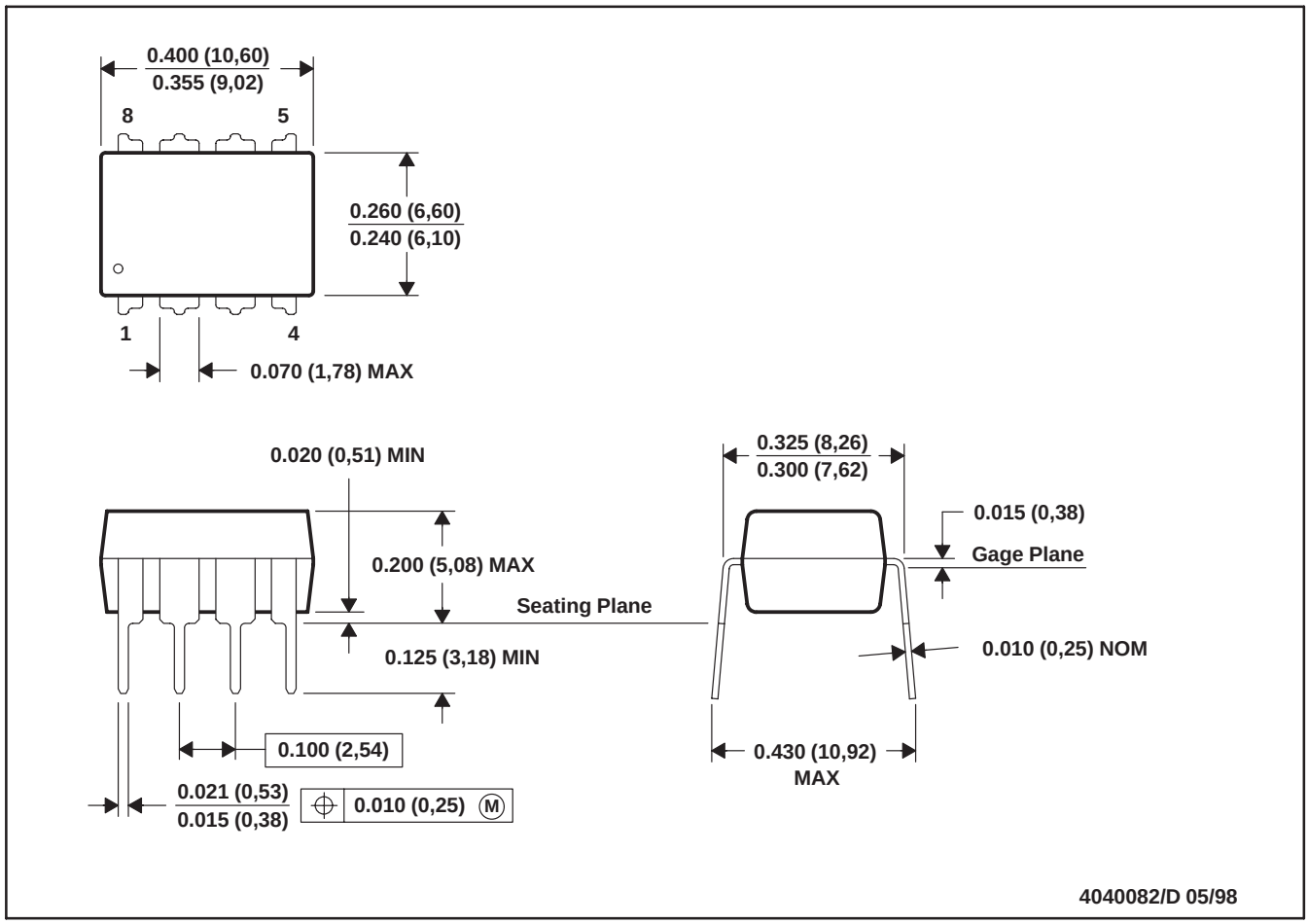
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{lkg}	Leakage current	V_I = 6 V at A, B, C, or D terminals			1	μA
$V_{(BR)}$	Breakdown voltage	V_I = 1 mA at A, B, C, or D terminals	6.5	7	8	V
C_{IN}	Input capacitance to ground	V_I = 0.4 sin (4E6πt) + 0.5 V		35		pF

APPLICATION INFORMATION



MPDI001A – JANUARY 1995 – REVISED JUNE 1999

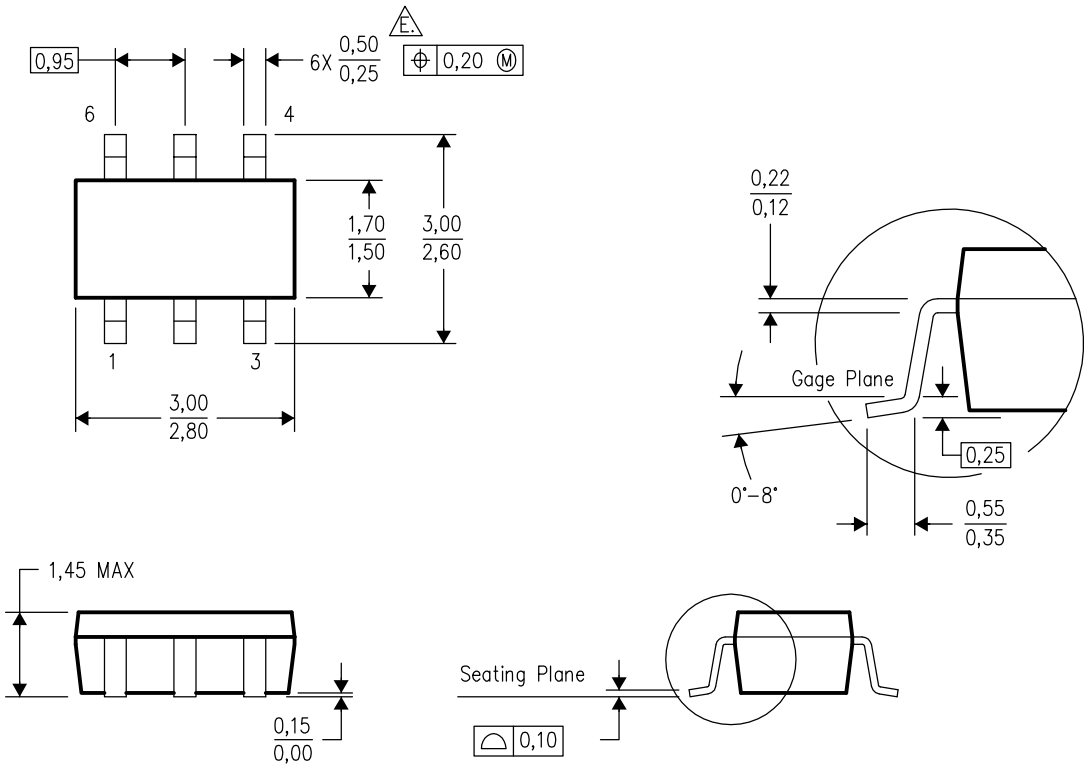
P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE

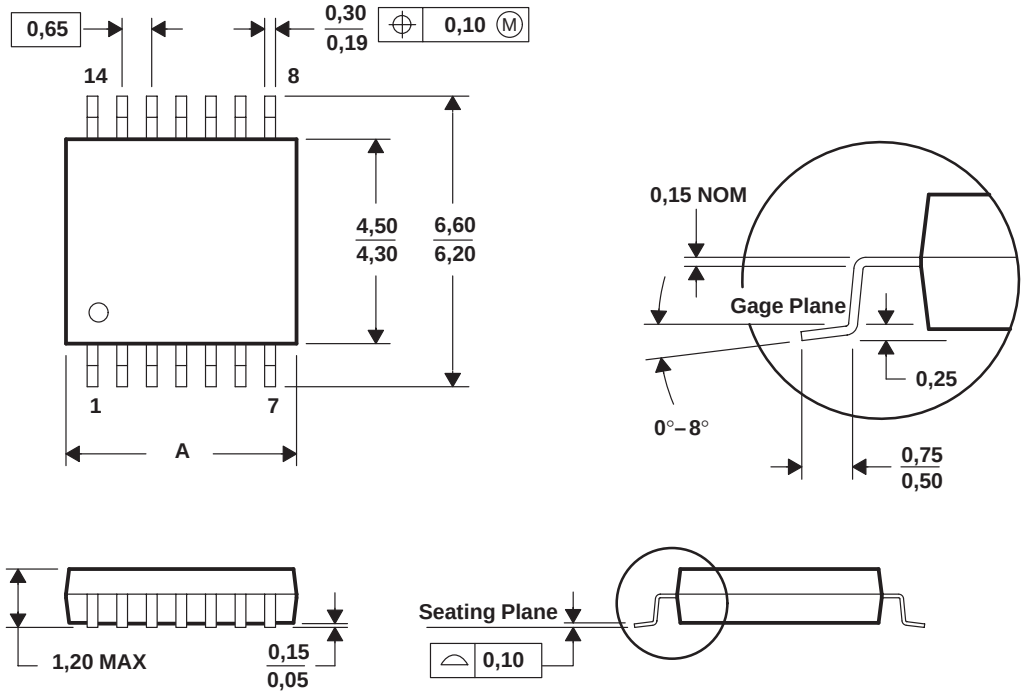


4073253–5/H 10/2003

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

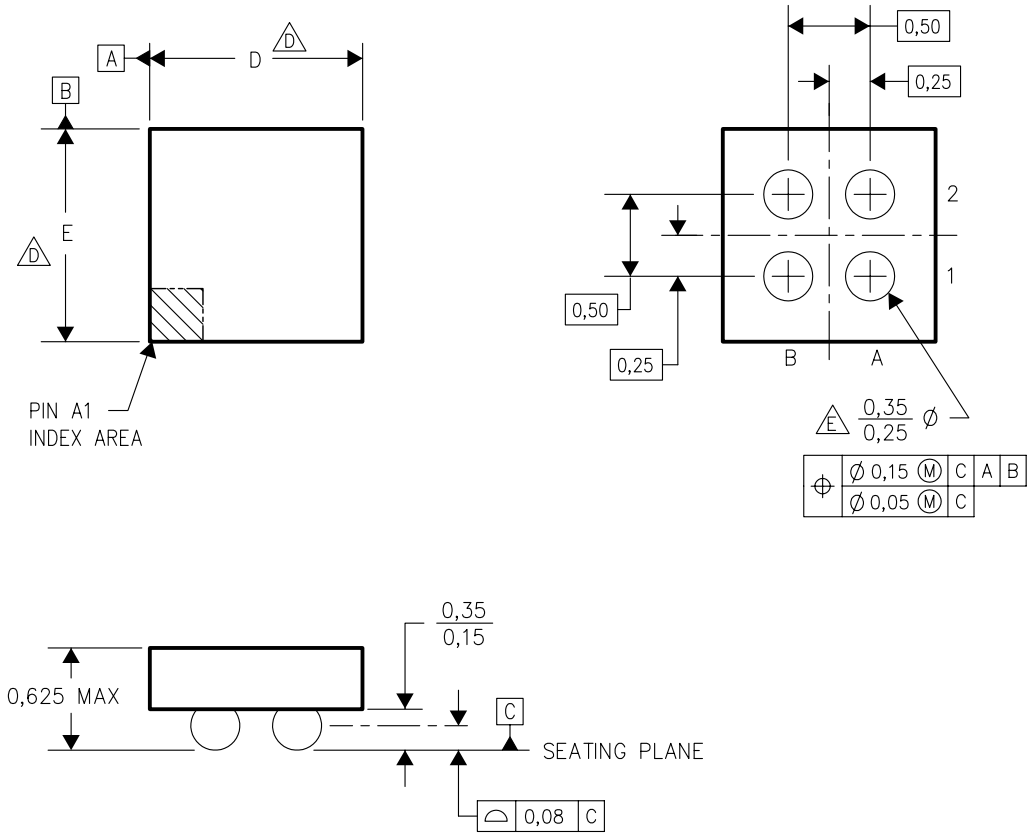


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

YZB (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



4205055/C 05/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZB package can have dimension D ranging from 0.85 to 1.65 mm and dimension E ranging from 0.85 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YEB (Drawing #4204178) for tin–lead (SnPb) balls.

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