

## 5-V, LOW POWER, 16-BIT, 200-KSPS SERIAL ANALOG-TO-DIGITAL CONVERTERS WITH AUTO-POWER DOWN

### FEATURES

- 200-KSPS Sampling Rate
- Built-In Conversion Clock
- INL:  $\pm 2.5$  LSB Max,  
DNL: 2 to -1 LSB Max
- SINAD = 84.5 dB, SFDR = 95 dB,  
THD = 94 dB at 15 kHz  $f_{in}$ , 200 KSPS
- SPI/DSP-Compatible Serial Interfaces With  
SCLK Input up to 15 MHz
- Single 5-V Supply
- Rail-to-Rail Analog Input With 500 kHz BW
- Two Input Options Available:
  - TLC4541 – Single Channel Input
  - TLC4545 – Single Channel,  
Pseudo-differential Input
- (TLC4541) Optimized DSP Interface –  
Requires FS Input Only
- Low Power With Auto-Power Down
  - Operating Current: 3.5 mA
  - Auto-Power Down Current: 5  $\mu$ A
- Pin Compatible 12/14/16-Bit Family in 8-Pin  
SOIC and MSOP Packages

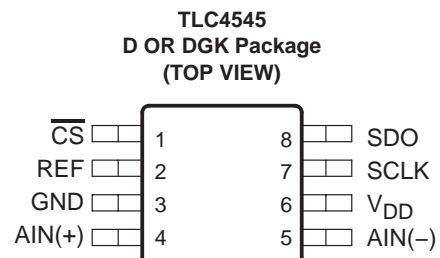
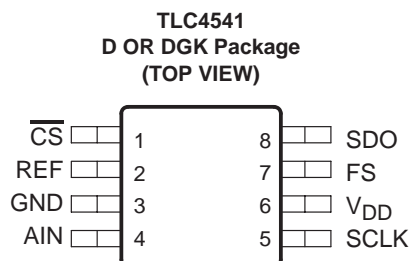
### APPLICATIONS

- ATE System
- Industrial Process Control
- Measurement
- Motor Control

### DESCRIPTION

The TLC4541 and TLC4545 are a family of high performance, 16-bit, low power, miniature CMOS analog-to-digital converters (ADCs). These devices operate from a single 5-V supply. Devices are available with single, dual, or single pseudo-differential inputs. All of these devices have a chip select ( $\overline{CS}$ ), serial clock (SCLK), and serial data output (SDO) that provides a direct 3-wire interface to the serial port of most popular host microprocessors (SPI interface). When interfaced with a DSP, a frame sync signal (FS) is used to indicate the start of a serial data frame on either pin 1 ( $\overline{CS}$ ) or pin 7 (FS) for the TLC4541. The TLC4545 ADC connects to the DSP via pin 1 only ( $\overline{CS}$ ).

The TLC4541 and TLC4545 are designed to operate with low power consumption. The power saving feature is further enhanced with an auto-power down mode. This product family features a high-speed serial link to modern host processors with an external SCLK up to 15 MHz. Both families use a built-in oscillator as the conversion clock, providing a 2.94  $\mu$ s maximum conversion time.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

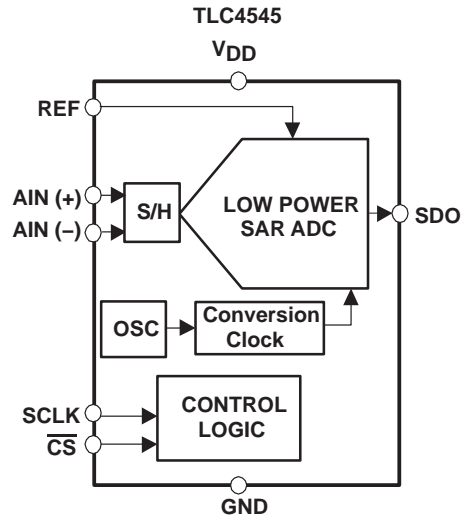
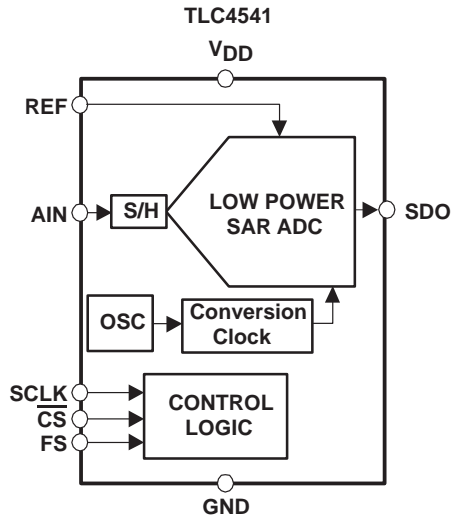
# TLC4541, TLC4545

SLAS293 – DECEMBER 2001

## AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES	
	8-MSOP (DGK)	8-SOIC (D)
-40°C to 85°C	TLC4541IDGK (PKG Code = ALM)	TLC4541ID
	TLC4545IDGK (PKG Code = AME)	TLC4545ID

## functional block diagram



## Terminal Functions

## TLC4541 single channel unipolar ADCs

TERMINAL NAME	NO.	I/O	DESCRIPTION
AIN	4	I	Analog input channel
$\overline{\text{CS}}$	1	I	Chip select. A high-to-low transition on the $\overline{\text{CS}}$ input removes SDO from a high-impedance state within a maximum delay time. If the TLC4541 is attached to a dedicated TMS320 DSP serial port using the FS input, $\overline{\text{CS}}$ can be grounded.
FS	7	I	DSP frame sync input. Indication of a start of a serial data frame. A low-to-high transition removes SDO from the high-impedance state and the MSB is presented. Tie this pin to $V_{\text{DD}}$ if not used.
GND	3	I	Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
SDO	8	O	The 3-state serial data output for the A/D conversion result. SDO is kept in the high-impedance state when $\overline{\text{CS}}$ is high. The output format is MSB first. Remaining data bits are presented on the rising edge of SCLK. When FS is not active (FS = 1 at the falling edge of $\overline{\text{CS}}$ ): The MSB is presented on the SDO pin on the falling edge of $\overline{\text{CS}}$ after a maximum delay time. Data is valid on each falling edge of SCLK until all data is read. When FS is active (FS = 0 at the falling edge of $\overline{\text{CS}}$ ): The MSB is presented to the SDO output on the rising edge of FS. Data is valid on the falling edge SCLK and changes on the rising edge SCLK (this is typically used with an active FS from a DSP). SDO returns to the high-impedance state after the 17th rising edge on SCLK. If a 17th SCLK cycle is not presented, as is the case when using an SPI host, SDO returns to the high-impedance state on the rising edge of $\overline{\text{CS}}$ .
SCLK	5	I	Serial clock. This terminal receives the serial SCLK from the host processor.
REF	2	I	External voltage reference input
$V_{\text{DD}}$	6	I	Positive supply voltage

## TLC4545 single channel pseudo-differential ADCs

TERMINAL NAME	NO.	I/O	DESCRIPTION
AIN0 (+)	4	I	Positive analog input for the TLC4545.
AIN1 (-)	5	I	Inverted analog input for the TLC4545.
$\overline{\text{CS}}$	1	I	Chip select. A high-to-low transition on $\overline{\text{CS}}$ removes SDO from the high-impedance state within a maximum delay time. The $\overline{\text{CS}}$ input can be connected to a DSP frame sync (FS) output when a dedicated TMS320 DSP serial port is used.
GND	3	I	Ground return for the internal circuitry. Unless otherwise noted, all voltage measurements are with respect to GND.
SDO	8	O	The 3-state serial data output for the A/D conversion result. SDO is kept in the high-impedance state when $\overline{\text{CS}}$ is high and presents output data after the $\overline{\text{CS}}$ falling edge until the LSB is presented. The output format is MSB first. The remaining data bits are presented on the rising edge of SCLK. Output data is valid on each falling edge of SCLK until all data is read. SDO returns to the high-impedance state after the 17th rising edge on SCLK. If a 17th SCLK cycle is not presented, as is the case when using an SPI host, SDO returns to the high-impedance state on the rising edge of $\overline{\text{CS}}$ .
SCLK	7	I	Serial clock. This terminal receives the serial SCLK from the host processor.
REF	2	I	External voltage reference input
$V_{\text{DD}}$	6	I	Positive supply voltage

## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, GND to $V_{DD}$ .....	-0.3 V to 6.5V
Analog input voltage range .....	-0.3 V to $V_{DD}+0.3$ V
Reference input voltage .....	$V_{DD}+0.3$ V
Digital input voltage range .....	-0.3 V to $V_{DD}+0.3$ V
Operating virtual junction temperature range, $T_J$ .....	-40°C to 150°C
Operating free-air temperature range: $T_A$ (I) .....	-40°C to 85°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .....	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$		4.5	5	5.5	V
Frequency, SCLK	$V_{DD} = 2.7$ V to 5.5 V	100		15000	kHz
Tolerable clock jitter, SCLK	$V_{DD} = 2.7$ V to 5.5 V			24	ps
Aperture jitter	$V_{DD} = 2.7$ V to 5.5 V		100		ps
External reference voltage input, $V_{REF}$		4		$V_{DD}$	V
VREF input impedance	$V_{DD} = 5$ V, $\overline{CS} = 1$ , SCLK = 0	100			MΩ
	$V_{DD} = 5$ V, $\overline{CS} = 0$ , SCLK = 15 MHz	20	25		kΩ
External reference input current	$V_{DD} = V_{REF} = 4.5$ V, $\overline{CS} = 0$ , SCLK = 15 MHz		0.02	1	mA
Analog input voltage	AIN, AIN(+)	0		$V_{DD}$	V
	AIN(-)	-0.2		0.2	V
High level control input voltage, $V_{IH}$		2.1			V
Low level control input voltage, $V_{IL}$				0.8	V
Operating free-air temperature, $T_A$	TLC4541/451	-40		85	°C

electrical characteristics over recommended operating free-air temperature range,  
 $V_{DD} = 5\text{ V}$ ,  $V_{REF} = 4.096\text{ V}$ , SCLK frequency = 15 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$V_{DD} = 4.5\text{ V}$ , $I_{OH} = -0.2\text{ mA}$	3.9			V
$V_{OL}$	Low-level output voltage	$V_{DD} = 4.5\text{ V}$ , $I_{OL} = 0.8\text{ mA}$			0.4	V
$I_{OZ}$	Off-state output current (high-impedance-state)	$V_O = V_{DD}$ , $\overline{CS} = V_{DD}$		1	2.5	$\mu\text{A}$
		$V_O = 0$ , $\overline{CS} = V_{DD}$		-1	-2.5	
$I_{IH}$	High-level input current	$V_I = V_{DD}$		0.005	2.5	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0$		-0.005	2.5	$\mu\text{A}$
$I_{CC}$	Operating supply current	$\overline{CS}$ at 0 V, $V_{DD} = 4.5\text{ V}$ to 5.5 V			3.5	mA
$I_{CC(PD)}$	Power-down supply current	For all digital inputs, $0 \leq V_I \leq 0.3\text{ V}$ or $V_I \geq V_{DD} - 0.3\text{ V}$ , SCLK= $V_{DD}$ , $V_{DD} = 4.5\text{ V}$ to 5.5 V		3	5	$\mu\text{A}$
	Selected analog input channel leakage current	Selected channel at $V_{DD}$			1	$\mu\text{A}$
		Selected channel at 0 V			-1	
$C_i$	Input capacitance	Analog inputs		11	14	pF
		Control Inputs		20	25	
$Z_i$	Input resistance	$V_{DD} = 5.5\text{ V}$			500	$\Omega$

#### ac specifications (TLC4541/45)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise ratio + distortion	$f_I = 15\text{ kHz}$ at 200 KSPS		84.5		dB
SNR	Signal-to-noise ratio	$f_I = 15\text{ kHz}$ at 200 KSPS		85		
THD	Total harmonic distortion	TLC4541	$f_I = 15\text{ kHz}$ at 200 KSPS	-94	-87	dB
		TLC4545	$f_I = 15\text{ kHz}$ at 200 KSPS	-94	-89	
ENOB	Effective number of bits	$f_I = 15\text{ kHz}$ at 200 KSPS		13.7		Bits
SFDR	Spurious free dynamic range	TLC4541	$f_I = 15\text{ kHz}$ at 200 KSPS	-95	-87	dB
		TLC4545	$f_I = 15\text{ kHz}$ at 200 KSPS	-95	-89	
	Full power bandwidth, -3 dB, analog input			1		MHz
	Full power bandwidth, -1 dB, analog input			500		kHz
Crosstalk		0.25 LBS		80		dB

#### dc specifications (TLC4541/45)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
INL	Integral linearity error (see Note 1)		-2.5		2.5	LSB
DNL	Differential linearity error		-1		2	LSB
$E_O$	Offset error (see Note 2)	TLC4541	-3.5		3.5	mV
		TLC4545	-1		1	
$E_G$	Gain error (see Note 2)	TLC4541	-2		2	mV
		TLC4545	-1.8		1.8	

† All typical values are at  $V_{DD} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

- NOTES: 1. Linear error is the maximum deviation from the best straight line through the A/D transfer characteristics.  
 2. Zero error is the difference between 0000h and the converted output for zero input voltage; full-scale error is the difference between ideal full-scale and the converted output for full-scale input voltage.

# TLC4541, TLC4545

SLAS293 – DECEMBER 2001

## timing requirements, $V_{DD} = 5\text{ V}$ , $V_{REF} = 4.096\text{ V}$ , SCLK frequency = 15 MHz (unless otherwise specified)

		MIN	TYP	MAX	UNIT
$t_{cyc}(\text{SCLK})$	SCLK cycle time, $V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$ (see Note 3)	66		10000	ns
$t_{w1}$	Pulse width, SCLK low	27		5000	ns
$t_{w2}$	Pulse width, SCLK high	27		5000	ns
$t_{h1}$	Hold time, $\overline{\text{CS}}$ high after SCLK falling edge	3			ns
$t_{su1}$	Setup time, $\overline{\text{CS}}$ falling edge before the first SCLK falling edge	15			ns
$t_{h2}$	Hold time, $\overline{\text{CS}}$ low after 16th SCLK falling edge	5			ns
$t_{w3}$	Pulse width, $\overline{\text{CS}}$ high	0.5			SCLKs
$t_{d1}$	Delay time, $\overline{\text{CS}}$ falling edge to SDO MSB valid, $V_{DD} = V_{REF} = 4.5\text{ V}$ , 20 pF		12	17	ns
$t_{d2}$	Delay time, SCLK rising edge to next SDO data bit valid, $V_{DD} = V_{REF} = 4.5\text{ V}$ , 20 pF			15	ns
$t_{d3}$	Delay time, 17 <sup>th</sup> SCLK rising edge to SDO 3-stated, $V_{DD} = V_{REF} = 4.5\text{ V}$ , 20 pF (see Note 4)			20	ns
$t_{su3}$	Setup time, $\overline{\text{CS}}$ falling edge before FS rising edge (TLC4541 only)	0.5	1		SCLKs
$t_{w4}$	Pulse width, FS high (TLC4541 only)	0.5	1		SCLKs
$t_{su4}$	Setup time, FS rising edge before SCLK falling edge (TLC4541 only)	12.5			ns
$t_{h4}$	Hold time, FS high after SCLK falling edge (TLC4541 only)	5			ns
$t_{su5}$	Setup time, FS falling edge before 1st SCLK falling edge (TLC4541 only)	12			ns
$t_{d4}$	Delay time, FS rising edge to SDO MSB valid, ( $V_{DD} = V_{REF} = 4.5\text{ V}$ , 20 pF TLC4541 only)			15	ns
$t_{h6}$	Hold time, $\overline{\text{CS}}$ low after 1st SCLK falling edge	5			ns
$t_{su6}$	Setup time, $\overline{\text{CS}}$ rising edge before 9th (or the last) SCLK falling edge	5			ns
$t_{h7}$	Hold time, FS low after 1st SCLK falling edge (TLC4541 only)	5			ns
$t_{su7}$	Setup time, FS rising edge before 9th (or the last) SCLK falling edge	5			ns
$t_{cyc}(\text{reset})$	Active $\overline{\text{CS}}$ /FS cycle time, SCLK falling edges required to initialize ADC	1		8	SCLKs
$t_{conv}$	Conversion time (22 conversion clocks based on 7.5-MHz to 12-MHz OSC)	1.83		2.94	$\mu\text{s}$
$t_s$	Sample time, 20 SCLKs, SCLK up to 15 MHz	1.33		200	$\mu\text{s}$

NOTES: 3. Timing specifications given for 40/60 to 60/40 duty cycle

4. SDO goes into the high impedance state after detection of the 17th rising SCLK edge or a rising  $\overline{\text{CS}}$  edge if a 17th SCLK is not presented.

## TYPICAL CHARACTERISTICS

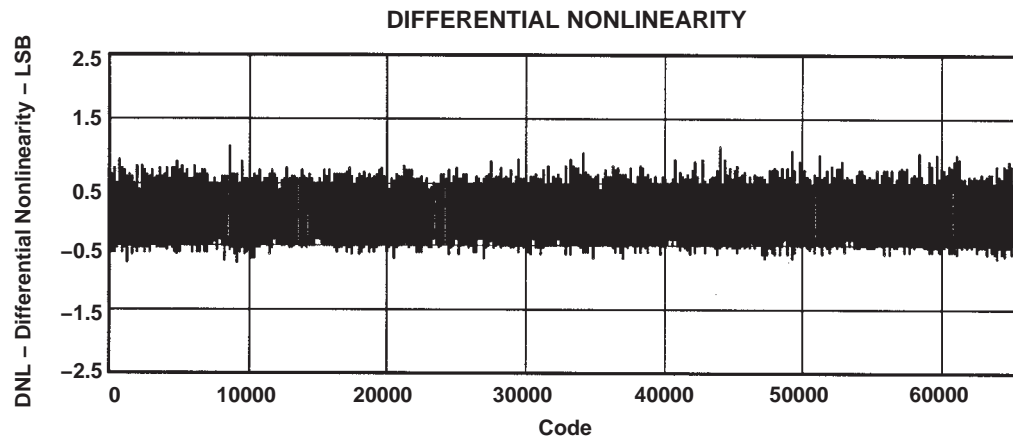


Figure 1

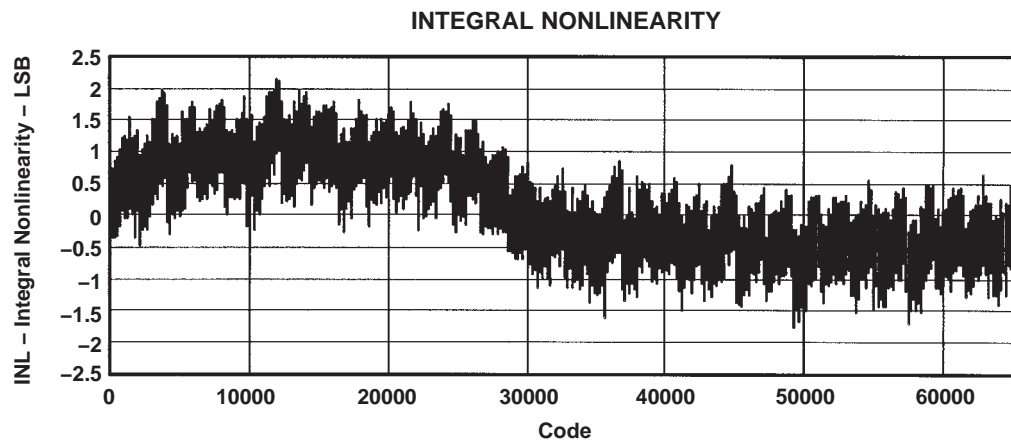


Figure 2

TYPICAL CHARACTERISTICS

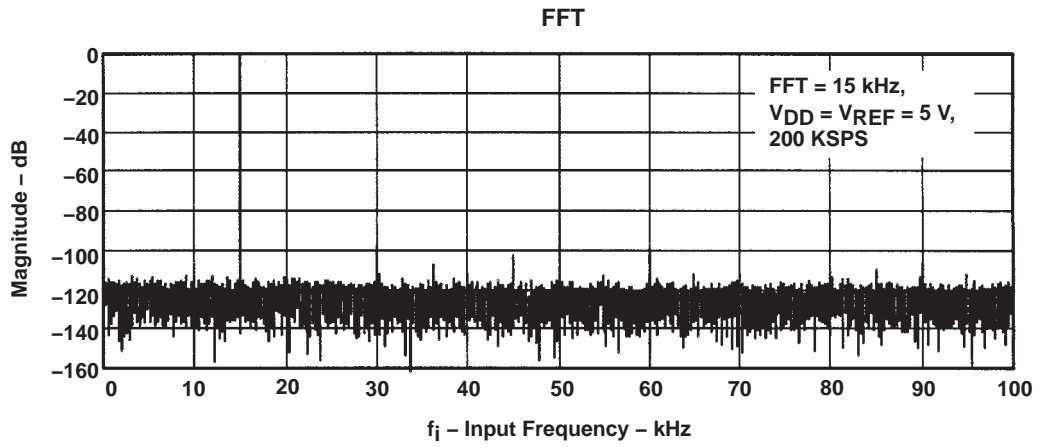


Figure 3

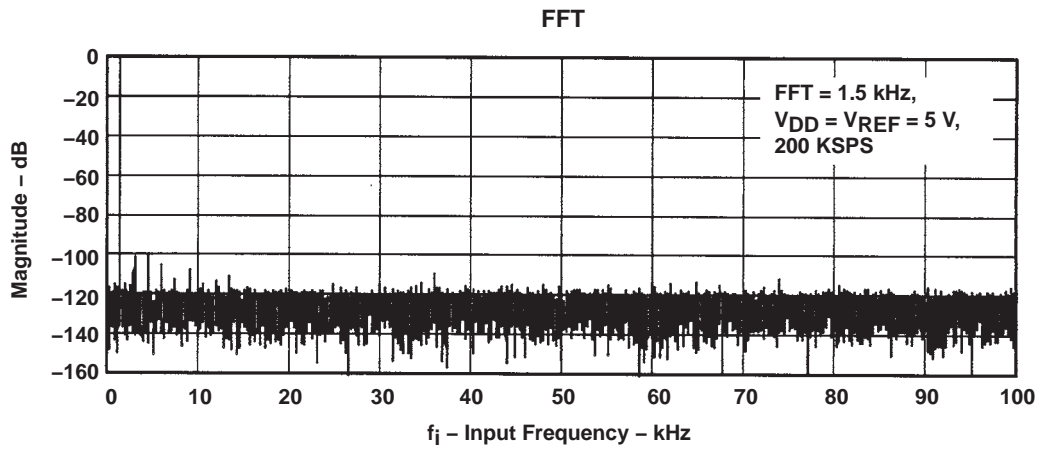


Figure 4



TYPICAL CHARACTERISTICS

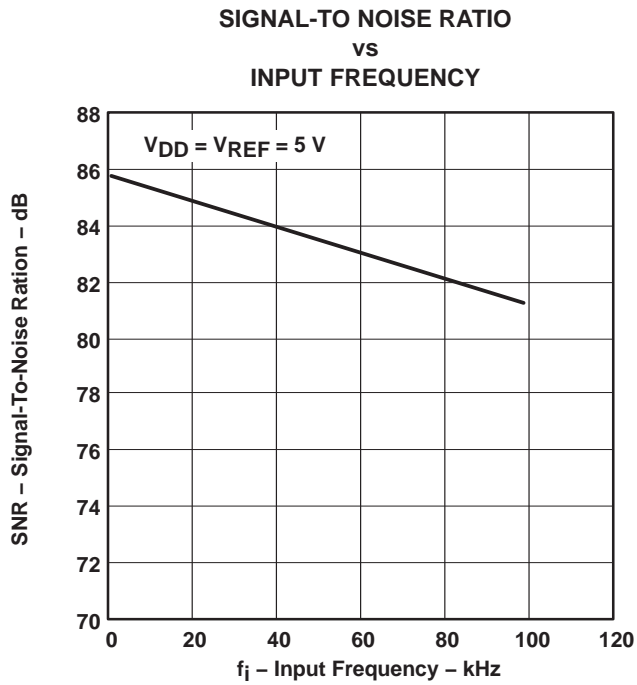


Figure 5

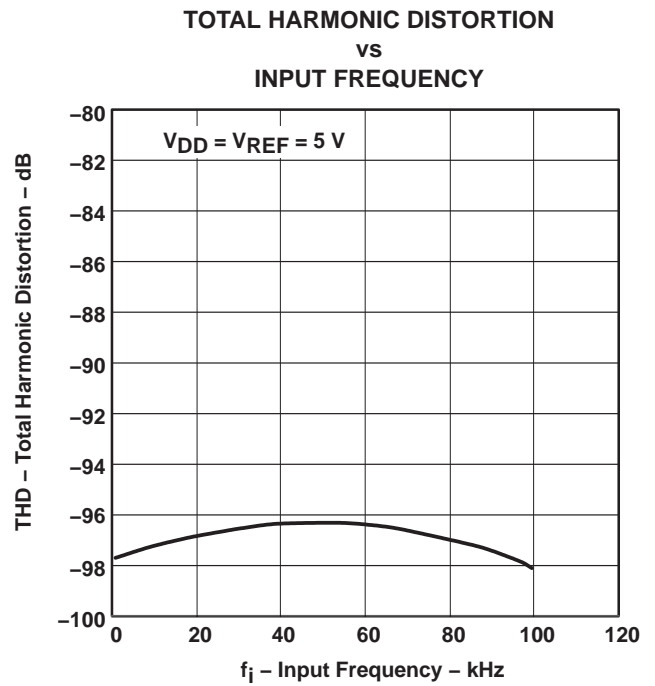


Figure 6

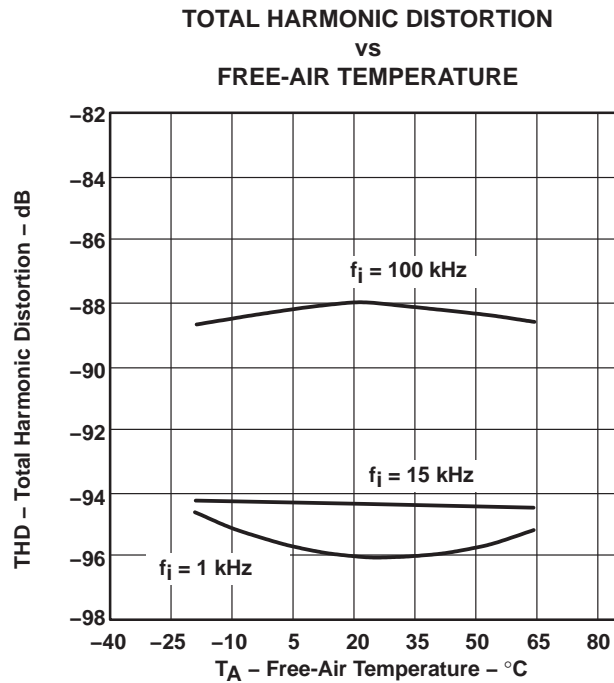


Figure 7

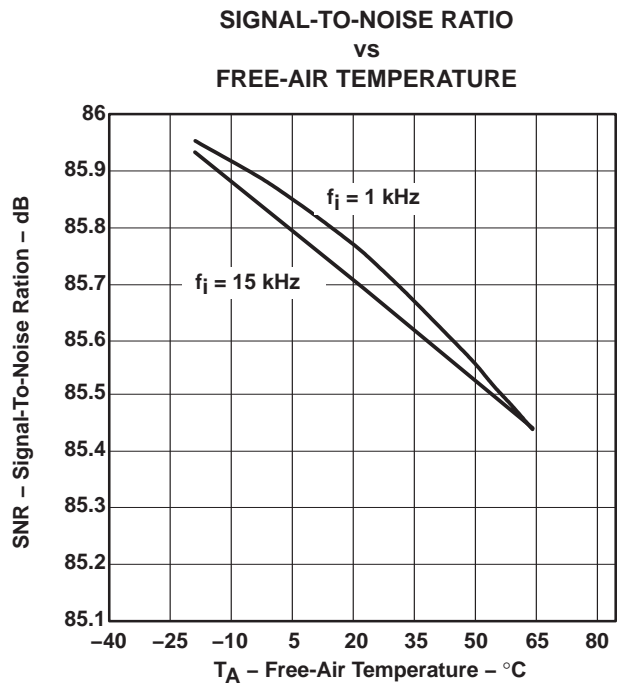


Figure 8

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION  
vs  
REFERENCE VOLTAGE

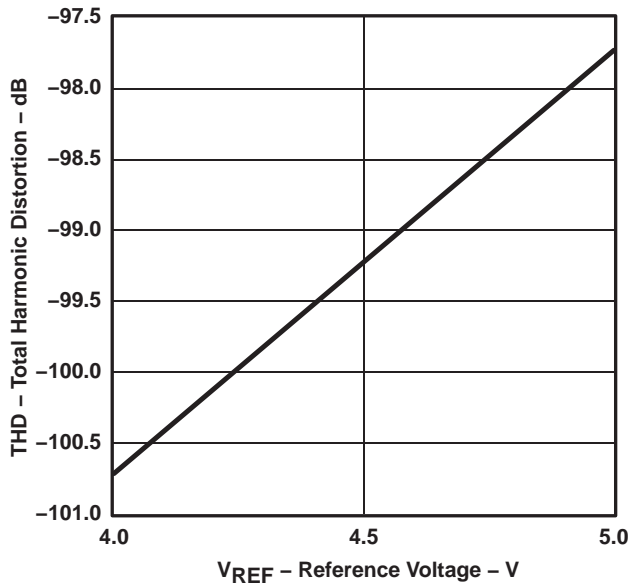


Figure 9

SIGNAL-TO-NOISE RATIO  
vs  
REFERENCE VOLTAGE

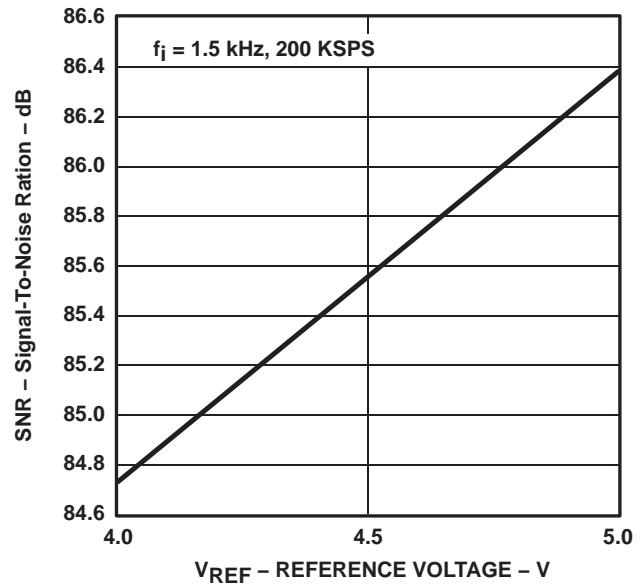


Figure 10

MAXIMUM DIFFERENTIAL NONLINEARITY  
vs  
REFERENCE VOLTAGE

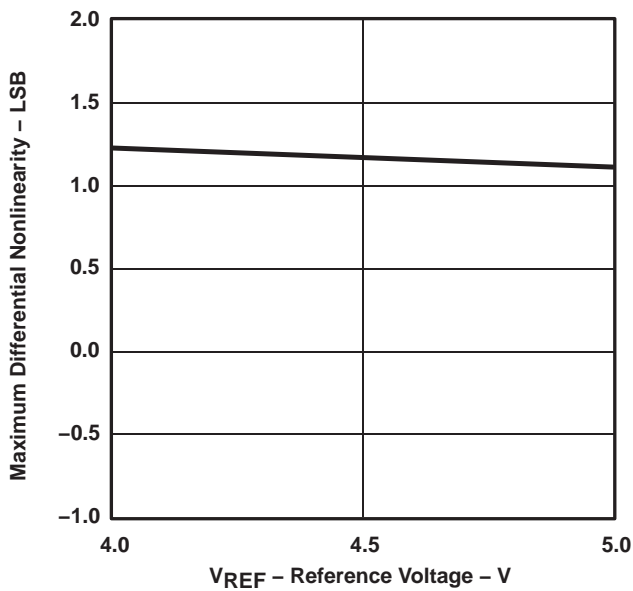


Figure 11

MINIMUM DIFFERENTIAL NONLINEARITY  
vs  
REFERENCE VOLTAGE

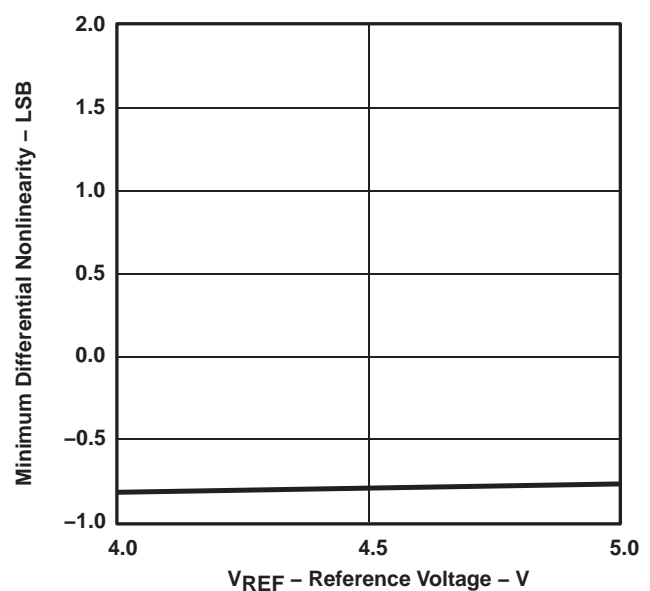


Figure 12

## TYPICAL CHARACTERISTICS

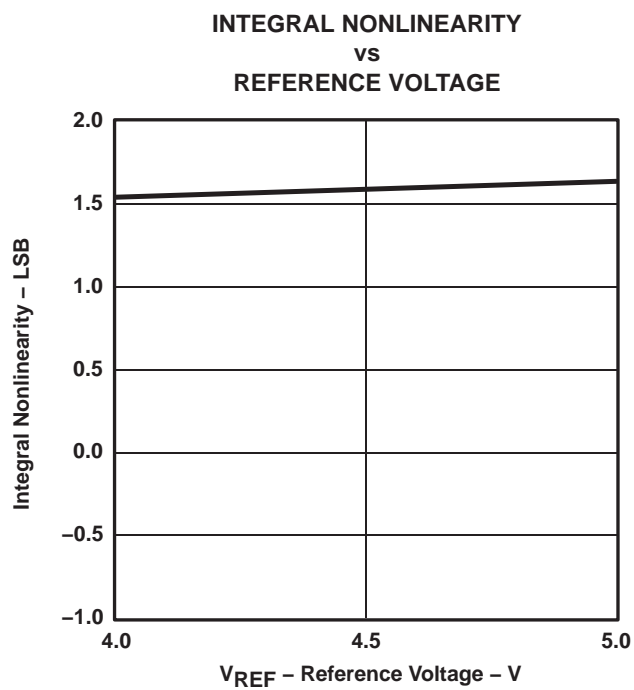


Figure 13

PRINCIPLES OF OPERATION

control and timing

device initialization/RESET cycle

The TLC4541/45 each require one RESET cycle after power-on for initialization in order to operate properly. This RESET cycle is initiated by asserting the  $\overline{CS}$  pin (pin 1) low for a minimum duration of at least one SCLK falling edge but no more than 8 SCLK falling edges in length. The RESET cycle is terminated by asserting  $\overline{CS}$  high. If a valid RESET cycle is issued, the data presented on the SDO output during the following cycle is FF00h. This output code is useful in determining when a valid reset/initialization has occurred.

The TLC4541 has separate  $\overline{CS}$  and FS pins. In this case, it is also possible to initiate the RESET cycle by asserting FS low if  $\overline{CS}$  is already low. The RESET cycle can be terminated by either asserting  $\overline{CS}$  high (as shown in the first RESET cycle in Figure 14), or by asserting FS high ( as shown in the second RESET cycle in Figure 14), whichever happens first.

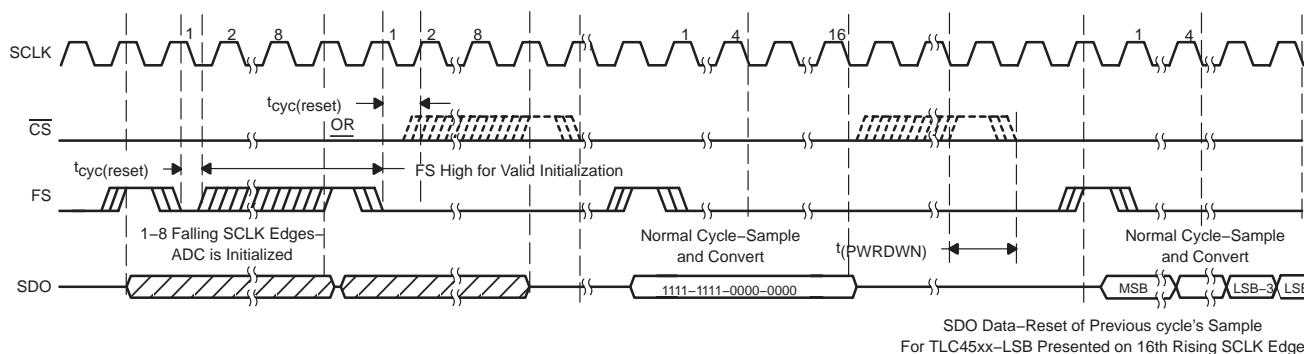


Figure 14. TLC4541/45 Initialization Timing

sampling

The converter sample time is 20 SCLKs in duration, beginning on the 5th SCLK received during an active signal on the  $\overline{CS}$  input (or FS input for the TLC4541.)

conversion

Each device completes a conversion in the following manner. The conversion is started after the 24th falling SCLK edge. The  $\overline{CS}$  input can be released at this point or at any time during the remainder of the conversion cycle. The conversion takes a maximum of 2.94  $\mu$ s to complete. Enough time (for conversion) should be allowed before the next falling edge on the  $\overline{CS}$  input (or rising edge on the FS input for the TLC4541) so that no conversion is terminated prematurely. If the conversion cycle is terminated early, the data presented on SDO during the following cycle is FF00h. This predefined output code is helpful in determining if the cycle time is not long enough to complete the conversion. The same code is also used to determine if a reset cycle is valid.

For all devices, the SDO data presented during a cycle is the result of the conversion of the sample taken during the previous cycle. The output data format is shown in the following table.

SERIAL OUTPUT DATA FORMAT		
	MSB [D15:D2]	LSB [D1:D0]
TLC4541/45	Conversion Result (OD15-OD2)	Conversion Result (OD1 – OD0)

## PRINCIPLES OF OPERATION

### control and timing (continued)

#### sampling and conversion cycle

TLC4541:

Control via pin 1,  $\overline{CS}$  (FS = 1 at the falling edge of  $\overline{CS}$ )– The falling edge of  $\overline{CS}$  is the start of the cycle. Transitions on  $\overline{CS}$  can occur when SCLK is high or low. The MSB may be read on the first falling SCLK edge after  $\overline{CS}$  is low. Output data changes on the rising edge of SCLK. This control method is typically used for a microcontroller with an SPI interface, although it can also be used for a DSP. The microcontroller SPI interface should be programmed for CPOL=0 (serial clock inactive low) and CPHA=1 (data valid on the falling edge of serial clock).

Control via pin 7, FS ( $\overline{CS}$  is tied/held low)– The rising edge of FS is the start of the cycle. Transitions on FS can occur when SCLK is high or low. The MSB is presented on SDO after the rising edge of FS. The MSB may be read on the first falling edge of SCLK after the FS falling edge. Output data changes on the rising edge of SCLK. This is the typical configuration when the ADC is the only device on the TMS320 DSP serial port.

Control via pin 1 and pin 7,  $\overline{CS}$  and FS– Transitions on  $\overline{CS}$  and FS can occur when SCLK is high or low. The MSB is presented after the rising edge of FS. The falling edge of FS is the start of the sampling cycle. The MSB may be read on the first falling edge of SCLK after the FS falling edge. Output data changes on the rising edge of SCLK. This is typically used for multiple devices connected to a single TMS320 DSP serial port.

TLC4545:

All control is provided using the  $\overline{CS}$  input (pin 1) on the TLC4545. Transitions on  $\overline{CS}$  can occur when SCLK is high or low. The cycle is started on the falling edge transition on the  $\overline{CS}$  input. This signal can be provided by either a  $\overline{CS}$  signal (when interfacing with an SPI microcontroller) or FS signal (when interfacing with a TMS320 DSP). The MSB is presented to SDO on the falling edge of the signal applied to pin 1 and may be read on the first falling SCLK edge after this input is low. Output data changes on the rising edge of SCLK.

### control modes

#### control via pin 1 ( $\overline{CS}$ , SPI interface)

All devices are compatible with this mode of operation. A falling edge on the  $\overline{CS}$  input initiates the cycle. (For the TLC4541, the FS input is tied to  $V_{DD}$ ). The  $\overline{CS}$  input remains low for the entire sampling time plus 4 SCLK decoding time (16 falling SCLK edges) and can then be released at any point during the remainder of the conversion. Enough time should be allowed before the next falling  $\overline{CS}$  edge so that the conversion cycle is not terminated prematurely. The microcontroller SPI interface should be programmed for CPOL=0 (serial clock inactive low) and CPHA=1 (data is valid on the falling edge of serial clock).

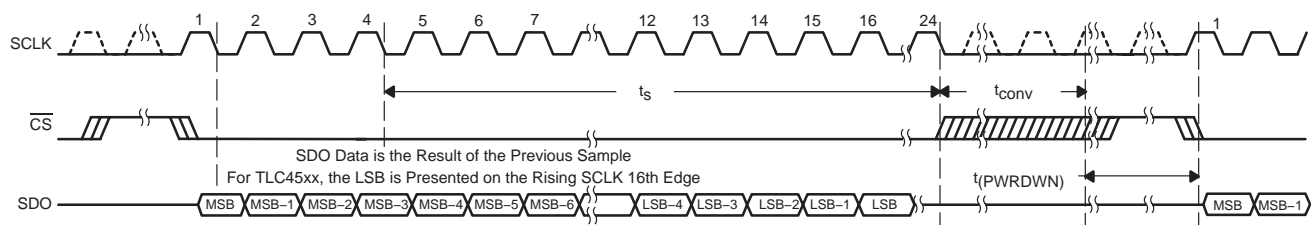


Figure 15. SPI Cycle Timing Using the CS Input (FS = 1 for TLC4541)

PRINCIPLES OF OPERATION

control via pin 1 ( $\overline{CS}$ , DSP interface)

All devices are compatible with this mode of operation. The FS signal from a DSP is connected directly to the  $\overline{CS}$  input of the ADC. A falling edge on the  $\overline{CS}$  input while SCLK is high or low initiates the cycle. (For TLC4541 in this configuration, the FS input is tied to  $V_{DD}$ .) Enough time should be allowed before the next rising  $\overline{CS}$  edge so that the conversion cycle is not terminated prematurely.

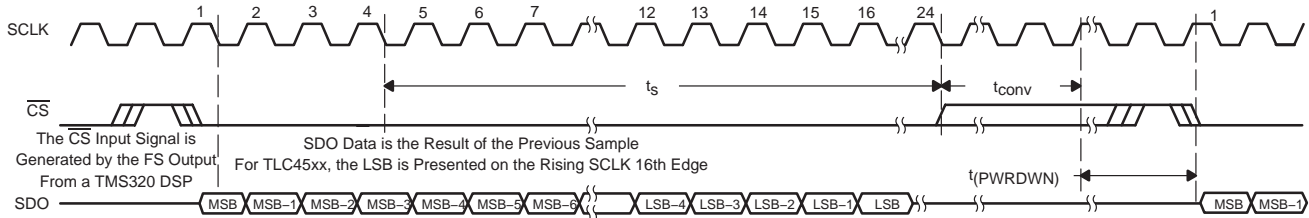


Figure 16. DSP Cycle Timing Using the CS Input (FS = 1 for TLC4541 Only)

control via pin 1 and pin 7 ( $\overline{CS}$  and FS or FS only, DSP interface)

Only TLC4541 is compatible with this mode of operation. The  $\overline{CS}$  input to the ADC can be controlled via a general-purpose I/O pin from the DSP or tied to ground. The FS signal from the DSP is connected directly to the FS input of the ADC. A rising FS edge releases the MSB to the SDO output. The falling edge on the FS input while SCLK is high or low initiates the cycle. The  $\overline{CS}$  input should remain low for the entire sampling time plus 4 SCLK decoding time after falling FS (24 falling SCLK edges) and can then be released at any time during the remainder of the conversion cycle. The optimum DSP interface is achieved when tying  $\overline{CS}$  to ground and using only the FS input to control the ADC.

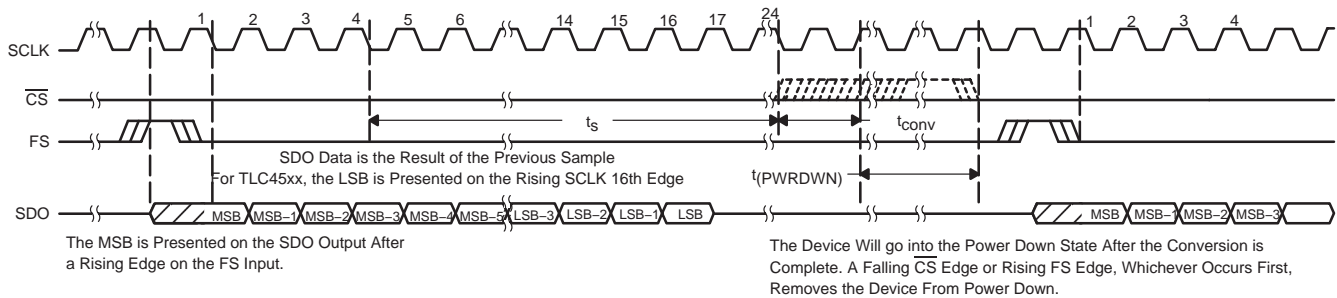


Figure 17. DSP Cycle Timing Using FS Only (or Using Both  $\overline{CS}$  and FS for the TLC4541)

PRINCIPLES OF OPERATION

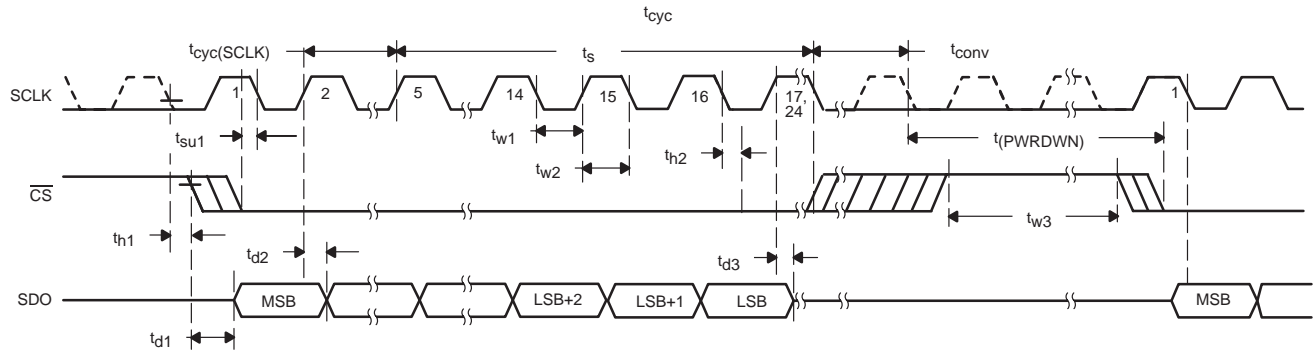


Figure 18. Critical Timing: Control Via CS Input (FS = 1 for TLC4541)

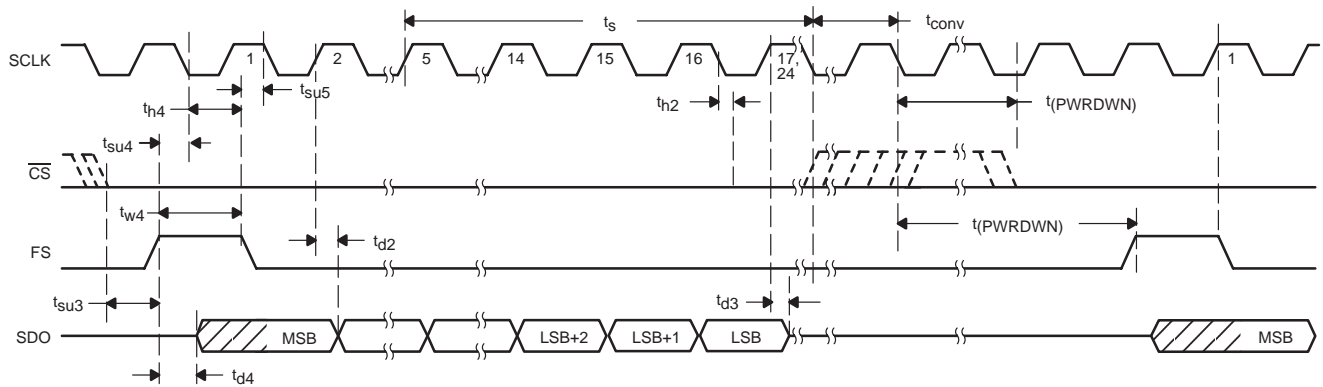


Figure 19. Critical Timing: Control Via CS and FS Inputs (TLC4541 Only)

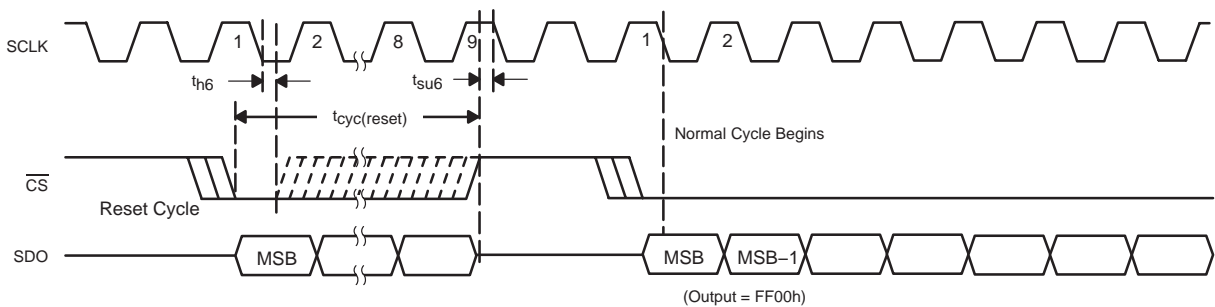


Figure 20. Critical Timing: Reset/Initialization Cycle (FS =1 for TLC4541)

PRINCIPLES OF OPERATION

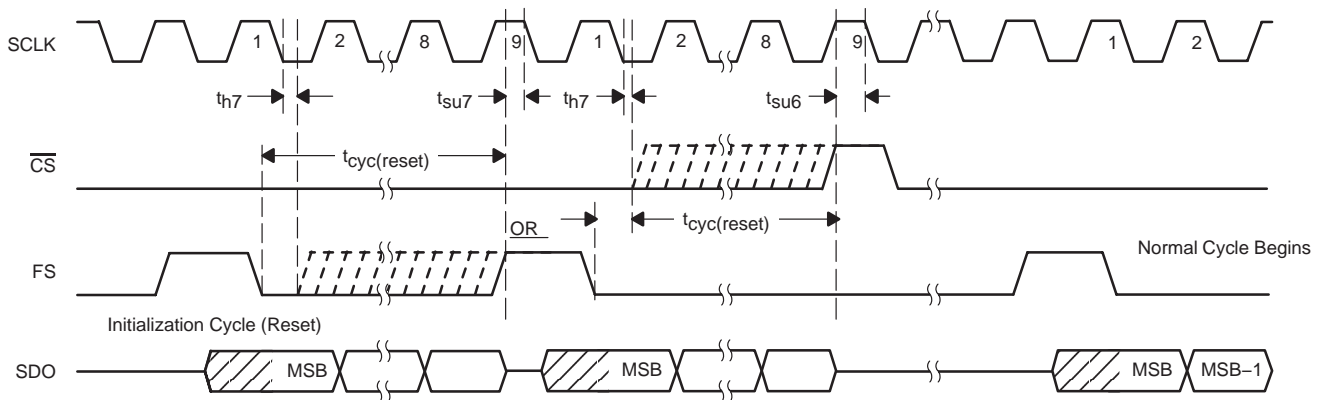


Figure 21. Critical Timing: Initialization Cycle (TLC4541 Only)

detailed description

The TLC4541/5 are successive approximation (SAR) ADCs utilizing a charge-redistribution DAC. Figure 22 shows a simplified version of the ADC. The sampling capacitor acquires the signal on AIN (or the AIN(+) pin for TLC4545) during the sampling period. When the conversion process starts, the SAR control logic and charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator into a balanced condition. When the comparator is balanced, the conversion is complete and the ADC output code is generated.

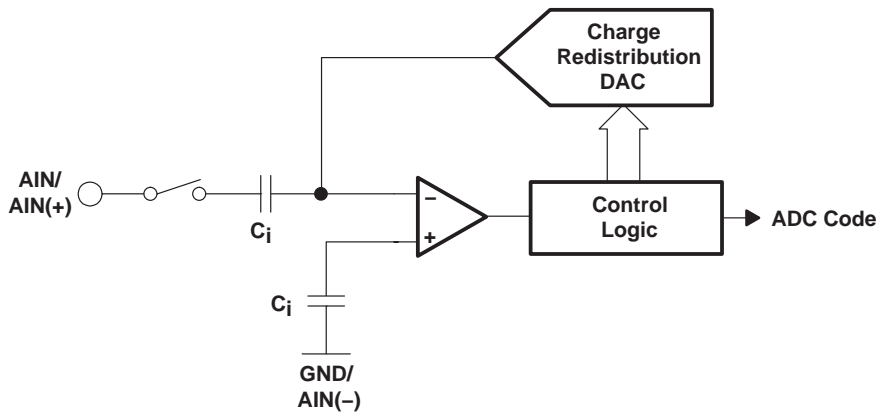


Figure 22. Simplified SAR Circuit



---

## PRINCIPLES OF OPERATION

### pseudo-differential inputs

The TLC4545 operate in pseudo-differential mode. The inverted input is available on pin 5. The inverted input can tolerate a maximum input ripple of  $\pm 0.2$  V. It is normally used for zero-scale offset cancellation or ground noise rejection.

### serial interface

Output data format is binary (unipolar straight binary).

### binary

- Zero Scale Code = 0000h,  $V_{AIN} = GND$
- Full Scale Code = FFFFh,  $V_{AIN} = V_{REF} - 1LSB$

### reference voltage

An external reference must be applied via pin 2,  $V_{REF}$ . The voltage level applied to this pin establishes the upper limit of the analog inputs to produce a full-scale reading. The value of  $V_{REF}$ , and the analog input should not exceed the positive supply or be less than GND, consistent with the specified absolute maximum ratings. The digital output is at full scale when the input signal is equal to or higher than  $V_{REF}$  and at zero when the input signal is equal to or less than GND.

### auto-power down and power up

Auto-power down is built into the devices in order to reduce power consumption. The wake-up time is fast enough to provide power down between each conversion cycle. The power down state is initiated at the end of conversion and wakes up on a falling  $\overline{CS}$  edge (or rising FS edge, whichever occurs first, for TLC4541 only).

APPLICATION INFORMATION

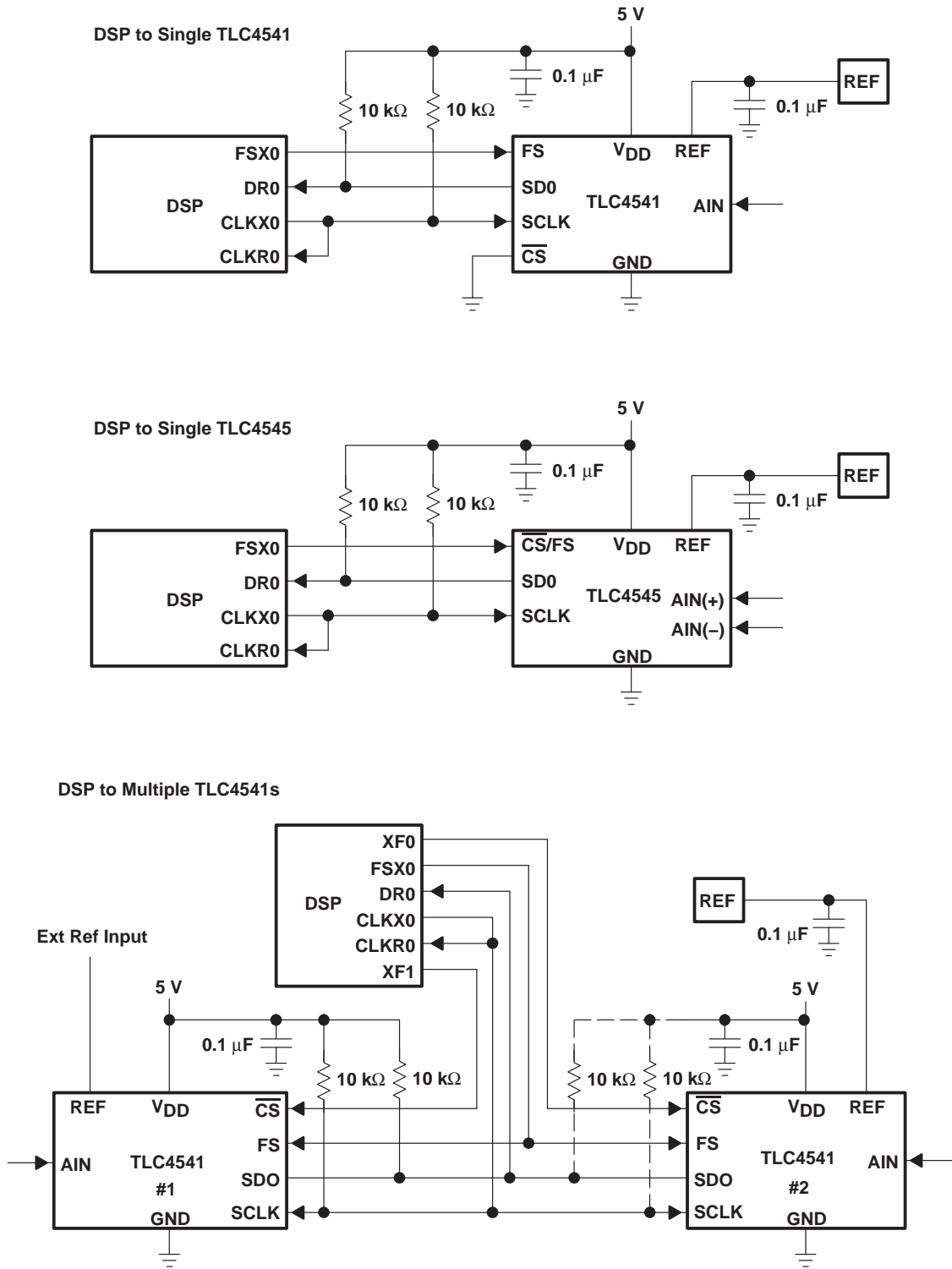


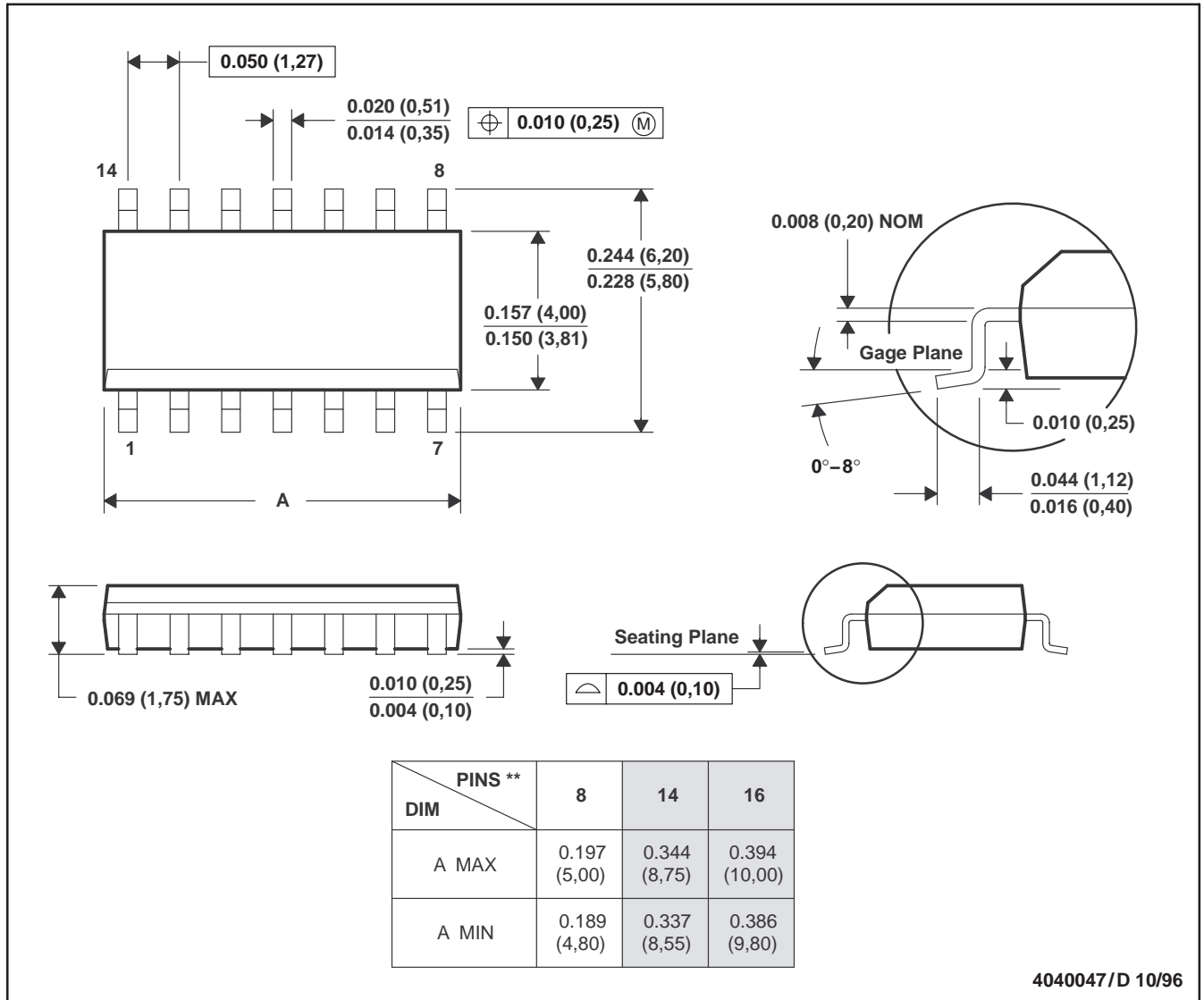
Figure 23. Typical ADC Interface to a TMS320 DSP

MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

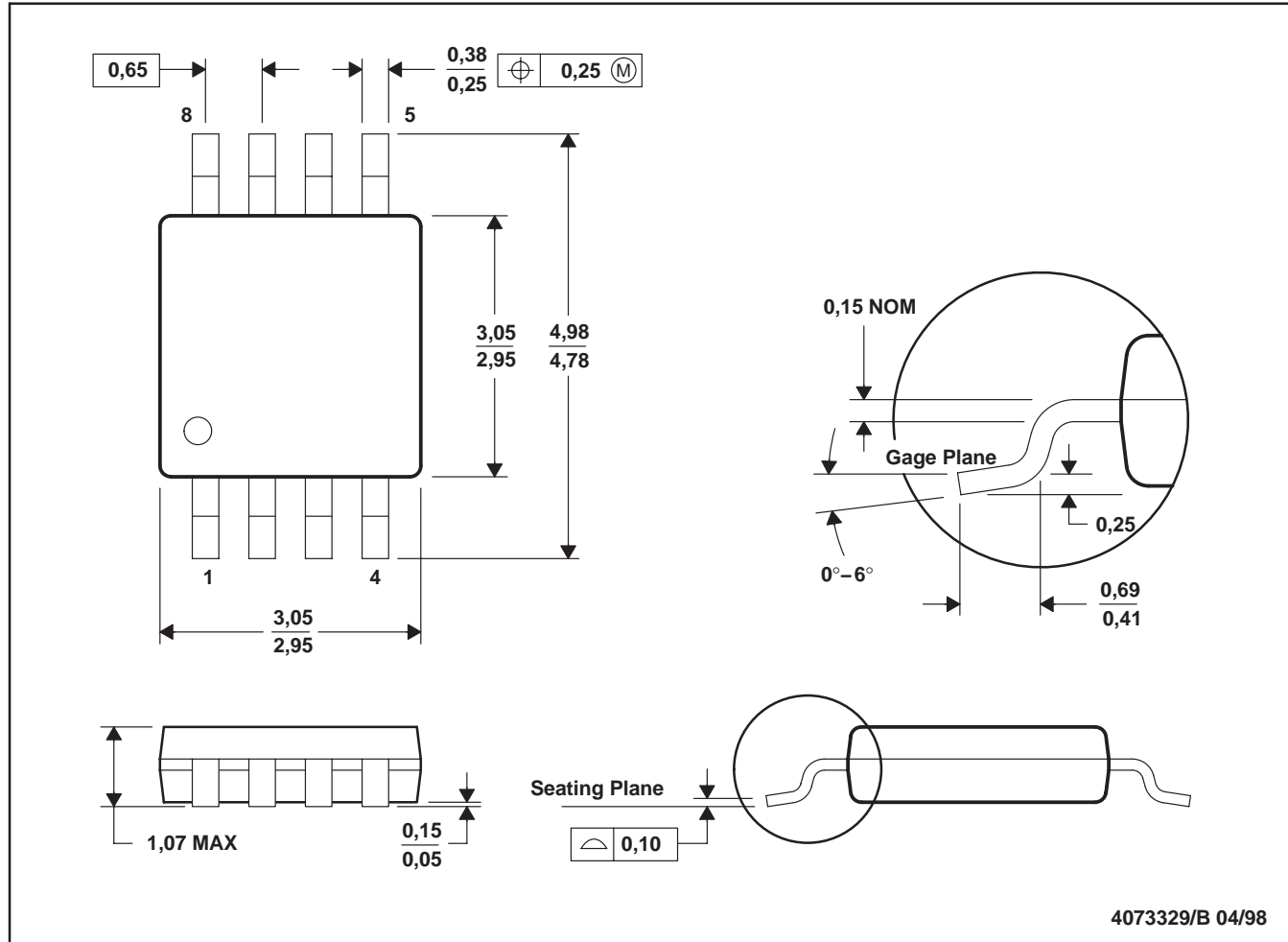


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-012

MECHANICAL DATA

DGK (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/B 04/98

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion.  
 D. Falls within JEDEC MO-187

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2003, Texas Instruments Incorporated