LP38500/2-ADJ, LP38500A/2A-ADJ 1.5A FlexCap Low Dropout Linear Regulator for 2.7V to 5.5V Inputs

Check for Samples: LP38500-ADJ, LP38502-ADJ

FEATURES

- **FlexCap: Stable with ceramic, tantalum, or aluminum capacitors**
- **Stable with 10 µF input/output capacitor**
- **Adjustable output voltage from 0.6V to 5V**
- **Low ground pin current**
- **25 nA quiescent current in shutdown mode**
- **Guaranteed output current of 1.5A**
- **Available in TO-263, TO-263 THIN, and LLP-8 packages**
- **Guaranteed V_{ADJ} accuracy of ±1.5% @ 25°C (A Grade)**
- **Guaranteed accuracy of ±3.5% @ 25°C (STD)**
- **Over-Temperature and Over-Current protection**
- **−40°C to +125°C operating T_J range**
- **Enable pin (LP38502)**

APPLICATIONS

- **ASIC Power Supplies In:**
  - **Printers, Graphics Cards, DVD Players**
  - **Set Top Boxes, Copiers, Routers**
- **DSP and FPGA Power Supplies**
- **SMPS Regulator**
- **Conversion from 3.3V or 5V Rail**

DESCRIPTION

National's FlexCap LDO's feature unique compensation that allows the use of any type of output capacitor with no limits on minimum or maximum ESR. The LP38500/2 series of low-dropout linear regulators operates from a +2.7V to +5.5V input supply. These ultra low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. Developed on a CMOS process, (utilizing a PMOS pass transistor), the LP38500/2 has low quiescent current that changes little with load current.

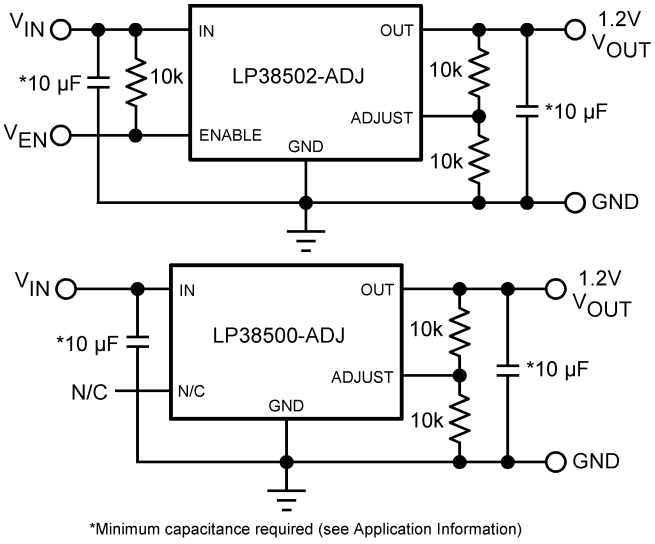
Ground Pin Current: Typically 2 mA at 1.5A load current.

Disable Mode: Typically 25 nA quiescent current when the Enable pin is pulled low.

Simplified Compensation: Stable with any type of output capacitor, regardless of ESR.

Precision Output: "A" grade versions available with 1.5% V_{ADJ} tolerance (25°C) and 3% over line, load and temperature.

Typical Application Circuit



*Minimum capacitance required (see Application Information)

Connection Diagrams for TO-263 (TS) Package

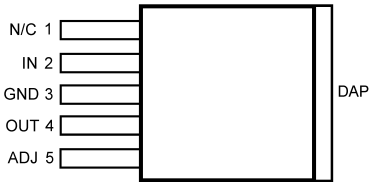


Figure 1. Top View (LP38500TS-ADJ)
TO-263 Package

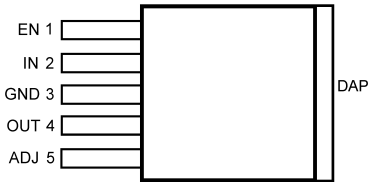


Figure 2. Top View (LP38502TS-ADJ)
TO-263 Package

Connection Diagrams for TO-263 THIN (TJ) Package

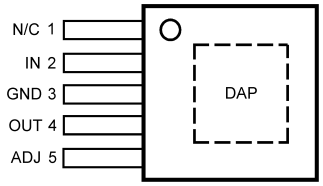


Figure 3. Top View (LP38500TJ-ADJ, LP38500ATJ-ADJ)
TO-263 THIN Package

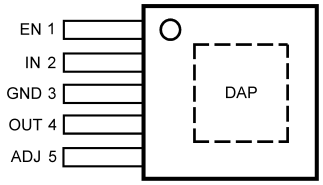


Figure 4. Top View (LP38502TJ-ADJ, LP38502ATJ-ADJ)
TO-263 THIN Package

Pin Descriptions for TO-263 (TS), TO-263 THIN (TJ) Packages

Pin #	Designation	Function
1	EN	Enable (LP38502 only). Pull high to enable the output, low to disable the output. This pin has no internal bias and must be either tied to the input voltage, or actively driven.
	N/C	In the LP38500, this pin has no internal connections. It can be left floating or used for trace routing.
2	IN	Input Supply
3	GND	Ground
4	OUT	Regulated Output Voltage
5	ADJ	Sets output voltage
DAP	DAP	The DAP is used to remove heat from the device by conducting it to the copper clad area on the PCB which acts as the heatsink. The DAP is electrically connected to the backside of the die. The DAP must be connected to ground potential, but can not be used as the only ground connection.

Connection Diagrams for LLP-8 (SD) Package

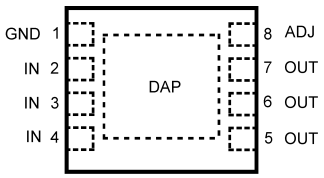


Figure 5. Top View (LP38500SD-ADJ, LP38500ASD-ADJ)
LLP-8 Package

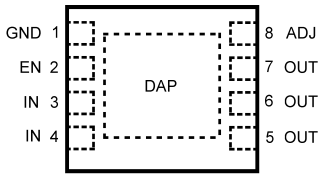


Figure 6. Top View (LP38502SD-ADJ, LP38502ASD-ADJ)
LLP-8 Package

Pin Descriptions for LLP-8 (SD) Package

Pin #	Designation	Function
1	GND	Ground
2	IN	Input Supply (LP38500 only). Input Supply pins share current and must be connected together on the PC Board.
	EN	Enable (LP38502 only). Pull high to enable the output, low to disable the output. This pin has no internal bias and must be either tied to the input voltage, or actively driven.
3, 4	IN	Input Supply. Input Supply pins share current and must be connected together on the PC Board.
5, 6, 7	OUT	Regulated Output Voltage. Output pins share current and must be connected together on the PC Board.
8	ADJ	Sets output voltage
DAP	DAP	The DAP is used to remove heat from the device by conducting it to a copper clad area on the PCB which acts as a heatsink. The DAP is electrically connected to the backside of the die. The DAP must be connected to ground potential, but can not be used as the only ground connection.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 5 sec.)	260°C
ESD Rating (2)	±2 kV
Power Dissipation (3)	Internally Limited
Input Pin Voltage (Survival)	−0.3V to +6.0V
Enable Pin Voltage (Survival)	−0.3V to +6.0V
Output Pin Voltage (Survival)	−0.3V to +6.0V
I_{OUT} (Survival)	Internally Limited

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.
(2) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.
(3) Operating junction temperature must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}). See Application Information.

Operating Ratings (1)

Input Supply Voltage	2.7V to 5.5V
Enable Input Voltage	0.0V to 5.5V
Output Current (DC)	0 to 1.5A
Junction Temperature (2)	−40°C to +125°C
V_{OUT}	0.6V to 5V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics.
(2) Operating junction temperature must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance (θ_{JA}). See Application Information.

Electrical Characteristics
LP38500/2–ADJ

Unless otherwise specified: V_{IN} = 3.3V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = V_{IN}, V_{OUT} = 1.8V. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ADJ}	Adjust Pin Voltage (1)	2.7V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 1.5A	0.584 **0.575**	0.605	0.626 **0.635**	V
V_{ADJ}	Adjust Pin Voltage (1) "A" GRADE	2.7V ≤ V_{IN} ≤ 5.5V 10 mA ≤ I_{OUT} ≤ 1.5A	0.596 **0.587**	0.605	0.614 **0.623**	V
I_{ADJ}	Adjust Pin Bias Current	2.7V ≤ V_{IN} ≤ 5.5V		50	**750**	nA
V_{DO}	Dropout Voltage (2)	I_{OUT} = 1.5A		220	275 **375**	mV
$\Delta V_{OUT}/\Delta V_{IN}$	Output Voltage Line Regulation (3) (1)	2.7V ≤ V_{IN} ≤ 5.5V	—	0.04 **0.05**	—	%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Output Voltage Load Regulation (4) (1)	10 mA ≤ I_{OUT} ≤ 1.5A	—	0.18 **0.33**	—	%/A
I_{GND}	Ground Pin Current In Normal Operation Mode	10 mA ≤ I_{OUT} ≤ 1.5A	—	2	3.5 **4.5**	mA
$I_{DISABLED}$	Ground Pin Current	V_{EN} < $V_{IL(EN)}$	—	0.025	0.125 **15**	µA
$I_{OUT(PK)}$	Peak Output Current	V_{OUT} ≥ $V_{OUT(NOM)}$ - 5%		3.6		A
I_{SC}	Short Circuit Current	V_{OUT} = 0V	**2**	3.7		A
Enable Input (LP38502 Only)						
$V_{IH(EN)}$	Enable Logic High	V_{OUT} = ON	**1.4**	—	—	V
$V_{IL(EN)}$	Enable Logic Low	V_{OUT} = OFF	—	—	**0.65**	V
$t_{d(off)}$	Turn-off delay	Time from V_{EN} < $V_{IL(EN)}$ to V_{OUT} = OFF I_{LOAD} = 1.5A	—	25	—	µs
$t_{d(on)}$	Turn-on delay	Time from V_{EN} >$V_{IH(EN)}$ to V_{OUT} = ON I_{LOAD} = 1.5A	—	25	—	µs
$I_{IH(EN)}$	Enable Pin High Current	V_{EN} = V_{IN}	—	1	—	nA
$I_{IL(EN)}$	Enable Pin Low Current	V_{EN} = 0V	—	0.1	—	nA
AC Parameters						
PSRR	Ripple Rejection	V_{IN} = 3.0V, I_{OUT} = 1.5A f = 120Hz	—	58	—	dB
		V_{IN} = 3.0V, I_{OUT} = 1.5A f = 1 kHz	—	56	—	dB
$\rho_{n(l/f)}$	Output Noise Density	f = 120Hz, C_{OUT} = 10 µF CER	—	1.0	—	µV/√Hz
e_n	Output Noise Voltage	BW = 100Hz – 100kHz C_{OUT} = 10 µF CER	—	100	—	µV (rms)
Thermal Characteristics						
T_{SD}	Thermal Shutdown	T_J rising	—	170	—	°C
ΔT_{SD}	Thermal Shutdown Hysteresis	T_J falling from T_{SD}	—	10	—	°C

(1) The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the adjust voltage tolerance specification.
(2) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. For any output voltage less than 2.5V, the minimum V_{IN} operating voltage is the limiting factor.
(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the voltage at the input.
(4) Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in the load current.

Electrical Characteristics
LP38500/2–ADJ (continued)

Unless otherwise specified: V_{IN} = 3.3V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = V_{IN}, V_{OUT} = 1.8V. Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

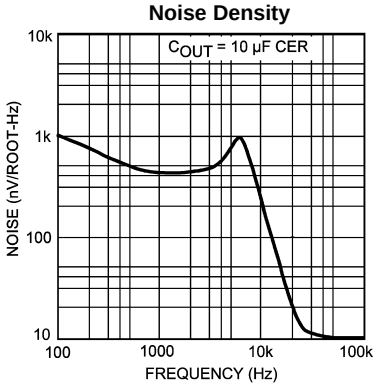
Symbol	Parameter	Conditions	Min	Typ	Max	Units
θ_{J-A}	Thermal Resistance Junction to Ambient	TO-263, TO-263 THIN(5) 1 sq. in. copper	—	37	—	°C/W
	Thermal Resistance Junction to Ambient	LLP-8 (6)	—	80	—	
θ_{J-C}	Thermal Resistance Junction to Case	TO-263, TO-263 THIN	—	5	—	°C/W
		LLP-8	—	16	—	

(5) The value of θ_{JA} for the TO-263 (TS) package and TO-263 THIN (TJ) package can range from approximately 30 to 60°C/W depending on the amount of PCB copper dedicated to heat transfer (See Application Information).
(6) θ_{JA} for the LLP-8 package was measured using the LP38502SD-ADJ evaluation board (See Application Information).

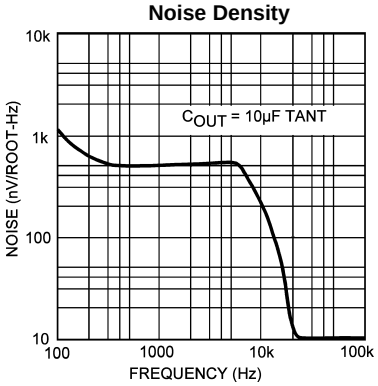
Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.7V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA, V_{OUT} = 1.8V

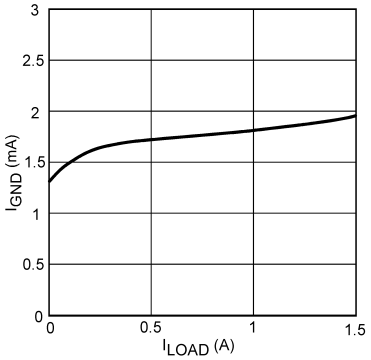
Noise Density



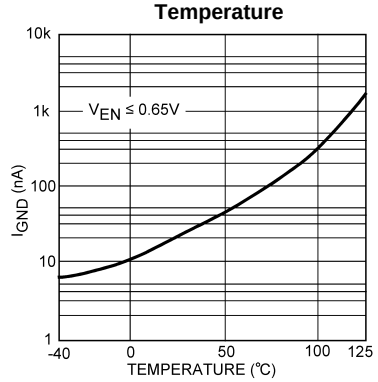
Noise Density



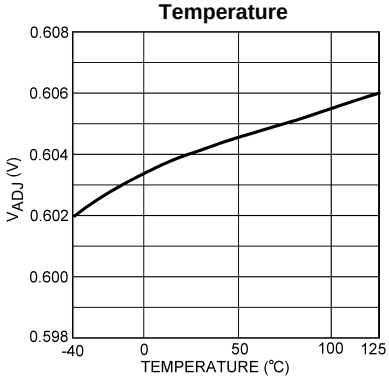
I_{GND} vs Load Current



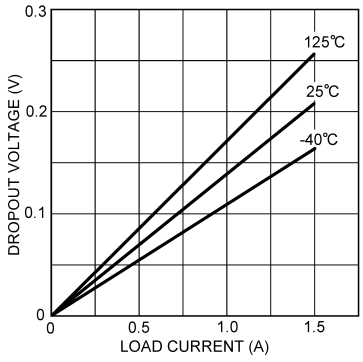
$I_{GND(OFF)}$ vs Temperature



V_{ADJ} vs Temperature



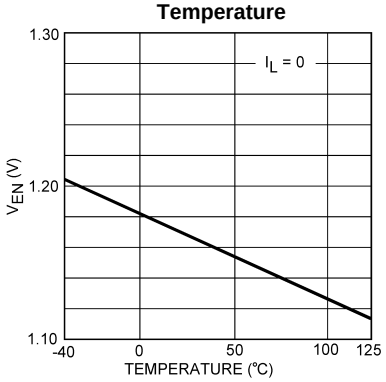
Dropout Voltage vs Load Current



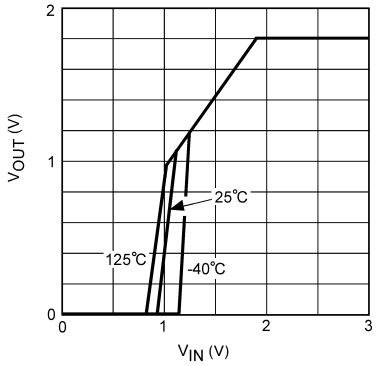
Typical Performance Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.7V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA, V_{OUT} = 1.8V

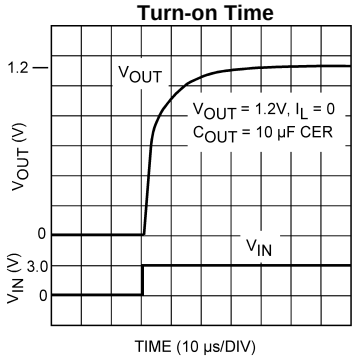
V_{EN} vs Temperature



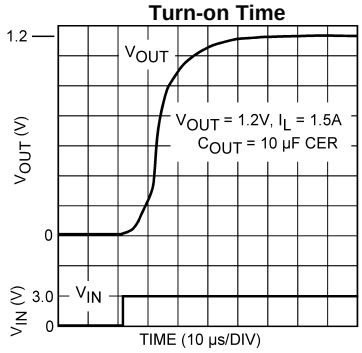
Turn-on Characteristics



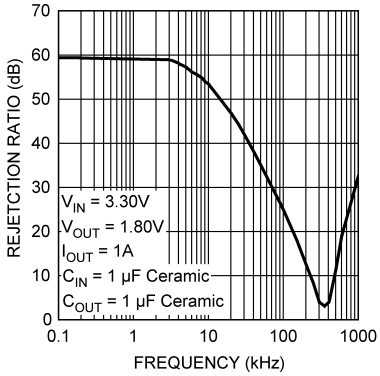
Turn-on Time



Turn-on Time



PSRR



Block Diagrams (TO-263, TO-263 THIN)

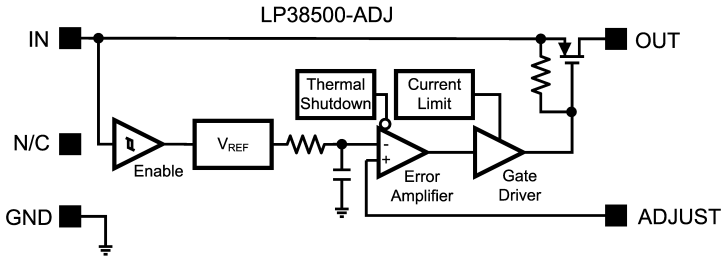


Figure 7. LP38500-ADJ TO-263 Block Diagram

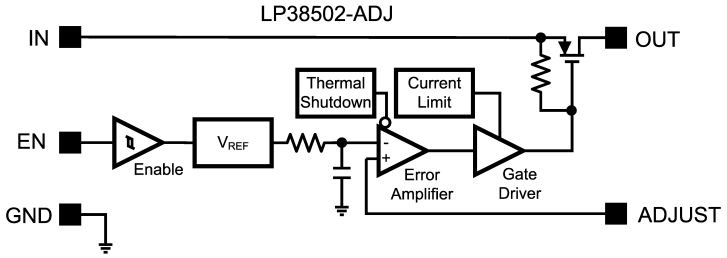


Figure 8. LP38502-ADJ TO-263 Block Diagram

Block Diagrams (LLP-8)

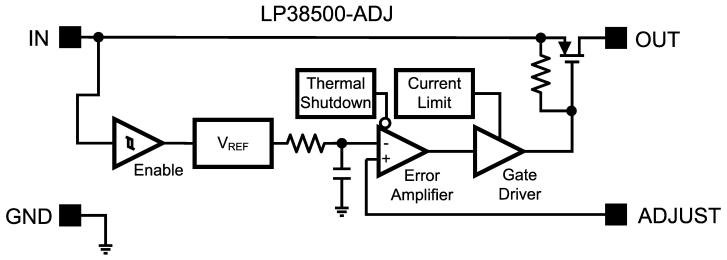


Figure 9. LP38500-ADJ LLP-8 Block Diagram

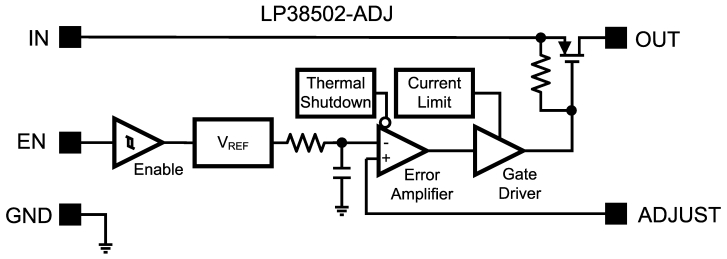


Figure 10. LP38502-ADJ LLP-8 Block Diagram

Application Information

EXTERNAL CAPACITORS

The LP3850X requires that at least 10 µF (±20%) capacitors be used at the input and output pins located within one cm of the IC. Larger capacitors may be used without limit on size for both C_{IN} and C_{OUT}. Capacitor tolerances such as temperature variation and voltage loading effects must be considered when selecting capacitors to ensure that they will provide the minimum required amount of capacitance under all operating conditions for the application.

In general, ceramic capacitors are best for noise bypassing and transient response because of their ultra low ESR. It must be noted that if ceramics are used, only the types with X5R or X7R dielectric ratings should be used (never Z5U or Y5F). Capacitors which have the Z5U or Y5F characteristics will see a drop in capacitance of as much as 50% if their temperature increases from 25°C to 85°C. In addition, the capacitance drops significantly with applied voltage: a typical Z5U or Y5F capacitor can lose as much as 60% of it's rated capacitance if only half of the rated voltage is applied to it. For these reasons, only X5R and X7R ceramics should be used.

INPUT CAPACITOR

All linear regulators can be affected by the source impedance of the voltage which is connected to the input. If the source impedance is too high, the reactive component of the source may affect the control loop's phase margin. **To ensure proper loop operation, the ESR of the capacitor used for C_{IN} must not exceed 0.5 Ohms**. Any good quality ceramic capacitor will meet this requirement, as well as many good quality tantalums. Aluminum electrolytic capacitors may also work, but can possibly have an ESR which increases significantly at cold temperatures. If the ESR of the input capacitor may exceed 0.5 Ohms, it is recommended that a 2.2 µF ceramic capacitor be used in parallel, as this will assure stable loop operation.

OUTPUT CAPACITOR

Any type of capacitor may be used for C_{OUT}, with no limitations on minimum or maximum ESR, as long as the minimum amount of capacitance is present. The amount of capacitance can be increased without limit. Increasing the size of C_{OUT} typically will give improved load transient response.

SETTING THE OUTPUT VOLTAGE

The output voltage of the LP38500/2-ADJ can be set to any value between 0.6V and 5V using two external resistors shown as R1 and R2 in Figure 11.

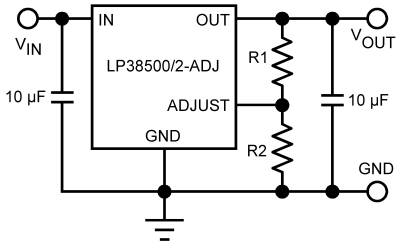


Figure 11.

The value of R2 should always be less than or equal to 10 kΩ for good loop compensation. R1 can be selected for a given V_{OUT} using the following formula:

$$V_{OUT} = V_{ADJ} (1 + R1/R2) + I_{ADJ} (R1) \quad (1)$$

Where V_{ADJ} is the adjust pin voltage and I_{ADJ} is the bias current flowing into the adjust pin.

STABILITY AND PHASE MARGIN

Any regulator which operates using a feedback loop must be compensated in such a way as to ensure adequate phase margin, which is defined as the difference between the phase shift and -180 degrees at the frequency where the loop gain crosses unity (0 dB). For most LDO regulators, the ESR of the output capacitor is required to create a zero to add enough phase lead to ensure stable operation. The LP38500/2-ADJ has a unique internal compensation circuit which maintains phase margin regardless of the ESR of the output capacitor, so any type of capacitor may be used.

Figure 12 shows the gain/phase plot of the LP38500/2-ADJ with an output of 1.2V, 10 µF ceramic output capacitor, delivering 1.5A of load current. It can be seen that the unity-gain crossover occurs at 150 kHz, and the phase margin is about 40° (which is very stable).

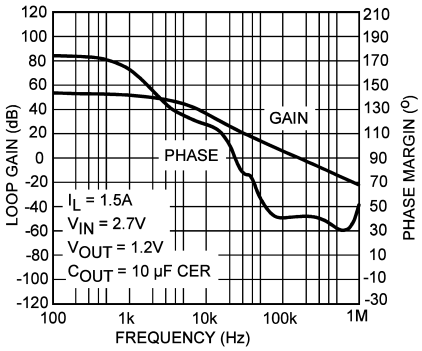


Figure 12. Gain-Bandwidth Plot for 1.5A Load

Figure 13 shows the gain and phase with no external load. In this case, the only load is provided by the gain setting resistors (about 12 kΩ total in this test). It is immediately obvious that the unity-gain frequency is significantly lower (dropping to about 500 Hz), at which point the phase margin is 125°.

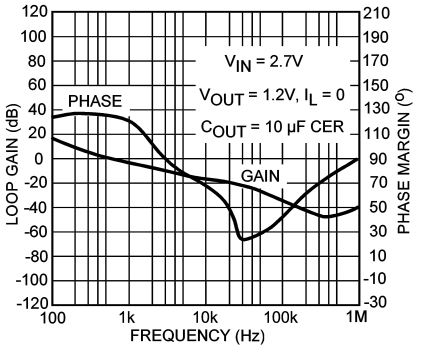


Figure 13. Gain-Bandwidth Plot for No Load

The reduction in unity-gain bandwidth as load current is reduced is normal for any LDO regulator using a P-FET or PNP pass transistor, because they have a pole in the loop gain function given by:

$$F_P = \frac{1}{2 \times \pi \times R_L \times C_{OUT}} \quad (2)$$

This illustrates how the pole goes to the highest frequency when R_L is minimum value (maximum load current). In general, LDO's have maximum bandwidth (and lowest phase margin) at full load current. In the case of the LP38500/2-ADJ, it can be seen that it has good phase margin even when using ceramic capacitors with ESR values of only a few milli Ohms.

LOAD TRANSIENT RESPONSE

Load transient response is defined as the change in regulated output voltage which occurs as a result of a change in load current. Many applications have loads which vary, and the control loop of the voltage regulator must adjust the current in the pass FET transistor in response to load current changes. For this reason, regulators with wider bandwidths often have better transient response.

The LP38500/2-ADJ employs an internal feedforward design which makes the load transient response much faster than would be predicted simply by loop speed: this feedforward means any voltage changes appearing on the output are coupled through to the high-speed driver used to control the gate of the pass FET along a signal path using very fast FET devices. Because of this, the pass transistor's current can change very quickly.

Figure 3 shows the output voltage load transient which occurs on a 1.8V output when the load changes from 0.1A to 1.5A at an average slew rate of 0.5A/µs. As shown, the peak output voltage change from nominal is about 40 mV, which is about 2.2%.

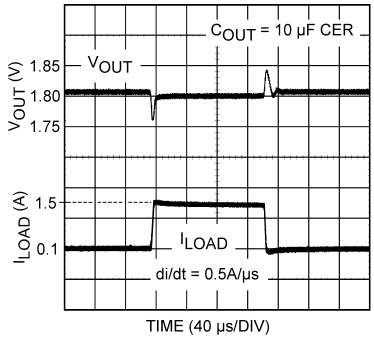


Figure 14. Load Transient Response

In cases where extremely fast load changes occur, the output capacitance may have to be increased. When selecting capacitors, it must be understood that the better performing ones usually cost the most. For fast changing loads, the internal parasitics of ESR (equivalent series resistance) and ESL (equivalent series inductance) degrade the capacitor's ability to source current quickly to the load. The best capacitor types for transient performance are (in order):

1. Multilayer Ceramic: with the lowest values of ESR and ESL, they can have ESR values in the range of a few milli Ohms. Disadvantage: capacitance values above about 22 µF significantly increase in cost.
2. Low-ESR Aluminum Electrolytics: these are aluminum types (like OSCON) with a special electrolyte which provides extremely low ESR values, and are the closest to ceramic performance while still providing large amounts of capacitance. These are cheaper (by capacitance) than ceramic.
3. Solid tantalum: can provide several hundred µF of capacitance, transient performance is slightly worse than OSCON type capacitors, cheaper than ceramic in large values.
4. General purpose aluminum electrolytics: cheap and provide a lot of capacitance, but give the worst performance.

In general, managing load transients is done by paralleling ceramic capacitance with a larger bulk capacitance. In this way, the ceramic can source current during the rapidly changing edge and the bulk capacitor can support the load current after the first initial spike in current.

PRINTED CIRCUIT BOARD LAYOUT

Good layout practices will minimize voltage error and prevent instability which can result from ground loops. The input and output capacitors should be directly connected to the IC pins with short traces that have no other current flowing in them (Kelvin connect).

The best way to do this is to place the capacitors very near the IC and make connections directly to the IC pins via short traces on the top layer of the PCB. The regulator's ground pin should be connected through vias to the internal or backside ground plane so that the regulator has a single point ground.

The external resistors which set the output voltage must also be located very near the IC with all connections directly tied via short traces to the pins of the IC (Kelvin connect). Do not connect the resistive divider to the load point or DC error will be induced.

RFI/EMI SUSCEPTIBILITY

RFI (Radio Frequency Interference) and EMI (Electro-Magnetic Interference) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the IC regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the IC to reduce the amount of EMI conducted into the IC.

If the LP38500/2-ADJ output is connected to a load which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the IC output. Since the bandwidth of the regulator loop is less than 300 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the IC at frequencies above 300 kHz is determined only by the output capacitor(s). Ceramic capacitors provide the best performance in this type of application.

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. In such cases, it is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load. PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane. In multi-layer PC Board applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

OUTPUT NOISE

Noise is specified in two ways:

Spot Noise or **Output noise density** is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.

Total output noise voltage or **Broadband noise** is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies. Attention should be paid to the units of measurement.

Spot noise is measured in units μV/√Hz or nV/√Hz and total output noise is measured in μV(rms). The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current.

Noise can generally be reduced in two ways: increase the transistor area or increase the reference current. However, enlarging the transisitors will increase die size, and increasing the reference current means higher total supply current (ground pin current).

SHORT-CIRCUIT PROTECTION

The LP38500/2-ADJ contains internal current limiting which will reduce output current to a safe value if the output is overloaded or shorted. Depending upon the value of V_{IN}, thermal limiting may also become active as the average power dissipated causes the die temperature to increase to the limit value (about 170°C). The hysteresis of the thermal shutdown circuitry can result in a “cyclic” behavior on the output as the die temperature heats and cools.

ENABLE OPERATION (LP38502-ADJ Only)

The Enable pin (EN) must be actively terminated by either a 10 kΩ pull-up resistor to V_{IN}, or a driver which actively pulls high and low (such as a CMOS rail to rail comparator). If active drive is used, the pull-up resistor is not required. This pin must be tied to V_{IN} if not used (it must not be left floating).

DROPOUT VOLTAGE

The dropout voltage of a regulator is defined as the input-to-output differential required by the regulator to keep the output voltage within 2% of the nominal value. For CMOS LDOs, the dropout voltage is the product of the load current and the $R_{DS(on)}$ of the internal MOSFET pass element.

Since the output voltage is beginning to "drop out" of regulation when it drops by 2%, electrical performance of the device will be reduced compared to the values listed in the Electrical Characteristics table for some parameters (line and load regulation and PSRR would be affected).

REVERSE CURRENT PATH

The internal MOSFET pass element in the LP38500/2-ADJ has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200 mA continuous and 1A peak. The regulator output pin should not be taken below ground potential. If the LP38500/2-ADJ is used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.

POWER DISSIPATION/HEATSINKING

The maximum power dissipation ($P_{D(MAX)}$) of the LP38500/2-ADJ is limited by the maximum junction temperature of 125°C, along with the maximum ambient temperature ($T_{A(MAX)}$) of the application, and the thermal resistance (θ_{JA}) of the package. Under all possible conditions, the junction temperature (T_J) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_{GND}) \quad (3)$$

where I_{GND} is the operating ground current of the device (specified under Electrical Characteristics).

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (4)$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = \Delta T_J / P_{D(MAX)} \quad (5)$$

The LP38500/2-ADJ is available in the TO-263 and LLP-8 packages. The thermal resistance depends on the amount of copper area allocated to heat transfer.

HEATSINKING TO-263 and TO-263 THIN PACKAGES

The TO-263 package and TO-263 THIN package use the copper plane on the PCB as a heatsink. The DAP of the package is soldered to the copper plane for heat sinking. Figure 15 shows a typical curve for the θ_{JA} of the TO-263 package for different copper area sizes (the thermal performance of both TO-263 and TO-263 THIN are the same). The tests were done using a PCB with 1 ounce copper on top side only, with copper patterns which were square in shape.

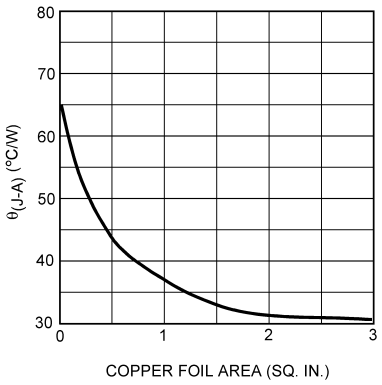


Figure 15. θ_{JA} vs Copper Area for TO-263 Package

As shown in the figure, increasing the copper area beyond 1.5 square inch produces very little improvement.

HEATSINKING LLP-8 PACKAGE

The junction-to-ambient thermal resistance for the LLP-8 package is dependent on how much PCB copper is present to conduct heat away from the device. The LP38502SD-ADJ evaluation board (980600046-100) was tested and gave a result of about 80°C/W with a power dissipation of 1W and no external airflow. This evaluation board is a two layer board using two ounce copper, and the copper area on topside for heatsinking is approximately two square inches. Multiple vias under the DAP also thermally connect to the backside layer which has about three square inches of copper dedicated to heatsinking.

Finite modeling of the LP38502SD-ADJ with a four layer board (JEDEC JESD51-7 and JESD51-5) with one thermal via directly under the DAP to the first copper plane predicts a θ_{JA} of 72°C/W.

With four thermal vias directly under the DAP to the first copper plane, the modeling predicts a θ_{JA} of 50°C/W.

Adding a dog-bone copper area with four additional thermal vias in the dog-bone area to the first copper plane can improve θ_{JA} to 45C°C/W.

See Application Note *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* for additional thermal considerations for printed circuit board layouts.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LP38500ASD-ADJ/NOPB	ACTIVE	WSON	NGS	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38500ASDX-ADJ/NOPB	ACTIVE	WSON	NGS	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38500ATJ-ADJ/NOPB	ACTIVE	PFM	NDQ	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38500SD-ADJ/NOPB	ACTIVE	WSON	NGS	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38500SDE-ADJ/NOPB	ACTIVE	WSON	NGS	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38500SDX-ADJ/NOPB	ACTIVE	WSON	NGS	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38500TJ-ADJ/NOPB	ACTIVE	PFM	NDQ	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38500TS-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	
LP38500TSX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	
LP38502ASD-ADJ/NOPB	ACTIVE	WSON	NGS	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38502ASDX-ADJ/NOPB	ACTIVE	WSON	NGS	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38502ATJ-ADJ/NOPB	ACTIVE	PFM	NDQ	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38502SD-ADJ/NOPB	ACTIVE	WSON	NGS	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38502SDE-ADJ/NOPB	ACTIVE	WSON	NGS	8	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38502SDX-ADJ/NOPB	ACTIVE	WSON	NGS	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38502TJ-ADJ/NOPB	ACTIVE	PFM	NDQ	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	
LP38502TS-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LP38502TSX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	

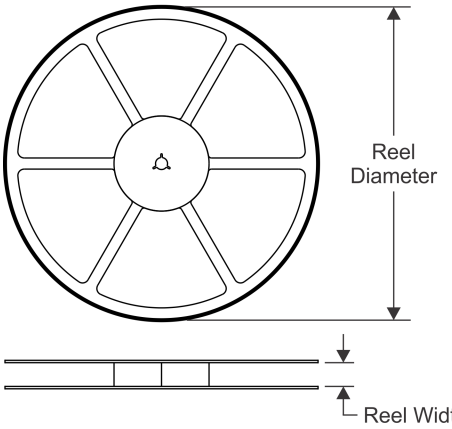
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

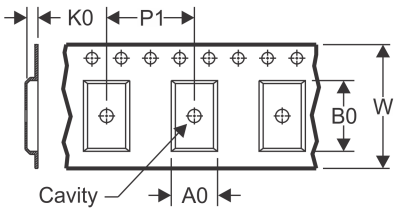
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

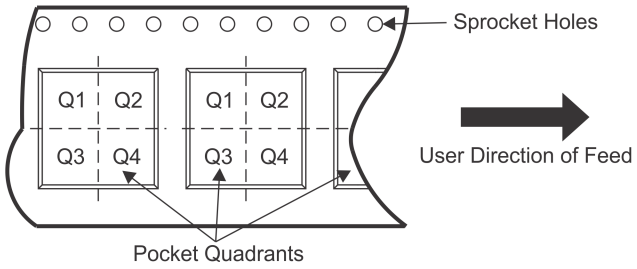


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

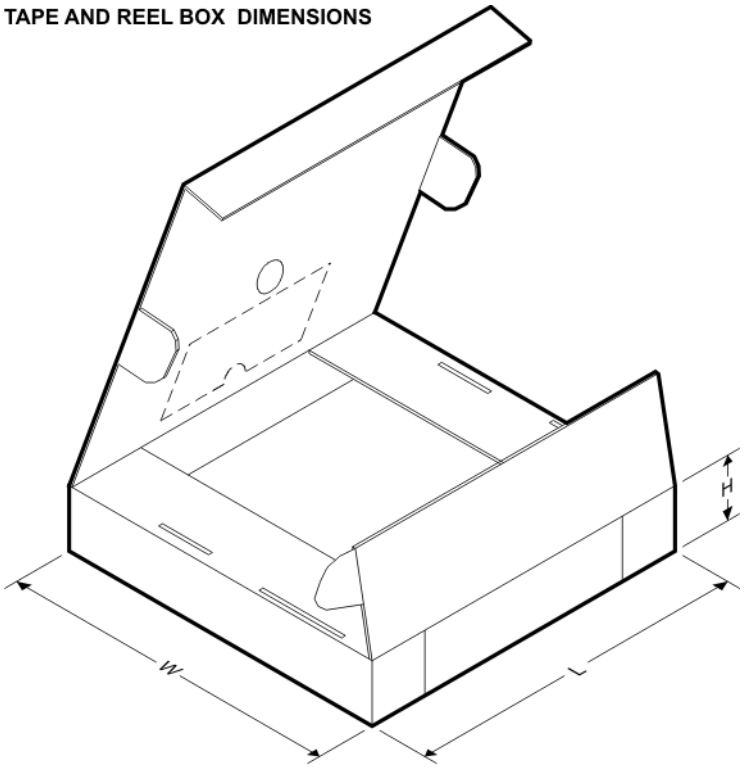


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38500ASD-ADJ/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500ASDX-ADJ/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500ATJ-ADJ/NOPB	PFM	NDQ	5	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LP38500SD-ADJ/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500SDE-ADJ/NOPB	WSON	NGS	8	250	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500SDX-ADJ/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500TJ-ADJ/NOPB	PFM	NDQ	5	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LP38500TSX-ADJ/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP38502ASD-ADJ/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38502ASDX-ADJ/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38502ATJ-ADJ/NOPB	PFM	NDQ	5	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LP38502SD-ADJ/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38502SDE-ADJ/NOPB	WSON	NGS	8	250	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38502SDX-ADJ/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38502TJ-ADJ/NOPB	PFM	NDQ	5	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LP38502TSX-ADJ/NOPB	DDPAK/	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	TO-263											

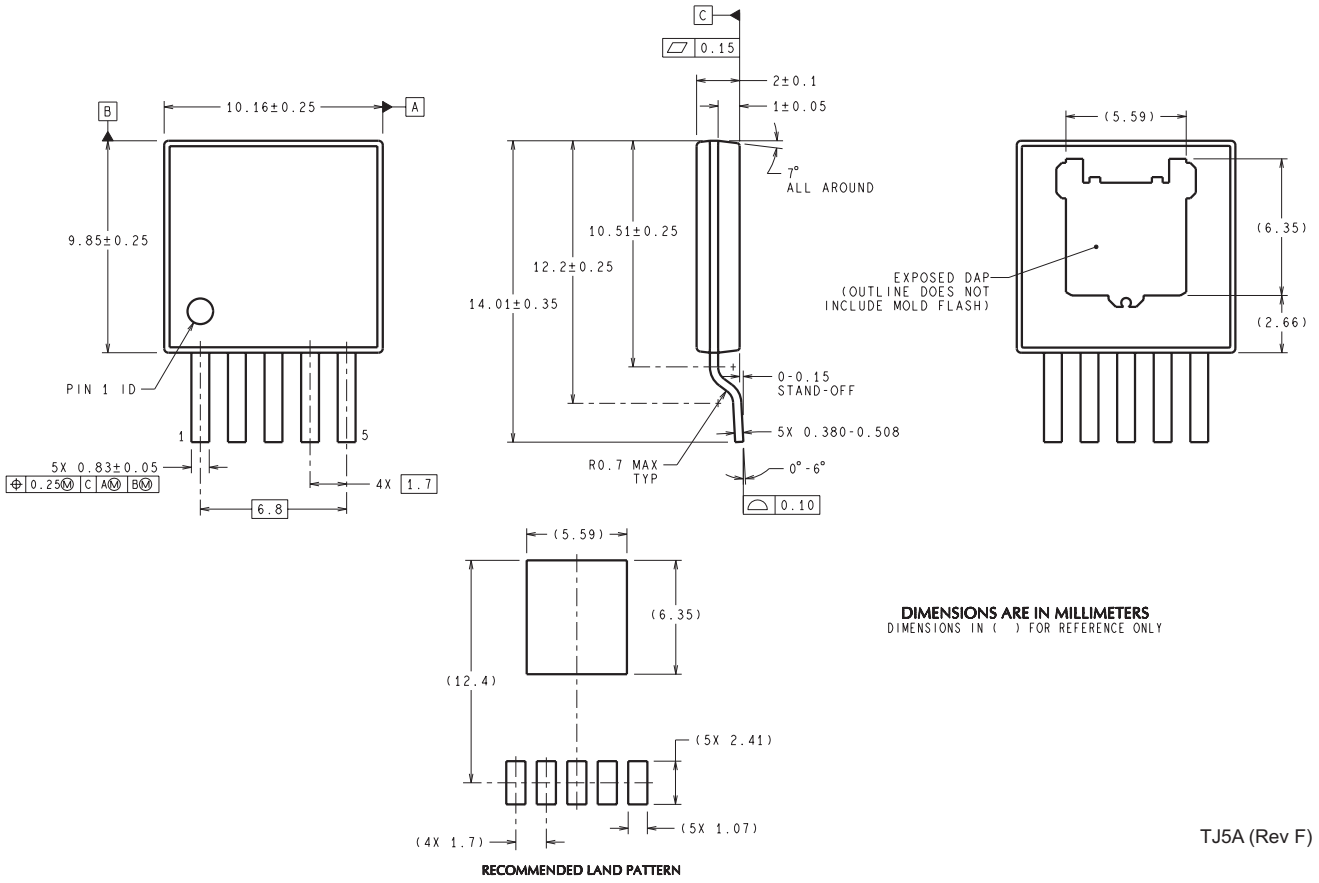
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38500ASD-ADJ/NOPB	WSON	NGS	8	1000	203.0	190.0	41.0
LP38500ASDX-ADJ/NOPB	WSON	NGS	8	4500	349.0	337.0	45.0
LP38500ATJ-ADJ/NOPB	PFM	NDQ	5	1000	349.0	337.0	45.0
LP38500SD-ADJ/NOPB	WSON	NGS	8	1000	203.0	190.0	41.0
LP38500SDE-ADJ/NOPB	WSON	NGS	8	250	203.0	190.0	41.0
LP38500SDX-ADJ/NOPB	WSON	NGS	8	4500	349.0	337.0	45.0
LP38500TJ-ADJ/NOPB	PFM	NDQ	5	1000	349.0	337.0	45.0
LP38500TSX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	358.0	343.0	63.0
LP38502ASD-ADJ/NOPB	WSON	NGS	8	1000	203.0	190.0	41.0
LP38502ASDX-ADJ/NOPB	WSON	NGS	8	4500	349.0	337.0	45.0
LP38502ATJ-ADJ/NOPB	PFM	NDQ	5	1000	349.0	337.0	45.0
LP38502SD-ADJ/NOPB	WSON	NGS	8	1000	203.0	190.0	41.0
LP38502SDE-ADJ/NOPB	WSON	NGS	8	250	203.0	190.0	41.0
LP38502SDX-ADJ/NOPB	WSON	NGS	8	4500	349.0	337.0	45.0
LP38502TJ-ADJ/NOPB	PFM	NDQ	5	1000	349.0	337.0	45.0
LP38502TSX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	358.0	343.0	63.0

NDQ0005A



DIMENSIONS ARE IN MILLIMETERS
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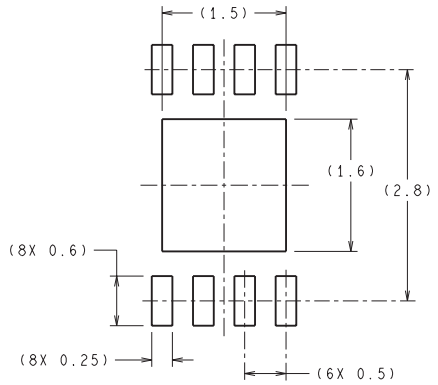
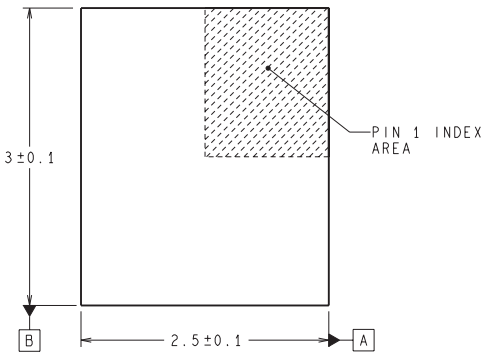
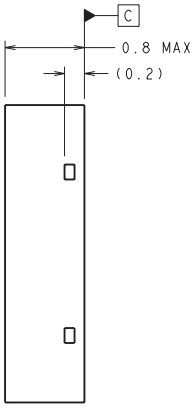
TJ5A (Rev F)

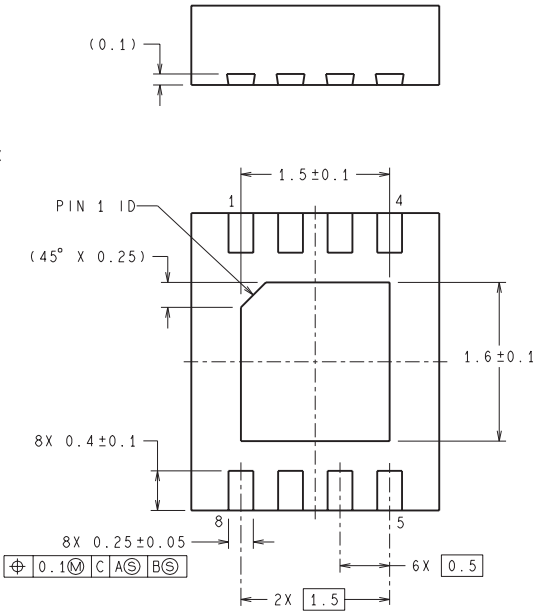


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

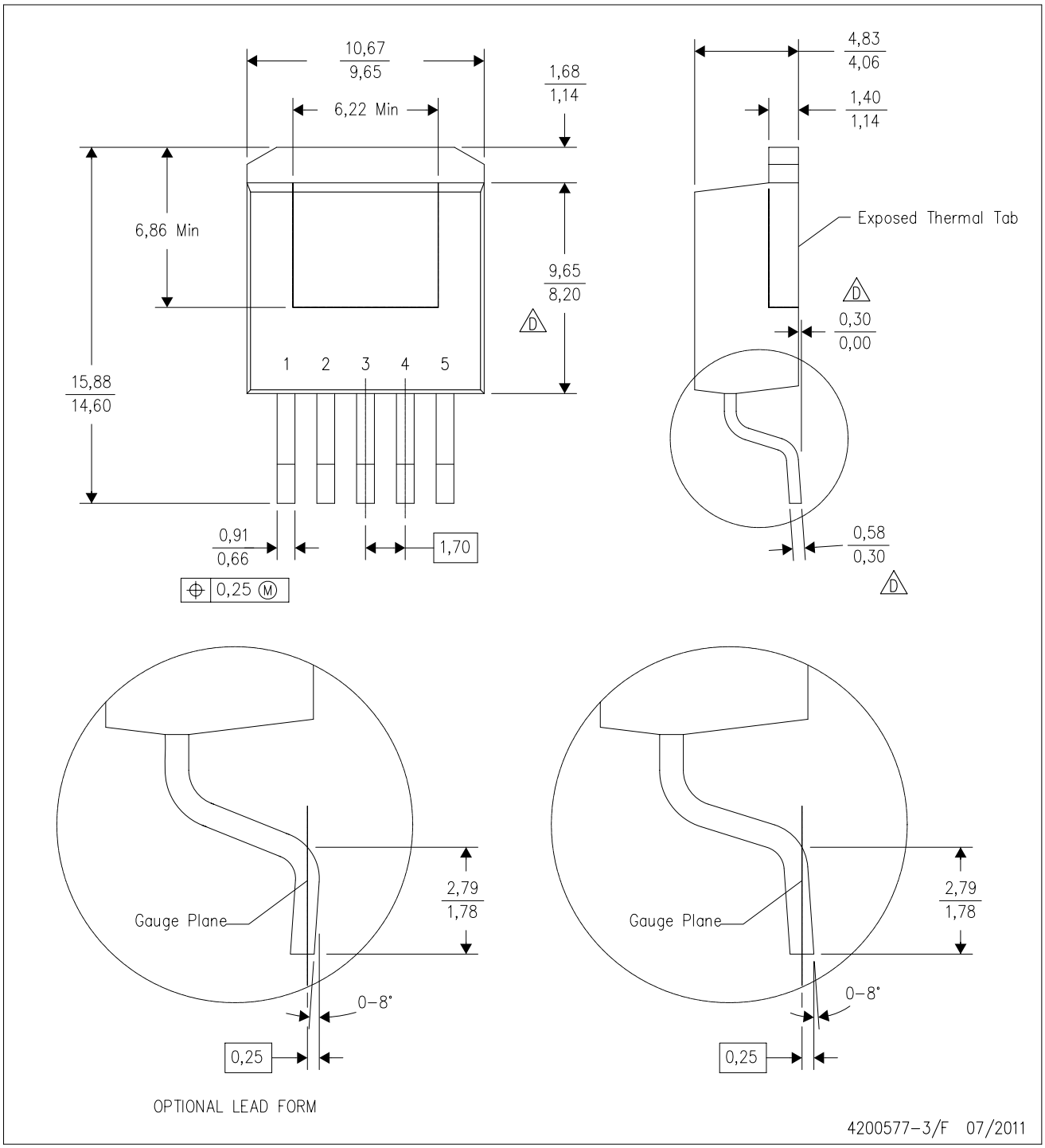






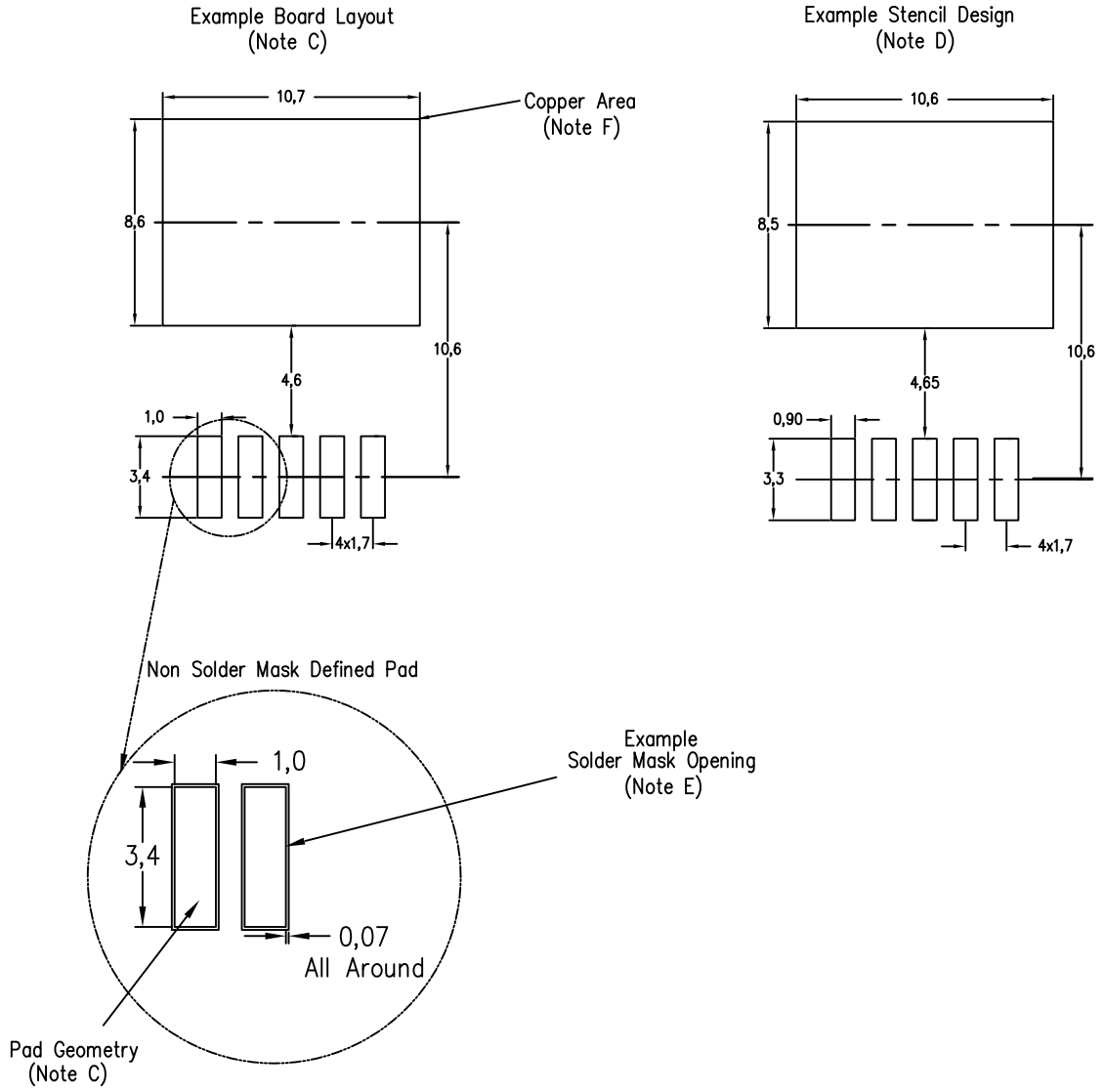
SDA08C (Rev A)

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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